US005442465A

United States Patent [19]

Compton

[11] Patent Number: 5,442,465

[45] Date of Patent: Aug. 15, 1995

[54] **APPARATUS AND METHOD FOR CONTROLLING A LINEAR IMAGING DEVICE**

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[21] Appl. No.: **298,725**

[22] Filed: **Aug. 31, 1994**

[51] **Int. Cl.**[6] **H04N 1/03**; H04N 1/191

[52] **U.S. Cl.** **358/482**; 358/483; 358/494; 250/208.1; 348/294; 348/295; 348/297; 348/298; 348/324

[58] **Field of Search** 358/483, 482, 494, 471, 358/443, 445, 444, 447, 513, 514; 250/208.1; 348/294, 295, 297, 298, 324

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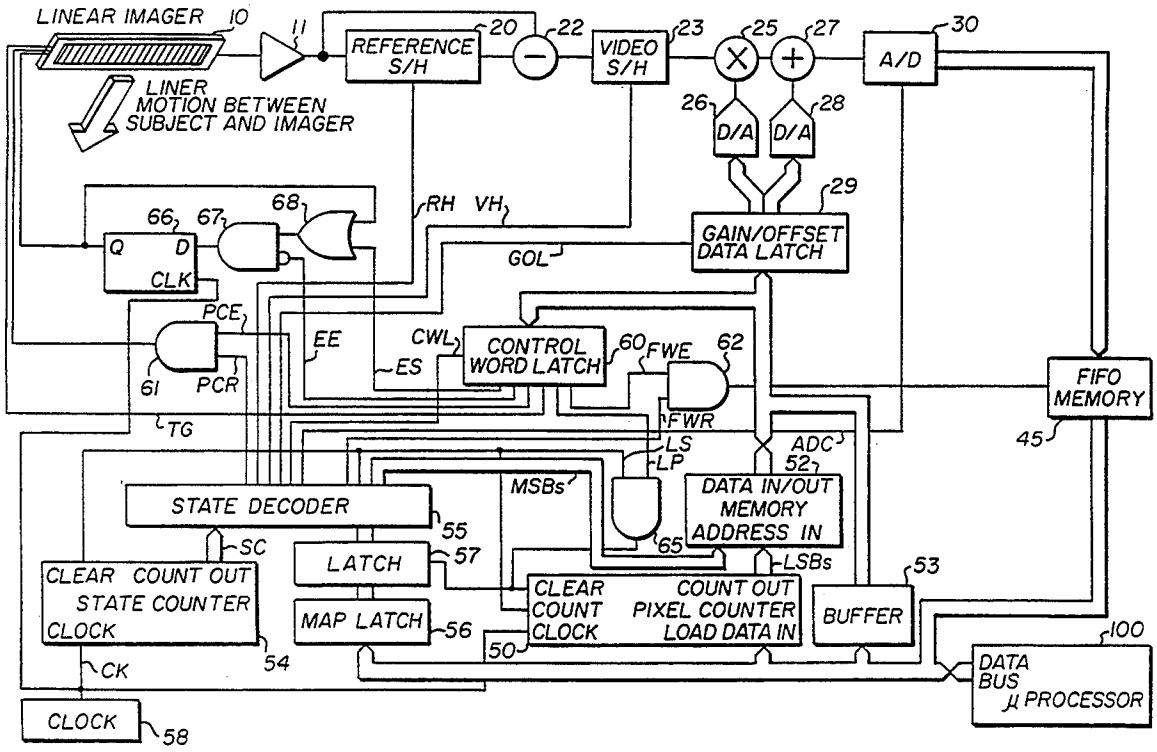
[57] **ABSTRACT**

A CCD linear imager is dynamically controlled on a pixel-by-pixel basis by a line-related map of control words stored in memory with individual control words addressed by a pixel counter operating in synchronism with processing of each imaging pixel in the CCD. Multiple control word maps may be stored in memory for programmed selection "on the fly" to vary the operating control of the CCD on a line-by-line basis.

6 Claims, 2 Drawing Sheets



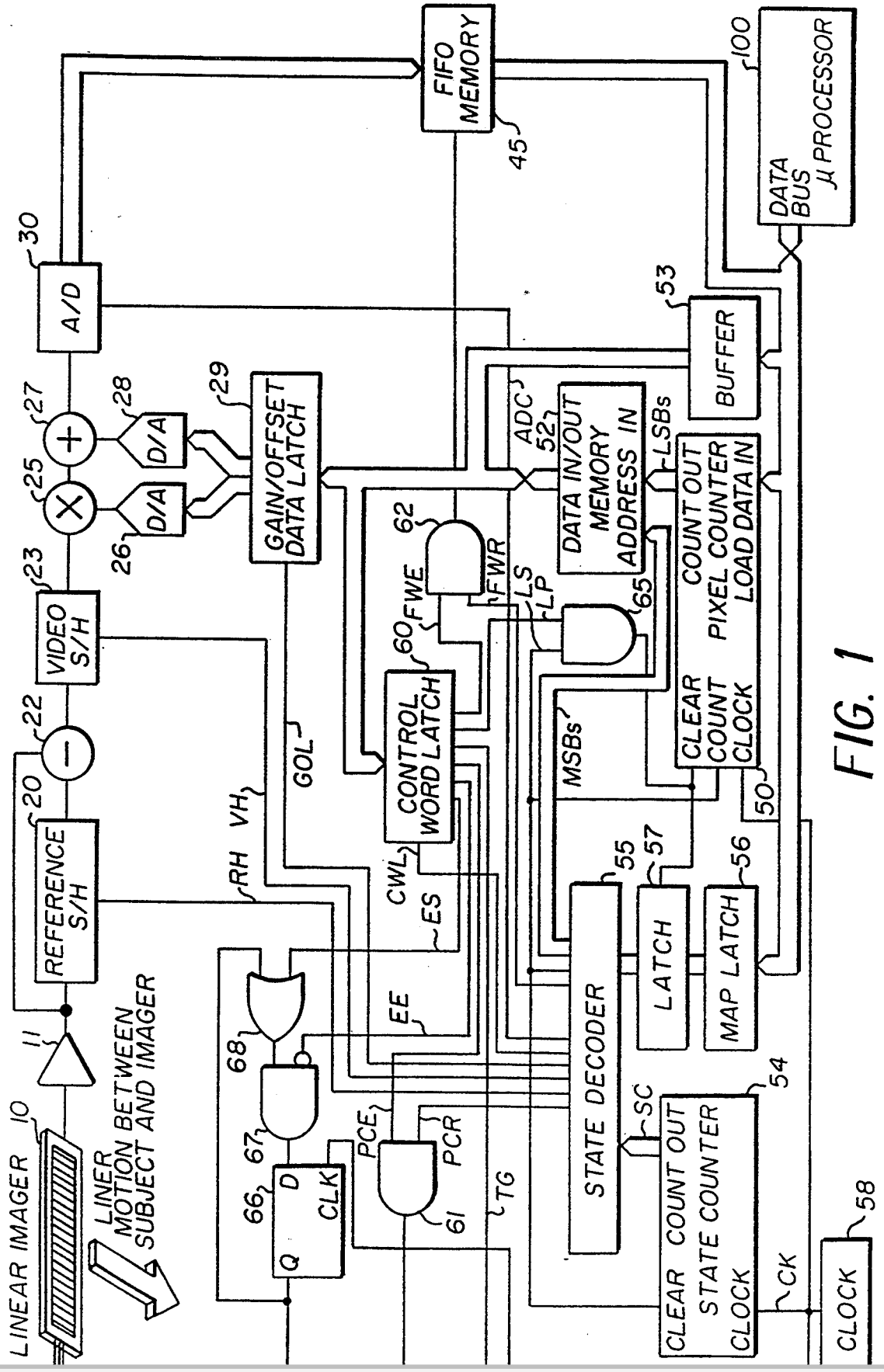


FIG. 1

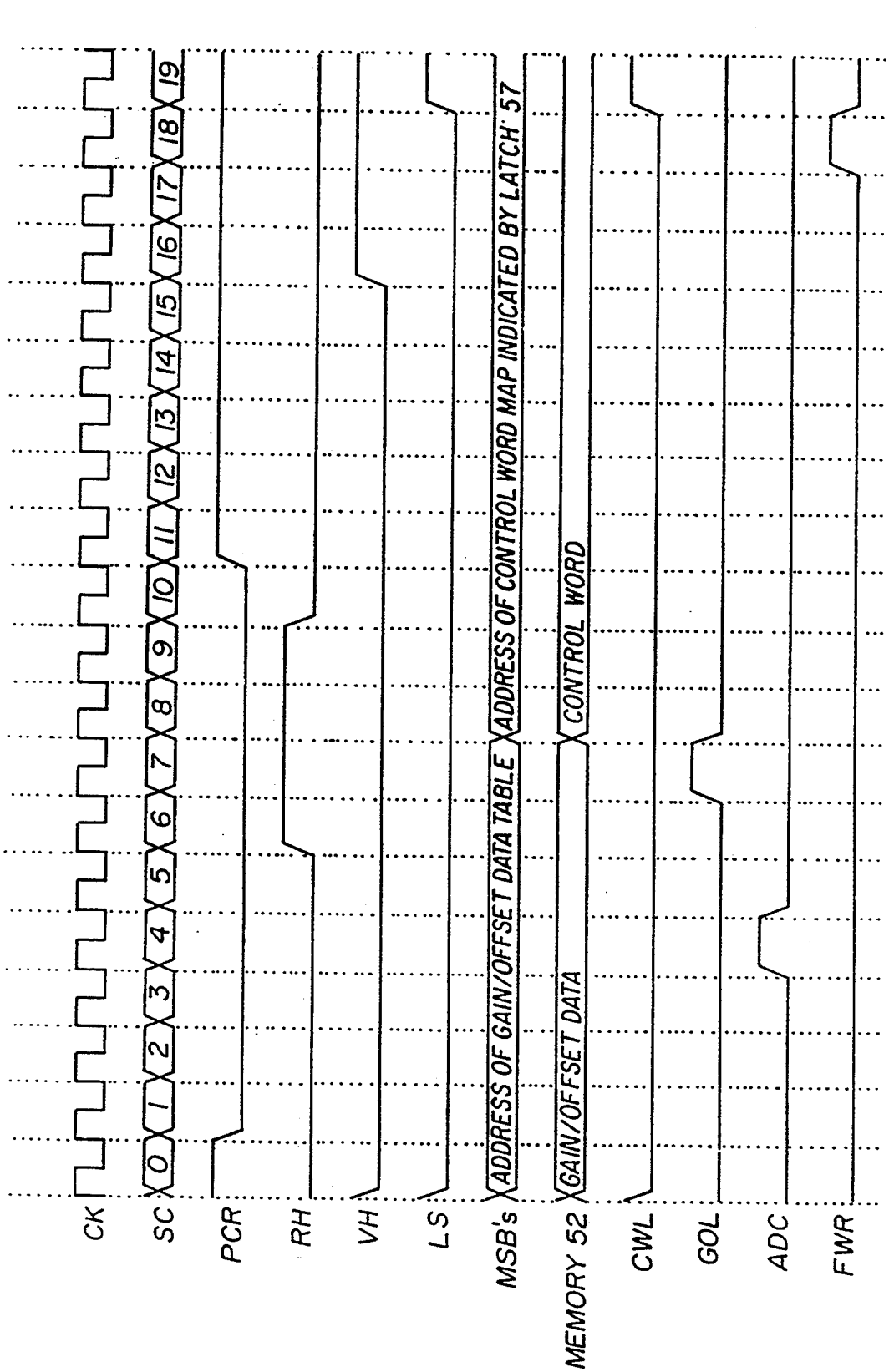


FIG. 2

APPARATUS AND METHOD FOR CONTROLLING A LINEAR IMAGING DEVICE

FIELD OF THE INVENTION

The invention relates generally to the field of film scanners and, in particular, to apparatus and method for controlling the operation of linear imaging devices in such scanners.

BACKGROUND OF THE INVENTION

Modern film scanners typically employ a linear imaging device such as a charge-coupled-device (CCD) for scanning film images to generate digital signals representative of the image information. A linear charge coupled device (CCD) imager contains a linear array of light detecting sites (hereafter "imaging pixels") which accumulate charge depending on the light energy projected onto them. After some charge accumulation time, the charges in the light detecting imaging pixels are transferred to a charge shifting structure so that the charges may be shifted out of the CCD and measured by some means in order to form a representation of the image projected onto the CCD. There are a number of signals which control the operation of the imager: clock signals which cause the charge to be shifted out of the imager, a transfer signal which causes the charge from the imaging pixels to be transferred to the shift structure, and one or more signals which electronically control exposure.

Typically, the control signals for the imager will be generated by a programmable logic device (PLD) or an application specific integrated circuit (ASIC). A counter circuit with a decoder is used to indicate when the charge clocking and transfer signals should be operated during the scan line. A counter with a reload value is used for each exposure control. These structures consume significant resources within a PLD or ASIC. Additionally, since they are embedded in the PLD program or the design of the ASIC, the structures are either inflexible or flexibility is gained at the cost of increased complexity and more resources.

If it is desired to make a change in the timing of control signals to a CCD imager, and the timing is embedded in the design of a PLD or ASIC, then the PLD or ASIC component must be physically removed from the system and replaced with an updated component. If this change is required as a field upgrade, the costs to upgrade will be significant. Additionally, if the component is an ASIC, significant costs may be incurred in modifying the design. There is therefore a need for an alternative, less costly and more flexible manner of controlling linear imaging devices when the control events occur during a line and this invention satisfies this need.

SUMMARY OF THE INVENTION

In accordance with the invention, therefore, there is provided apparatus for controlling operation of a linear imaging device having a line of light-responsive imaging pixels, wherein the apparatus comprises pixel counter means for supplying pixel counts corresponding to individual pixels in the imaging device; and means for supplying a map of operating control words, the control words each comprising programmably variable bit content defining pixel-by-pixel operating characteristics of the line of imaging pixels. The apparatus further includes memory means for storing the map of control words at memory addresses corresponding to the pixel counts; and means for outputting the control words from the memory to the imaging device in synchronism with the pixel counts to control the operation of the imaging device on a pixel-by-pixel basis in accordance with the bit content of each control word.

The method of the invention comprises providing a map of operating control words each of which comprises programmably variable bit content defining pixel-by-pixel operating characteristics of a line of imaging pixels in a linear imaging device; storing the control words in imaging pixel related address locations in a memory and accessing said control words from the memory on a pixel-by-pixel basis and using the accessed control words to control operation of the imaging device on a pixel-by-pixel basis.

It will be appreciated that, by utilizing a list of control words in a memory for pixel-by-pixel control of the operation of a linear imaging device, flexibility is gained and PLD or ASIC resources and size are reduced at the same time.

These and other aspects, objects, features and advantages of the present invention will be more clearly understood and appreciated from a review of the following detailed description of the preferred embodiments and appended claims, and by reference to the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

In the drawings:

FIG. **1** is a block diagram of a film scanner system including imaging device control apparatus of the present invention.

FIG. **2** is a timing diagram useful in explaining the operation of the system of FIG. **1**.

DETAILED DESCRIPTION OF THE INVENTION

FIG. **1** shows an arrangement of circuit elements in the signal processing circuitry of a CCD based linear scanner. A linear CCD imaging device **10** integrates the charges produced by each imaging pixel in the CCD for a period of time and then transfers the charges to a shifting structure so that the charges can be shifted out of the CCD in a serial fashion. The signal produced by the CCD for each imaging pixel comprises two phases: a reference phase followed by a video phase. The reference phase provides a reference level against which the video phase that follows may be compared. The video phase represents the magnitude of charge accumulated at the imaging pixel. The serial signal coming from the CCD **10** is amplified by amplifier **11**, the output of which goes to a subtracter circuit **22** and a reference sample-and-hold circuit **20**. The reference sample-and-hold **20** samples the signal from the CCD during each image pixel's reference phase. The subtracter **22** removes the sampled and held reference signal from the subsequent video phase. Hence, the output of the subtracter **22** is normalized to the reference level. This normalized signal is sampled by a video sample-and-hold circuit **23** during the video phase of the signal provided by the imager.

The sampled-and-held normalized video signal at the output of video S/H **23** is operated on by a multiplier circuit **25** and a summer circuit **27**. These two circuits provide gain and offset compensation for variations in the video signal caused by such factors as variations in imaging pixel sensitivity, non uniformity of illumina-

tion, variations in signal offset and the like. The digital-to-analog converter **26** provides the gain correction value for multiplier **25** and the digital-to-analog converter **28** provides the offset correction value for summer **27**. Data representing the offset and gain compensation values are provided to the two analog-to-digital converters **25** and **27** on a pixel-by-pixel basis with the arrival of the normalized video signal for each imaging pixel of CCD **10** by means of pixel counter **50**, RAM memory **52**, and gain/offset data latch **29**. The pixel counter **50** increments synchronously with readout of the imaging pixel signals from the CCD **10**. The output of pixel counter **50** is used to provide an address to memory **52** which holds gain and offset values for each imaging pixel. The gain and offset data output from the memory is latched by data latch **29** which provides the data to digital-to-analog (D/A) converters **26** and **28**. A buffer circuit **53** allows a microprocessor **100** to gain access to memory **52** in order to change the gain and offset values as the result of a calibration process. The output of summer circuit **27** is coupled to analog-to-digital converter **30** wherein the normalized and gain/-offset-corrected video signal is converted to a numeric value which is then written to the FIFO memory **45** for readout and subsequent utilization by microprocessor **100**. The single CCD output and related signal processing circuits as just described would provide a monochrome video signal. For a three color video signal, the CCD **10** would comprise three in-line CCD's each provided with a separate color filter, such as red, green and blue, and the outputs of each linear CCD would be coupled to separate processing circuits.

Timing of the various CCD and signal processing functions is determined by state control signals provided from state decoder **55**. These state control signals are illustrated in FIG. **2** showing a sequence of twenty operating states occurring during the processing of each imaging pixel in CCD **10**. Referring jointly to FIGS. **1** and **2**, a clock signal CK from clock generator **58** causes state counter **54** to produce a sequential count data signal SC applied to the input of state decoder **55** which operates to decode the state count SC to produce the state control signals. The phase control raw (PCR) signal is applied to AND circuit **61** during states **11** through **0** (next sequence) to perform transfer of the image pixel signal out of the CCD. Actual timing of the phase control signal operation is determined by the phase enable (PE) signal from a control word latch **60** as will be described in more detail subsequently. The reference sample-and-hold operation is performed by the RH state signal during states **6–9** and the video sample-and-hold is performed by the VH state signal during states **16–19**. The GOL state signal causes latching of the gain and offset data from memory **52** into data latch **29** during state **7**. State control signal ADC enables analog-to-digital converter **30** to convert the analog image pixel signal during state **4** and the FIFO write raw (FWR) state control signal is applied to AND circuit **62** to allow writing of pixel data into FIFO memory **45** when enabled by a FIFO write enable (FWE) signal from control word latch **60**. It will be appreciated that because of the serial nature of the signal processing, the illustrated state operations are not being performed on the same pixel data. For example, during a given pixel processing twenty state period, the enabled state signal PCR+PCE results in the transfer of pixel signal "n" out of CCD **10**. In turn, state signal GOL latches gain/offset data for pixel "n" which state signals RH and VH are currently sampling. State signal ADC causes A/D converter **30** to convert the previously sampled/compensated signal for pixel "n−1" and the enabled state signal FWR+FWE writes previously converted pixel data for pixel "n−1" into FIFO memory **45**.

Having described the general structure and operation of the CCD signal processing circuit, there will now be described the apparatus for controlling the operation of the linear CCD **10** in accordance with the invention. Means for supplying a bit map of control words to be used in controlling the operation of CCD **10** includes microprocessor **100** and buffer **53**. The control words each comprise programmably variable bit content defining pixel-by-pixel operating characteristics of the CCD **10**. The architecture of a 6-bit control word is set forth in Table I which summarizes the functions of the bits within the control word. As will be seen, for a CCD having a line of **530** imaging pixels, a bit map of **530** of these control words is used to control the operation of the CCD for one entire scan line of the CCD.

TABLE I

Bit	Name	Function
0	LP	Last Pixel - Reset pixel counter 50 when the last state signal LS is provided by state decoder
1	FWE	FIFO Write Enable - Allow FIFO write raw signal FWR from state decoder 55 to write data from A/D converter 30 into FIFO memory 45
2	PCE	Phase Clock Enable - Allow phase clock raw signal PCR from state decoder 55 to be sent to linear imager 10
3	TG	Transfer Gate - Transfer charge from the light detecting sites to the charge shifting structure of linear imager 10
4	EE	Exposure End - End the exposure cycle in linear imager 10
5	ES	Exposure Start - Start the exposure cycle in linear imager 10

The apparatus of the invention further includes memory means, including memory **52** for storing the bit map of control words at memory addresses corresponding to individual imaging pixels in CCD **10**. Address means, including pixel counter **50**, is provided for supplying a sequence of pixel counts corresponding to the individual imaging pixels in the CCD for use in accessing the stored bit map of control words on a pixel-by-pixel basis. To provide microprocessor **100** access to the memory **52**, the pixel counter **50** is disabled from counting and an address is loaded directly into pixel counter **50** by microprocessor **100**; then buffer **53** is enabled so that the microprocessor **100** can write data to memory **52** at the memory location specified by the address previously loaded into pixel counter **50**. To provide for multiple bit maps, two of the most significant bits (MSB) of the address data are provided from the microprocessor **100** to state decoder **55** via map latch **56** and latch **57** for use in selecting from within memory **52** the control word bit map to be used in controlling the operation of the CCD during generation of the next line of signal data in CCD **10**. It is noted that the "last state" bit (LS) of the state control signal from state decoder **55** is used to advance the count of the pixel counter **50** and the combination of a "last pixel" (LP) signal from latch **60** with the "last state" signal (LS) is used to clear the pixel counter and latch the MSB address data for the bit map to be used in pixel-by-pixel control of the next line of signal data generation in CCD **10**.

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