Sample-and-Hold Amplifiers

INTRODUCTION AND HISTORICAL PERSPECTIVE

The *sample-and-hold amplifier*, or SHA, is a critical part of most data acquisition systems. It captures an analog signal and holds it during some operation (most commonly analog-digital conversion). The circuitry involved is demanding, and unexpected properties of commonplace components such as capacitors and printed circuit boards may degrade SHA performance.

When the SHA is used with an ADC (either externally or internally), the SHA performance is critical to the overall dynamic performance of the combination, and plays a major role in determining the SFDR, SNR, etc., of the system.

Although today the SHA function has become an integral part of the *sampling* ADC, understanding the fundamental concepts governing its operation is essential to understanding ADC dynamic performance.

When the sample-and-hold is in the sample (or track) mode, the output follows the input with only a small voltage offset. There do exist SHAs where the output during the *sample* mode does not follow the input accurately, and the output is only accurate during the *hold* period (such as the AD684, AD781, and AD783). These will not be considered here. Strictly speaking, a sample-and-hold with good tracking performance should be referred to as a *track-and-hold* circuit, but in practice the terms are used interchangeably.

The most common application of a SHA is to maintain the input to an ADC at a constant value during conversion. With many, but not all, types of ADC the input may not change by more than 1 LSB during conversion lest the process be corrupted—this either sets very low input frequency limits on such ADCs, or requires that they be used with a SHA to hold the input during each conversion.

From a historial perspective, it is interesting that the ADC described by A. H. Reeves in his famous PCM patent of 1939 (Reference 1) was a 5-bit 6-kSPS counting ADC where the analog input signal drove a vacuum tube pulse-width-modulator (PWM) directly—the sampling function was incorporated into the PWM. Subsequent work on PCM at Bell Labs led to the use of electron-beam encoder tubes and successive approximation ADCs; and Reference 2 (1948) describes a companion 50-kSPS vacuum tube sample-and-hold circuit based on a pulse transformer drive circuit.

There was increased interest in sample-and-hold circuits for ADCs during the period of the late 1950s and early 1960s as transistors replaced vacuum tubes. One of the first analytical treatments of the errors produced by a solid-state sample-and-hold was published in 1964 by Gray and Kitsopolos of Bell Labs (Reference 3). Edson and Henning of Bell Labs describe the results of experimental work done on a 224-Mbps PCM system, including the 9-bit ADC and a companion 12-MSPS sample-and-hold. References 4, 5 , and 6 are representative of work done on sample-and-hold circuits during the 1960s and early 1970s.

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In 1969, the newly acquired Pastoriza division of Analog Devices offered one of the first commercial sample-and-holds, the SHA1 and SHA2. The circuits were offered on PC boards, and the SHA1 had an acquisition time of 2 µs to 0.01%, dissipated 0.9 W, and cost approximately $225. The faster SHA2 had an acquisition time of 200 ns to 0.01%, dissipated 1.7 W, and cost approximately $400. They were designed to operate with 12-bit successive approximation ADCs also offered on PC boards.

Modular and hybrid technology quickly made the PC board sample-and-holds obsolete, and the demand for sample-and-holds increased as IC ADCs, such as the industry-standard AD574, came on the market. In the 1970s and into the 1980s, it was quite common for system designers to purchase separate sample-and-holds to drive such ADCs, because process technology did not allow integrating them together onto the same chip. IC SHAs such as the AD582 (4-µs acquisition time to 0.01%), AD583 (6-µs acquisition time to 0.01%), and the AD585 (3-µs acquisition time to 14-bit accuracy) served the lower speed markets of the 1970s and 1980s.

Hybrid SHAs such as the HTS-0025 (25-ns acquisition time to 0.1%), HTC-0300 (200-ns acquisition time to 0.01%), and the AD386 (25-µs acquisition time to 16-bits) served the high-speed, high-end markets. By 1995, Analog Devices offered approximately 20 sample-and-hold products for various applications, including the following high-speed ICs: AD9100/AD9101 (10-ns acquisition time to 0.01%), AD684 (quad 1-µs acquisition time to 0.01%) and the AD783 (250-ns acquisition time to 0.01%).

However, ADC technology was rapidly expanding during the same period, and many ADCs were being offered with internal SHAs (i.e., *sampling* ADCs). This made them easier to specify and certainly easier to use. Integration of the SHA function was made possible by new process developments including high-speed complementary bipolar processes and advanced CMOS processes. In fact, the proliferation and popularity of sampling ADCs has been so great that today (2003), one rarely has the need for a separate SHA.

The advantage of a sampling ADC, apart from the obvious ones of smaller size, lower cost, and fewer external components, is that the overall dc and ac performance is fully specified, and the designer need not spend time ensuring that there are no specification, interface, or timing issues involved in combining a discrete ADC and a discrete SHA. This is especially important when one considers dynamic specifications such as SFDR and SNR.

Although the largest applications of SHAs are with ADCs, they are also occasionally used in DAC deglitchers, peak detectors, analog delay circuits, simultaneous sampling systems, and data distribution systems.

BASIC SHA OPERATION

Regardless of the circuit details or type of SHA in question, all such devices have four major components. The input amplifier, energy storage device (capacitor), output buffer, and switching circuits are common to all SHAs as shown in the typical configuration of Figure 1.

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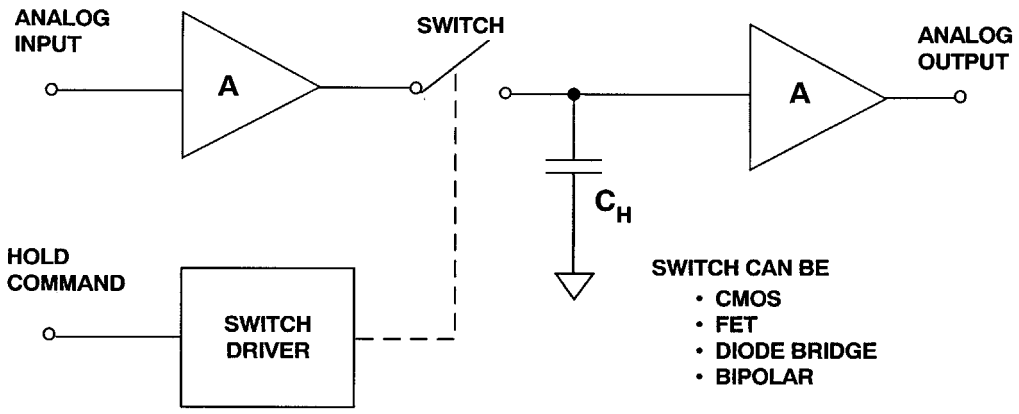

Figure 1: Basic Sample-and-Hold Circuit

The energy-storage device, the heart of the SHA, is a capacitor. The input amplifier buffers the input by presenting a high impedance to the signal source and providing current gain to charge the hold capacitor. In the *track* mode, the voltage on the hold capacitor follows (or tracks) the input signal (with some delay and bandwidth limiting). In the *hold* mode, the switch is opened, and the capacitor retains the voltage present before it was disconnected from the input buffer. The output buffer offers a high impedance to the hold capacitor to keep the held voltage from discharging prematurely. The switching circuit and its driver form the mechanism by which the SHA is alternately switched between track and hold.

There are four groups of specifications that describe basic SHA operation: track mode, track-to-hold transition, hold mode, hold-to-track transition. These specifications are summarized in Figure 2, and some of the SHA error sources are shown graphically in Figure 3. Because there are both dc and ac performance implications for each of the four modes, properly specifying a SHA and understanding its operation in a system is a complex matter.

SAMPLE MODE	SAMPLE-TO-HOLD TRANSITION	HOLD MODE	HOLD-TO-SAMPLE TRANSITION
STATIC: ◆ Offset ◆ Gain Error ◆ Nonlinearity	STATIC: ◆ Pedestal ◆ Pedestal Nonlinearity	STATIC: ◆ Droop ◆ Dielectric ◆ Absorption	
DYNAMIC: ◆ Settling Time ◆ Bandwidth ◆ Slew Rate ◆ Distortion ◆ Noise	DYNAMIC: ◆ Aperture Delay Time ◆ Aperture Jitter ◆ Switching Transient ◆ Settling Time	DYNAMIC: ◆ Feedthrough ◆ Distortion ◆ Noise	DYNAMIC: ◆ Acquisition Time ◆ Switching Transient

Figure 2: Sample-and-Hold Specifications

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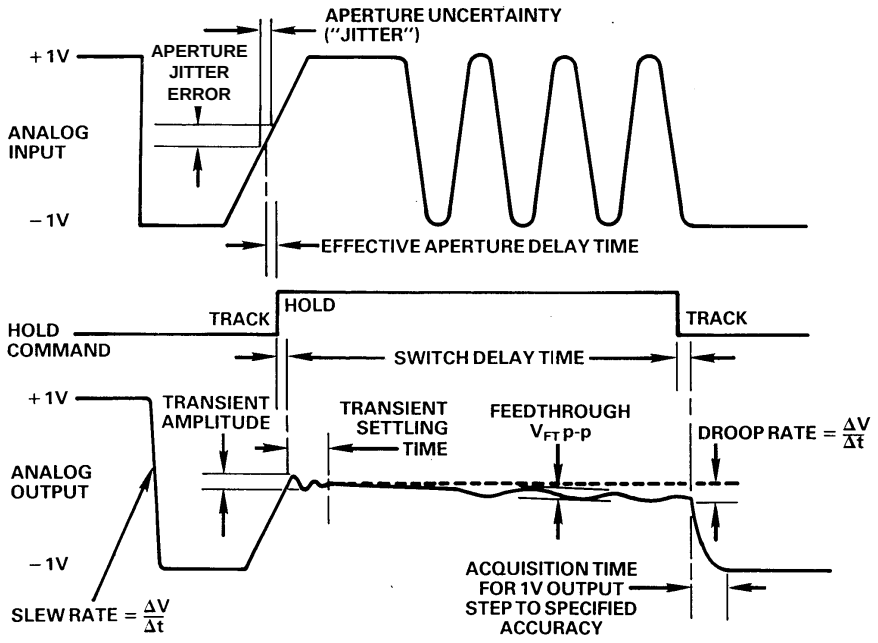

Figure 3: Some Sources of Sample-and-Hold Errors

TRACK MODE SPECIFICATIONS

Since a SHA in the sample (or track) mode is simply an amplifier, both the static and dynamic specifications in this mode are similar to those of any amplifier. (SHAs which have degraded performance in the track mode are generally only specified in the hold mode.) The principle track mode specifications are *offset*, *gain*, *nonlinearity*, *bandwidth*, *slew rate*, *settling time*, *distortion*, and *noise*. However, distortion and noise in the track mode are often of less interest than in the hold mode.

TRACK-TO-HOLD MODE SPECIFICATIONS

When the SHA switches from track to hold, there is generally a small amount of charge dumped on the hold capacitor because of non-ideal switches. This results in a hold mode dc offset voltage which is called *pedestal* error as shown in Figure 4. If the SHA is driving an ADC, the pedestal error appears as a dc offset voltage which may be removed by performing a system calibration. If the pedestal error is a function of input signal level, the resulting nonlinearity contributes to hold-mode distortion.

Pedestal errors may be reduced by increasing the value of the hold capacitor with a corresponding increase in acquisition time and a reduction in bandwidth and slew rate.

Switching from track to hold produces a transient, and the time required for the SHA output to settle to within a specified error band is called *hold mode settling time*. Occasionally, the peak amplitude of the switching transient is also specified.

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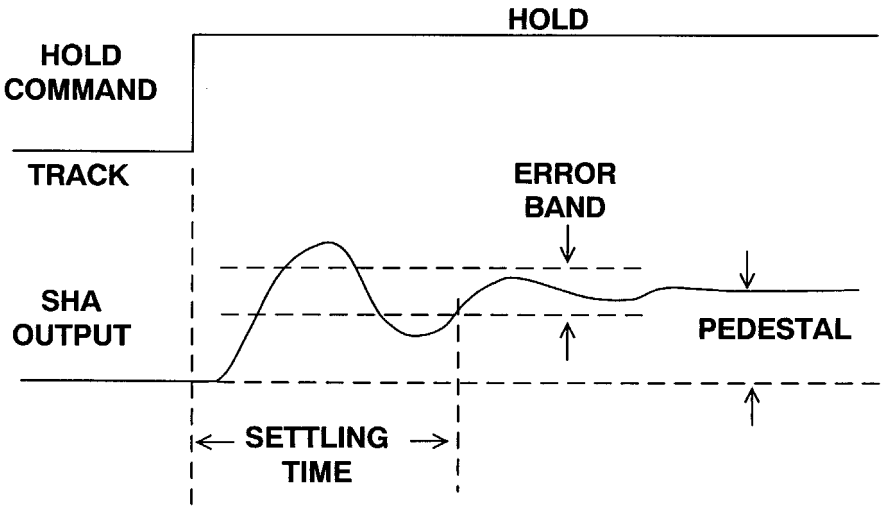

Figure 4: Track-to-Hold Mode Pedestal, Transient, and Settling Time Errors

Perhaps the most misunderstood and misused SHA specifications are those that include the word *aperture*. The most essential dynamic property of a SHA is its ability to disconnect quickly the hold capacitor from the input buffer amplifier. The short (but non-zero) interval required for this action is called *aperture time*. The various quantities associated with the internal SHA timing are shown in the Figure 5.

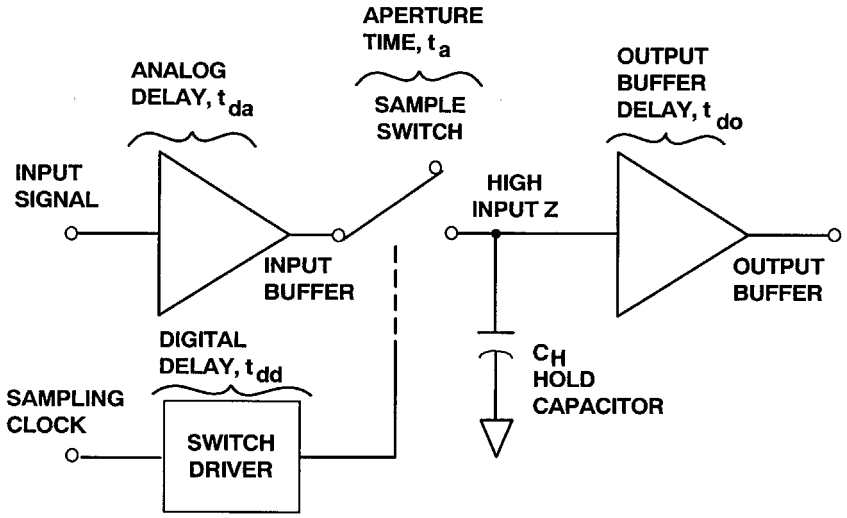

Figure 5: SHA Circuit Showing Internal Timing

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