UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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APPLE INC.,

Petitioner,

v.

PAPST LICENSING GMBH & CO. KG,

Patent Owner.

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Case IPR2016-01840
Patent 9,189,437 B2

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Before JONI Y. CHANG, JAMES B. ARPIN, and MIRIAM L. QUINN,
Administrative Patent Judges.

ARPIN, *Administrative Patent Judge.*

DECISION
Denying Institution of *Inter Partes* Review
37 C.F.R. § 42.108

I. INTRODUCTION

Apple Inc. ("Petitioner") filed a Petition requesting *inter partes* review of claims 1, 4–6, 9–16, 18, 30, 34, 43, and 45 ("the challenged claims") of U.S. Patent No. 9,189,437 B2 (Ex. 1001, "the '437 patent"). Paper 2 ("Pet."), 1. Papst Licensing GmbH & Co., KG ("Patent Owner"), filed a Preliminary Response. Paper 9 ("Prelim. Resp."). Under 35 U.S.C. § 314, an *inter partes* review may not be instituted "unless . . . the information presented in the petition . . . shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition."

For the reasons that follow, we do not institute an *inter partes* review as to any of the challenged claims.

A. *Related Matters*

Petitioner indicates that the '437 patent is involved in *Papst Licensing GmbH & Co., KG v. Apple Inc.*, Case No. 6-15-cv-01095 (E.D. Tex.); *Papst Licensing GmbH & Co., KG v. LG Electronics, Inc.*, Case No. 6-15-cv-01099 (E.D. Tex.); *Papst Licensing GmbH & Co., KG v. ZTE Corp.*, Case No. 6-15-cv-01100 (E.D. Tex.); *Papst Licensing GmbH & Co., KG v. Samsung Electronics Co. Ltd.*, Case No. 6:15-cv-01102 (E.D. Tex.); and *Papst Licensing GmbH & Co., KG v. Lenovo (United States) Inc.*, Case No. 6-15-cv-01111 (E.D. Tex.). Pet. 2; *see* Paper 8, 4–5. In addition to the instant Petition, various petitioners have filed at least seven other petitions seeking *inter partes* review of claims of the '437 patent:

| Proceeding	Petitioner	Status
IPR2016-01733	Samsung Electronics Co. Ltd.	Review Instituted
IPR2016-01841	Apple Inc.	Review Denied
IPR2016-01842	Apple Inc.	Pending
IPR2016-01844	Apple Inc.	Review Denied
IPR2017-00156	Apple Inc.	Review Denied
IPR2017-00712	ZTE Corp.	Pending
IPR2017-01038	LG Electronics, Inc.	Review Instituted; Joined with IPR2016-01733

See Pet. 2; Paper 8, 2–4. More than forty petitions have been filed by various petitioners challenging claims of five related patents: U.S. Patent Nos. 6,470,399 B1; 6,895,449 B2; 8,504,746 B2; 8,966,144 B2; and 9,189,437 B2, owned by Patent Owner. *See LG Electronics, Inc. v. Papst Licensing GmbH & Co.*, Case IPR2017-01038, Paper 5, 1–2.

B. The '437 Patent

The '437 patent describes an interface device for communication between a computer host device and a data transmit/receive device (e.g., a multi-meter, transmitting measured data to a computer). Ex. 1001, 1:18–22, 1:54–57. According to the '437 patent, using a specific driver to match very closely to an individual host system would achieve high data transfer rates across the interface, but the specific driver cannot be used with other host systems. *Id*. at 2:4–19. Several solutions to this problem were known in the art. *Id*. at 2:20–3:25. For example, IOtech offered an interface device for laptops, using a plug-in card for converting the personal computer memory card association ("PCMCIA") interface into a known standard interface (i.e., IEEE 1284). *Id*. at 2:20–29. The plug-in card provided a printer interface

for enhancing data transfer rates. *Id.* at 2:29–33. In another example, a floppy disk drive interface was used for connecting a host device to a peripheral device. *Id.* at 3:10–14. The interface appeared as floppy disk drive to the host, allowing a floppy disk drive and another peripheral device to be connected to the host device. *Id.* at 3:17–19.

The '437 patent indicates that the purported "invention is based on the finding that both a high data transfer rate and host device-independent use can be achieved if a driver for an input/output device customary in a host device" is utilized. *Id.* at 3:33–37. Figure 1 of the '437 patent, reproduced below, illustrates a block diagram of an interface device.

Fig. 1
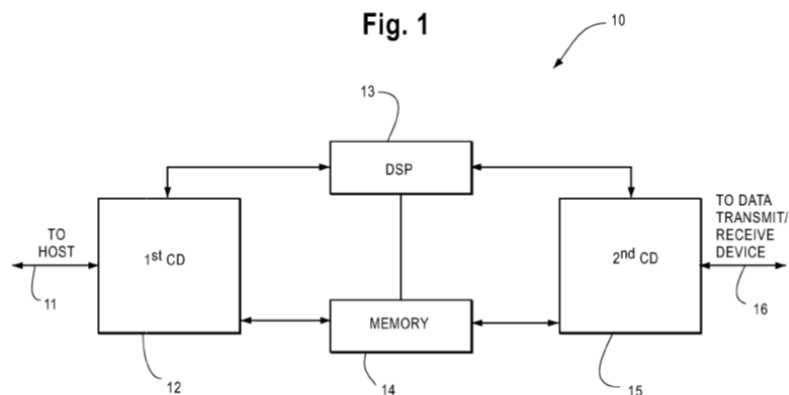
As shown in Figure 1, interface device 10 connects to a host device via host line 11, and to a data transmit/receive device via output line 16. *Id.* at 4:62–5:10. Interface device 10 includes first connecting device 12, second connecting device 15, digital signal processor 13, and memory means 14. *Id.* Output line 16 connects interface 10 to a data transmit/receive device and implements an analog input, for example, with a sampling rate of 1.25 MHz and quantization of 12 bits, such as by means of the blocks 1505-1535, as depicted in Figure 2. *Id.* at 9:41–44. By means of

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programmable amplifier 1525, depicted in Figure 2 of the '437 patent, multiple channels can be programmed independently of each other, for example, in voltage ranges up to a maximum of ±10 V. *Id*. at 9:45–48. In a preferred embodiment, the interface device is attached to a host device via a multi-purpose interface—e.g., a small computer systems interface ("SCSI") interface—which includes both an interface card and the driver for the interface card. *Id*. at 3:51–57, 8:42–46. According to the '437 patent, SCSI interfaces were known to be present on most host devices or laptops. *Id*. at 8:42–46. By using a standard interface of the host device and by simulating an input/output device to the host device, the interface device "is automatically supported by all known host systems without any additional sophisticated driver software." *Id*. at 11:38–44.

C. Illustrative Claim

Of the challenged claims, claims 1 and 43 are independent. Claims 4–6, 9–16, 18, 30, and 34 depend directly from claim 1; and claim 45 depends directly from claim 43. Claims 1 and 43 are illustrative:

> 1. An analog data generating and processing device (ADGPD), comprising:
>
> an input/output (i/o) port;
>
> a program memory;
>
> a data storage memory;
>
> a processor operatively interfaced with the i/o port, the program memory and the data storage memory;
>
> *wherein the processor is adapted to implement a data generation process by which analog data is acquired from each respective analog acquisition channel of a plurality of independent analog acquisition channels, the analog data*

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