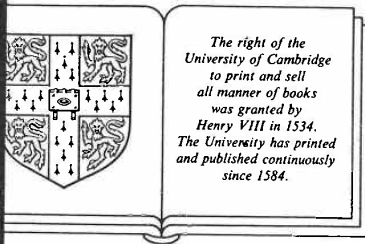


THE ART OF ELECTRONICS

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In the second circuit, an enhancement-mode MOSFET does the switching. Here the gate circuit is simplified, and the circuit works with signals of either polarity. If the output is known to be of positive polarity only, the gate signal can go from ground to some positive voltage, with the body terminal grounded.

See Section 6.18 for an interesting circuit modification that eliminates the effects of leakage currents in the FET.

Multiplexers

A nice application of FET switches is the "multiplexer" (or MUX), a circuit that allows you to select any of several inputs, as specified by a digital control signal. Since a FET that is ON looks like a small resistor (R_{ON}), such a circuit is an analog (or linear) multiplexer, and it will faithfully pass through to the output the actual voltage present on the selected input. Figure 6.41 shows the basic

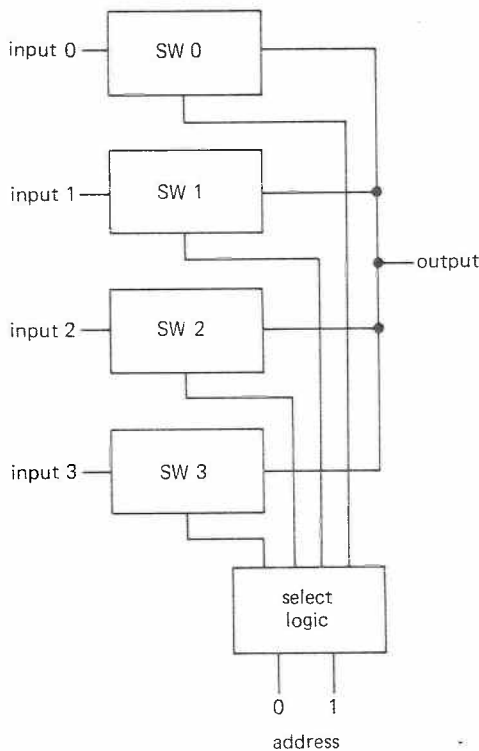


Figure 6.41

scheme. Each of the switches SW0 through SW3 is a CMOS transmission gate of the type discussed in the preceding section. The "select logic" decodes the address and "enables" (jargon for "turns on") the

addressed switch only, disabling the remaining switches. Such a multiplexer will usually be used in conjunction with digital circuitry that will generate the appropriate addresses. A typical situation might involve a data-acquisition instrument in which a number of analog input voltages must be sampled in turn, converted to digital quantities, and recorded (or become the input to some on-line computations done by associated computing apparatus).

Since transmission gates are bidirectional, an analog multiplexer such as this is also a "demultiplexer": A signal can be fed into the "output" and will appear on the selected "input." When we discuss digital circuitry in Chapters 8 and 9, you will see that an analog multiplexer such as this can also be used as a "digital multiplexer/demultiplexer," since logic levels are, after all, nothing but voltages that happen to be interpreted as 1s and 0s.

Typical of analog multiplexers are the 506, 507, and 508 series and the IH6108 and IH6116 types, 8- or 16-input MUX circuits that accept TTL or CMOS logic levels for the address inputs and operate with analog voltages up to 35 volts. The 4051-4053 devices in the CMOS digital family are analog multiplexers/demultiplexers with up to 8 inputs, but with 15 volt pp maximum signal levels.

Sample-and-hold circuits

FET switches are the basic ingredients of "sample-and-hold" and "peak-detector" circuits. Figure 6.42 shows the idea. IC₁ is a follower to provide a low-impedance replica of the input. Q₁ passes the signal through

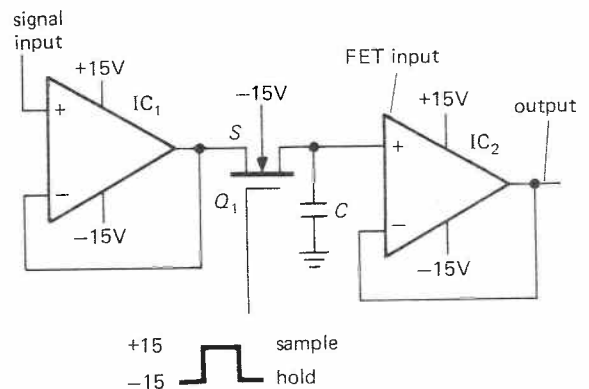


Figure 6.42

during "sample" and disconnects it during "hold." Whatever signal was present when Q_1 was turned OFF is held on capacitor C . IC_2 is a high-input-impedance follower (FET inputs), so that capacitor current during "hold" is minimized. The value of C is a compromise: Leakage currents in Q_1 and the follower cause C 's voltage to "droop" during the "hold" interval, according to $dV/dT = I_{leakage}/C$. Thus C should be large to minimize droop. But Q_1 's ON resistance forms a low-pass filter in combination with C , so C should be small if high-speed signals are to be followed accurately. IC_1 must be able to supply C 's charging current $I = CdV/dT$ and must have sufficient slew rate to follow the input signal. In practice, the slew rate of the whole circuit will be limited by IC_1 's output current and Q_1 's ON resistance. See Section 6.18 for an improved sample-and-hold circuit.

EXERCISE 6.7

Suppose IC_1 can supply 10mA of output current, and $C = 0.01\mu F$. What is the maximum input slew rate the circuit can accurately follow? If Q_1 has 50 ohms ON resistance, what will be the output error for an input signal slewing at $0.1V/\mu s$? If the combined leakage of Q_1 and IC_2 is 1nA, what is the droop rate during the "hold" state?

FETs are useful in peak-detector circuits, in which the highest value of a waveform is held on a capacitor. Figure 6.43 shows one

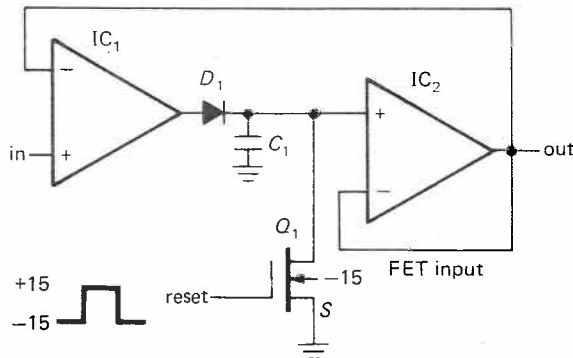


Figure 6.43

possibility. IC_1 drives C_1 to the highest point reached by the input waveform since the last reset pulse applied to Q_1 's gate. IC_2 buffers the output. IC_1 could take its feedback from

C_1 , but the connection shown makes it easier to eliminate offsets, at the risk of reduced stability. IC_2 should be a FET-input op-amp, and D_1 should be a low-leakage diode, to minimize droop.

6.15 Limitations of FET switches

Speed

FET switches have ON resistances R_{ON} of 25 to 200 ohms. In combination with substrate and stray capacitances, this resistance forms a low-pass filter that limits operating speeds to frequencies of a few megahertz or less. FETs with lower R_{ON} tend to have larger capacitance (up to 50pF with some MUX switches), so no gain in speed results.

ON resistance

CMOS switches operated from a relatively high supply voltage (15V, say) will have low R_{ON} over the entire signal swing, because one or the other of the transmission FETs will have a forward gate bias at least half the supply voltage. However, when operated with lower supply voltages, the switch's R_{ON} value will rise, the maximum occurring when the signal is about halfway between the supply and ground (or halfway between the supplies, for dual-supply voltages). Figure 6.44 shows why. As V_{DD} is reduced, the

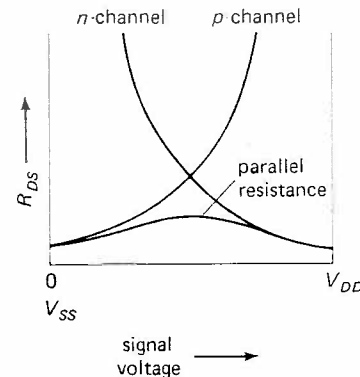


Figure 6.44

FETs begin to have significantly higher ON resistance at $V_{GS} = 0.5V_{DD}$, since for enhancement-mode FETs V_T is at least a few volts, and a gate-source voltage of as much

of 1% in each section would result in an overall feedthrough of 0.01% (-80dB) in the open state. If R_{ON} is 100 ohms, the signal is essentially unattenuated (99.7% of its input amplitude) when the switch is closed, which means that variations of R_{ON} with signal swing contribute negligible nonlinearity. To get equivalent feedthrough performance with a single stage would require a load resistor of 1.0k, which would result in unsatisfactory attenuation in the closed state (10% attenuation), not to mention nonlinearity due to changing R_{ON} with signal level.

The second circuit does the same sort of thing, using FET switches to short the signal to ground. In this case the use of several stages allows you to keep the series resistors reasonably small.

A third possibility is to use a pair of switches, one in series with the signal and one between the output and ground, as shown in the third circuit in Figure 6.54. By alternately enabling the two switches, you get the best of both worlds, i.e., low feedthrough in the OFF state and good linearity with negligible attenuation in the ON state. CMOS SPDT switches with controlled break-before-make are available commercially in single packages; in fact, you can get a pair of SPDT switches in a single package. Examples are the DG188, IH5042, and IH5142, as well as the DG191, IH5043, and IH5143 (dual SPDT units). Because of the availability of such convenient CMOS switches, it is easy to use this SPDT configuration to achieve excellent performance.

□ **Another look at the integrator**

In the integrator circuits in Section 6.14, drain-source leakage sinks a small current from the summing junction when the FET is OFF. With an ultra-low-input-current op-amp and low-leakage capacitor, this can be the dominant error in the integrator. Figure 6.55 shows a clever circuit solution. Both n -channel FETs are switched together, but it may be desirable to switch Q_1 with gate voltages of zero and +15 volts so that all the gate leakage effects are eliminated during the OFF state (zero gate voltage). In the ON state the capacitor is discharged as before, but with twice R_{ON} . In the OFF state,

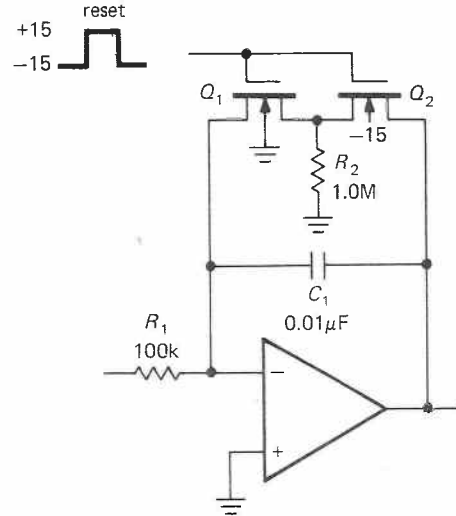


Figure 6.55

Q_2 's small leakage passes to ground through R_2 with negligible drop. There is no leakage current at the summing junction because Q_1 's source, drain, and substrate are all at the same voltage. Compare this circuit with the "zero-leakage" peak detector in Section 3.15.

EXERCISE 6.8

Assume that Q_1 and Q_2 in Figure 6.55 behave like 10,000M resistors when OFF. Calculate the rate at which the integrator's output will drift, due to FET leakage, for both this configuration and the simple FET reset switch circuit (Fig. 6.40), when the integrator's output is at +10 volts.

□ **Another look at sample-and-hold circuits**

Figure 6.56 shows an improved sample-and-hold circuit. Q_2 and Q_3 are parallel complementary switches, maintaining low ON resistance for all signal levels. Q_1 is turned on during HOLD to prevent saturation in the input op-amp, with its usual problems of slew-rate-limited recovery time. Q_1 could be replaced by a pair of back-to-back diodes. The second op-amp should have a FET input for low droop.

The same trick used to eliminate the effects of drain-source leakage in the integrator (Fig. 6.55) can be used to advantage here. There's a hint in Exercise 6.9.

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