Filed on behalf of TQ Delta LLC
By: Peter J. McAndrews
McAndrews, Held & Malloy, Ltd.
500 W. Madison St., 34th Floor
Chicago, IL 60661
Tel: 312-775-8000
Fax: 312-775-8100
E-mail: pmcandrews@mcandrews-ip.com

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

CISCO SYSTEMS, INC.,
Petitioner,

v.

TQ DELTA, LLC,
Patent Owner.

Case IPR2016-01760
Patent No. 9,094,268

PATENT OWNER'S MOTION FOR OBSERVATION

Patent Owner TQ Delta, LLC ("Patent Owner") submits this motion for observation regarding cross-examination of Dr. Sayfe Kiaei, a reply declarant for Petitioner.

Observation #1: In Ex. 2017, on page 90, line 19 to page 91, line 7, Dr. Kiaei testified that the superframe structure and initialization described in the ADSL Standard, Ex. 1009 are ADSL standard requirements: "So the framing structure is one of those ADSL standard requirements, and initialization exchange and all that stuff is part of that as well." This testimony is relevant to Dr. Kiaei's declaration testimony that "even if Yamano's burst-mode protocol does not result in a continuous stream of superframes [as required by the ADSL standard], a POSITA would still find Yamano and the ANSI standard compatible." (Ex. 1012 at ¶ 23). The testimony is relevant because it contradicts Dr. Kiaei declaration testimony and Petitioner's Reply assertion that Yamano's burst-mode embodiment is compatible with the ADSL standard. *See* Reply at 19-20.

Observation #_2: Dr. Kiaei admits that the objective of synchronization is to lock the frequency of the transmitter and the frequency of the receiver. Ex. 2017, at page 53, line 25 to page 54, line 3 ("**THE WITNESS**: In line 44 [of col. 5 of the '404 patent] its talking *about locking the frequencies* . . . . The objective of this whole operation is to *lock the frequency of the transmitter and the frequency of the*

receiver.")[1]. Separately, Dr. Kaiei admits that an embodiment described in the'268 patent, performs synchronization of the frequency of the master clock of the transmitter with the CPE by using a PLL to minimize the difference/error between the master clock in the transmitter and the clock in the receiver. Ex. 2017, at page 50, line 19 ("**THE WITNESS**: the PLL, that is one example of synchronization used here."); *id*. at page 54, line 14 to page 55, line 5 ("**THE WITNESS**: The PLL is a block that the input of it is a reference clock . . . And *the output signal has a frequency which is related to the input frequency*. So what [the PLL] tries to do is to *minimize the difference* between the output frequency in a relationship . . . [The PLL] *does look at a difference in the error in terms of output frequency and the input frequency*."); *id*. at page 55, lines 9 to 12 ("[The patent] is talking about the pilot tone . . . which has a pure tone of fixed frequency and phase. It's *synchronizing it with the receiver to make sure that the frequency of it is the same* . . . .") (emphasis added); *See also*, Ex. 2017, at pages 59, line 24-page 60, line 25 (confirming PLL corrects errors as set forth in Ex. 2016 at p. 184).

This testimony is relevant because it undermines Dr. Kiaei declaration testimony that "[t]he claims at issue . . . do [not] require correcting errors or differences in the timing between transceivers." *See* Ex. 1012 at ¶ 5. This

[1] US Patent 9,094,268 and US Patent 8,611,404 share a common specification.

testimony is further relevant because it confirms Dr. Chrissan's opinions set forth in his declaration and deposition testimony regarding the proper construction of the claimed "maintaining synchronization with a second transceiver." Ex. 2005 at ¶¶ 83-86 and Ex. 1011 at 63:4 – 69:1 and 83:11 – 89:6.

Observation # 3: Dr. Kiaei admits that the objective of synchronization in the context of the '268 patent specification is to lock the frequency of the transmitter and the frequency of the receiver. Ex. 2017, at page 53, line 25 to page 54, line 3 ("**THE WITNESS**: In line 44 [of col. 5 of the '404 patent] its talking *about locking the frequencies* . . . . The objective of this whole operation is to *lock the frequency of the transmitter and the frequency of the receiver*."). Dr. Kiaei testified that in Yamano "[t]he synchronization is done to synchronize periodically enabling the non-idle detector such that the non-idle detector is activated and is enabled by the time that the non-idle detector signal arrives and is able to enable that to perform the -- to indicate there is a packet data coming or not." Ex. 2004, at page 174, lines 18-24. Dr. Kiaei's testimony is relevant because it supports Patent Owner and its Expert's contention that Yamano does not disclose "maintaining synchronization with a second transceiver," as this limitation is understood in view of the specification. Response at pages 29-34.

Observation # 4: Dr. Kiaei agrees that bit allocation and fine gain parameters are

derived, in part, from signal-to-noise ratio, that in turn is, in part, determined from attenuation that, in turn, is representative of the electronic characteristic of the loop. Ex. 2017, at page 14, lines 10-16 ("**A**. Yes if the line resistance changes, the attenuation of the line will change."); Ex. 2017, at page 15, lines 14-17 ("**THE WITNESS**: . . . one of the parameters that determines the signal-to-noise ratio is the attenuation of the line."); and Ex. 2017, at page 17, lines 4-7 ("[f]rom the signal-to-noise ratio and other parameters, [the modem] determines the bits and gains and so forth."). Dr. Kiaei maintains that Bowie's stored loop characteristics include not just parameters that are values representing the electronic characteristics of the particular wire loop but also include parameters like "signal to noise ratio and so forth, including bits and gains" that are, in part, a function of the electronic characteristics of the particular wire loop. Ex. 2017, at page 20, lines 5-8; Ex. 2004, page 56, lines 16-17 ("**A**. The number of bits is part of the characteristics -- the loop characteristics."). However, in *Wi-Lan Inc. v. Westell Tech., Inc.*, a patent infringement case involving Bowie, Ex. 1005, and where Dr. Kiaei was retained as plaintiff's expert witness (*see* Ex. 1004 at. 4), the court interpreted Bowie's loop characteristics as "values representing the electronic characteristics of the particular wire loop" and rejected a construction that Bowie's loop characteristics are "values that are a function of the electronic characteristics

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