UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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CISCO SYSTEMS, INC.,
Petitioner

v.

TQ DELTA LLC,
Patent Owner

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**SECOND DECLARATION OF DR. SAYFE KIAEI
UNDER 37 C.F.R. § 1.68 IN SUPPORT OF PETITIONER'S REPLIES
IN IPR2016-01466 AND IPR2016-01760**

Ex. 1012

Table of Contents

Ex. 1012

I. INTRODUCTION

I, Sayfe Kiaei, do hereby declare as follows:

1. I previously submitted different Declarations as Exhibit 1003 in each
of IPR2016-01466 and IPR2016-01760, setting forth my background and
credentials and my curriculum vitae which provides further details.

2. I submit this Declaration in reply to the Declaration of Douglas
Chrissan, PhD, filed as Ex.2005 in IPR2016-01466 and Ex.2005 in IPR2016-
01760, and the Board's Institution Decisions in each case.

II. CLAIM CONSTRUCTION

A. "maintaining synchronization with a second transceiver" / "synchronization signal"

1. Dr. Chrissan's constructions are not the broadest reasonable.

3. I understand Dr. Chrissan to have provided substantially similar
constructions for these terms in IPR2016-01760 pertaining to U.S. Patent No.
9,094,268 ("the '268 patent") and IPR2016-01466 pertaining to U.S. Patent No.
8,611,404 ("the '404 patent"). I understand that the '268 and '404 patents are part
of the same patent family and share the substantially same specification.

4. Dr. Chrissan concluded that the term "maintaining synchronization
with a second transceiver" as defined by the specification of the '268 patent is
"*maintaining a timing relationship between two transceivers by correcting errors*

Ex. 1012

or differences in the timing of the timing reference of the transceiver and a timing

reference of a second transceiver." IPR2016-01760, Ex.2005, ¶83. Similarly, Dr.

Chrissan concluded that the term "synchronization signal" as defined by the

specification of the '404 patent is "*a signal used to maintain a timing relationship*

between transceivers by correcting errors or differences between a timing

reference of the transmitter of the signal and a timing reference of the receiver of

the signal." IPR2016-01466, Ex.2005, ¶81. A person of ordinary skill in the art

("POSITA") would not understand either of these constructions to be the broadest

reasonable in light of the specification.

5.   The claims at issue never limit synchronization to any specific type

and much less do they require correcting errors or differences in the timing

between transceivers. Although the patents at issue disclose using "a pure tone of

fixed frequency and phase which is synchronized with the Master Clock in the

transmitter," they broadly recognize that "[o]ther forms of timing signal may, of

course, be used" for synchronization. Ex.1001, 5:47-50. Since the specification

encompasses other forms of timing signals for synchronization and not just a pure

tone, a POSITA would have understood that the claims are not limited to

correcting errors or differences in the timing references of the transmitter and

receiver, as Dr. Chrissan states.

6.   Accordingly, it is my opinion that Dr. Chrissan's proposed

interpretation is not the broadest reasonable in light of the specification. As I have

previously stated in my prior declarations, a POSITA would understand that the

broadest reasonable interpretation for these terms includes "*maintaining a timing

relationship between transceivers*." IPR2016-01466, Ex. 1003, ¶56.

2.   The specification discloses both frame synchronization and timing synchronization.

7.   I agree with Dr. Chrissan that the patent specifications discloses both

frame synchronization and timing synchronization. *See* IPR2016-01760, Ex.2005,

¶81; IPR2016-01466, Ex.2005, ¶82. Frame synchronization is performed in full

power mode when a transceiver "receives … a plurality of superframes" that

comprise "a plurality of data frames followed by a synchronization frame."

IPR2016-01466, Ex.1001, 10:30-32. Frame synchronization also provides for

timing synchronization. IPR2016-01760, Ex.2008, 62; IPR2016-01466, Ex.1007,

62 (sections 6.9.1.2 & 6.9.3). Timing synchronization, however, can be performed

in either full power mode or low power mode by reception of a "synchronization

signal." *See* IPR2016-01466, Ex.1001, 10:33, 39-40. Consequently, the

construction of "synchronization signal" in the claims must be broad enough to

include timing synchronization rather than just frame synchronization.

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