## 12.9 Timing

**12.9.1 Overview.** The successful interconnection of multivendor system components mandates that delay and bit loss be allocated fairly and realistically among the various system elements. The balance of this section defines the upper limits of delay and bit loss allocated to each component. These values allow proper operation with the worst-case system configuration of five levels of hubs, special links, maximum-length cable segments throughout the network, and colliding DTEs at extremes of the network.

**12.9.2 DTE Timing.** DTE Initial Transmit Delay is the time from the first full transition (due to the first OUTPUT_UNIT of preamble) from the MAC to the first full transition (after startup bit loss, if any) at the MDI. This delay shall not exceed 3BT. The start bit loss shall not exceed 1 bit.

DTEs shall correctly receive frames that are preceded by 13 or more bits of preamble plus 8 bits of <sfd>.

There is a delay between the reception of signal at the PMA input of a DTE and operation of the deferral process in the MAC. Therefore, there is a window in which a DTE may fail to defer to a transmission even after it has arrived at the input. The DTE Deference Delay is the time from the receipt of the first transition of the preamble at the MDI until the last moment that the DTE might start transmitting at the MDI. This delay includes the following components:

(1) The delay from the first input transition at the MDI to CARRIER_ON at the PLS-MAC interface
(2) The delay through the MAC processes from CARRIER_ON to the last moment that a new transmission would miss being deferred
(3) The delay from the first OUTPUT_UNIT at the MAC-PLS interface to the first output transition at the MDI

The DTE Deference Delay shall be no more than 21BT.

The DTE Collision Shutdown Delay is the time from the first CVL or CVH arriving at the MDI of a transmitting DTE until that DTE transmits IDL at that interface. This time shall be no more than 26BT + jamSize=58BT. This limit shall not start until after the <sfd> has been transmitted.

**12.9.3 Medium Timing.** The Medium Transit Delay is the time from when a signal enters the medium until that signal leaves the medium. This delay shall not exceed 4BT.

**12.9.4 Special Link Timing.** The Special Link Transit Delay is the time from when a signal enters a special link until that signal leaves the special link. This delay shall not, exceed 15BT. The preamble leaving a special link shall be no more than 2 bit cells longer than the preamble sent to that special link and no more than 1 bit cell shorter than the preamble sent to that special link. For the purposes of these limits only, the first bit transmitted shall be considered part of the silence of the preceding IDL unless it meets the requirements for the succeeding bits specified in 12.5.3.1.1 and 12.5.3.1.2.

**12.9.5 Hub Timing.** Hub Startup Delay is the time from when the first bit cell of the preamble arrives at a hub until the first bit cell (also preamble) leaves that hub. This time shall be no greater than 12BT. The preamble sent by a hub shall be no more than 1 bit cell longer than the preamble sent to that hub or more than 4 bit cells shorter than the preamble sent to that hub. For the purposes of these limits only, the first bit transmitted shall be considered part of the silence of the preceding IDL unless it meets the requirements for the succeeding bits specified in 12.5.3.1.1 and 12.5.3.1.2.

Hub Idle Collision Startup Delay applies to any case in which CP arrives preceded by fewer (or no) bit times of preamble than the Hub Startup Delay. The time from arrival of the first bit cell (either preamble or CP) until the first bit cell leaves the hub shall be no greater than 12BT.

Hub Transit Delay is the time from the arrival of any bit cell at a hub to the transmission of the corresponding bit cell from the hub. This delay shall not exceed 9BT, excluding the cumulative effects of clock tolerance.

The transit (propagation) delay between the upward and downward sides of the Header Hub shall be negligible.

Hub Delay Stretch/Shrink is the increase or decrease in a hub's transit delay due to the effects of differing clock rates. The clock rate tolerance of 0.01% specified in 12.3.2.4.1 and the maximum frame size of 1518 octets specified in 4.4.2.2 yield a maximum stretch or shrink of $(56 + 8 + 1518 \cdot 8) \cdot 0.01\% \cdot 2 < 3BT$, both at any given hub and through an entire network.

Hub Collision Detect Delay is the time required for a hub to detect multiple incoming signals and initiate transmission of CP. The time until transmission of the first CVH or CVL shall be no greater than 21BT.

Hub Active Collision Startup Delay is the time from the arrival of the first CVH or CVL of a CP pattern at a hub that is repeating bit cells until transmission of the first CVH or CVL from the hub. This delay shall be no greater than 12BT in either the upward or downward direction.

Hub Collision Shutdown Delay is the time from IDL arriving at a hub that is passing on or generating CP until that hub starts transmitting IDL. This delay shall be limited to 9BT. The limit is relaxed to 25BT, however, for the upward side of a hub that is generating CP. This extra allowance is made to avoid requiring implementation of a separate <etd> detection mechanism in each port of the hub.

**12.10 Safety.** Implementors are urged to consult the relevant local, national, and international safety regulations to ensure compliance with the appropriate standards. EIA CB8-1981 (see Annex [12]) provides additional guidance concerning many relevant regulatory requirements.

Sound installation practice, as defined by applicable codes and regulations, shall be followed. ECMA-97 (see Annex [11]) describes safety requirements for local area networks.

**12.10.1 Isolation.** Each PMA/MDI interface lead shall be isolated from frame ground. This electrical separation shall withstand at least one of the following electrical strength tests:

(1) 1500 V (rms) at 50 to 60 Hz for 60 s, applied as specified in Section 5.3.2 of IEC Publication 950 [8].

(2) 2250 V (dc) for 60 s, applied as specified in Section 5.3.2 of IEC Publication 950 (see Reference [8]).

(3) A sequence of ten 2400 V impulses of alternating polarity, applied at intervals of not less than 1 s. The shape of the impulses shall be 1.2/50 $\mu$s (1.2 $\mu$s virtual front time, 50 $\mu$s virtual time of half value), as defined in IEC Publication 60 (see Reference [11]).

There shall be no insulation breakdown, as defined in Section 5.3.2 of IEC Publication 950 (see Reference [8]), during the test. The resistance after the test shall be at least 2 MΩ, measured at 500 V (dc).

**12.10.2 Telephony Voltages.** The use of building wiring brings with it the possibility of wiring errors that may connect telephony voltages to 1BASE5 equipment. Other than voice signals (which are very low voltage), the primary voltages that may be encountered are the "battery" and ringing voltages. Although there is no universal standard that constrains them, the following maximums generally apply:

(1) Battery voltage to an on-hook telephone line is about –56 V (dc) applied to the line through a balanced 400 Ω source impedance. This voltage is used to power the telephone instrument and detect the off-hook condition. Source inductance can cause large spikes on disconnect.

(2) Battery voltage to an off-hook telephone line is also about –56 V (dc) applied to the line through a balanced 400 Ω source impedance, but most of the voltage appears across the source impedance because the telephone instrument's impedance is relatively much lower.

(3) Ringing voltage is a composite signal. The first portion can be up to 175 V peak at 20 to 66 Hz, limited by a 100 Ω source resistance or a 400 to 600 Ω source inductive impedance. The second portion is –56 V (dc) limited by a 300 to 600 Ω source impedance. Large spikes can occur at the start and end of each ring.

Although 1BASE5 equipment is not required to survive such wiring hazards without damage, application of any of the above voltages shall not result in any safety hazard.

NOTE: Wiring errors may impose telephony voltages differentially across the 1BASE5 transmitters or receivers. Because the termination resistance likely to be present across a receiver's input is of substantially lower impedance than an off-hook telephone instrument, however, receivers will generally appear to the telephone system as off-hook telephones. Full ring voltages, therefore, will be applied for only short periods of time. Transmitters that are coupled using transformers will similarly appear like off-hook telephones (though perhaps a bit more slowly) due to low resistance of the transformer coil.

# 13. System Considerations for Multisegment 10 Mb/s Baseband Networks

**13.1 Overview.** This section provides information on building multisegment 10 Mb/s baseband networks within a single collision domain. The proper operation of a CSMA/CD network requires network size to be limited to control round-trip propagation delay to meet the requirements of 4.2.3.2.3 and 4.4.2.1, and the number of repeaters between any two Data Terminal Equipments (DTEs) to be limited in order to limit the shrinkage of the interpacket gap as it travels through the network. This section applies only to networks that contain 10BASE-T segments.

NOTE: Information on 10BASE-T is included to begin the process of developing this section. It is intended that 8.6.1 and 10.7.1 be merged into this section in the future and that any new 10BASE segments be added to this section.

**13.2 Definitions.** Terminology used in Section 13 is defined here:

**collision domain.** A single CSMA/CD network. If two or more Media Access Control (MAC) sublayers are within the same collision domain and both transmit at the same time, a collision will occur. MAC sublayers separated by a repeater are within the same collision domain. MAC sublayers separated by a bridge are within different collision domains.

**link segment.** The point-to-point full duplex medium connection between two and only two Medium-Dependent Interfaces (MDIs).

**segment.** The medium connection, including connectors, between MDIs in a CSMA/CD LAN.

**13.3 Transmission System Model.** The physical size of a 10BASE-T network, or mixed-media network containing 10BASE-T link segments, is constrained by the limits of individual network components. These limits include the following:

(1) Cable length and its associated propagation time delay.
(2) Delay of repeater units (start-up and steady-state).
(3) Delay of MAUs (start-up and steady-state).
(4) Interpacket gap shrinkage.
(5) Delays within the DTE associated with the CSMA/CD access method.

Table 13-1 summarizes the delays for the various network media segments:

**Table 13-1**
**Delays for Network Media Segments**

| Media Segment Type | Maximum Number of MAUs per Segment | Maximum Segment Length (m) | Minimum Medium Propagation Velocity* | Maximum Medium Delay per Segment (ns) |
|---|---|---|---|---|
| Coaxial | | | | |
| 10BASE5 | 100 | 500 | 0.77 c | 2165 |
| 10BASE2 | 30 | 185 | 0.65 c | 950 |
| Link | | | | |
| FOIRL | 2 | 1000 | 0.66 c | 5000 |
| 10BASE-T | 2 | 100† | 0.59 c | 1000 |
| AUI‡ | 1 DTE/1 MAU | 50 | 0.65 c | 257 |

*$c = 3 \times 10^8$ m/s
†Actual maximum segment length depends on cable characteristics; see 14.1.1.3.
‡AUI is not a segment.

In addition, Table 14-1 summarizes the delays for the 10BASE-T MAU; Section 8, the delays for the 10BASE5 MAU; Section 10, the delays for the 10BASE2 MAU; and Section 9, the delays of the fiber optic inter-repeater link (FOIRL) and the repeater.

The following network topology constraints apply for 10BASE-T networks as well as mixed-media networks containing 10BASE-T link segments:

(1) Repeater sets are required for all segment interconnection.
(2) MAUs that are part of repeater sets count toward the maximum number of MAUs on a segment.
(3) The transmission path permitted between any two DTEs may consist of up to five segments, four repeater sets (including optional AUIs), two MAUs, and two AUIs.
(4) When a network path consists of four repeater sets and five segments, up to three of the segments may be coaxial and the remainder must be link segments (Figs 13-1 and 13-2). When five segments are present, each FOIRL link segment should not exceed 500 m.
(5) When a network path consists of three repeater sets and four segments, the maximum allowable length of the FOIRL segments is 1000 m each, as specified in 9.9 (Fig 13-3).

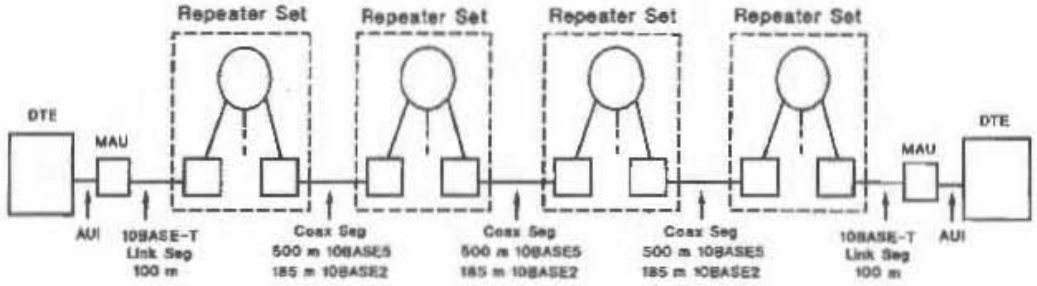



**Fig 13-1**
**Maximum Transmission Path with Three Coaxial Cable Segments**

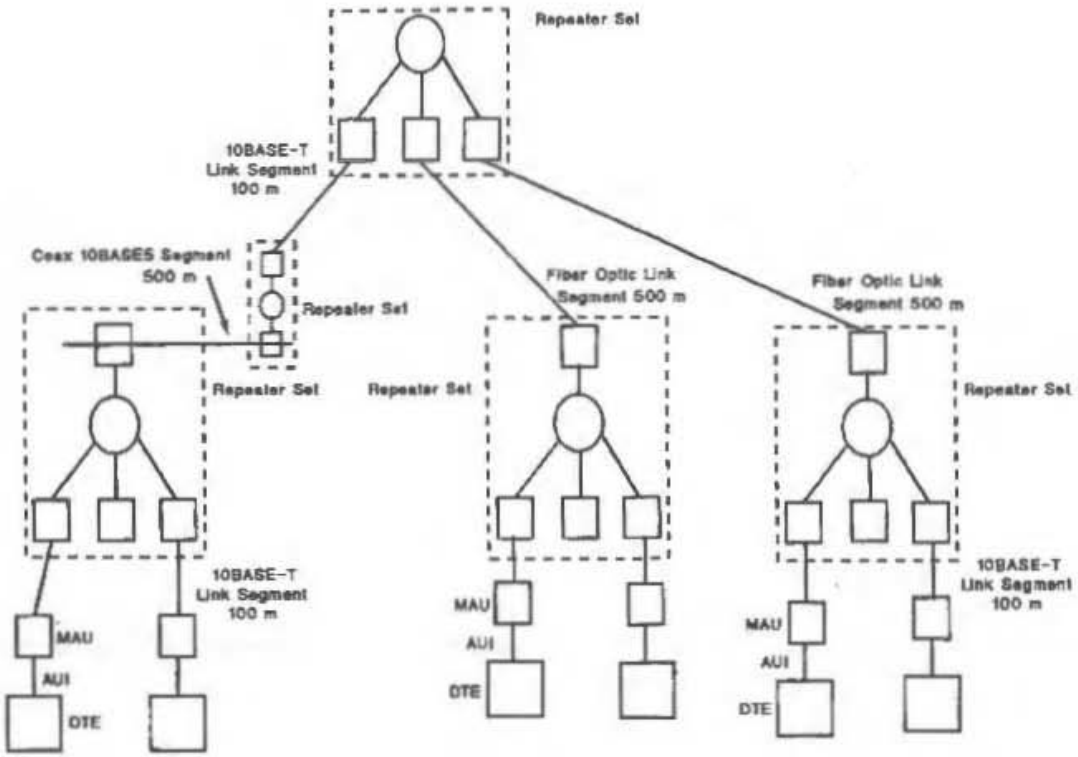



**Fig 13-2**
**Example of Maximum Transmission Path Using Coaxial Cable Segments, 10BASE-T Link Segments, and Fiber Optic Link Segments**

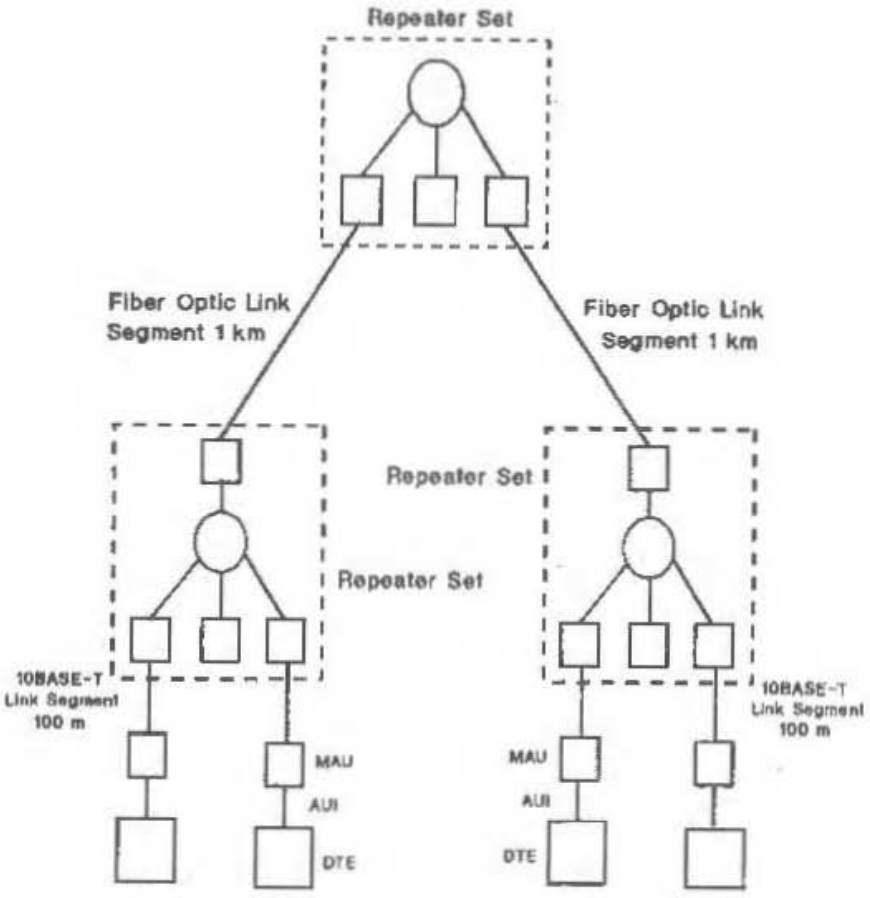



**Fig 13-3**
**Example of Maximum Transmission Path with Three Repeater Sets, Four Link Segments (Two are 100 m 10BASE-T and Two are 1 km Fiber)**

# 14. Twisted-Pair Medium Attachment Unit (MAU) and Baseband Medium, Type 10BASE-T

## 14.1 Scope

**14.1.1 Overview.** Section 14 defines the functional, electrical, and mechanical characteristics of the Type 10BASE-T MAU and one specific medium for use with that MAU. The relationship of this specification to the entire ISO/IEC 8802-3 CSMA/CD Local Area Network Specification is shown in Fig 14.1. The purpose of the MAU is to provide a simple, inexpensive, and flexible means of attaching devices to the medium.

This MAU and medium specification is aimed primarily at office applications where twisted-pair cable is often installed. Installation and reconfiguration simplicity is allowed by the type of cable and connectors used.

The 10BASE-T specification builds upon Sections 1 through 7 and Section 9 of this standard.

**14.1.1.1 Medium Attachment Unit (MAU).** The MAU has the following general characteristics:

(1) Enables coupling the Physical Signaling (PLS) sublayer by way of the Attachment Unit Interface (AUI) to the baseband twisted-pair link defined in Section 14.
(2) Supports message traffic at a data rate of 10 Mb/s.
(3) Provides for operating over 0 m to at least 100 m (328 ft) of twisted pair without the use of a repeater.
(4) Permits the Data Terminal Equipment (DTE) or repeater to confirm operation of the MAU and availability of the medium.
(5) Supports network configurations using the CSMA/CD access method defined in ISO/IEC 8802-3 : 1993 with baseband signaling.
(6) Supports a point-to-point interconnection between MAUs and, when used with repeaters having multiple ports, supports a star wiring topology.
(7) Allows incorporation of the MAU within the physical bounds of a DTE or repeater.

**14.1.1.2 Repeater Unit.** The repeater unit is used to extend the physical system topology and provides for coupling two or more segments. Repeaters are an integral part of all 10BASE-T networks with more than two DTEs (see Figs 13-1 and 13-2). The repeater unit is defined in Section 9. Multiple repeater units are permitted within a single collision domain to provide the maximum connection path length specified in Section 13. The repeater unit is not a DTE and therefore has slightly different requirements for its attached MAUs, as defined in 9.4.1. Repeater sets with 10BASE-T MAUs are required to provide the auto-partition/reconnection algorithm on those ports, as specified in 9.6.6.2.

**14.1.1.3 Twisted-Pair Media.** The medium for 10BASE-T is twisted-pair wire. The performance specifications of the simplex link segment are contained in 14.4. This wiring normally consists of 0.4 mm to 0.6 mm diameter [26 AWG to 22 AWG] unshielded wire in a multipair cable. The performance specifications are generally met by 100 m of 0.5 mm telephone twisted pair. Longer lengths are permitted providing the simplex link segment meets the requirements of 14.4. A length of 100 m, the design objective, will be used when referring to the length of a twisted-pair link segment.

**14.1.2 Definitions.** This section defines the terminology specific to Type 10BASE-T MAUs and their application to repeater units.

**bit time (BT).** The duration of one bit symbol (1/BR).

**collision.** A condition that results from concurrent transmissions from multiple signal sources.

**common-mode voltage.** The instantaneous algebraic average of two signals applied to a balanced circuit, both signals referred to a common reference. Also called longitudinal voltage.

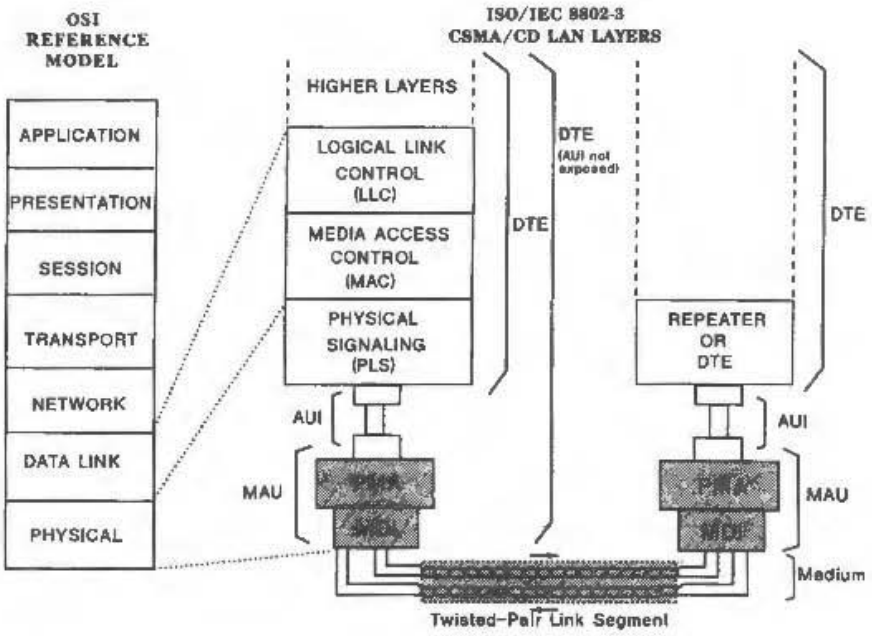



**Fig 14-1**
**10BASE-T Relationship to the ISO Open Systems Interconnection (OSI) Reference Model and the IEEE 802.3 CSMA/CD LAN Model**

**cross connect.** A group of connection points often wall- or rack-mounted in a wiring closet, used to mechanically terminate and interconnect twisted-pair building wiring.

**differential-mode voltage.** The instantaneous algebraic difference between two signals applied to a balanced circuit, both signals referred to a common reference. Also called metallic voltage.

**Medium-Dependent Interface (MDI).** The mechanical and electrical interface between the twisted-pair link segment and the MAU.

**Physical Medium Attachment (PMA) sublayer.** The portion of the MAU that contains the functional circuitry.

**Physical Signaling (PLS) sublayer.** The portion of the Physical Layer, contained within the DTE, that provides the logical and functional coupling between the MAU and the Data Link Layer.

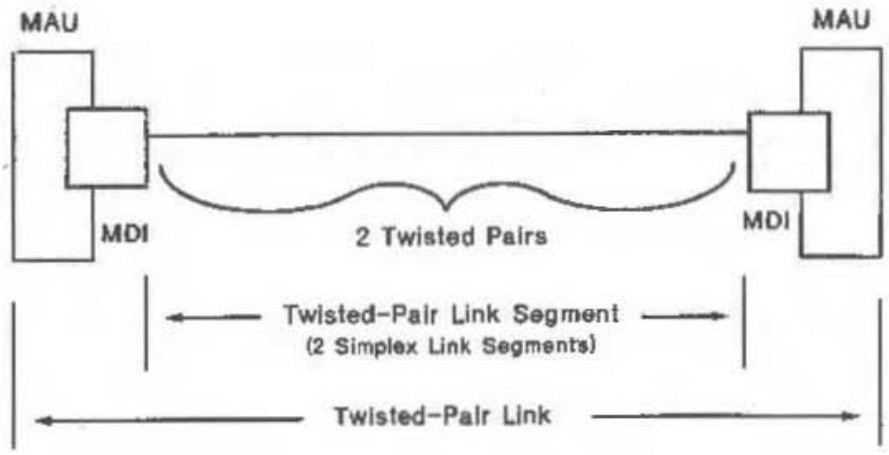
**simplex link segment.** A two-wire path between two MAUs including the terminating connectors, consisting of one or more twisted pairs joined serially with appropriate connection devices, for example, patch fields and wall plates (see Fig 14-2).

**twisted pair.** Two continuous insulated conductors helically twisted around one another (see Fig 14-2).

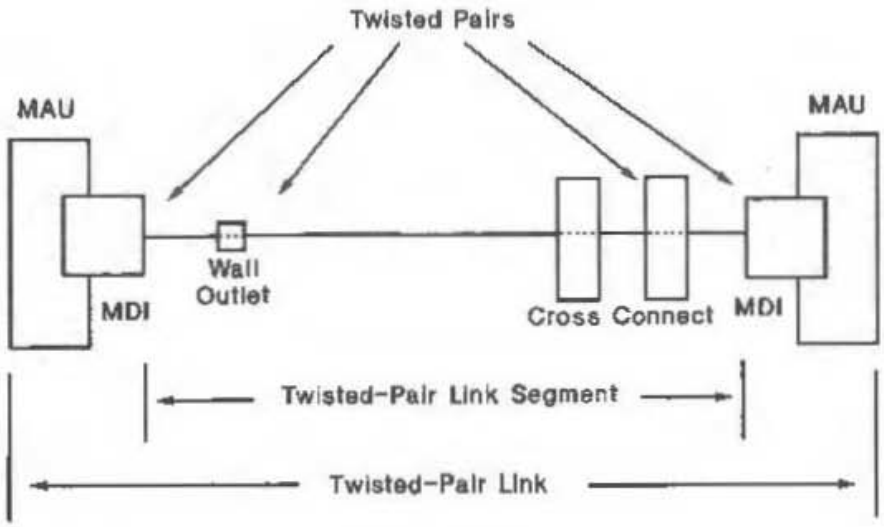
**twisted-pair cable.** A group of twisted pairs within a single protective sheath.

**twisted-pair cable binder group.** A group of twisted pairs within a cable that are bound together. Large telephone cables have multiple binder groups with high interbinder group near-end crosstalk loss.

**twisted-pair link.** A twisted-pair link segment and its two attached MAUs (see Fig 14-2).




(a)




(b)

**Fig 14-2**
**Twisted-Pair Link**

**twisted-pair link segment (duplex link segment).** Two simplex link segments for connecting two MAUs (see Fig 14-2).

**14.1.3 Application Perspective.** This section states the broad objectives and assumptions underlying the specifications defined throughout Section 14.

#### 14.1.3.1 Objectives

(1) Provide the physical means for communication between LAN Data Link Layer Entities.
(2) Ensure compatibility of independently developed physical and electrical interfaces.
(3) Provide a communication channel with a mean bit error rate, at the physical layer service interface of less than one part in $10^8$.
(4) Provide for ease of installation and service.
(5) Ensure that fairness of DTE access is not compromised.
(6) Provide for low-cost networks, as related to both equipment and cabling.
(7) Make use of telephone twisted-pair building wiring and telephony wiring practices.

**14.1.3.2 Compatibility Considerations.** All implementations of the twisted-pair link shall be compatible at the MDI. The MAU and the medium are defined to provide compatibility among devices designed by different manufacturers. Designers are free to implement circuitry within the MAU in an application-dependent manner provided the MDI and AUI (when implemented) specifications are met.

**14.1.3.3 Mode of Operation.** The 10BASE-T MAU is capable of operating in *normal* mode only (see 7.1.4). The MAU shall not operate in *monitor* mode.

When normal mode is in operation, the MAU functions as a direct connection between the medium and the DTE or repeater. Data from the DTE or repeater is output to one of the simplex link segments of the link segment, and data received on the other simplex link segment is input to the DTE or repeater.

**14.1.4 Relationship to PLS and AUI.** A close relationship exists between Section 14 and Section 7. Section 14 specifies the physical medium parameters and the PMA logical functions residing in the physical MAU. The MAU provides services to the PLS defined in Section 7 by means of the AUI. 10BASE-T MAUs support a subset of the AUI services specified in Section 7. 10BASE-T MAUs do not support the optional isolate function, the optional CO circuit, or the optional CS1 signal on the CI circuit.

The design of an external MAU component requires the use of both Section 14 and Section 7 for the PLS and AUI specifications.

The figures and numerous textual references throughout Section 14 refer to terminology associated with the AUI (that is, DO, DI, and CI). Since an embodiment of the 10BASE-T MAU does not require the implementation of an AUI, the DO, DI, and CI circuits may not physically exist. However, they are logically present and MAU operation is defined in terms of them.

**14.2 MAU Functional Specifications.** The MAU provides the means by which signals on the three AUI signal circuits to and from the DTE or repeater and their associated interlayer messages are coupled to the twisted-pair link segment. The MAU provides the following functional capabilities to handle message flow between the DTE or repeater and the twisted-pair link segment:

(1) Transmit function. Provides the ability to transfer Manchester-encoded data from the DO circuit to the TD circuit. While not sending Manchester-encoded data on the TD circuit, the MAU sends an idle signal, TP_IDL, on the TD circuit.
(2) Receive function. Provides the ability to transfer Manchester-encoded data from the RD circuit to the DI circuit. While not sending Manchester-encoded data on the DI circuit, the MAU sends an idle signal, IDL, on the DI circuit.
(3) Loopback function. Provides the ability to transfer Manchester-encoded data from the DO to the DI circuit when the MAU is sending Manchester-encoded data to the TD circuit.
(4) Collision Presence function. Provides the ability to detect simultaneous occurrence of Manchester-encoded data on the RD and DO circuits and to report such an occurrence as a collision.
(5) *signal_quality_error* Message (SQE) Test function. Provides the ability to indicate to the DTE that the Collision Presence function is operational and that the *signal_quality_error* message can be sent by the MAU.
(6) Jabber function. Provides the ability to prevent abnormally long reception of Manchester-encoded data on the DO circuit from indefinitely disrupting transmission on the network. While such a condition is present, transfer of Manchester-encoded data by the Transmit and Loopback functions is disabled.

(7) Link Integrity Test function. Provides the ability to protect the network from the consequences of failure of the simplex link attached to the RD circuit. While such a failure is present, transfer of Manchester-encoded data by the Transmit, Receive, and Loopback functions is disabled.

**14.2.1 MAU Functions.** The MAU shall provide the Transmit, Receive, Loopback, Collision Presence, Jabber, and Link Integrity Test functions. The SQE Test function shall be performed by MAUs that are connected to DTEs and shall not be performed by MAUs that are connected to repeaters. A capability may be provided in the MAU to activate or inhibit the SQE Test function. It is not required that a MAU determine that it is connected to either a DTE or a repeater and automatically activate or inhibit the SQE Test function.

**14.2.1.1 Transmit Function Requirements.** The MAU shall receive the signals on the DO circuit and send them to the TD circuit of the MDI. A positive signal on the A lead relative to the B lead of the DO circuit shall result in a positive signal on the TD+ (Transmit Data +) lead of the MDI with respect to the TD– lead.

At the start of a packet transmission, no more than 2 bits may be received from the DO circuit and not transmitted on the TD circuit. In addition, it is permissible for the first bit sent to contain phase violations or invalid amplitude. All subsequent bits of the packet shall be reproduced with the differential voltage specified in 14.3.1.2.1 and with no more jitter than is specified in 14.3.1.2.3. The second bit transmitted on the TD circuit shall be transmitted with the correct timing and signal levels. The steady-state propagation delay between the DO circuit input and the TD circuit shall not exceed 2 BT.

For any two packets that are separated by 9.6 μs or less, the start-up delay (bit loss plus steady-state propagation delay) of the first packet shall not exceed that of the second packet by more than 2 BT.

Whenever data is not being transmitted on the TD circuit, an idle signal, TP_IDL, shall be transmitted on the TD circuit. TP_IDL is a start of idle, as defined in 14.3.1.2.1, followed by a repeating sequence of a 16 ms ± 8 ms period of silence (the time where the differential voltage remains at 0 mV ± 50 mV) and a link test pulse (see 14.3.1.2.1). Following a packet and start of idle, the repeating sequence shall start with a period of silence.

Transmission of TP_IDL may be terminated at any time with respect to the link test pulse. It shall be terminated such that no more than the first transmitted bit of a packet is corrupted, and with no more delay than is specified for bit loss and steady-state propagation.

**14.2.1.2 Receive Function Requirements.** The MAU shall receive the signals on the RD circuit of the MDI and send them to the DI circuit. A positive signal on the RD+ (Receive Data +) lead relative to the RD– lead of the MDI shall result in a positive signal on the A lead with respect to the B lead of the DI circuit.

At the start of a packet reception from the RD circuit, no more than 5 bits may be received on the RD circuit and not transmitted onto the DI circuit. In addition, it is permissible for the first bit sent on the DI circuit to contain phase violations or invalid data; however, all successive bits of the packet shall be sent with no more than the amount of jitter specified in 14.3.1.3.1. The steady-state propagation delay between the RD circuit and the DI circuit shall not exceed 2 BT.

For any two packets that are separated by 9.6 μs or less, the start-up delay of the first packet shall not exceed that of the second packet by more than 2 BT.

**14.2.1.3 Loopback Function Requirements.** When the MAU is transmitting on the TD circuit and is not receiving *RD_input* messages (14.2.2.4) on the RD circuit, the MAU shall transmit on the DI circuit the signals received on the DO circuit in order to provide loopback of the transmitted signal. At the start of packet transmission on the TD circuit, no more than 5 bits of information may be received from the DO circuit and not transmitted to the DI circuit. In addition, it is permissible for the first bit sent on the DI circuit to contain phase violations or invalid data; however, all successive bits of the packet shall meet the jitter specified in 14.3.1.3.1 (that is, 13.5 ns plus 1.5 ns). The steady-state propagation delay between the DO circuit and the DI circuit shall not exceed 1 BT.

**14.2.1.4 Collision Presence Function Requirements.** The MAU shall detect as a collision the simultaneous occurrence of activity on the DO circuit and the RD circuit while in the Link Test Pass state. While a collision is detected, a CS0 signal (see 7.3.1.2) shall be sent on the CI circuit. The signal shall be

presented to the CI circuit no more than 9 BT after the occurrence of a collision. The signal shall be deasserted within 9 BT after the DO circuit or the RD circuit changes from active to idle.

When CS0 is asserted on the CI circuit due to a collision, the data on the RD circuit shall be sent to the DI circuit within 9 BT.

When the RD circuit changes from active to idle and data is present on the DO circuit, the data on the DO circuit shall be sent to the DI circuit within 9 BT.

The signal presented on the CI circuit in the absence of collision, SQE test, or Jabber shall be the IDL signal.

**14.2.1.5 *signal_quality_error* Message (SQE) Test Function Requirements.** The SQE Test function shall be performed by MAUs that are connected to DTEs and shall not be performed by MAUs that are connected to repeaters. When the SQE test is performed, the MAU shall send CS0 on the CI circuit for a time 'SQE_test' beginning a time 'SQE_test_wait' after the last positive transition of a packet on the DO circuit. The value of 'SQE_test' shall be 10 BT ± 5 BT and the value of 'SQE_test_wait' shall be between 0. μs and 1.6 μs. This function should use as much of the normal collision detection and signaling circuitry as possible without introducing extraneous signals on the TD circuit or the DI circuit.

The CS0 signal shall not be sent by the SQE Test function while in any of the Link Test Fail states.

**14.2.1.6 Jabber Function Requirements.** The MAU shall contain a self-interrupt capability to prevent an illegally long transmission by a DTE from permanently disrupting transmission on the network and to disable loopback to the DI circuit (Fig 14-5). The MAU shall provide a window 'xmit_max' during which time the Transmit function may continuously transmit *TD_output* messages to the TD circuit. The value of 'xmit_max' shall be between 20 ms and 150 ms. If a transmission exceeds this duration, the Jabber function shall inhibit the Loopback function and the transmission of *TD_output* messages by the Transmit function, and shall send the CS0 signal on the CI circuit. This shall continue until *output_idle* has been continuously present on the DO circuit for a time 'unjab'. The value of 'unjab' shall be 0.5 ms ± 0.25 s.

It is permissible to activate the Jabber function when the TD circuit transmitter is sending *TD_output* messages for longer than 'xmit_max'.

The MAU shall not activate its Jabber function when the repeater's MAU Jabber Lockup Protection function operates at its longest permitted time as specified in 9.6.5.

**14.2.1.7 Link Integrity Test Function Requirements.** In order to protect the network from the consequences of a simplex link segment failure, the MAU shall monitor the RD circuit for *RD_input* and link test pulse activity. If neither *RD_input* nor a link test pulse is received for a time 'link_loss', the MAU shall enter the Link Test Fail state and cause the *input_idle* message to be sent on the DI circuit and the *TD_idle* message to be sent on the TD circuit (Fig 14-6). The value of 'link_loss' shall be between 50 ms and 150 ms. When RD_input or a number 'lc_max' of consecutive link test pulses is received on the RD circuit, the MAU shall exit the Link Test Fail state. The value of 'lc_max' shall be between 2 and 10 inclusive.

Only link test pulses that occur within time 'link_test_max' of each other shall be considered consecutive. The value of 'link_test_max' shall be between 25 ms and 150 ms. In addition, detected pulses that occur within a time 'link_test_min' of a previous pulse or packet shall be ignored while in the Link Test Pass state. In the Link Test Fail state, such pulses shall reset the counted number of consecutive link test pulses to zero. The value of 'link_test_min' shall be between 2 ms and 7 ms. Re-enabling shall be deferred until the signals on the RD and DO circuits become idle. The MAU shall not detect a link test pulse as *RD_input*. Additionally, a MAU may exit the Link Test Fail Extend state and enter the Link Test Pass state when the RD circuit becomes idle and the Jabber function has disabled transmission on the TD circuit.

While the MAU is not in the Link Test Pass state, the Link Integrity Test function shall disable the bit transfer of the Transmit, Receive, and Loopback functions, and the Collision Presence and SQE Test functions.

At PowerOn, in place of entering the Link Test Pass state as shown in Fig 14-6, a MAU may optionally enter the Link Test Fail Reset state.

If a visible indicator is provided on the MAU to indicate the link status, it is recommended that the color be green and that the indicator be labeled appropriately. It is further recommended that the indicator be on when the MAU is in the Link Test Pass state and off otherwise.

**14.2.2 PMA Interface Messages.** The messages between the PLS in the DTE and the PMA in the MAU shall comply with the PMA interface messages described in 7.2.1. These messages also are used in repeater

unit to PMA communication. These and the messages between the PMAs over the MDI are summarized below.

**14.2.2.1 PLS to PMA Messages.** The following messages are sent by the PLS in the DTE or repeater to the PMA in the MAU:

| Message | Circuit | Signal | Meaning |
|---|---|---|---|
| *output* | DO | CD1,CD0 | Output information |
| *output_idle* | DO | IDL | No data to be output |

**14.2.2.2 PMA to PLS Messages.** The following messages are sent by the MAU to the PLS in the DTE or repeater:

| Message | Circuit | Signal | Meaning |
|---|---|---|---|
| *input* | DI | CD1,CD0 | Input information |
| *input_idle* | DI | IDL | No information to input |
| *mau_available* | CI | IDL | MAU is available for output |
| *signal_quality_error* | CI | CS0 | Error detected by MAU |

Retiming of CD1 and CD0 signals within the MAU is neither prohibited nor required. Considerable jitter may be present (see 14.3.1.3.1).

**14.2.2.3 PMA to Twisted-Pair Link Segment Messages**

| Message | Circuit | Signal | Meaning |
|---|---|---|---|
| *TD_output* | TD | CD1,CD0 | Output information |
| *TD_idle* | TD | TP_IDL | No information to output |

The encoding for TP_IDL is defined in 14.2.1.1. The encoding for CD1 and CD0 is the same as that used on the AUI. Retiming of CD1 and CD0 signals within the MAU is neither prohibited nor required.

**14.2.2.4 Twisted-Pair Link Segment to PMA Messages**

| Message | Circuit | Signal | Meaning |
|---|---|---|---|
| *RD_input* | RD | CD1,CD0 | Input information |
| *RD_idle* | RD | TP_IDL | No information to input |

The encoding for TP_IDL is defined in 14.2.1.1. The encoding for CD1 and CD0 is the same as that used on the AUI.

**14.2.2.5 Interface Message Time References.** Delay and bit loss specifications are measured from the occurrence of messages at the MDI and MAU AUI. The following describes the point where each message starts:

| Message | Reference |
|---|---|
| *output* | leading bit cell boundary (BCB) of first valid CD1 or CD0 |
| *output_idle* | last positive-going transition prior to start of IDL |
| *input* | leading BCB of first valid CD1 or CD0 |
| *input_idle* | last positive-going transition prior to start of IDL |
| *signal_quality_error* | first transition of valid amplitude |
| *mau_available* | last positive-going transition prior to start of IDL |
| *TD_output* | leading BCB of first valid CD1 or CD0 |
| *TD_idle* | last positive-going transition prior to start of TP_IDL |
| *RD_output* | leading BCB of first valid CD1 or CD0 |
| *RD_idle* | last positive-going transition prior to start of TP_IDL |

**14.2.3 MAU State Diagrams.** The state diagrams of Figs 14-3, 14-4, 14-5, and 14-6 depict the full set of allowed MAU state functions relative to the circuits of the AUI and MDI.

The notation used in the state diagrams follows the conventions in 1.2.1. The variables and timers used in the state diagrams are defined in the following sections.

**14.2.3.1 State Diagram Variables.** Variables are used in the state diagrams to indicate the status of MAU inputs and outputs, to control MAU operation, and to pass state information between functions.

In the variable definitions, the name of the variable is followed by a brief description of the variable and a list of values the variable may take. For those variables that are state diagram outputs, one value will be identified as the default. The variable has the default value when no active state contains a term assigning a different value.

For example, the variable 'xmit' has the value 'disable' whenever the Jabber function or the Link Integrity Test function is in a state that asserts 'xmit=disable'. The variable has the default value 'enable' all other times.

The variables used in the state diagrams are defined as follows:

**DI.** Controls the signal sent by the MAU on the DI circuit.
Values: idle; MAU is sending *input_idle*, IDL (default).
DO; MAU sends the signal received on the DO circuit.
lpbk = disable overrides this and causes *input_idle* to be sent.
RD; MAU sends the signal received on the RD circuit.
rcv = disable overrides this and causes *input_idle* to be sent.

**CI.** Controls the signal sent by the MAU on the CI circuit.
Values: idle; MAU sends *mau_available*, IDL (default).
SQE; MAU sends *signal_quality_error*, CS0.

**DO.** Status of the signal received by the MAU on the DO circuit.
Values: idle; MAU is receiving *output_idle*, IDL.
active; MAU is receiving *output*, CD0 or CD1.

**TD.** Controls the signal sent by the MAU on the TD circuit.
Values: idle; MAU sends *TD_idle*, TP_IDL (default).
DO; MAU sends the signal received on the DO circuit.
xmit = disable overrides this and causes *TD_idle* to be sent.

**RD.** Status of the signal received by the MAU on the RD circuit.
Values: idle; MAU is receiving silence or a link test pulse.
active; MAU is detecting signals which meet the requirements of 14.3.1.3.2.

**link_test_rcv.** Status of the link test signal received by the MAU on the RD circuit.
Values: false; MAU is not detecting a link test pulse.
true; MAU is detecting a link test pulse.

**link_count.** Count of the number of consecutive link test pulses received while in the Link Fail state.
Values: non-negative integers.

**lc_max.** The number of consecutive link test pulses required before exit from the Link Fail state.
Values: positive integer between 2 and 10 inclusive.

**rcv.** Controls the path from the RD circuit to the DI circuit.
Values: enable; receive is enabled (default).
disable; the output to the DI circuit is *input_idle* when DI=RD.

**lpbk.** Controls the path from the DO circuit to the DI circuit.
Values: enable; loopback is enabled (default).
disable; the output to the DI circuit is *input_idle* when DI=DO.

**xmit.** Controls the path from the DO circuit to the TD circuit.
Values: enable; transmit is enabled (default).
disable; transmit is disabled and the signal sent on the TD circuit is TP_IDL.

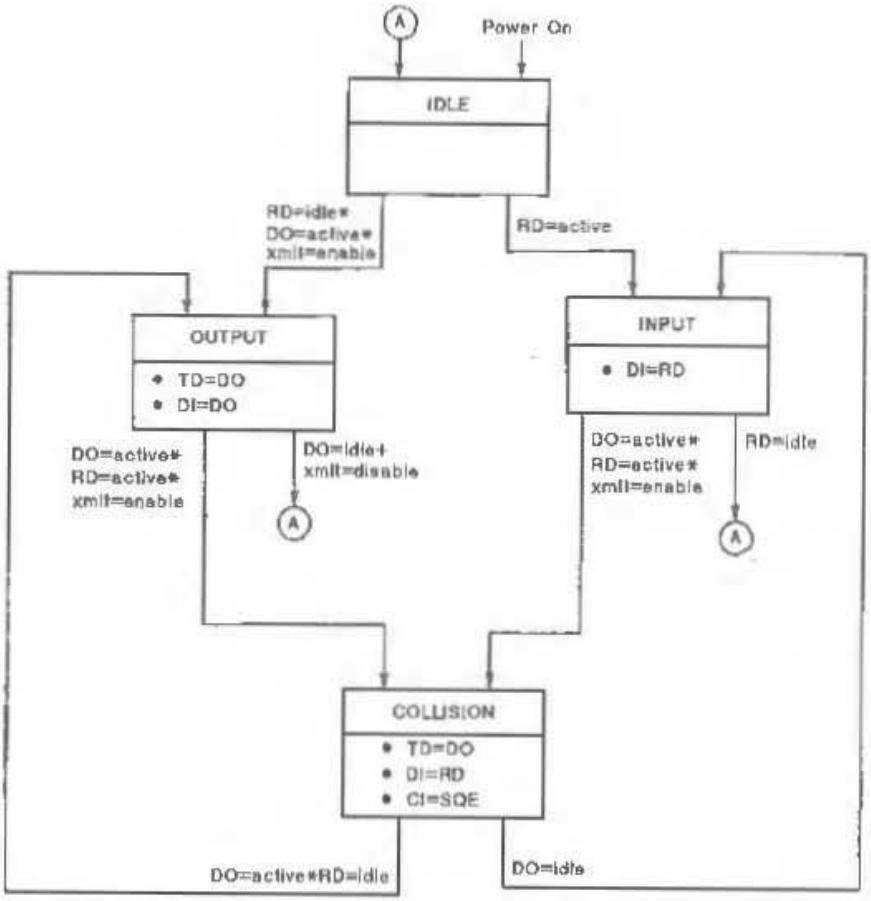



**Fig 14-3**
**MAU Transmit, Receive, Loopback, and Collision Presence Functions State Diagram**

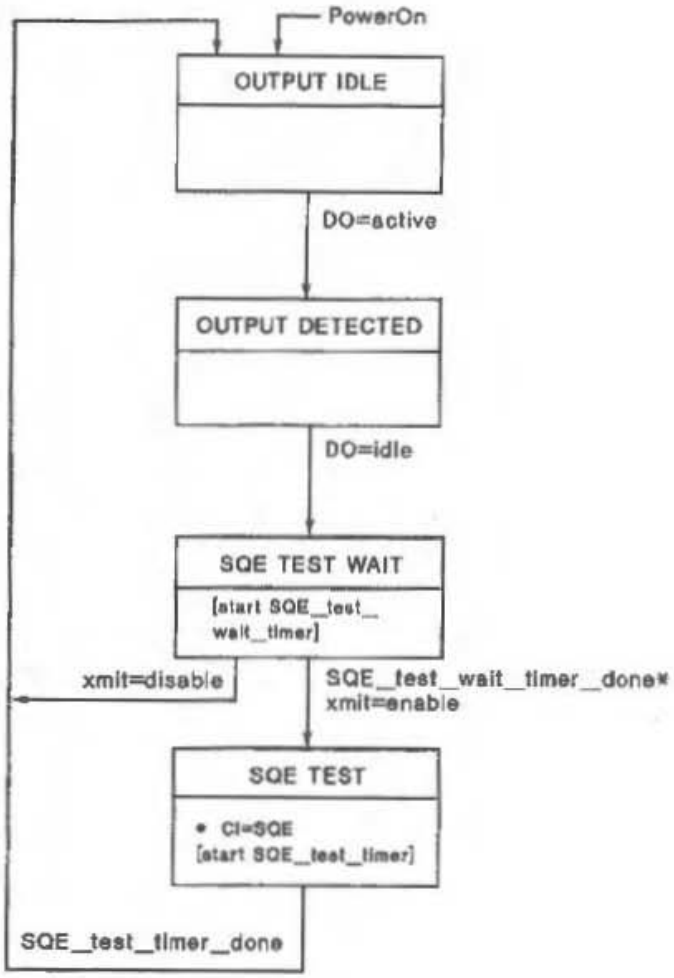



**Fig 14-4**
***signal_quality_error* Message Test Function State Diagram**

**14.2.3.2 State Diagram Timers.** All timers operate in the same fashion. A timer is reset and starts counting upon entering a state where 'start x_timer' is asserted. Time 'x' after the timer has been started, 'x_timer_done' is asserted and remains asserted until the timer is reset. At all other times, 'x_timer_not_done' is asserted.

When entering a state where 'start x_timer' is asserted, the timer is reset and restarted even if the entered state is the same as the exited state; for example, when in the Link Test Pass state of the Link Integrity Test function state diagram, the 'link_loss_timer' and the 'link_test_min_timer' are reset each time the term 'RD = active + (link_test_rcv=true • link_test_min_timer_done)' is satisfied.

**link_loss_timer.** Timer for longest time input activity can be missing before the MAU determines that a link fail condition exists (14.2.1.7).

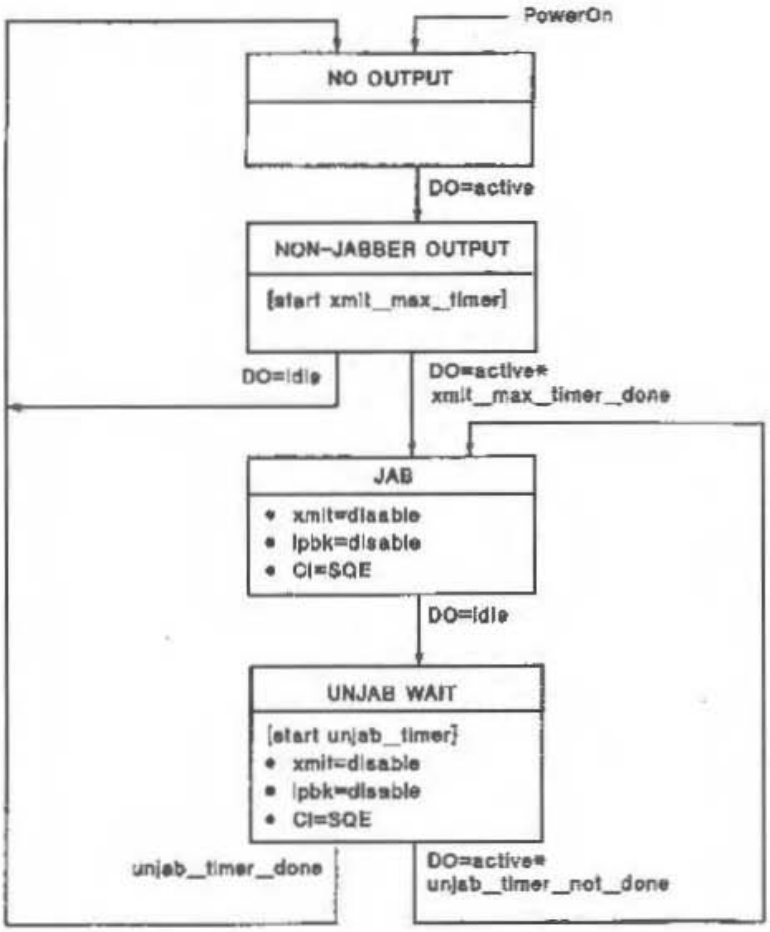



**Fig 14-5**
**Jabber Function State Diagram**

**link_test_min_timer.** Timer for the minimum time between valid link test pulses (14.2.1.7).

**link_test_max_timer.** Timer for maximum time input activity can be missing before Link Fail state is exited (14.2.1.7).

**SQE_test_timer**. Timer for the duration of the CS0 signal used for the SQE Test function (14.2.1.5).

**SQE_test_wait_timer.** Timer for the delay from end of packet to the start of the CS0 signal used for the SQE Test function (14.2.1.5).

**xmit_max_timer.** Timer for excessively long transmit time (14.2.1.6).

**unjab_timer.** Timer for the length of time the DO circuit must be continuously idle to allow transmission to be re-enabled (14.2.1.6).

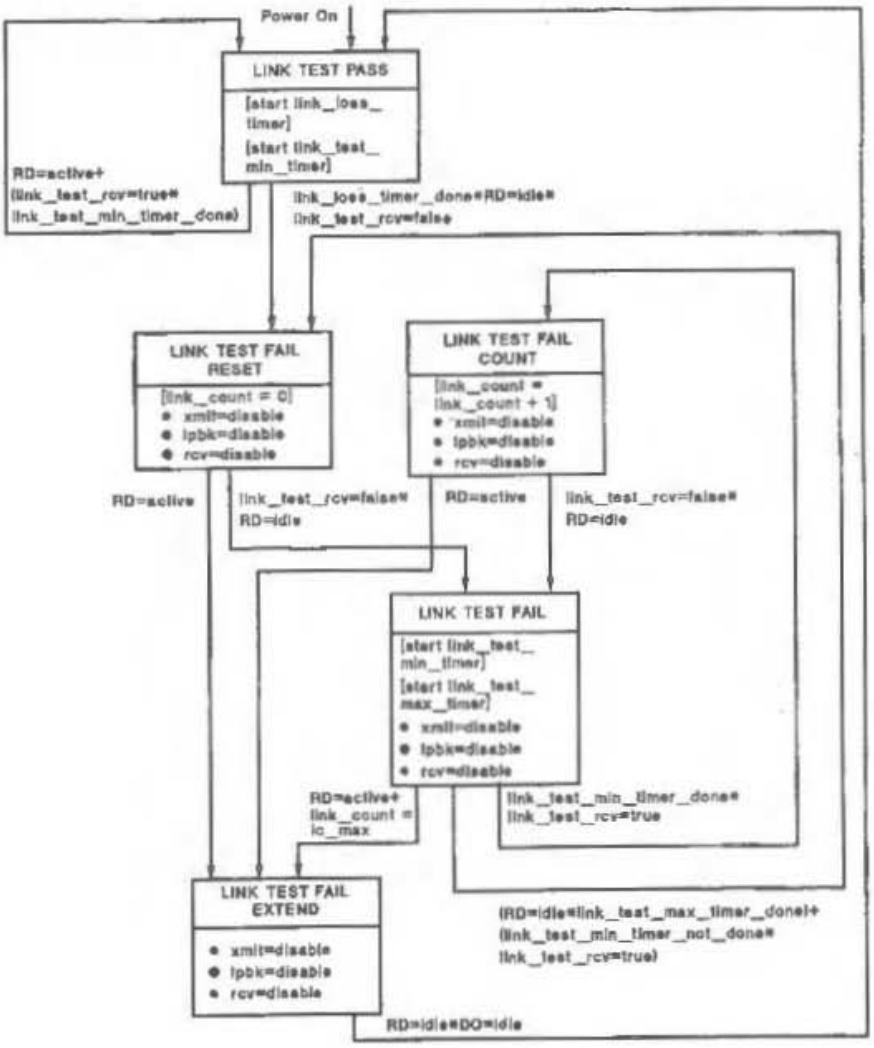



**Fig 14-6**
**Link Integrity Test Function State Diagram**

**14.3 MAU Electrical Specifications.** This section defines the electrical characteristics of the MAU at the MDI and the AUI. The MAU shall also meet the AUI requirements specified in Section 7 when the AUI is implemented.

Additional information relative to conformance testing is given in A4.3.

The ground for all common-mode tests is circuit PG, Protective Ground of the AUI. In implementations without an AUI, chassis ground is used as circuit PG. All components in test circuits shall be ±1% unless otherwise stated.

### 14.3.1 MAU-to-MDI Interface Characteristics

**14.3.1.1 Isolation Requirement.** The MAU shall provide isolation between the DTE Physical Layer circuits including frame ground and all MDI leads including those not used by 10BASE-T. This electrical separation shall withstand at least one of the following electrical strength tests.

(1) 1500 V rms at 50 Hz to 60 Hz for 60 s, applied as specified in Section 5.3.2 of IEC Publication 950 [8].
(2) 2250 Vdc for 60 s, applied as specified in Section 5.3.2 of IEC Publication 950 [8].
(3) A sequence of ten 2400 V impulses of alternating polarity, applied at intervals of not less than 1 s. The shape of the impulses shall be 1.2/50 μs (1.2 μs virtual front time, 50 μs virtual time of half value), as defined in IEC Publication 60 [11].

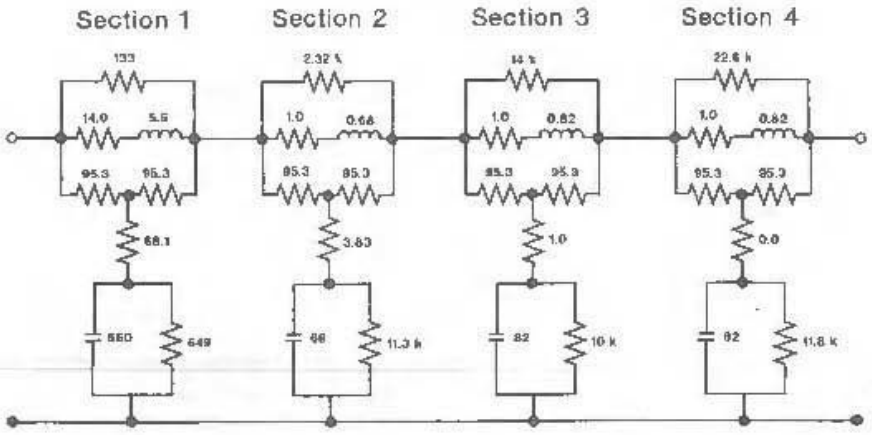
There shall be no insulation breakdown, as defined in Section 5.3.2 of IEC Publication 950 [8], during the test. The resistance after the test shall be at least 2 MΩ, measured at 500 Vdc.

**14.3.1.2 Transmitter Specifications.** The MAU shall provide the Transmit function specified in 14.2.1.1 in accordance with the electrical specifications of this section.

Where a load is not specified, the transmitter shall meet requirements of this section when connected to a 100 Ω resistive load. The use of 100 Ω terminations simplifies the measurement process when using 50 Ω measurement equipment as 50 Ω to 100 Ω impedance matching transformers are readily available.

Some tests in this section require the use of an equivalent circuit that models the distortion introduced by a simplex link segment. This twisted-pair model shall be constructed according to Fig 14-7 with component tolerances as follows: Resistors, ±1%; capacitors, ±5%; inductors, ±10%. Component tolerance specifications shall be met from 5.0 MHz to 15 MHz. For all measurements, the TD circuit shall be connected through a balun to Section 1 and the signal measured across a load connected to Section 4 of the model. The balun shall not affect the peak differential output voltage specified in 14.3.1.2.1 by more than 1% when inserted between the 100 Ω resistive load and the TD circuit.

The insertion loss of the twisted-pair model when measured with a 100 Ω source and 100 Ω load shall be between 9.70 dB and 10.45 dB at 10 MHz, and between 6.50 dB and 7.05 dB at 5 MHz.




NOTE: Care must be taken that layout and parasitics do not exceed R, C, and L tolerance values.

Resistances are in Ω
Capacitances are in pF
Inductances are in μH

**Fig 14-7**
**Twisted-Pair Model**

**14.3.1.2.1 Differential Output Voltage.** Some of the text and figures of this section describe the differential voltage in terms of magnitudes. These requirements apply to negative as well as positive pulses.

The peak differential voltage on the TD circuit when terminated with a 100 Ω resistive load shall be between 2.2 V and 2.8 V for all data sequences. When the DO circuit is driven by an all-ones Manchester-encoded signal, any harmonic measured on the TD circuit shall be at least 27 dB below the fundamental.

NOTE: The specification on maximum spectral components is not intended to ensure compliance with regulations concerning RF emissions. The implementor should consider any applicable local, national, or international regulations. Additional filtering of spectral components may therefore be necessary.

The output signal $V_o$, is defined at the output of the twisted-pair model as shown in Fig 14-8. The TD transmitter shall provide equalization such that the output waveform shall fall within the template shown in Fig 14-9 for all data sequences. Voltage and time coordinates for inflection points on Fig 14-9 are given in Table 14-1. (Zero crossing points are different for external and internal MAUs. The zero crossings depicted in Fig 14-9 apply to an external MAU.) The template voltage may be scaled by a factor of 0.9 to 1.1 but any scaling below 0.9 or above 1.1 shall not be allowed. The recommended measurement procedure is described in A4.3.1. Time t = 0 on the template represents a zero crossing, with positive slope, of the output waveform. During this test the twisted-pair model shall be terminated in 100 Ω and driven by a transmitter with a Manchester-encoded pseudo-random sequence with a minimum repetition period of 511 bits.

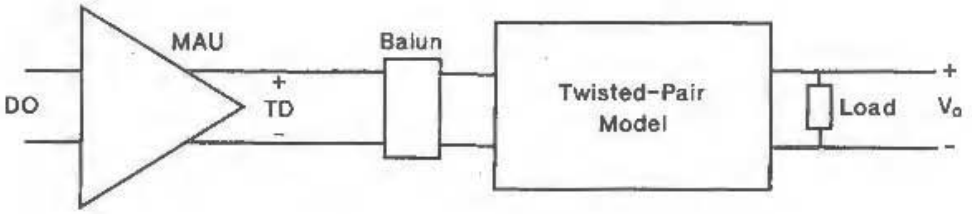



**Fig 14-8**
**Differential Output Voltage Test**

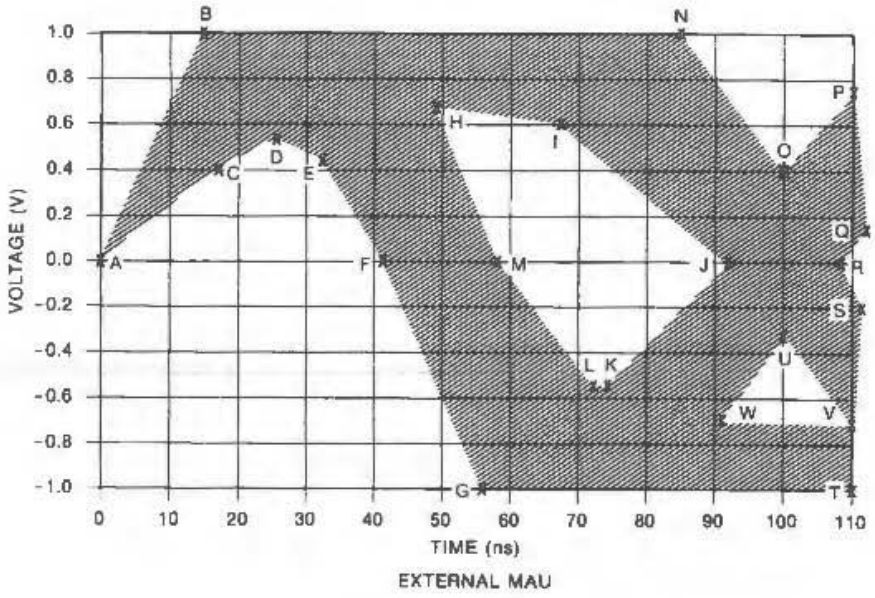



**Fig 14-9**
**Voltage Template**

**Table 14-1**
**Voltage Template Values for Fig 14-9**

| Reference | Time (ns) External MAU | Time (ns) Internal MAU | Voltage (V) |
|---|---|---|---|
| A | 0 | 0 | 0 |
| B | 15 | 15 | 1.0 |
| C | 15 | 15 | 0.4 |
| D | 25 | 25 | 0.55 |
| E | 32 | 32 | 0.45 |
| F | 42 | 39 | 0 |
| G | 57 | 57 | –1.0 |
| H | 48 | 48 | 0.7 |
| I | 67 | 67 | 0.6 |
| J | 92 | 89 | 0 |
| K | 74 | 74 | –0.55 |
| L | 73 | 73 | –0.55 |
| M | 58 | 61 | 0 |
| N | 86 | 85 | 1.0 |
| O | 100 | 100 | 0.4 |
| P | 110 | 110 | 0.75 |
| Q | 111 | 111 | 0.15 |
| R | 108 | 111 | 0 |
| S | 111 | 111 | –0.15 |
| T | 110 | 110 | –1.0 |
| U | 100 | 100 | –0.3 |
| V | 110 | 110 | –0.7 |
| W | 90 | 90 | –0.7 |

This test shall be repeated with the template inverted about the time axis. In that case, t = 0 on the template represents a zero crossing, with negative slope, of the output waveform. When testing an external MAU the input waveform to the DO circuit of the MAU shall contribute no more than 0.5 ns of jitter. Adherence to this template does not verify that the requirements of 14.3.1.2.3 are met. (See A4.3.3 for modification of the template to test jitter.)

The TP_IDL shall always start with a positive waveform when a waveform conforming to Fig 7-12 is applied to the DO circuit. If the last bit transmitted was a CD1, the last transition will be at the bit cell center of the CD1. If the last bit transmitted was a CD0, the PLS will generate an additional transition at the bit cell boundary following the CD0. After the zero crossing of the last transition, the differential voltage shall remain within the shaded area of Fig 14-10. Once the differential voltage has gone more negative than –50 mV, it shall not exceed +50 mV. The template requirements of Fig 14-10 shall be met when measured across each of the test loads defined in Fig 14-11, both with the load connected directly to the TD circuit and with the load connected through the twisted-pair model as defined in Figs 14-7 and 14-8.

The link test pulse shall be a single positive (TD+ lead positive with respect to TD– lead) pulse, which falls within the shaded area of Fig 14-12. Once the differential output voltage has become more negative than –50 mV, it shall remain less than +50 mV. The template requirements of Fig 14-12 shall be met when measured across each of the test loads defined in Fig 14-11; both with the load connected directly to the TD circuit and with the load connected through the twisted-pair model as defined in Figs 14-7 and 14-8.

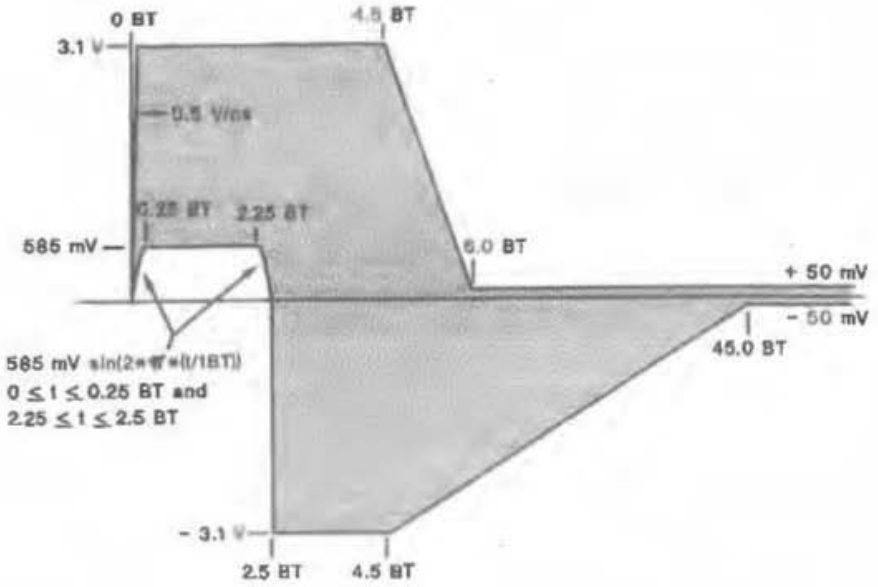
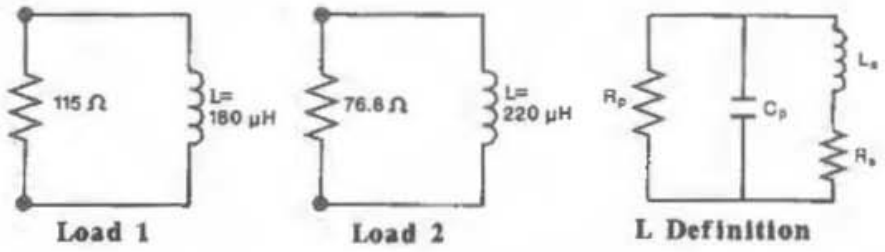



**Fig 14-10**
**Transmitter Waveform for Start of TP_IDL**




All parameters are defined over the frequency range of 250 kHz to 6 MHz.

$L_s = L \pm 1\%$ $\quad R_p \geq 2\ k\Omega$
$C_p = 12\ pF \pm 20\%$ $\quad R_s \leq 0.5\ \Omega$

**Fig 14-11**
**Start-of-TP_IDL Test Load**

**14.3.1.2.2 Transmitter Differential Output Impedance.** The differential output impedance as measured on the TD circuit shall be such that any reflection, due to differential signals incident upon the TD circuit from a simplex link segment having any impedance within the range specified in 14.4.2.2, shall be at least 15 dB below the incident, over the frequency range of 5.0 MHz to 10 MHz. This return loss shall be maintained at all times when the MAU is powered, including when the TD circuit is sending TP_IDL.

**14.3.1.2.3 Output Timing Jitter.** The transmitter output jitter is measured at the output of the twisted-pair model terminated in a 100 Ω load, as shown in Fig 14-8. The jitter added to the signal on the DO circuit as it propagates through the MAU and the twisted-pair model shall be no more than ±3.5 ns.

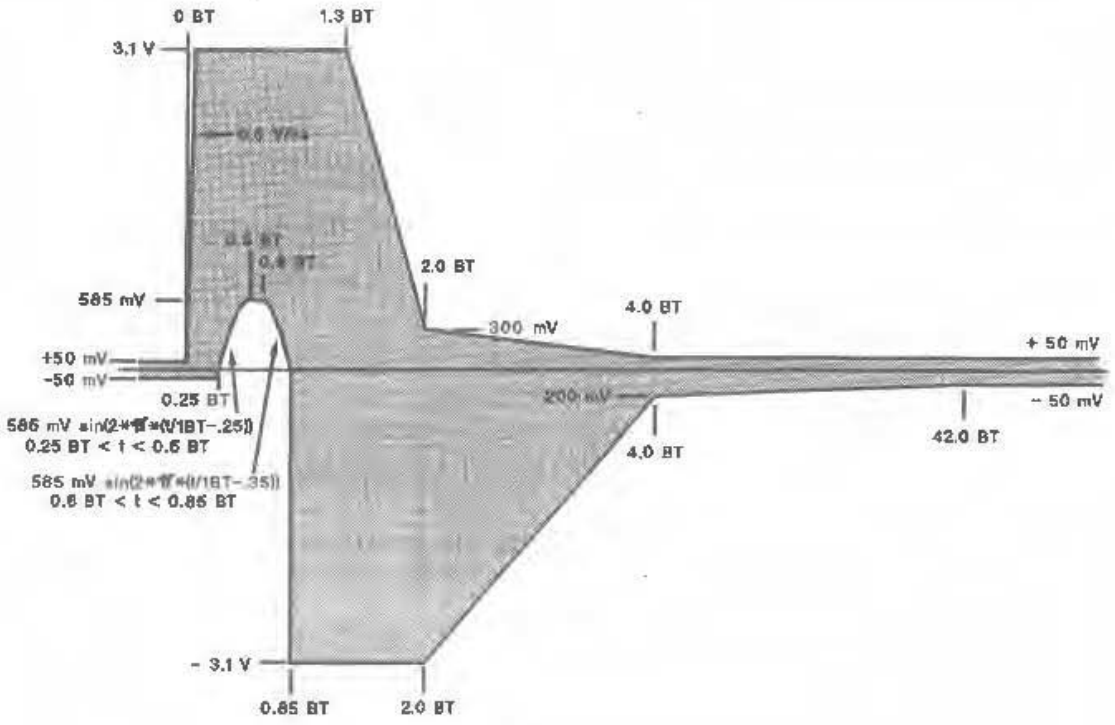



**Fig 14-12**
**Transmitter Waveform for Link Test Pulse**

Additionally, the MAU shall add no more than ±8 ns of jitter to the signal received on the DO circuit when the TD circuit is directly driving a 100 Ω resistive load.

**14.3.1.2.4 Transmitter Impedance Balance.** The common-mode to differential-mode impedance balance of the TD circuit shall exceed $29 - 17 \log_{10}(f/10)$ dB (where f is the frequency in MHz) over the frequency range 1.0 MHz to 20 MHz. This balance is defined as $20 \log_{10}(E_{cm}/E_{dif})$, where $E_{cm}$ is an externally applied sine wave voltage as shown in Fig 14-13.

NOTE: The balance of the test equipment (such as the matching of the 147 Ω resistors) must exceed that required of the transmitter.

**14.3.1.2.5 Common-Mode Output Voltage.** The magnitude of the total common-mode output voltage of the transmitter, $E_{cm}$, measured as shown in Fig 14-14, shall be less than 50 mV peak.

NOTE: This specification is not intended to ensure compliance with regulations concerning RF emissions. The implementor should consider any applicable local, national, or international regulations. Driving unshielded twisted pairs with high-frequency, common-mode voltages may result in interference to other equipment.

**14.3.1.2.6 Transmitter Common-Mode Rejection.** The application of $E_{cm}$, as shown in Fig 14-13, shall not change the differential voltage at the TD circuit, $E_{dif}$, by more than 100 mV for all data sequences. Additionally, the edge jitter added by the application of $E_{cm}$ shall be no more than 1.0 ns. $E_{cm}$ shall be a 15 V peak 10.1 MHz sine wave.

**14.3.1.2.7 Transmitter Fault Tolerance.** Transmitters, when either idle or non-idle, shall withstand without damage the application of short circuits across the TD circuit for an indefinite period of time and shall resume normal operation after such faults are removed. The magnitude of the current through such a short circuit shall not exceed 300 mA.

Transmitters, when either idle or non-idle, shall withstand without damage a 1000 V common-mode impulse applied at $E_{cm}$ of either polarity (as indicated in Fig 14-15). The shape of the impulse shall be 0.3/50 μs (300 ns virtual front time, 50 μs virtual time of half value), as defined in IEC Publication 60 [11].

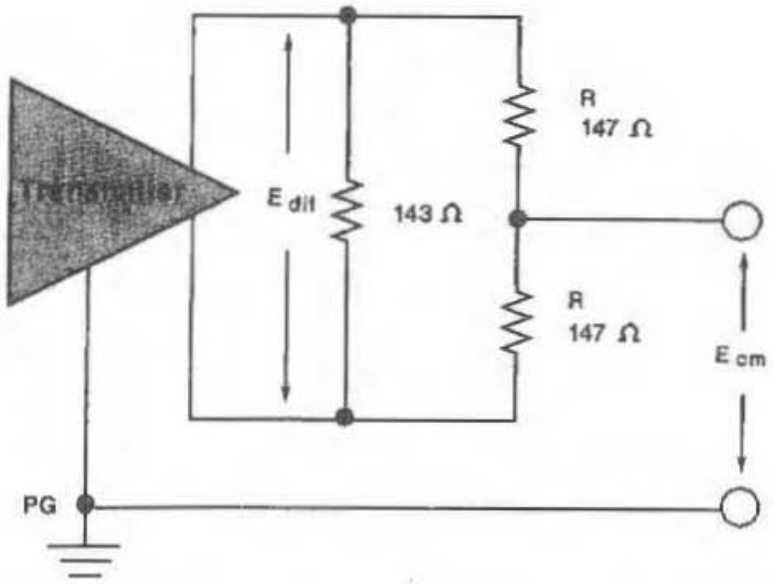



**Fig 14-13**
**Transmitter Impedance Balance and Common-Mode Rejection Test Circuit**

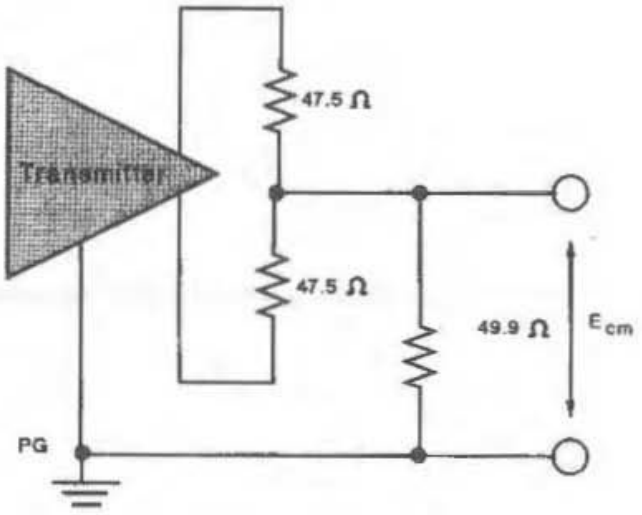



**Fig 14-14**
**Common-Mode Output Voltage Test Circuit**

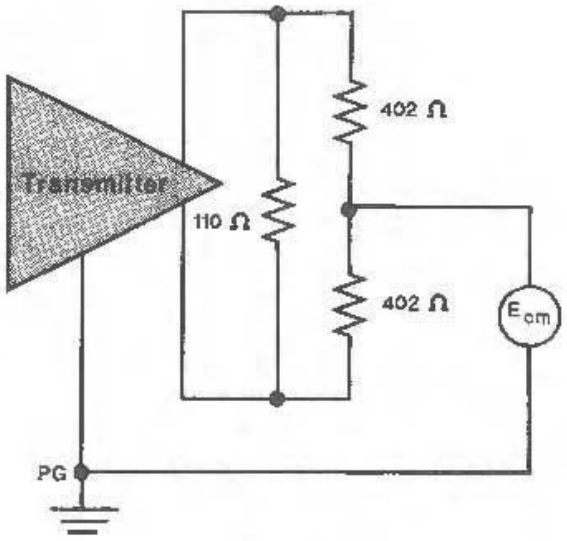



Fig 14-15
**Transmitter Fault Tolerance Test Circuit**

**14.3.1.3 Receiver Specifications.** The MAU shall provide the Receive function specified in 14.2.1.2 in accordance with the electrical specifications of this section.

**14.3.1.3.1 Receiver Differential Input Signals.** Differential signals received on the RD circuit that are within the envelope of Fig 14-16 and 14-17, and have a maximum zero crossing jitter up to ±13.5 ns from the ideal shall be sent to the DI circuit. The 13.5 ns includes jitter caused by an encoder, AUI cable and transmitting MAU, the twisted pair, and noise. Additionally, the MAU receiver shall add no more than ±1.5 ns jitter to the receive signal before sending the signal to the DI circuit.

**14.3.1.3.2 Receiver Differential Noise Immunity.** The receiver, when presented with Manchester-encoded data meeting the requirements of 14.3.1.3.1, shall send this data to the DI circuit with a bit loss of no more than that specified in 14.2.1.2. In addition, the receiver, when presented with a signal meeting the requirements of 14.2.1.1 and within the envelope of Fig 14-12, shall accept it as a link test pulse.

The receiver, while in the Idle state, shall reject as *RD_input* the following signals:

(1) All signals that when measured at the output of the following filter would produce a peak magnitude less than 300 mV. The filter is a 3-pole low-pass Butterworth with a 3 dB cutoff at 15 MHz (refer to A4.2).

(2) All continuous sinusoidal signals of amplitude less than 6.2 V peak-to-peak and frequency less than 2 MHz.

(3) All sine waves of single cycle duration, starting with phase 0 or 180 degrees, and of amplitude less than 6.2 V peak-to-peak where the frequency is between 2 MHz and 15 MHz. For a period of 4 BT before and after this single cycle, the signal shall be less than 300 mV when measured through the filter specified in (1) above.

**14.3.1.3.3 Idle Input Behavior.** The idle condition shall be detected within 2.3 BT of the last low-to-high transition at the receiver. The receiver shall take precautions to ensure that the high-to-silence transition of the start of idle is not falsely interpreted as a silence-to-non-idle-transition, even in the presence of signal droop, overshoot, ringing, slow voltage decay, or a combination thereof due to capacitive and inductive effects in the transmitter, link segment, and receiver.

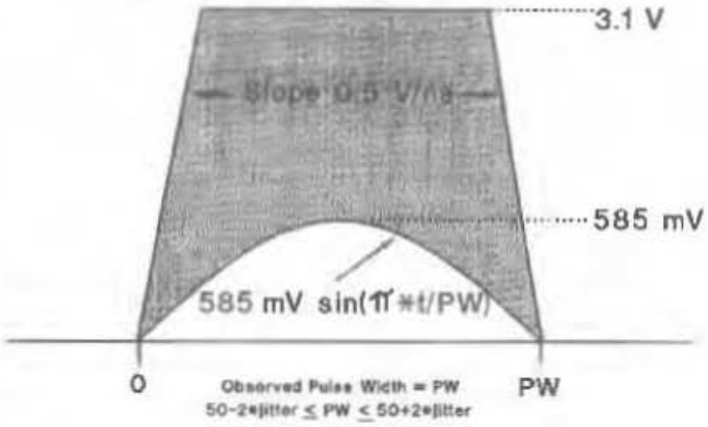



**Fig 14-16**
**Receive Differential Input Voltage—Narrow Pulse**

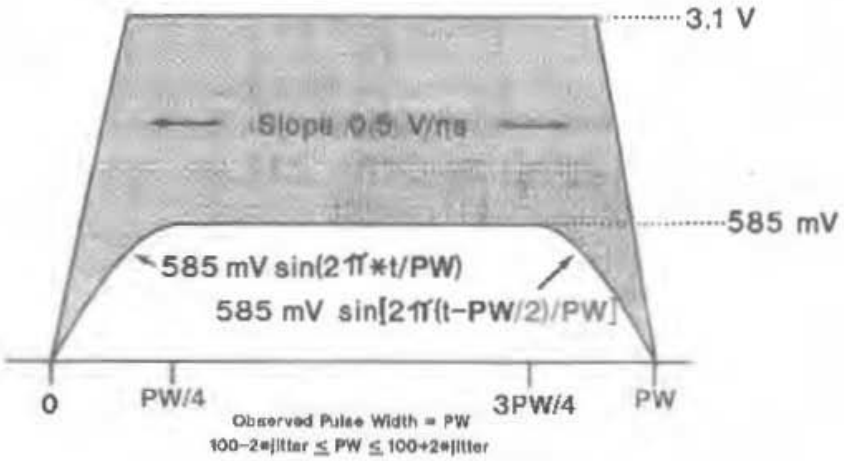



**Fig 14-17**
**Receiver Differential Input Voltage—Wide Pulse**

**14.3.1.3.4 Receiver Differential Input Impedance.** The differential input impedance shall be such that any reflection, due to differential signals incident upon the RD circuit from a twisted pair having any impedance within the range specified in 14.4.2.2 shall be at least 15 dB below the incident over the frequency range of 5.0 MHz to 10 MHz. The return loss shall be maintained when the MAU is powered.

**14.3.1.3.5 Common-Mode Rejection.** Receivers shall assume the proper state on DI for any differential input signal $E_s$ that results in a signal $E_{dif}$ that meets 14.3.1.3.1 even in the presence of common-mode voltages $E_{cm}$ (applied as shown in Fig 14-18). $E_{cm}$ shall be a 25 V peak-to-peak square wave, 500 kHz or lower in frequency, with edges no slower than 4 ns (20%–80%). Additionally, $E_{cm}$ shall contribute no more than 2.5 ns of edge jitter to the signal transmitted on the DI circuit. The combination of the receiver timing jitter of 14.3.1.3.1 and the common-mode induced jitter are such that the MAU shall add no more than 4.0 ns of edge jitter to $E_s$ before sending the signal on the DI circuit.

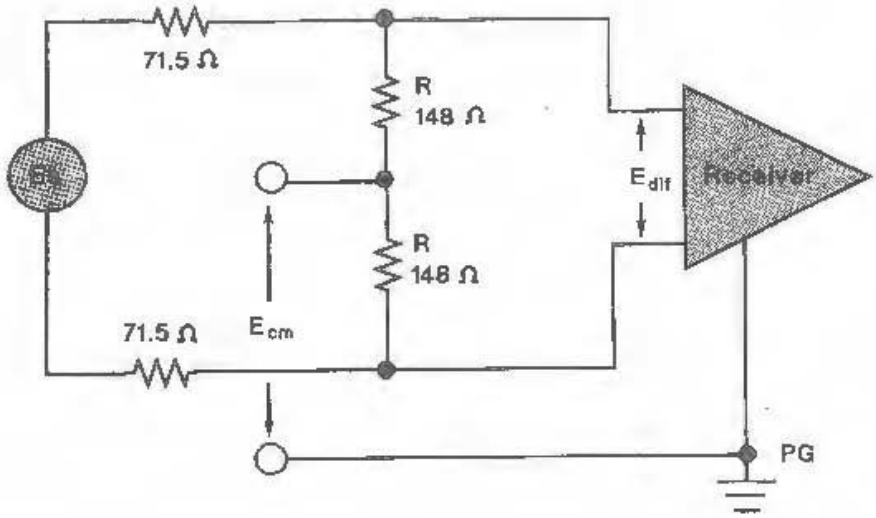



**Fig 14-18**
**Receiver Common-Mode Rejection Test Circuit**

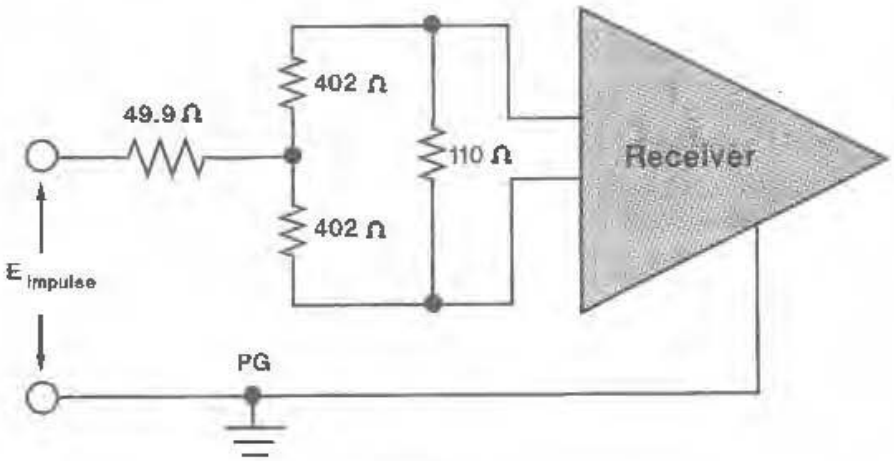



**Fig 14-19**
**Common-Mode Impulse Test Circuit**

**14.3.1.3.6 Receiver Fault Tolerance.** The receiver shall tolerate the application of short circuits between the leads of the RD circuit for an indefinite period of time without damage and shall resume normal operation after such faults are removed. Receivers shall withstand without damage a 1000 V common-mode impulse of either polarity ($E_{impulse}$ as indicated in Fig 14-19). The shape of the impulse shall be 0.3/50 μs (300 ns virtual front time, 50 μs virtual time of half value), as defined in IEC Publication 60 [11].

**14.3.2 MAU-to-AUI Specification.** When a MAU contains a physical AUI connector, the following specifications shall be met.

**14.3.2.1 MAU-AUI Electrical Characteristics.** The electrical characteristics for the driver and receiver components within the MAU that are connected to the AUI shall be identical to those specified in

7.4 and 7.5. Additionally, the AUI DO receiver, while in the Idle state, shall reject an input waveform of less than ±160 mV differential.

**14.3.2.2 MAU-AUI Mechanical Connection.** The MAU shall be provided with a 15-pin male connector as specified in 7.6.

**14.3.2.3 Power Consumption.** Following PowerOn, the surge current drawn by the MAU shall be such that $I_p \times T_w$ is less than or equal to $2 \times 10^{-3}$ ampere-seconds, where $I_p$ is the peak surge current and $T_w$ is the time during which the current exceeds the larger of 0.5 A or $0.5 \times I_p$. After the 100 ms following PowerOn, the current drawn by the MAU shall not exceed 0.5 A when powered by the AUI.

The MAU shall be capable of operating from all possible voltage sources, including those current limited to 0.5 A, as supplied by the DTE or repeater through the resistance of all permissible AUI cables.

The MAU shall not introduce extraneous signals on the TD, CI, or DI circuits during normal power-up and power-down.

**14.4 Characteristics of the Simplex Link Segment.** Except where otherwise stated, the simplex link segment shall be tested with source and load impedances of 100 Ω.

**14.4.1 Overview.** The medium for 10BASE-T is twisted-pair wiring. Since a significant number of 10BASE-T networks are expected to be installed utilizing in-place unshielded telephone wiring and typical telephony installation practices, the end-to-end path including different types of wiring, cable connectors, and cross connects must be considered. Typically, a DTE connects to a wall outlet using a twisted-pair patch cord. Wall outlets connect through building wiring and a cross connect to the repeater MAU in a wiring closet.

NOTE: EIA/TIA 568 (1991) [A19] provides specifications for media and installation practices suitable for use with this standard.

**14.4.2 Transmission Parameters.** Each simplex link segment shall have the following characteristics. All characteristics specified apply to the total simplex link segment unless otherwise noted. These characteristics are generally met by 100 m of unshielded twisted-pair cable composed of 0.5 mm [24 AWG] twisted pairs.

**14.4.2.1 Insertion Loss.** The insertion loss of a simplex link segment shall be no more than 11.5 dB at all frequencies between 5.0 and 10 MHz. This consists of the attenuation of the twisted pairs, connector losses, and reflection losses due to impedance mismatches between the various components of the simplex link segment. The insertion loss specification shall be met when the simplex link segment is terminated in source and load impedances that satisfy 14.3.1.2.2 and 14.3.1.3.4.

NOTE: Multipair PVC-insulated 0.5 mm [24 AWG] cable typically exhibits an attenuation of 8 dB to 10 dB/100 m at 20 °C. The loss of PVC-insulated cable exhibits significant temperature dependence. At temperatures greater than 40 °C, it may be necessary to use a less temperature-dependent cable, such as most plenum-rated cables.

**14.4.2.2 Differential Characteristic Impedance.** The magnitude of the differential characteristic impedance of a 3 m length of twisted pair used in a simplex link segment shall be between 85 Ω and 111 Ω for all frequencies between 5.0 MHz and 10 MHz. Since characteristic impedance tends to decrease with increasing frequency, the above requirement is generally implied by the condition that the magnitude of the characteristic impedance over the frequency band 1 MHz to 16 MHz is 100 Ω ± 15 Ω. Also, the magnitude of the input impedance averaged over the 5.0 MHz to 10 MHz frequency band of a simplex link segment terminated in 100 Ω shall be between 85 Ω and 111 Ω.

**14.4.2.3 Medium Timing Jitter.** Intersymbol interference and reflections due to impedance mismatches between tandem twisted pairs of a twisted-pair link segment and effects of connection devices can introduce jitter to the CD1 and CD0 signals received on the RD circuit. No more than ±5.0 ns of jitter shall be introduced to a test signal by a simplex link segment. The test signal shall have a peak amplitude of 3.0 V and 10% to 90% rise and fall times of 12 ns. The content of the test signal shall be a Manchester-encoded pseudo-random sequence with a minimum repetition period of 511 bits.

NOTE: Branches off a twisted pair (often referred to as "bridged taps" or "stubs") will generally cause excessive jitter and so should be avoided.

**14.4.2.4 Delay.** The maximum propagation delay of twisted pair shall be 5.7 ns/m (minimum velocity of 0.585 × c). The maximum propagation delay of a link segment shall not exceed 1000 ns.

**14.4.3 Coupling Parameters.** To avoid excessive coupling of signals between twisted pairs of a twisted-pair cable, the crosstalk must be limited. Crosstalk loss is specified for the twisted pairs in a twisted-pair cable or twisted-pair cable binder group that are used as 10BASE-T twisted-pair links. Crosstalk loss is specified with the far ends of both the disturbed and the disturbing pairs and the near end of the disturbed pair terminated in 100 Ω. Drivers of disturbing pairs shall have a source impedance of 100 Ω.

**14.4.3.1 Differential Near-End Crosstalk (NEXT) Loss.** The NEXT loss between any two twisted pairs of a twisted-pair cable is dependent upon the geometry of the twisted-pair cable. Since the proximity of any two twisted pairs is influenced by the size of the twisted-pair cable, the NEXT loss is affected by twisted-pair cable size.

**14.4.3.1.1 Twenty-Five-Pair Cable and Twenty-Five-Pair Binder Groups.** The NEXT loss between any two twisted pairs in a twenty-five-pair twisted-pair cable or binder group used for 10BASE-T applications shall be at least $30 - 15 \log_{10}(f/10)$ dB (where f is the frequency in MHz) over the frequency range 5.0 MHz and 10 MHz.

**14.4.3.1.2 Four-Pair Cable.** The NEXT loss between any two twisted pairs in a four-pair twisted-pair cable used for 10BASE-T applications shall be at least $26 - 15 \log_{10}(f/10)$ dB (where f is the frequency in MHz) over the frequency range 5.0 MHz and 10 MHz.

**14.4.3.1.3 Other Cables.** The NEXT loss requirement for all other twisted-pair cables shall be the multiple-disturber NEXT loss of 14.4.3.2.

**14.4.3.2 Multiple-Disturber NEXT (MDNEXT) Loss.** When a twisted-pair cable or twisted-pair cable binder group contains twisted pairs from multiple 10BASE-T twisted-pair link segments, the multiple-disturber crosstalk loss is dependent upon the specific selection of disturbing and disturbed pairs. For each 10BASE-T receive pair, MDNEXT is measured by having the remaining near-end transmit pairs (excluding the transmit pair associated with the receive pair under test) driven with identical and synchronized sine wave signals. MDNEXT may then be determined from the signal level observed on the receive pair under test. By examining all pair combinations with a fixed number of disturbers, a cumulative distribution of MDNEXT is obtained at each frequency of interest. The one percentile of this cumulative distribution shall be at least $23 - 15 \log_{10}(f/10)$ (where f is the frequency in MHz) at 5.0 MHz, 7.5 MHz, and 10 MHz. When the number of possible combinations allowed by a cable is fewer than 100, the MDNEXT loss for all combinations shall be at least $23 - 15 \log_{10}(f/10)$ (where f is the frequency in MHz) at 5.0 MHz, 7.5 MHz, and 10 MHz. Refer to 12.7.3.2 and Appendix A3 for a tutorial and method for estimating the MDNEXT loss for a complete n-pair cable.

**14.4.4 Noise Environment.** The noise level on the link segments shall be such that the objective error rate is met. The noise environment consists generally of two primary contributors: crosstalk from other 10BASE-T circuits; and externally induced impulse noise, typically from telephone ringing and dialing signals, and other office and building equipment.

**14.4.4.1 Impulse Noise.** The average rate of occurrence of impulses greater than 264 mV shall be less than or equal to 0.2/s as measured at the output of the following specified filter. Following the start of any particular impulse that is counted, any additional impulse shall be ignored for a period of 1 μs. The simplex link segment shall be terminated at the far end in 100 Ω. The filter is a 3-pole Butterworth low-pass with a 3 dB cutoff at 15 MHz (refer to A4.2).

NOTE: Typically, the impulse noise occurrence rate changes inversely by one decade for each 5 dB to 9 dB change in the threshold voltage. If a count rate of N counts/s is measured on a specific twisted pair and filter at the specified voltage threshold, the media noise margin is approximately $7 \log_{10}(0.2/N)$ dB. Impulse noise may be a burst phenomenon and should be measured over an extended period of time.

**14.4.4.2 Crosstalk Noise.** The level of crosstalk noise on a simplex link segment depends on the level of the disturbing signal(s) and the crosstalk loss between the pair(s) carrying the signal(s) and the dis-

turbed pair. With the maximum transmit level (14.3.1.2), the sinusoidal crosstalk loss (14.4.3.2), and multiple, random Manchester-encoded disturbers, the peak self-crosstalk noise levels as measured at the output of the following specified filter shall be less than or equal to 264 mV. The filter is a 3-pole Butterworth low-pass with a 3 dB cutoff at 15 MHz (refer to A4.2).

**14.5 MDI Specification.** This section defines the MDI for the twisted-pair link segment. The link topology requires a crossover function between PMAs. Implementation and location of this crossover is also defined in this section.

**14.5.1 MDI Connectors.** Eight-pin connectors meeting the requirements of Section 3 and Figures 1–5 of ISO 8877 [20] shall be used as the mechanical interface to the twisted-pair link segment. The plug connector shall be used on the twisted-pair link segment and the jack on the MAU. These connectors are depicted (for informational use only) in Figs 14-20 and 14-21. The following table shows the assignment of signals to connector contacts.

| CONTACT | MDI SIGNAL |
|---|---|
| 1 | TD+ |
| 2 | TD– |
| 3 | RD+ |
| 4 | Not used by 10BASE-T |
| 5 | Not used by 10BASE-T |
| 6 | RD– |
| 7 | Not used by 10BASE-T |
| 8 | Not used by 10BASE-T |

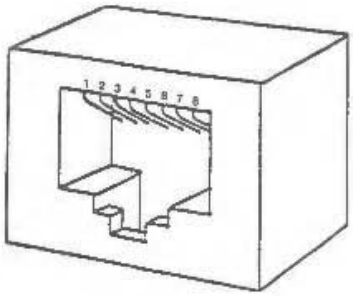



**Fig 14-20**
**MAU MDI Connect**

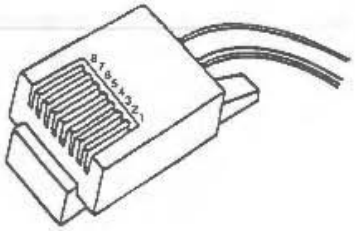
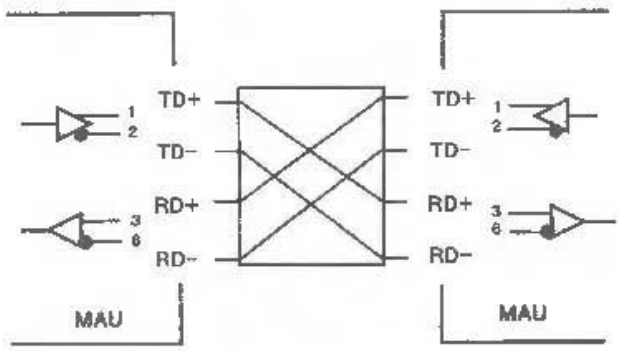
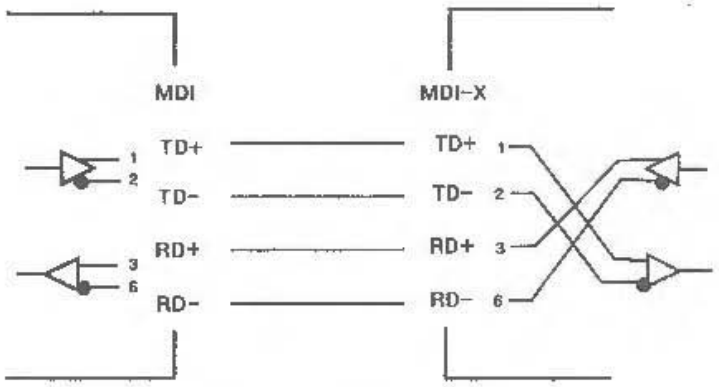


**Fig 14-21**
**Twisted-Pair Link Segment Connector**

**14.5.2 Crossover Function.** A crossover function shall be implemented in every twisted-pair link. The crossover function connects the transmitter of one MAU to the receiver of the MAU at the other end of the twisted-pair link. Crossover functions may be implemented internally to a MAU or elsewhere in the twisted-pair link. For MAUs that do not implement the crossover function, the signal names of 14.5.1 refer to their own internal circuits. For MAUs that do implement the crossover function, the signal names refer to the remote MAU of the twisted-pair link. Additionally, the MDI connector for a MAU that implements the crossover function shall be marked with the graphical symbol "X". Internal and external crossover functions are shown in Fig 14-22.




**(a) External Crossover Function**




**(b) MAU-Embedded Crossover Function**

**Fig 14-22**
**Crossover Function**

When a twisted-pair link connects a DTE to a repeater, it is recommended that the crossover be implemented in the MAU local to the repeater. If both MAUs of a twisted-pair link contain internal crossover functions, an additional external crossover is necessary. It is recommended that the crossover be visible to an installer from one of the MAUs. When both MAUs contain internal crossovers, it is further recommended in networks in which the topology identifies either a central backbone segment or a central hub that the MAU furthest from the central element be assigned the external crossover to maintain consistency.

Implicit implementation of the crossover function within a twisted-pair cable, or at a wiring panel, while not expressly forbidden, is beyond the scope of this standard.

**14.6 System Considerations.** The repeater unit specified in Section 9 forms the central unit for interconnecting 10BASE-T twisted-pair links in networks of more than two nodes. It also provides the means for connecting 10BASE-T twisted-pair links to other 10 Mb/s baseband segments. The proper operation of a CSMA/CD network requires network size to be limited to control round-trip propagation delay to meet the requirements of 4.2.3.2.3 and 4.4.2.1, and the number of repeaters between any two DTEs to be limited in order to limit the shrinkage of the interpacket gap as it travels through the network. Configuration rules, which ensure that these limits are not exceeded, are given in Section 13.

### 14.7 Environmental Specifications

**14.7.1 General Safety.** All equipment meeting this standard shall conform to one of the following IEC Publications: 380 [5], 435 [6], or 950 [8].

NOTE: For ISO/IEC 8802-3 : 1993, conformance shall be to IEC 950 [8].

**14.7.2 Network Safety.** This section sets forth a number of recommendations and guidelines related to safety concerns; the list is neither complete nor does it address all possible safety issues. The designer is urged to consult the relevant local, national, and international safety regulations to ensure compliance with the appropriate requirements.

LAN cable systems described in this section are subject to at least four direct electrical safety hazards during their installation and use. These hazards are as follows:

(1) Direct contact between LAN components and power, lighting, or communications circuits.
(2) Static charge buildup on LAN cables and components.
(3) High-energy transients coupled onto the LAN cable system.
(4) Voltage potential differences between safety grounds to which various LAN components are connected.

Such electrical safety hazards must be avoided or appropriately protected against for proper network installation and performance. In addition to provisions for proper handling of these conditions in an operational system, special measures must be taken to ensure that the intended safety features are not negated during installation of a new network or during modification or maintenance of an existing network. Isolation requirements are defined in 14.3.1.1.

**14.7.2.1 Installation.** Sound installation practice, as defined by applicable local codes and regulations, shall be followed in every instance in which such practice is applicable.

**14.7.2.2 Grounding.** Any safety grounding path for the MAU shall be provided through the circuit PG of the AUI connection.

WARNING: It is assumed that the equipment to which the MAU is attached is properly earthed, and not left floating nor serviced by a "doubly insulated ac power distribution system." The use of floating or insulated equipment, and the consequent implications for safety are beyond the scope of this standard.

**14.7.2.3 Installation and Maintenance Guidelines.** During installation and maintenance of the cable plant, care shall be taken to ensure that uninsulated network cable conductors do not make electrical contact with unintended conductors or ground.

**14.7.2.4 Telephony Voltages.** The use of building wiring brings with it the possibility of wiring errors that may connect telephony voltages to 10BASE-T equipment. Other than voice signals (which are low voltage), the primary voltages that may be encountered are the "battery" and ringing voltages. Although there is no universal standard, the following maximums generally apply.

Battery voltage to a telephone line is generally 56 Vdc applied to the line through a balanced 400 Ω source impedance.

Ringing voltage is a composite signal consisting of an ac component and a dc component. The ac component is up to 175 V peak at 20 Hz to 60 Hz with a 100 Ω source resistance. The dc component is 56 Vdc with a 300 Ω to 600 Ω source resistance. Large reactive transients can occur at the start and end of each ring interval.

Although 10BASE-T equipment is not required to survive such wiring hazards without damage, application of any of the above voltages shall not result in any safety hazard.

NOTE: Wiring errors may impose telephony voltages differentially across 10BASE-T transmitters or receivers. Because the termination resistance likely to be present across a receiver's input is of substantially lower impedance than an off-hook telephone instrument, receivers will generally appear to the telephone system as off-hook telephones. Therefore, full-ring voltages will be applied for only short periods. Transmitters that are coupled using transformers will similarly appear like off-hook telephones (though perhaps a bit more slowly) due to the low resistance of the transformer coil.

### 14.7.3 Environment

**14.7.3.1 Electromagnetic Emission.** The twisted-pair link shall comply with applicable local and national codes for the limitation of electromagnetic interference.

**14.7.3.2 Temperature and Humidity.** The twisted-pair link is expected to operate over a reasonable range of environmental conditions related to temperature, humidity, and physical handling (such as shock and vibration). Specific requirements and values for these parameters are considered to be beyond the scope of this standard.

It is recommended that manufacturers indicate in the literature associated with the MAU the operating environmental conditions to facilitate selection, installation, and maintenance.

It is recommended that manufacturers indicate, in the literature associated with the components of the twisted-pair link segment, the distance and operating environmental conditions over which the specifications of 14.4 will be met.

**14.8 MAU Labeling.** It is recommended that each MAU (and supporting documentation) be labeled in a manner visible to the user with at least these parameters:

(1) Data rate capability in Mb/s,
(2) Power level in terms of maximum current drain (for external MAUs),
(3) Any applicable safety warnings.

See also 14.5.2.

**14.9 Timing Summary.** Table 14-2 summarizes the timing requirements for the 10BASE-T twisted-pair link. This table is a summary; for complete descriptions of the timing requirements, refer to the referenced sections.

**Table 14-2**
**Maximum Timing Parameters**

| Symbol | Function | Bit Loss† | Invalid Bits† | Steady-State Propagation Delay† | Start-up Delay† Maximum | Start-up Delay† Variability‡ | Specified in |
|---|---|---|---|---|---|---|---|
| M1 | *RD_input* to *input* on DI | 5.0 | 1.0 | 2.0 | 8.0 | 2.0 | 14.2.1.2 |
| M2 | *output* on DO to *TD_output* | 2.0 | 1.0 | 2.0 | 5.0 | 2.0 | 14.2.1.1 |
| M3 | *RD_input* * *output* to *signal_quality_error* | — | — | — | 9.0 | — | 14.2.1.4 |
| M4 | *RD_idle* + *output_idle* (end of collision) to *mau_available* | — | — | — | 9.0 | — | 14.2.1.4 |
| M5 | *RD_input* * *output* to *input* on DI from circuit RD | — | — | — | 9.0 | — | 14.2.1.4 |
| M6 | *RD_idle* * *output* to *input* on DI from circuit DO | — | — | — | 9.0 | — | 14.2.1.4 |
| M7 | *output_idle* on DO to *signal_quality_error* | — | — | — | $6 < x < 16$ | — | 14.2.1.5 |
| M8 | *signal_quality_error* duration for SQE test | — | — | — | $5 < x < 15$ | — | 14.2.1.5 |
| M9 | *output* on DO to *input* on DI | 5.0 | 1.0 | 1.0 | 7.0 | — | 14.2.1.3 |
| T1 | twisted-pair propagation | 0 | 0 | 10.00 | 10.00 | — | 14.4.2.4 |
| A1 | AUI cable propagation (50 m) | 0 | 0 | 2.57 | 2.57 | — | 7.4.3.7 |

†All Time in BT.
‡For an explanation of the meaning of variability, see 14.2.11 and 14.2.12.

# Annex
# Additional Reference Material

(This Annex is not a part of this International Standard but is a part of ANSI/IEEE Std 802.3, 1993.)

[A1] ANSI/EIA 364A-1987, Standard Test Procedures for Low-Frequency (Below 3 MHz) Electrical Connector Test Procedure.[14]

[A2] ANSI/IEEE Std 770X3.97-1983, IEEE Standard Pascal Computer Programming Language.[15]

[A3] Material from this reference is now incorporated into the base standard.

[A4] Material from this reference is now incorporated into the base standard.

[A5] ANSI/NFPA 70-1987, National Electrical Code.[16]

[A6] ANSI/UL 94-1985, Tests for Flammability of Plastic Materials for Parts in Devices and Appliances.[17]

[A7] ANSI/UL 114-1982, Safety Standard for Office Appliances and Business Equipment.

[A8] ANSI/UL 478-1979, Safety Standard for Electronic Data-Processing Units and Systems.

[A9] ECMA-97 (1985), Local Area Networks Safety Requirements.[18]

[A10] EIA CB8-1981, Components Bulletin (Cat 4) List of Approved Agencies, US and Other Countries, Impacting Electronic Components and Equipment.

[A11] FCC Docket 20780-1980 (Part 15), Technical Standards for Computing Equipment. Amendment of Part 15 to redefine and clarify the rules governing restricted radiation devices and low-power communication devices. Reconsidered First Report and Order, April 1980.[19]

[A12] MIL-C-17F-1983, General Specification for Cables, Radio Frequency, Flexible and Semirigid.[20]

[A13] MIL-C-24308B-1983, General Specifications for Connector, Electric, Rectangular, Miniature Polarized Shell, Rack and Panel.

[A14] UL Subject No 758: UL VW-1, Description of Appliance Wiring Material.[21]

[A15] AMP, Inc., Departmental Publication 5525, Design Guide to Coaxial Taps. Harrisburg, PA 17105.

[A16] AMP, Inc., Instruction Sheet 6814, Active Tap Installation. Harrisburg, PA 17105.

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[14] All ANSI publications are available from the Sales Department, American National Standards Institute, 11 West 42nd Street, New York, NY 10036, USA; EIA publications are available from the Standards Sales Department, Electronic Industries Association, 1001 Eye Street, NW, Washington, DC 20006, USA.

[15] IEEE publications are available from the Service Center, Institute of Electrical and Electronics Engineers, 445 Hoes Lane, P.O. Box 1331, Piscataway, NJ 08855-1331, USA.

[16] NFPA publications are available from Publications Sales, National Fire Protection Association, Batterymarch Park, Quincy, MA 02269-9101, USA.

[17] UL publications are available from Publications Sales, Underwriters Laboratories, Inc., 333 Pfingston Rd., Northbrook, IL 60020, USA.

[18] ECMA publications are available from European Computer Manufacturers Association, 114 Rue du Rhone, 1204 Geneva, Switzerland.

[19] FCC publications are available from the Federal Communications Commission, Washington, DC 20402, USA.

[20] MIL publications are available from US Navy Publications and Forms Center, 5801 Tabor Avenue, Philadelphia, PA 19120, USA.

[21] Information on this subject is available from Underwriters Laboratories, Inc., 1285 Walt Whitman Road, Melville, NY 11747, USA.

[A17] Brinch Hansen, P. The Architecture of Concurrent Programs. Englewood Cliffs, NJ: Prentice Hall, 1977.

[A18] Hammond, J.L., Brown, J.E., and Liu, S.S. Development of a Transmission Error Model and Error Control Model. Technical Report RADC-TR-75-138. Rome: Air Development Center (1975).

[A19] EIA/TIA 568 (1991), Commercial Building Wiring Standard.

# Appendixes

(These Appendixes are not a part of this International Standard or of ANSI/IEEE Std 802.3, 1993 Edition.)

# Appendix A
# System Guidelines

## A1. Baseband System Guidelines and Concepts

**A1.1 Overall System Objectives.** The CSMA/CD Access Method, supported by baseband technology, depends on a variety of analog system components at and below the physical level of the OSI Reference Model. These components provide basic interconnection facilities for the CSMA/CD access mechanism itself and are defined throughout Sections 6, 7, and 8.

Overall performance of the analog baseband medium and related physical layer capabilities depends on an optimal and known set of analog capabilities within each of these critical system elements: the coaxial trunk cable, MAUs, branch cables, DTEs, and repeater units. These system elements affect the integrity with which the serial data bit stream analog signals are carried between open systems. There are at least three critical parameters of interest: bits lost in the transmission system, signal delays, and phase jitter. It is important that these be apportioned properly among the affected system elements.

The successful interconnection of multivendor system components mandates that the values for bits lost, signal delays, and phase jitter be allocated fairly and realistically among the various system elements. The balance of Appendix A identifies the upper limits of values to be placed on the subject parameters. These values are based on the maximal system configuration (for example, four repeater units, 2.5 km trunk coaxial cable medium).

**A1.2 Analog System Components and Parameter Values.** The values given in the following table are in terms of bits and are stated as maximum values except for values given within ranges.

The initial mnemonic under each component entry refers to the system component as identified in Fig A1. System parameters are stated in terms of the intralayer or interlayer messages sent within a station. Specific delays are called out as = delay.

The repeater concepts described throughout this section are considered to be an acceptable set of specifications for a multirepeatered system. It is noted that the exact parametric values specified for the repeater environment are subject to minor refinement.

| Component and Parameter | | Start Up Delay | Last In to Last Out Delay | Start Up Loss |
|---|---|---|---|---|
| **MEDIUM** | | | | |
| Trunk Coaxial Cable | | | | |
| C1 | Propagation | 0.0 | 21.65 | 0.0 |
| **POINT TO POINT LINK** | | | | |
| P1 | Propagation | 0.0 | 25.64 | 0.0 |
| AUI | | | | |
| A1 | Propagation | 0.0 | 2.57 | 0.0 |
| **MEDIUM ACCESS UNIT** | | | | |
| M1 | DATA IN ASSERT → INPUT | 6.0 | 0.5 | 5.0 |
| M2 | OUTPUT → DATA OUT ASSERT | 3.0 | 0.5 | 2.0 |
| M3 | DATA IN COLLISION → SQE ASSERT | 17.0 | — | — |
| M4 | COLLISION DEASSERT → SQE DEASSERT | 20.0 | — | — |
| M5 | OUTPUT IDLE → SQE ASSERT | $6 < x < 16$ | — | — |
| M6 | SQE TEST ASSERT → SQE DEASSERT | $5 \leq x \leq 15$ | — | — |

| Component and Parameter | | Start Up Delay | Last In to Last Out Delay | Start Up Loss |
|---|---|---|---|---|
| **DTE** | | | | |
| D1 | INPUT → INPUT UNIT | 18.0 | — | 18.0 |
| D2 | OUTPUT UNIT → OUTPUT | — | 3.0 | — |
| D3 | INPUT → CARRIER STATUS = CARRIER ON | 3.0 | — | — |
| D4 | INPUT IDLE → CARRIER STATUS = OFF | 3.0 < x ≤ 6.0 | — | — |
| D5 | SQE ASSERT → CARRIER STATUS = ON | 3.0 | — | — |
| D6 | SQE DEASSERT → CARRIER STATUS = OFF | 3.0 < x ≤ 6.0 | — | — |
| D7 | SQE ASSERT → SIGNAL STATUS = ERROR | 3.0 | — | — |
| D8 | SQE DEASSERT → SIGNAL STATUS = NO ERROR | 3.0 < x ≤ 6.0 | — | — |
| D9 | CARRIER STATUS = OFF → OUTPUT UNIT | 96 ≤ x ≤ 100 | — | — |
| D10 | INPUT → OUTPUT | 8.0 | — | — |
| D11 | SIGNAL STATUS = ERROR → JAM OUTPUT | 16.0 | — | — |
| D12 | JAM OUTPUT DURATION | =32.0 | — | — |
| **REPEATER UNIT** | | | | 22 < x < 34 |
| R1 | INPUT 1,2 → OUTPUT 2,1 | 7.5 | — | — |
| R2 | INPUT IDLE 1,2 → OUTPUT IDLE 2,1 | — | 12.5 | — |
| R3 | INPUT 1,2 → CARRIER STATUS = ON | 3.0 | — | — |
| R4 | SQE → SOURCED OUTPUT | 6.5 | — | — |
| R5 | JAM OUTPUT → OUTPUT IDLE | =96.0 | — | — |

Figure A1 indicates the maximal system configuration and identifies the various system component parameters considered critical in determining analog system performance.

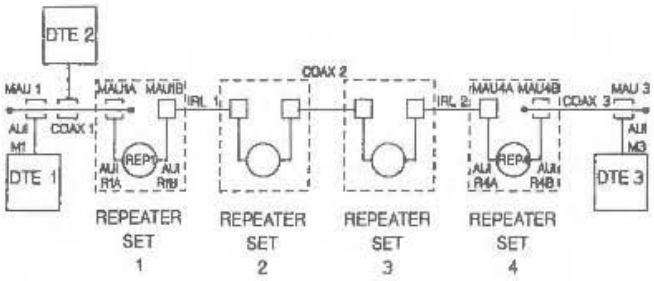


**Fig A1**
**Maximal System Configuration Bit Budget Apportionments**

**A1.3 Minimum Frame Length Determination.** The following table indicates the system elements that make up the minimum frame length calculation based on the worst-case numbers as outlined in the bit budget of A1.2. The compilation in the following table is based on the following scenario:

(1) DTE 1 transmits to an adjacent DTE 2 on coaxial segment 1.
(2) DTE 3 transmission collides with DTE 1 transmission.
(3) DTE 3 is assumed to be the worst-case distance from DTE 1 and its transmission just misses deferring to the DTE 1 message.
(4) The collision fragment travels back down the network to inform DTE 1 that a collision has occurred on its message.

The frame length is constrained by two parameters:

(a) The message from DTE 1 shall be long enough so that it is still sending when the collision is detected.
(b) The message from DTE 1 shall be short enough such that DTE 2 can throw out the message on the basis of being too short.

| Component and Function | Direction | Table Entry | Delay | Total Delay |
|---|---|---|---|---|
| **DTE 1 STARTS TO PUT OUT FIRST BIT** | | | | 0.0 |
| DTE 1 | FWD | D2 | 3.0 | 3.0 |
| AUI M1 | FWD | A1 | 2.57 | 5.57 |
| MAU1 | FWD | M2 | 3.0 | 8.6 |
| COAX1 | FWD | C1 | 21.65 | 30.2 |
| **REPEATER SET 1** | | | | |
| MAU 1A | FWD | M1 | 6.0 | 36.2 |
| AUI R1A | FWD | A1 | 2.57 | 38.8 |
| REP 1 | FWD | R1 | 7.5 | 46.3 |
| AUI R1B | FWD | A1 | 2.57 | 48.9 |
| MAU 1B | FWD | M2 | 3.0 | 51.9 |
| **REPEATER SET TOTAL** | | | 21.64 | |
| IRL 1 | FWD | P1 | 25.64 | 77.5 |
| REPEATER SET 2 | FWD | | 21.6 | 99.1 |
| COAX 2 | FWD | C1 | 21.65 | 120.8 |
| REPEATER SET 3 | FWD | | 21.6 | 142.4 |
| IRL 2 | FWD | P1 | 25.64 | 168.1 |
| REPEATER SET 4 | FWD | | 21.6 | 189.7 |
| COAX 3 | FWD | C1 | 21.65 | 211.4 |
| MAU 3 | FWD | M1 | 6.0 | 217.4 |
| AUI 3 | FWD | A1 | 2.57 | 219.9 |
| DTE 3 PUTS OUT A BIT | REV | D10 | 8.0 | 227.9 |
| AUI 3 | REV | A1 | 2.57 | 230.5 |
| MAU 3 | REV | M2 | 3.0 | 233.5 |
| COAX 3 | REV | C1 | 21.65 | 255.1 |
| **REPEATER SET 4** | | | | |
| MAU 4B | REV | M3 | 17.0 | 272.1 |
| AUI 4B | REV | A1 | 2.57 | 274.7 |
| REP 4 | REV | R4 | 6.5 | 281.2 |
| AI 4A | REV | A1 | 2.57 | 283.8 |
| MAU 4A | REV | M2 | 3.0 | 286.8 |
| **REPEATER SET TOTAL** | | | 31.64 | |
| IRL 2 | REV | P1 | 25.64 | 312.4 |
| REPEATER SET 3 | REV | | 31.64 | 344.1 |
| COAX 2 | REV | C1 | 21.65 | 365.7 |
| REPEATER 2 | REV | | 31.64 | 397.4 |
| IRL 1 | REV | P1 | 25.64 | 423.0 |
| REPEATER SET 1 | REV | | 31.64 | 454.6 |
| COAX 1 | REV | C1 | 21.65 | 476.3 |
| MAU 1 | REV | M3 | 17.0 | 493.3 |
| AUI M1 | REV | A1 | 2.57 | 495.9 |
| DTE 1 | REV | D7 | 3.0 | 498.9 |

The above table provides the scenario that enables DTE 1 to determine a collision is taking place. DTE 1 shall transmit for at least 499 bit times. To determine how much longer DTE 2 will continue to receive bits, assume that DTE 1 is the last transmitter to provide bits to the DTE 2 MAU. DTE 2 then sees the following:

| Component and Function | Direction | Table Entry | Delay | Total Delay |
|---|---|---|---|---|
| DTE 1 | FWD | D11 | 16.0 | 514.9 |
| DTE 1 | FWD | D12 | 32.0 | 547.9 |
| AUI M1 | FWD | A1 | 2.57 | 549.4 |

If Repeater Set 1 is the last system component to provide bits to DTE 2, then DTE 2 will see the following:

| Component and Function | Direction | Table Entry | Delay | Total Delay |
|---|---|---|---|---|
| **REPEATER SET 1 (1st JAM BIT)** | | | | 454.6 |
| REP 1 | REV | R5 | 96.0 | 550.6 |
| COAX 1 | REV | C1 | 21.65 | 572.3 |

The Repeater Set is the last transmitter to provide a bit to DTE 2. The DTE 2 MAU starts seeing bits at time 8.6, which means that DTE 2 sees 563.7 bits (572.3 – 8.6). DTE 2 sees a minimum of 61 preamble bits and 8 SFD bits. The preamble and SFD bits can be deleted from the 563.7 total because they are not counted in minimum frame length.

The minimum frame length determination from the above scenario is then 564.7 – 69.0 = 494.7 bits. The 10 Mb/s system value for minimum frame length has been set at 512 bits.

**A1.4 System Jitter Budgets.** The typical jitter budget expected for the baseband system is apportioned in the following manner:

| | |
|---|---|
| Encoder | 0.5 ns |
| AUI Cable | 1.0 ns (transmit end) |
| MAU Transmit | 2.0 ns |
| Trunk Coax | 7.0 ns |
| MAU Receive | –1.0 ns (with compensation) |
| AUI Cable | 1.0 ns (receive end) |
| SNR on COAX | 5.0 ns (SNR = 5:1) |
| SNR on AUI | 0.5 ns (SNR = 5:1, transmit end) |
| SNR on AUI | 0.5 ns (SNR = 5:1; receive end) |
| | 16.5 ns |

The 18 ns jitter budget leaves adequate design margin for implementation-dependent considerations.

**A1.4.1 Nominal Jitter Values.** The jitter budget values given above are not expected to accommodate all step changes in phase jitter due to system parameter variations within one or a few bit times.

**A1.4.2 Decoder Evaluation.** The phase decoder in the PLS sublayer should correctly decode a Manchester-encoded signal whose data transition point (center of a bit cell) has a peak-to-peak jitter of no more than 36 ns (± 18 ns deviation from the bit cell center). See Figs A2 and A3 for test method.

Evaluation of decoder performance may be simulated and tested by application of three distinct waveforms representing worst-case and normal conditions. The waveforms contain Manchester-encoded bits whose center transitions represent the extremes of maximum skew. A 5 MHz (repetition rate) pulse train whose pulse width is either 64 ns or 136 ns simulates the two worst-case jitter conditions. The data output from the decoder should remain stable for each of the three test patterns and shifts between these extremes where there is a low rate of change in center transition skew. Note that the actual transmission system is not expected to permit sudden drastic changes in the steady-state edge deviation during the reception of any given frame. The above evaluation process is not intended to guarantee proper decoder performance under all operating conditions.

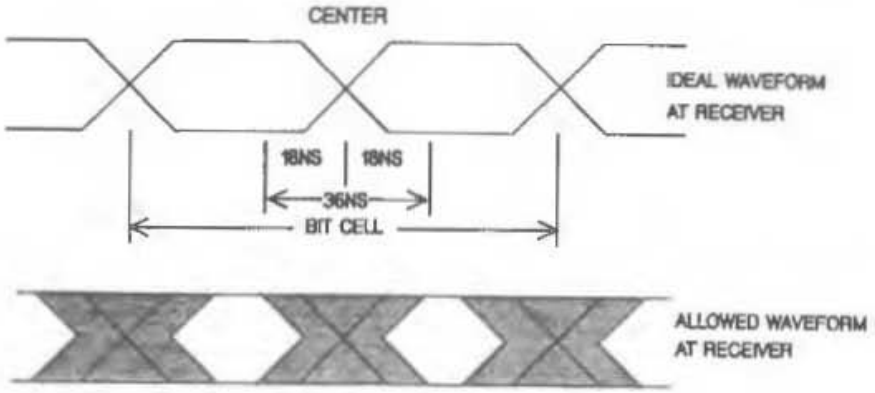


**Fig A2**
**Typical Signal Waveforms**

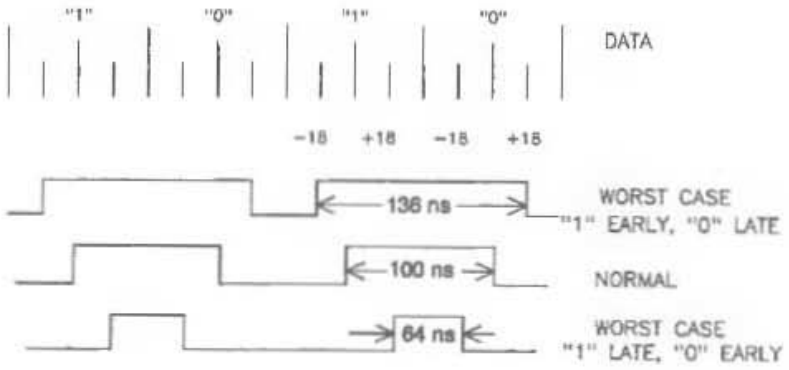


**Fig A3**
**Worst-Case Signal Waveform Variations**

## A2. System Parameters and Budgets for 1BASE5

**A2.1 Delay Budget.** The successful interconnection of multivendor system components mandates that the values for bits lost and signal delays be allocated fairly and realistically among the various system elements. The following table summarizes and indicates the derivation of some of the delays specified in 12.9. The breakdowns shown for the parameters are illustrative only; implementors are free to make other allocations of delay *within* a device so long as the specifications of 12.9 are not violated.

| Component | Delay (BT) |
|---|---|
| DTE Initial Transmit Delay (see 12.9.2) | 3 |
| DTE Deference Delay (see 12.9.2) | 21 |
| unsquelch | 3 |
| Carrier detect | 5 |
| MAC detects carrier and defers | 10 |
| DTE Initial Transmit Delay | 3 |
| DTE Collision Shutdown Delay (see 12.9.2) | 58 |
| detect CP and report SIGNAL_ERROR | 10 |
| detect SIGNAL_ERROR and start jamming | 16 |
| jamSize | 32 |
| Medium Transit Delay (see 12.9.3) | 4 |
| Special Link Transit Delay (see 12.9.4) | 15 |
| Hub Startup Delay (see 12.9.5) | 12 |
| unsquelch | 4 |
| half fill FIFO | 6 |
| analogue of DTE Initial Transmit Delay | 3 |
| Hub Idle Collision Startup Delay (see 12.9.5) (same as Hub Startup Delay) | 12 |
| Hub Transit Delay (see 12.9.5) | 9 |
| half fill FIFO | 6 |
| analogue of DTE Initial Transmit Delay | 3 |
| Hub Delay Stretch/Shrink (see 12.9.5) ((preamble + <sfd> + maxFrameSize) · 0.01% · 2) | 3 |
| Hub Collision Detect Delay (see 12.9.5) | 21 |
| unsquelch | 3 |
| detect collision | 6 |
| Hub Transit Delay | 9 |
| First CVL or CVH may be preceded by CD0s and CD1s | 3 |
| Hub Active Collision Startup Delay (see 12.9.5) | 12 |
| Hub Transit Delay | 9 |
| First CVL or CVH may be preceded by CD0s and CD1s | 3 |

| Component | Delay (BT) |
|---|---|
| Hub Collision Shutdown Delay (downward) (see 12.9.5) (same as Hub Transit Delay) | **9** |
| Hub Collision Shutdown Delay (upward) (see 12.9.5) | **25** |
| detect loss of carrier | 20 |
| clear FIFO, if necessary | 2 |
| analogue of DTE Initial Transmit Delay | 3 |

**A2.2 Minimum Frame Length Determination.** The minimum frame length for 1BASE5 is determined using the values specified in 4.4.2.2 and 12.9, applied to the following (worst) case:

(1) DTE 1, connected to Hub 1 at a network extremity, transmits a message upward toward Hub 5.
(2) There is a special link in the path between Hub 1 and Hub 5.
(3) DTE 2, also connected to Hub 1, transmits, just missing deferring to the downward signal from DTE 1 that was wrapped around at Hub 5.
(4) DTE 3, also connected to Hub 1, receives the transmission from DTE 1.
(5) Hub 1 generates CP, which travels up and then back down the network to inform DTE 1 and DTE 2 that a collision has occurred on their messages.
(6) DTE 1 and DTE 2 continue to transmit until they have received CP, reacted to it, and completed their jams.
(7) DTE 3 continues to receive until the end of CP.

The minimum frame length must allow both of the following conditions to be met:

(1) DTE 1 is still sending when CP is received and recognized.
(2) DTE 3 can discard the message fragment it receives because it is too short.

| Event | Bits | Total |
|---|---|---|
| DTE 1 → DTE 2 | | |
| DTE Initial Transmit Delay | 3 | 3 |
| 8 · Medium Transit Delay | 32 | 35 |
| 2 · Special Link Transit Delay | 30 | 65 |
| 10 · Hub Startup Delay | 120 | 185 |
| DTE Deference Delay | 21 | 206 |
| DTE 2 → HUB 1 CP | | |
| Medium Transit Delay | 4 | 210 |
| Hub Collision Detect Delay | 21 | 231 |
| HUB 1 CP → HUB 5 CP | | |
| 3 · Medium Transit Delay | 12 | 243 |
| Special Link Transit Delay | 15 | 358 |
| 4 · max(Hub Startup Delay, Hub Active Collision Startup Delay, Hub Idle Collision Startup Delay) | 48 | 306 |
| HUB 5 CP → DTE 1 receives CP | | |
| 5 · Hub Active Collision Startup Delay | 60 | 366 |
| 4 · Medium Transit Delay | 16 | 382 |
| Special Link Transit Delay | 15 | 397 |
| DTE 1 receives CP → DTE 1 stops transmitting | | |
| DTE Collision Shutdown Delay | 58 | 455 |

| | | |
|---|---|---|
| COMPUTATION OF MINIMUM FRAME SIZE<br>original preamble + <sfd> | –64 | 391 =<br>data bits<br>transmitted |
| 5 · (Hub Collision Shutdown Delay<br>(upward)<br>-Hub Transit Delay) | 80 | 471 |
| 5 · (Hub Collision Shutdown Delay<br>(downward)<br>-Hub Transit Delay) | 0 | 471 |
| Tiny fraction of Hub Delay<br>Stretch/Shrink | 0 | 471 =<br>data bits received |

The minimum frame length must exceed both the maximum number of bits sent before recognizing CP (391 – jamsize = 359) and the maximum collision fragment size (471), as computed above. The 1BASE5 system value for minimum frame length has been set at 512 bits, which exceeds both of these values with a margin for error.

**A2.3 Jitter Budget.** The total edge jitter of the signals on each link must be limited to allow proper decoding at the receiver. The following budget has been used to allocate jitter to the indicated components that contribute to the total jitter on each link:

| Component | Jitter |
|---|---|
| Transmitter skew | ±10 ns |
| Cable intersymbol interference | 9 |
| Cable reflections | 8 |
| Reflections due to receiver termination mismatch | 5 |
| Total | ±32 ns |

The cable intersymbol interference and reflection allowances form the basis for the limit specified in 12.7.2.3; the reflection component is sufficient to allow a single 20 Ω impedance mismatch anywhere along a cable segment. The receiver-mismatch allowance is derived from the reflection attenuation specified in 12.5.3.2.4. The total forms the basis for the specification in 12.5.3.2.2.

The remainder of the jitter that can be tolerated by the Manchester decoder in a receiver is reserved to allow for distortion of the signal due to noise, receiver threshold offset, receiver skew, and receiver sampling timing error.

A simple clocked receiver/decoder with an 8 MHz sampling rate (the worst case allowed for in the design of this standard), can achieve proper decoding with up to ± 125 ns of jitter between two edges, which is equivalent to ±62.5 ns on each edge. Other receiver designs may tolerate more edge jitter. For example, a 6 MHz sampling rate would allow up to ±83.33 ns of jitter on each edge and a 16 MHz sampling rate allows up to ±93.75 ns of jitter.

It may be necessary to use a low-pass filter as part of the receiver to reduce the noise level seen by that receiver (see 12.7.4 for a description of the noise environment). A filter that reduces the noise may also have an effect on the amplitude and edge rate of the received signal. The filtered signal's edge rate near the zero-crossing is used in the critical translation from mV of noise and receiver offset into ns of jitter.

An example receiver design using an 8 MHz sampling rate and a 2 MHz Butterworth input filter might be based on the following jitter budget:

| Component | Jitter |
|---|---|
| Input jitter (from above) | ±32 ns |
| Noise and receiver threshold offset | 19.5 |
| Receiver skew (analog) | 4 |
| Receiver skew (digital) | 7 |
| Total | ±62.5 ns |

The two primary contributors to noise in a 1BASE5 cable are self-crosstalk and impulse noise (see 12.7.4). Because it is unlikely that both will be present at their 1% worst-case levels on any particular cable, the required bit error rate attributable to each source can be set at half of the one in $10^8$ error rate required by 12.5.3.2.6.

Crosstalk noise is specified to be no more than 105 mV (peak) through a 2 MHz filter (see 12.7.4.2). Because crosstalk is present for the entire transmission of a packet, some crosstalk will coincide with the most sensitive part of the received signal. Therefore, the receiver must operate without error in the presence of this 105 mV of noise.

Impulse noise has a peak amplitude of 170 mV for ≤0.005 counts/s through the 2 MHz filter (see 12.7.4.1). This threshold does not directly correlate to jitter, however, because the derivation of the 62.5 ns jitter tolerance for an 8 MHz clock assumed worst-case sampling error. Assuming a random phasing of the sampling clock to the received signals, it can be shown that the 170 mV of noise is equivalent to a level of 85 mV with a worst-phase clock.

Jitter due to noise should be computed using the larger of the above two levels. The 105 mV for crosstalk noise, therefore, should be added to 50 mV for receiver threshold offset and the result should be divided by the edge rate of the filtered signal near the zero-crossing (7.9 mV/ns for the 2 MHz filter), yielding the 19.5 ns indicated above.

## A3. Example Crosstalk Computation for Multiple Disturbers

A method for computing multiple-disturber, near end, crosstalk attenuation (MDNEXT) into each 1BASE5 pair is specified in 12.7.3.2. This appendix provides example computations of MDNEXT using that method when only the distribution of $X_{ij}$ is known.

The single-disturber probability distribution curve (labelled "1") shown in Fig A4 is based on actual measurement of 25-pair, 24-gauge, unshielded, twisted pair cable. The remaining probability distribution curves (labelled with the number of disturbing pairs) were computed using Monte Carlo simulation. To compute each sample $MDNEXT_j$ for N disturbers, N values of crosstalk attenuation ($X_i$) were chosen from the single-disturber distribution and N values of crosstalk phase ($\theta_i$) were chosen from a uniform distribution between 0 and $2\pi$ rad. These values were then used with the following equations to compute $MDNEXT_j$:

$$H_j = \sum_{1 \le i \le N} 10^{(-X_i/20)} \cos\theta_i$$

$$V_j = \sum_{1 \le i \le N} 10^{(-X_i/20)} \sin\theta_i$$

$$MDNEXT_j = 10\log_{10}(H_j^2 + V_j^2)$$

Iterating this process several hundred times, each time producing a single $MDNEXT_j$ sample, resulted in distributions for MDNEXT that are summarized in the following table and Fig A4:

| Disturbers | Iterations | MDNEXT: Mean | Std. Dev. | 99% |
|---|---|---|---|---|
| 1 | | 61.2 dB | 7.0 dB | 48.6 dB |
| 2 | 500 | 57.2 | 6.2 | 46.4 |
| 3 | 500 | 55.1 | 5.8 | 45.2 |
| 6 | 500 | 52.0 | 5.7 | 42.5 |
| 13 | 1000 | 48.5 | 5.4 | 39.1 |
| 18 | 500 | 47.1 | 5.3 | 37.8 |
| 24 | 500 | 45.9 | 5.9 | 36.2 |

Because two pairs are used for each 1BASE5 connection, the entries in this table for 18 and 24 disturbers are not applicable for normal installation of 25-pair cables. Furthermore, telephone cables with larger

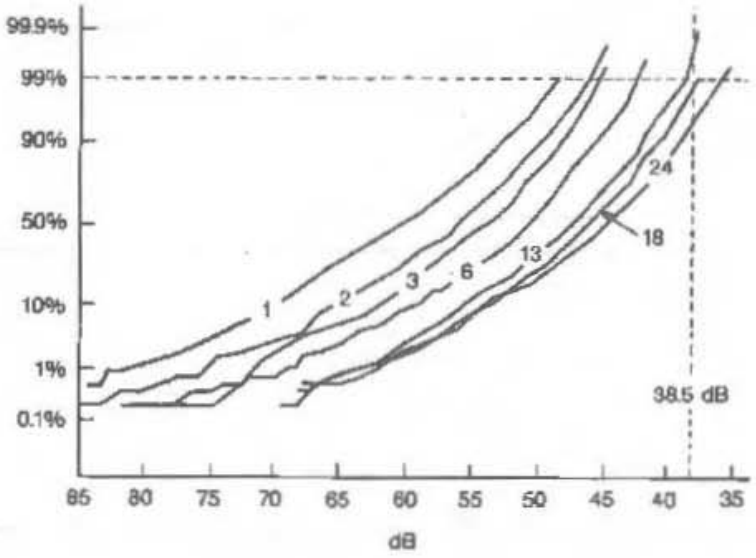


**Fig A4**
**MDNEXT Cumulative Probability Distribution**

numbers of pairs are often constructed using sub-bundles of 25 pairs each and so might yield similar results (for example, the curves for 13 or fewer disturbers would be the most applicable ones).

The calculation method of this Appendix, though not the numeric values, applies to 10BASE-T.

## A4. 10BASE-T

**A4.1 System Jitter Budget.** The jitter budget for 10BASE-T is apportioned as follows:

| Jitter budget | Maximum-Length Twisted-Pair Link | Short-Length Twisted-Pair Link |
|---|---|---|
| | (jitter expressed in ns) | |
| Encoder | 0.5 | 0.5 |
| AUI cable including SNR (DO pair) | 1.5 | 1.5 |
| MAU transmitter | 2.0 | 2.0 |
| Twisted-pair medium with equalization | 1.5 | 6.0 |
| Noise jitter on twisted-pair medium | 8.0 | 2.5 |
| MAU receiver | 1.5 | 1.5 |
| AUI cable including SNR (DI pair) | 1.5 | 1.5 |
| Total | 16.5 | 15.5 |

NOTE: Total transmit jitter for the combination of the MAU transmitter and link segment (14.3.1.2.3) is ±3.5 ns and ±8.0 ns for maximum- and short-length twisted-pair link segments, respectively. It is the sum of the entries for MAU transmitter and twisted-pair medium with equalization. The individual components cannot be easily observed on MAUs. Short-length segment is defined as a short, non-zero-length twisted-pair link. A short- rather than a zero-length segment is used in the calculation since a zero-length segment will have no significant noise and is a less severe case.

**A4.2 Filter Characteristics.** The implementation of the 3-pole, low-pass Butterworth filter should have the following characteristics:

| | |
|---|---|
| 3 dB cutoff frequency | 15 MHz |
| Insertion loss (5 MHz to 10 MHz) | ≤1.0 dB |
| 30 MHz attenuation | ≥17.5 dB |
| Input impedance (5 MHz to 10 MHz) | 100 Ω |
| Return loss with 100 Ω load (5 MHz to 10 MHz) | ≥20 dB |

This filter is only used for the tests described in 14.3.1.3.2, 14.4.4.1, and 14.4.4.2. A buffer may be needed to achieve the above return loss when using an LC implementation of this filter.

**A4.3 Notes for Conformance Testing.** The following notes are provided to assist in developing the conformance test.

**A4.3.1 Notes for 14.3.1.2.1 on Differential Output Voltage.** For testing harmonics measured on the TD circuit when the DO circuit is driven by an all-ones Manchester-encoded signal, it is acceptable to use a pattern of maximum length packets whose data field is all ones.

For testing of the maximum and minimum output signal to the template in Fig 14-9, the recommended measurement procedure is described as follows. An oscilloscope set for a zero voltage trigger with a positive slope is allowed to accumulate an eye pattern that must be within the template. Acquisition must be long enough to ensure that all data variations have been observed. When using packetized data, the TP_IDL and the first transmitted bit should be excluded from this measurement. Also, the interpacket interval may be adjusted so that transition-to-idle transient effects are excluded. When testing with the inverted template, the slope of the scope trigger should be negative.

**A4.3.2 Note for 14.3.1.2.2 on Transmitter Differential Output Impedance.** The return loss (RL) is defined as follows:

$$RL = 20\log_{10}\frac{|Z_{transmitter} + Z_{cable}|}{|Z_{transmitter} - Z_{cable}|}$$

and also

$$RL = 20\log_{10}\frac{|V_i|}{|V_r|}$$

where

$Z_{transmitter}$ is the impedance of the transmitter
$Z_{cable}$ is the impedance of the cable
$V_i$ is the differential voltage incident upon the transmitter
$V_r$ is the differential voltage reflected from the transmitter

(1) A transmitter with a purely resistive source impedance of 96 Ω ± 20% will satisfy this requirement.
(2) The requirement of 14.3.1.2.2 is equivalent to the following two constraints:
    (a) The return loss when measured with an 85 Ω resistive source is at least 15 dB in the frequency range of 5 MHz to 10 MHz.
    (b) The return loss when measured with a 111 Ω resistive source is at least 15 dB in the frequency range of 5 MHz to 10 MHz.

**A4.3.3 Note for 14.3.1.2.3 on Output Timing Jitter.** Adherence to the template of 14.3.1.2.1 with a jitterless source driving DO and the zero crossings constrained to 46.5 ns to 53.5 ns and 96.5 ns to 103.5 ns is sufficient to demonstrate compliance with the 3.5 ns jitter requirement. When measuring an integrated MAU, the zero crossing time interval should be constrained to 44.5 ns to 55.5 ns and 94.5 ns to 105.5 ns due to the additional allocation for encoder and AUI jitter. This test is simpler to perform than the test which follows, but failure of this test does not demonstrate noncompliance.

When triggering on one edge of the transmitted signal and observing another edge, the observed jitter measures the difference between the jitter of the triggering edge and the observed edge. When the two

edges are separated such that the jitter of the edges is independent and clock drift is insignificant, the observed jitter is twice that of a single edge.

Therefore, a test that demonstrates compliance or noncompliance is as follows: Observe the zero crossings 8 BT and 8.5 BT from the triggering zero crossing while transmitting a pseudo-random data sequence of at least 511 bits. An external MAU with a jitterless source driving DO is compliant when all zero crossings fall within the time intervals 8.0 BT ± 7 ns and 8.5 BT ± 7 ns. An integrated MAU is compliant when all zero crossings fall within the time intervals 8.0 BT ± 11 ns and 8.5 BT ± 11 ns.

When using packetized data, the TP_IDL and the first transmitted bit should be excluded from these measurements.

**A4.3.4 General Note on Common-Mode Tests.** When performing tests specified as balanced or common-mode, the balance of the test equipment (such as matching resistors) must exceed that required by the test.

**A4.3.5 Note for 14.3.1.3.4 on Receiver Differential Input Impedance.** The return loss (RL) is defined as follows:

$$RL = 20\log_{10}\frac{|Z_{receiver} + Z_{cable}|}{|Z_{receiver} - Z_{cable}|}$$

and also

$$RL = 20\log_{10}\frac{|V_i|}{|V_r|}$$

where

$Z_{receiver}$ is the impedance of the receiver

$Z_{cable}$ is the impedance of the cable

$V_i$ is the differential voltage incident upon the receiver

$V_r$ is the differential voltage reflected from the receiver

(1) A receiver with a resistive input impedance of 96 Ω ± 20% will satisfy this requirement.

(2) The requirement of 14.3.1.3.4 is equivalent to the following two constraints:

(a) The return loss when measured with an 85 Ω resistive source is at least 15 dB in the frequency range of 5 MHz to 10 MHz.

(b) The return loss when measured with a 111 Ω resistive source is at least 15 dB in the frequency range of 5 MHz to 10 MHz.

**A4.3.6 Note for 14.3.1.3.3 on Receiver Idle Input Behavior.** For conformance testing of receivers, the start of idle shall conform to the template shown in Fig 14-10. Additionally, the magnitude of the voltage-time integral of the undershoot (measured from the negative zero crossing that ends the positive idle pulse to the time when the differential signal settles to 0.0 mV ± 50 mV) shall be no greater than 1.2 times the voltage-time integral of the positive idle pulse (measured from the last positive zero crossing to the negative zero crossing).

**A4.3.7 Note for 14.3.1.3.5 on Receiver Common-Mode Rejection.** For a stand-alone MAU, the receiver common-mode test may be performed with a jitterless $E_s$, so that the DI circuit should have no more than 4.0 ns of edge jitter.

For an integrated MAU, the common-mode test is performed with an $E_s$ that has zero crossing jitter up to 11 ns from the ideal.

# Appendix B
# State Diagram, MAC Sublayer

## B1. Introduction

This Appendix contains a generalized state machine description of the CSMA/CD procedures for MAC. It is supportive of the formal procedures defined in 4.2. It is assumed that the reader is familiar with those formal descriptions.

The state diagrams of this Appendix are descriptive rather than definitional; the formal statements of 4.2 provide the definitive specifications.

## B2. CSMA/CD Media Access Control State Machine Overview

The CSMA/CD MAC consists of two components: the transmit component and the receive component. These components operate concurrently and independently.

**B2.1 Transmit Component Overview.** The transmit component is responsible for handling all events that affect the transmission of a frame onto the medium (see Fig B1 and Table B1).

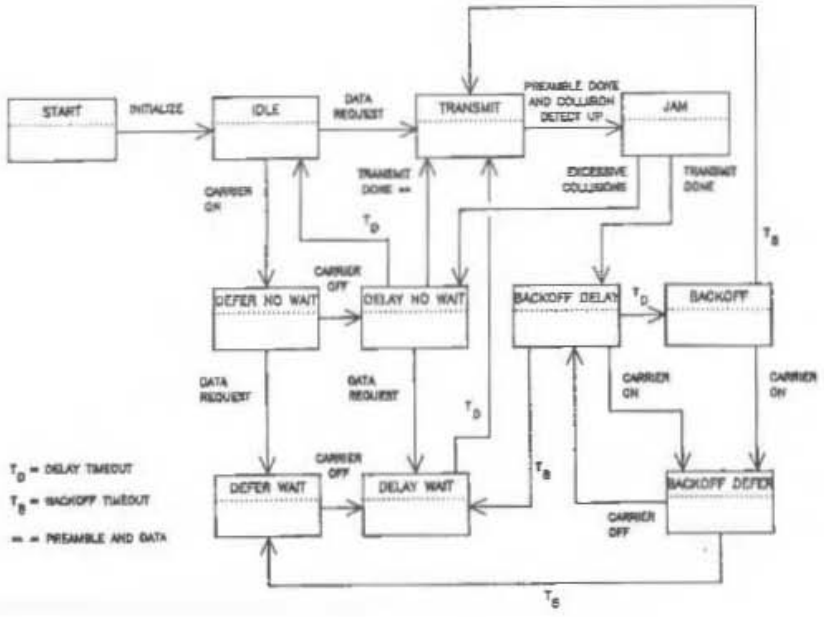


**Fig B1**
**Transmit Component State Diagram**

### B2.2 Transmit Component Event Descriptions

**Initialize.** This event is generated by management to start up the component.

**Data Request.** This event is generated by the LLC sublayer. It indicates there is a PDU to be transmitted.

**Table B1**
**Transmit Component State Transition**

| Current State | Event | Action | Next State |
|---|---|---|---|
| 0. Start | Initialize | - Perform Initialization | Idle |
| 1. Idle | Data Request | - Construct Frame<br>- Start Frame Transmission<br>- No Action | Transmit |
| | Carrier On | | Defer No Wait |
| 2. Transmit | Preamble Done AND Collision Detect Up | - Start Jam Transmission<br>- Increment Attempt Count | Jam |
| | Transmit Done | - Start Delay Timer<br>- Reset Attempt Count<br>- Indicate successful Transmission | Delay No Wait |
| 3. Jam | Transmit Done | - Start Delay Timer<br>- Start Backoff Timer | Backoff Delay |
| | Excessive Collisions | - Start Delay Timer<br>- Indicate Transmit Excessive Collisions | Delay No Wait |
| 4. Backoff | Carrier On | - No Action | Backoff Defer |
| | Backoff Timeout | - Start Frame Transmission | Transmit |
| 5. Backoff Defer | Carrier Off | - Start Delay Timer | Backoff Delay |
| | Backoff Timeout | - No Action | Defer Wait |
| 6. Backoff Delay | Carrier On | - Stop Delay Timer | Backoff Defer |
| | Delay Timeout | - No Action | Backoff |
| | Backoff Timeout | - No Action | Delay Wait |
| 7. Defer No Wait | Data Request | - Construct Frame | Defer Wait |
| | Carrier Off | - Start Delay Timer | Delay No Wait |
| 8. Delay No Wait | Data Request | - Construct Frame | Delay Wait |
| | Delay Timeout | - No Action | Idle |
| 9. Defer Wait | Carrier Off | - Start Delay Timer | Delay Wait |
| 10. Delay Wait | Delay Timeout | - Start Frame Transmission | Transmit |

**Carrier On.** This event indicates that the physical layer has detected a change in carrier sense from no carrier to carrier.

**Carrier Off.** This event indicates that the physical layer has detected a change in the state of carrier sense from carrier to no carrier.

**Preamble Done AND Collision Detect Up.** This event indicates that the physical layer has detected a collision with the frame being transmitted and the transmission of the preamble sequence is completed.

**Delay Timeout.** This event indicates that the interframe time delay has completed.

**Backoff Timeout.** This event indicates that the time period for backing off has completed.

**Transmit Done.** The bit transmitter has transmitted all of the bits in the transmit buffer specified by the transmit buffersize (which includes preamble and data).

**Excessive Collisions.** The bit transmitter has transmitted all of the bits in the transmit buffer specified by the transmit buffersize, and the attempt count is equal to the maximum transmit attempt count allowed.

### B2.3 Transmit Component Action Descriptions

**Construct Frame.** This action encapsulates the data field with the Preamble, SFD, DA, SA, Length, PAD, and FCS fields.

**Start Frame Transmission.** This action initiates bit transmission of the frame.

**Start Jam Transmission.** This action causes the bit transmitter to transmit the bits of the jam pattern.

**Indicate Successful Transmission.** This action reports that the transmission was successful.

**Indicate Transmit Failure.** This action reports the failure of transmission and the reason.

**Increment Attempt Count.** This action increments the counter used to record the number of attempts made to transmit the same frame.

**Reset Attempt Count.** This action initializes the attempt count to 0.

**Start Backoff Timer.** This action computes the random backoff delay time and sets the backoff timer to that time.

**Start Delay Timer.** This action sets the delay timer to the interframe gap time.

**Stop Delay Timer.** This action turns the delay timer off.

**Perform Initialization.** This action turns all timers off and ensures that carrier is considered off and collision detect down. All counters are reset. Any implementation specific variables are initialized.

### B2.4 Transmit Component State Descriptions

**Start.** The transmit component has not been initialized by management.

**Idle.** The transmit component is not transmitting any data nor is it in a state where it is prevented from transmitting date.

**Transmit.** The transmit component is actively transmitting bits onto the medium.

**Jam.** The transmit component is actively transmitting jam bits onto the medium.

**Backoff.** The transmit component is waiting for its random backoff delay to expire before attempting to retransmit a frame.

**Backoff Defer.** The transmit component is waiting for both the medium to become available and for its backoff time delay to expire before attempting to retransmit a frame.

**Backoff Delay.** The transmit component is waiting for the interframe gap and the backoff delays to expire before attempting to retransmit a frame.

**Defer No Wait.** The transmit component has no frame to transmit and it cannot transmit one if it gets one because the medium is busy.

**Delay No Wait.** The transmit component has no frame to transmit and it could not if it had one because it is waiting for the interframe gap time to expire.

**Defer Wait.** The transit component is waiting for the medium to become free before attempting to transmit or retransmit the frame.

**Delay Wait.** The transmit component is waiting for the interframe gap time to expire before attempting to transmit or retransmit the frame.

## B3. Receive Component Overview

The receive component is responsible for handling all events that affect the reception of a frame from the media. (See Fig B2 and Table B2.)

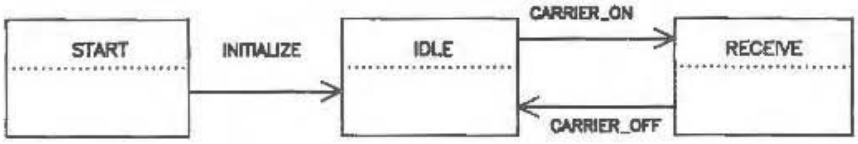


**Fig B2**
**Receive Component State Diagram**

**Table B2**
**Receive Component State Transition**

| Current State | Event | Action | Next State |
|---|---|---|---|
| 0. Start | Initialize | - Perform Initialization | Idle |
| 1. Idle | Carrier On | - Start Receiving | Receive |
| 2. Receive | Carrier Off | - Process Frame Received | Idle |

### B3.1 Receive Component Event Descriptions

**Initialize.** This event is generated by management to start up the component.

**Carrier On.** This event indicates that the physical layer has detected a change in carrier sense from no carrier to carrier.

**Carrier Off.** This event indicates that the physical layer has detected a change in the state of carrier sense from carrier to no carrier.

### B3.2 Receive Component Action Descriptions

**Perform Initialization.** This action turns all timers off and ensures that carrier is considered off and collision detect down. All counters are reset. Any implementation specific variables are initialized.

**Start Receiving.** This action begins the processes of accepting bits and appending them to the buffer used to contain the frame.

**Process Frame Received.** If the frame is not addressed to this station, then ignore the frame. Otherwise, check the frame for errors. If there are no errors, pass frame up to the LLC sublayer indicating no error. Otherwise, pass the frame to the LLC sublayer indicating the error.

### B3.3 Receive Component State Descriptions

**Start.** The receive component has not been initialized by management.

**Idle.** The receive component is not actively receiving bits of data from the line.

**Receive.** The receive component is receiving bits of data from the line.

# Appendix C
# Application Context, Selected Medium Specifications

## C1. Introduction

This Appendix provides general guidance, to both the design engineer and the eventual user of specific product implementations, on what particular sections of the ISO 8802-3 CSMA/CD Local Area Network Standard might be considered useful for different application environments. It is to be emphasized that the material in this Appendix is very general, as the standard specifications are intended to be relatively application-independent. Nevertheless, certain specifications may apply more to one application environment than another. What follows are brief descriptions of application environments and lists of those generic parameters of the physical layer specifications thought to be useful in relating a general set of user requirements to a specific standard specification and its related medium. *Once a basic relationship is identified, the reader is directed to a specific section of the standard for detailed design specifications.*

## C2. Type 10BASE5 Applications

One of the major arenas for local area networks is the interconnection of work stations throughout a large department or single building. The ability to handle all kinds of message traffic at relatively high data rates among a large set of work stations are typical characteristics of these environments. Usually the basic interconnection trunk cable is installed and left in place permanently or for extended periods while work station placement may shift from time to time. The Type 10BASE5 specification provides the primary baseband backbone for intraplant CSMA/CD interconnections. Sections 7 and 8 of the standard provide detailed specifications for the physical layers associated with Type 10BASE5 environments. The generic physical layer parameters are as follows:

| | |
|---|---|
| Maximum unrepeatered cable segment | 500 m |
| Maximum number of MAUs per segment | 100 |
| Connector type | Type N or coaxial "tap" |
| Breakdown voltage, MAU function | 250 V ac rms |
| MTBF | 1 million hours |
| Total Segment Resistance | 5 Ω |
| MAU separation | 2.5 m |
| Connection shunt capacitance | 4 pF |
| AUI functionality | DO, DI, CI, (CO optional) |

## C3. Type 10BASE2 Applications

Another major arena for local area networks is the interconnection of work stations throughout a small department or work area. The ability to handle all kinds of message traffic at relatively high data rates among a selected set of locally clustered work stations are the typical characteristics of these environments. In addition, the basic interconnection trunk cable is likely to be moved frequently by the local users of the equipment to suit evolving needs. The Type 10BASE2 specification provides an interconnection schema that complements the Type 10BASE5 backbone in a hierarchical manner for intradepartment or work area CSMA/CD interconnections. Sections 7 and 10 of the standard provide detailed specifications for the physical layers associated with Type 10BASE2 environments. The generic physical layer parameters are as follows:

| | |
|---|---|
| Maximum unrepeatered cable segment | 185 m |
| Maximum number of MAUs per segment | 30 |
| Connector type | Type BNC "T" |
| Breakdown voltage, MAU function | 500 V ac rms |
| MTBF | 100 000 hours |
| Total Segment Resistance | 10 Ω |
| MAU separation | 0.5 m |
| Connection shunt capacitance | 8 pF |
| AUI functionality | DO, DI, CI |

## C4. Type FOIRL Applications

Applications information for use of 50/125 μm optical fiber is under consideration.

# Appendix D
# Receiver Wavelength Design Considerations

Reference 9.9.4.1.1, wavelength.

The center wavelength of the optical source emission is currently specified to be between 790 nm and 860 nm. Although these limits are acceptable, it is currently recognized, through the examination of manufacturers' current data, that greater choices of emitters can be obtained by extending the allowable wavelength to 910 nm.

An upper limit of 910 nm allows the selection of devices nominally centered at a lower wavelength, for example, 880 nm. This allows a tolerance for manufacturing variations, for example, ±20 nm, and a tolerance for an operating temperature range (typically, 0.3 nm/°C).

It is anticipated that future fiber optic applications including Local Area Networks will use the 910 nm upper limit for first window systems. It is therefore recommended that implementors specify receiver sensitivity over a center wavelength range from 790 nm to 910 nm.

UDC 681.3:621.39

**Descriptors**: data processing, information interchange, network interconnection, local area networks, models, mode of data transmission.

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