MII	media independent interface
MP	message page
NEXT	near-end crosstalk
NLP	normal link pulse
NPA	next page algorithm
NRZI	non return to zero and invert on ones
PCS	physical coding sublayer
PDV	path delay value
PHY	Physical Layer entity sublayer
PICS	protocol implementation conformance statement
PLS	physical signaling sublayer
PMA	physical medium attachment
PMD	physical medium dependent
PMI	physical medium independent
PVV	path variability value
RS	reconciliation sublayer
SSD	start-of-stream delimiter
SDV	segment delay value
SFD	start-of-frame delimiter
SR	symbol rate
ST	symbol time
STA	station management entity
STP	shielded twisted pair (copper)
SVV	segment variability value
UCT	unconditional transition
UP	unformatted page
UTP	unshielded twisted pair

21.3 References

References are shown beginning on pages 2 and 23 of this document (as updates to 1.3 and annex A).

21.4 Definitions

Definitions are shown beginning on page 5 of this document (as an update to 1.4).

21.5 State diagrams

State machine diagrams take precedence over text.

The conventions of 1.2 are adopted, with the following extensions.

21.5.1 Actions inside state blocks

The actions inside a state block execute instantaneously. Actions inside state blocks are atomic (i.e., uninter-ruptible).

After performing all the actions listed in a state block one time, the state block then continuously evaluates its exit conditions until one is satisfied, at which point control passes through a transition arrow to the next block. While the state awaits fulfillment of one of its exit conditions, the actions inside do not implicitly repeat.

The characters • and [bracket] are *not* used to denote any special meaning.

Valid state actions may include .indicate and request messages.

No actions are taken outside of any state block.

21.5.2 State diagram variables

Once set, variables retain their values as long as succeeding blocks contain no references to them.

Setting the parameter of a formal interface message assures that, on the next transmission of that message, the last parameter value set will be transmitted.

Testing the parameter of a formal interface messages tests the value of that message parameter that was received on the last transmission of said message. Message parameters may be assigned default values that persist until the first reception of the relevant message.

21.5.3 State transitions

The following terms are valid transition qualifiers:

a) Boolean expressions
b) An event such as the expiration of a timer: timer_done
c) An event such as the reception of a message: PMA_UNITDATA.indicate
d) An unconditional transition: UCT
e) A branch taken when other exit conditions are not satisfied: ELSE

Any open arrow (an arrow with no source block) represents a global transition. Global transitions are evaluated continuously whenever any state is evaluating its exit conditions. When a global transition becomes true, it supersedes all other transitions, including UCT, returning control to the block pointed to by the open arrow.

21.5.4 Operators

The state machine operators are shown in table 21-1.

Table 21-1—State machine operators

Character	Meaning
∗	Boolean AND
+	Boolean OR
∧	Boolean XOR
!	Boolean NOT
<	Less than
≤	Less than or equal to
=	Equals (a test of equality)
≠	Not equals
≥	Greater than or equal to
>	Greater than
( )	Indicates precedence
⇐	Assignment operator
∈	Indicates membership
∉	Indicates nonmembership
ELSE	No other state condition is satisfied

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21.6 Protocol Implementation Conformance Statement (PICS) proforma

21.6.1 Introduction

The supplier of a protocol implementation that is claimed to conform to any part of the IEEE 802.3u 100BASE-T clauses 21 through 30 shall complete a Protocol Implementation Conformance Statement (PICS) proforma.

A completed PICS proforma is the PICS for the implementation in question. The PICS is a statement of which capabilities and options of the protocol have been implemented. A PICS is included at the end of each clause as appropriate. The PICS can be used for a variety of purposes by various parties, including the following:

a) As a checklist by the protocol implementor, to reduce the risk of failure to conform to the standard through oversight;

b) As a detailed indication of the capabilities of the implementation, stated relative to the common basis for understanding provided by the standard PICS proforma, by the supplier and acquirer, or potential acquirer, of the implementation;

c) As a basis for initially checking the possibility of interworking with another implementation by the user, or potential user, of the implementation (note that, while interworking can never be guaranteed, failure to interwork can often be predicted from incompatible PICS);

d) As the basis for selecting appropriate tests against which to assess the claim for conformance of the implementation, by a protocol tester.

21.6.2 Abbreviations and special symbols

The following symbols are used in the PICS proforma:

M	mandatory field/function
O	optional field/function
O.\<n\>	optional field/function, but at least one of the group of options labeled by the same numeral \<n\> is required
O/\<n\>	optional field/function, but one and only one of the group of options labeled by the same numeral \<n\> is required
X	prohibited field/function
\<item\>:	simple-predicate condition, dependent on the support marked for \<item\>
\<item1\>*\<item2\>:	AND-predicate condition, the requirement must be met if both optional items are implemented

21.6.3 Instructions for completing the PICS proforma

The first part of the PICS proforma, Implementation Identification and Protocol Summary, is to be completed as indicated with the information necessary to identify fully both the supplier and the implementation.

The main part of the PICS proforma is a fixed-format questionnaire divided into subclauses, each containing a group of items. Answers to the questionnaire items are to be provided in the right-most column, either by simply marking an answer to indicate a restricted choice (usually Yes, No, or Not Applicable), or by entering a value or a set or range of values. (Note that there are some items where two or more choices from a set of possible answers can apply; all relevant choices are to be marked.)

Each item is identified by an item reference in the first column; the second column contains the question to be answered; the third column contains the reference or references to the material that specifies the item in the main body of the standard; the sixth column contains values and/or comments pertaining to the question

to be answered. The remaining columns record the status of the items—whether the support is mandatory, optional or conditional—and provide the space for the answers.

The supplier may also provide, or be required to provide, further information, categorized as either Additional Information or Exception Information. When present, each kind of further information is to be provided in a further subclause of items labeled A<i> or X<i>, respectively, for cross-referencing purposes, where <i> is any unambiguous identification for the item (e.g., simply a numeral); there are no other restrictions on its format or presentation.

A completed PICS proforma, including any Additional Information and Exception Information, is the Protocol Implementation Conformance Statement for the implementation in question.

Note that where an implementation is capable of being configured in more than one way, according to the items listed under Major Capabilities/Options, a single PICS may be able to describe all such configurations. However, the supplier has the choice of providing more than one PICS, each covering some subset of the implementation's configuration capabilities, if that would make presentation of the information easier and clearer.

21.6.4 Additional information

Items of Additional Information allow a supplier to provide further information intended to assist the interpretation of the PICS. It is not intended or expected that a large quantity will be supplied, and the PICS can be considered complete without any such information. Examples might be an outline of the ways in which a (single) implementation can be set up to operate in a variety of environments and configurations; or a brief rationale, based perhaps upon specific application needs, for the exclusion of features that, although optional, are nonetheless commonly present in implementations.

References to items of Additional Information may be entered next to any answer in the questionnaire, and may be included in items of Exception Information.

21.6.5 Exceptional information

It may occasionally happen that a supplier will wish to answer an item with mandatory or prohibited status (after any conditions have been applied) in a way that conflicts with the indicated requirement. No preprinted answer will be found in the Support column for this; instead, the supplier is required to write into the Support column an X<i> reference to an item of Exception Information, and to provide the appropriate rationale in the Exception item itself.

An implementation for which an Exception item is required in this way does not conform to this standard.

Note that a possible reason for the situation described above is that a defect in the standard has been reported, a correction for which is expected to change the requirement not met by the implementation.

21.6.6 Conditional items

The PICS proforma contains a number of conditional items. These are items for which both the applicability of the item itself, and its status if it does apply—mandatory, optional, or prohibited—are dependent upon whether or not certain other items are supported.

Individual conditional items are indicated by a conditional symbol of the form "<item>:<s>" in the Status column, where "<item>" is an item reference that appears in the first column of the table for some other item, and "<s>" is a status symbol, M (Mandatory), O (Optional), or X (Not Applicable).

If the item referred to by the conditional symbol is marked as supported, then 1) the conditional item is applicable, 2) its status is given by "<s>", and 3) the support column is to be completed in the usual way. Otherwise, the conditional item is not relevant and the Not Applicable (N/A) answer is to be marked.

Each item whose reference is used in a conditional symbol is indicated by an asterisk in the Item column.

21.7 Relation of 100BASE-T to other standards

Suitable entries for table G1 of ISO/IEC 11801: 1995, annex G, would be as follows:

a) Within the section Balanced Cable Link Class C (specified up to 16 MHz):
CSMA/CD 100BASE-T4   ISO/IEC 8802-3/DAD   1995   4
b) Within the section Optical Link:
CSMA/CD 100BASE-FX   ISO/IEC 8802-3/DAD   1995   2
c) Within the section Balanced Cable Link Class D (Defined up to 100 MHz):
CSMA/CD 100BASE-TX   ISO/IEC 8802-3/DAD   1995   2

NOTE—To support 100BASE-T4 applications, class C links shall have a NEXT value of at least 3 dB in excess of the values specified in 6.2.4.

Suitable entries for table G2 of ISO/IEC 11801: 1995, annex G, would be as follows:

	Balanced cabling per clauses 5, 7, and 8							Performance based cabling per clause 6											
								Class A			Class B			Class C			Class D		
	Cat 3 100 Ω	Cat 4 100 Ω	Cat 5 100 Ω	Cat 3 120 Ω	Cat 4 120 Ω	Cat 5 120 Ω	150 Ω	100 Ω	120 Ω	150 Ω	100 Ω	120 Ω	150 Ω	100 Ω	120 Ω	150 Ω	100 Ω	120 Ω	150 Ω
8802-3: 100BASE-T4	I*	I*	I*		I	I								I			I*	I	
8802-3: 100BASE-TX			I*				I*										I*		I*

* 8802-3 imposes additional requirements on propagation delay.

A suitable entry for table G3 of ISO/IEC 11801: 1995, annex G, would be as follows:

	Fibre per 5, 7, and 8			Optical link per clause 8								
				Horizontal			Building backbone			Campus backbone		
	62.5/125 μm MMF	50/125 μm MMF	10/125 μm MMF	62.5/125 μm MMF	50/125 μm MMF	10/125 μm MMF	62.5/125 μm MMF	50/125 μm MMF	10/125 μm MMF	62.5/125 μm MMF	50/125 μm MMF	10/125 μm MMF
8802-3: 100BASE-FX	N	I		N	I		N	I		N	I	

21.8 MAC delay constraints (exposed MII)

100BASE-T makes the following assumptions about MAC performance. These assumptions apply to any MAC with an exposed MII used with a 100BASE-T PHY.
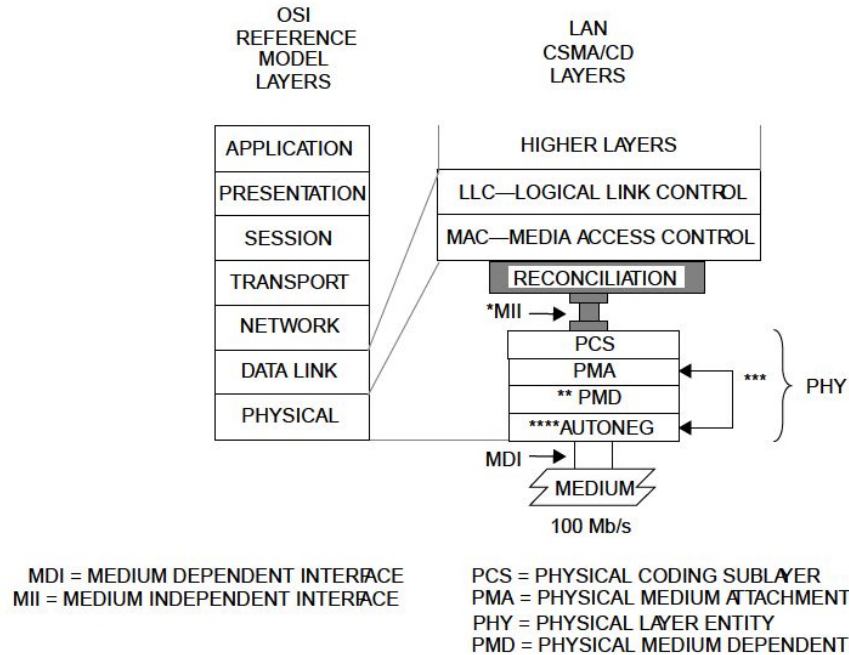
Table 21-2—MAC delay assumptions (exposed MII)

Sublayer measurement points	Event	Min (bits)	Max (bits)	Input timing reference	Output timing reference
MAC ⇔ MII	MAC transmit start to TX_EN sampled		4		TX_CLK rising
	CRS assert to MAC detect	0	8		
	CRS de-assert to MAC detect	0	8		
	CRS assert to TX_EN sampled (worst case nondeferred transmit)		16		TX_CLK rising
	COL assert to MAC detect	0	8		
	COL de-assert to MAC detect	0	8		
	COL assert to TXD = Jam sampled (worst-case collision response)		16		TX_CLK rising; first nibble of jam

22. Reconciliation Sublayer (RS) and Media Independent Interface (MII)

22.1 Overview

This clause defines the logical, electrical, and mechanical characteristics for the Reconciliation Sublayer (RS) and Media Independent Interface (MII) between CSMA/CD media access controllers and various PHYs. Figure 22-1 shows the relationship of the Reconciliation sublayer and MII to the ISO (IEEE) OSI reference model.

MDI = MEDIUM DEPENDENT INTERFACE
MII = MEDIUM INDEPENDENT INTERFACE

PCS = PHYSICAL CODING SUBLAYER
PMA = PHYSICAL MEDIUM ATTACHMENT
PHY = PHYSICAL LAYER ENTITY
PMD = PHYSICAL MEDIUM DEPENDENT

* MII is optional for 10 Mb/s DTEs and for 100 Mb/s systems and is not specified for 1 Mb/s systems.
** PMD is specified for 100BASE-TX and -FX only; 100BASE-T4 does not use this layer.
*** AUTONEG communicates with the PMA sublayer through the PMA service interface messages PMA_LINK.request and PMA_LINK.indicate
**** AUTONEG is optional.

Figure 22-1—MII location in the protocol stack

The purpose of this interface is to provide a simple, inexpensive, and easy-to-implement interconnection between Media Access Control (MAC) sublayer and PHYs, and between PHYs and Station Management (STA) entities.

This interface has the following characteristics:

a)   It is capable of supporting both 10 Mb/s and 100 Mb/s data rates.
b)   Data and delimiters are synchronous to clock references.
c)   It provides independent four bit wide transmit and receive data paths.
d)   It uses TTL signal levels, compatible with common digital CMOS ASIC processes.
e)   It provides a simple management interface.
f)   It is capable of driving a limited length of shielded cable.

22.1.1 Summary of major concepts

a) Each direction of data transfer is serviced with seven (making a total of 14) signals: Data (a four-bit bundle), Delimiter, Error, and Clock.

b) Two media status signals are provided. One indicates the presence of carrier, and the other indicates the occurrence of a collision.

c) A management interface comprised of two signals provides access to management parameters and services.

d) The Reconciliation sublayer maps the signal set provided at the MII to the PLS service definition specified in clause 6.

22.1.2 Application

This clause applies to the interface between MAC sublayer and PHYs, and between PHYs and Station Management entities. The implementation of the interface may assume any of the following three forms:

a) A chip-to-chip (integrated circuit to integrated circuit) interface implemented with traces on a printed circuit board.

b) A motherboard to daughterboard interface between two or more printed circuit boards.

c) An interface between two printed circuit assemblies that are attached with a length of cable and an appropriate connector.

Figure 22-2 provides an example of the third application environment listed above. All MII conformance tests are performed at the mating surfaces of the MII connector, identified by the line A-A.
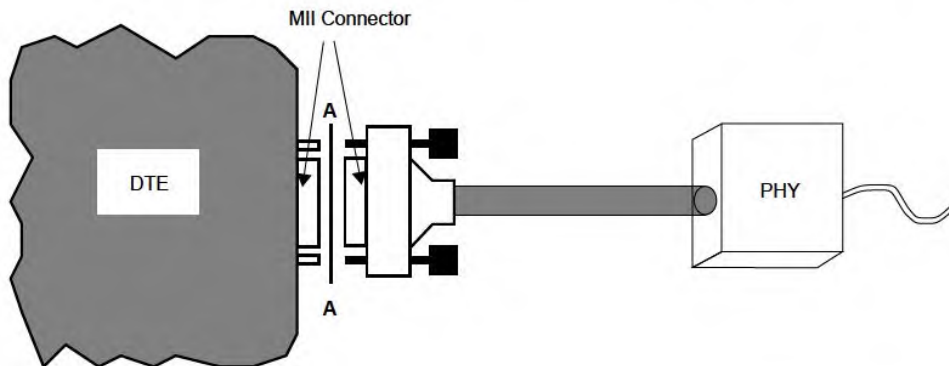

Figure 22-2—Example application showing location of conformance test

This interface is used to provide media independence for various forms of unshielded twisted-pair wiring, shielded twisted-pair wiring, fiber optic cabling, and potentially other media, so that identical media access controllers may be used with any of these media.

To allow for the possibility that multiple PHYs may be controlled by a single Station Management entity, the MII management interface has provisions to accommodate up to 32 PHYs, with the restriction that a maximum of one PHY may be attached to a management interface via the mechanical interface defined in 22.6.

22.1.3 Rates of operation

The MII can support two specific data rates, 10 Mb/s and 100 Mb/s. The functionality is identical at both data rates, as are the signal timing relationships. The only difference between 10 Mb/s and 100 Mb/s operation is the nominal clock frequency.

PHYs that provide an MII are not required to support both data rates, and may support either one or both. PHYs must report the rates they are capable of operating at via the management interface, as described in 22.2.4.

22.1.4 Allocation of functions

The allocation of functions at the MII is such that it readily lends itself to implementation in both PHYs and MAC sublayer entities. The division of functions balances the need for media independence with the need for a simple and cost-effective interface.

While the Attachment Unit Interface (AUI) was defined to exist between the Physical Signaling (PLS) and Physical Media Attachment (PMA) sublayers for 10 Mb/s DTEs, the MII maximizes media independence by cleanly separating the Data Link and Physical Layers of the ISO (IEEE) seven-layer reference model. This allocation also recognizes that implementations can benefit from a close coupling of the PLS or PCS sublayer and the PMA sublayer.

22.2 Functional specifications

The MII is designed to make the differences among the various media absolutely transparent to the MAC sublayer. The selection of logical control signals and the functional procedures are all designed to this end. Additionally, the MII is designed to be easily implemented at minimal cost using conventional design techniques and manufacturing processes.

22.2.1 Mapping of MII signals to PLS service primitives and Station Management

The Reconciliation sublayer maps the signals provided at the MII to the PLS service primitives defined in clause 6. The PLS service primitives provided by the Reconciliation sublayer behave in exactly the same manner as defined in clause 6. The MII signals are defined in detail in 22.2.2 below.

Figure 22-3 depicts a schematic view of the Reconciliation sublayer inputs and outputs, and demonstrates that the MII management interface is controlled by the Station Management entity (STA).

22.2.1.1 Mapping of PLS_DATA.request

22.2.1.1.1 Function

Map the primitive PLS_DATA request to the MII signals TXD<3:0>, TX_EN and TX_CLK.

22.2.1.1.2 Semantics of the service primitive

PLS_DATA request (OUTPUT_UNIT)

The OUTPUT_UNIT parameter can take one of three values: ONE, ZERO, or DATA_COMPLETE. It represents a single data bit. The values ONE and ZERO are conveyed by the signals TXD<3>, TXD<2>, TXD<1> and TXD<0>, each of which conveys one bit of data while TX_EN is asserted. The value DATA_COMPLETE is conveyed by the de-assertion of TX_EN. Synchronization between the Reconciliation sublayer and the PHY is achieved by way of the TX_CLK signal.
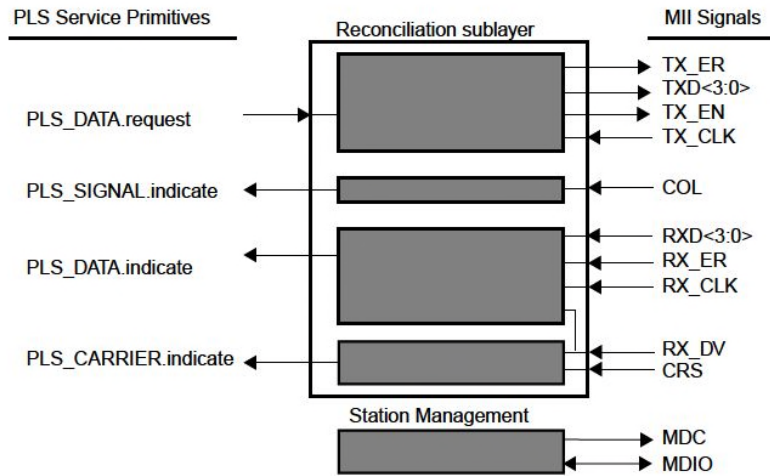
**Figure 22-3—Reconciliation Sublayer (RS) inputs and outputs
and STA connections to MII**

22.2.1.1.3 When generated

The TX_CLK signal is generated by the PHY. The TXD<3:0> and TX_EN signals are generated by the Reconciliation sublayer after every group of four PLS_DATA request transactions from the MAC sublayer to request the transmission of four data bits on the physical medium or to stop transmission.

22.2.1.2 Mapping of PLS_DATA.indicate

22.2.1.2.1 Function

Map the primitive PLS_DATA.indicate to the MII signals RXD<3:0>, RX_DV, RX_ER, and RX_CLK.

22.2.1.2.2 Semantics of the service primitive

PLS_DATA.indicate (INPUT_UNIT)

The INPUT_UNIT parameter can take one of two values: ONE or ZERO. It represents a single data bit. The values ONE and ZERO are derived from the signals RXD<3>, RXD<2>, RXD<1>, and RXD<0>, each of which represents one bit of data while RX_DV is asserted.

The value of the data transferred to the MAC is controlled by the RX_ER signal, see 22.2.1.5, Response to RX_ER indication from MII.

Synchronization between the PHY and the Reconciliation sublayer is achieved by way of the RX_CLK signal.

22.2.1.2.3 When generated

This primitive is generated to all MAC sublayer entities in the network after a PLS_DATA.request is issued. Each nibble of data transferred on RXD<3:0> will result in the generation of four PLS_DATA.indicate transactions.

22.2.1.3 Mapping of PLS_CARRIER.indicate

22.2.1.3.1 Function

Map the primitive PLS_CARRIER.indicate to the MII signals CRS and RX_DV.

22.2.1.3.2 Semantics of the service primitive

PLS_CARRIER.indicate (CARRIER_STATUS)

The CARRIER_STATUS parameter can take one of two values: CARRIER_ON or CARRIER_OFF. The values CARRIER_ON and CARRIER_OFF are derived from the MII signals CRS and RX_DV.

22.2.1.3.3 When generated

The PLS_CARRIER.indicate service primitive is generated by the Reconciliation sublayer whenever the CARRIER_STATUS parameter changes from CARRIER_ON to CARRIER_OFF or vice versa.

While the RX_DV signal is de-asserted, any transition of the CRS signal from de-asserted to asserted must cause a transition of CARRIER_STATUS from the CARRIER_OFF to the CARRIER_ON value, and any transition of the CRS signal from asserted to de-asserted must cause a transition of CARRIER_STATUS from the CARRIER_ON to the CARRIER_OFF value. At any time after CRS and RX_DV are both asserted, de-assertion of RX_DV must cause CARRIER_STATUS to transition to the CARRIER_OFF value. This transition of CARRIER_STATUS from the CARRIER_ON to the CARRIER_OFF value must be recognized by the MAC sublayer, even if the CRS signal is still asserted at the time.

NOTE—The behavior of the CRS signal is specified within this clause so that it can be mapped directly (with the appropriate implementation-specific synchronization) to the carrierSense variable in the MAC process Deference, which is described in 4.2.8. The behavior of the RX_DV signal is specified within this clause so that it can be mapped directly to the carrierSense variable in the MAC process BitReceiver, which is described in 4.2.9, provided that the MAC process BitReceiver is implemented to receive a nibble of data on each cycle through the inner loop.

22.2.1.4 Mapping of PLS_SIGNAL.indicate

22.2.1.4.1 Function

Map the primitive PLS_SIGNAL.indicate to the MII signal COL.

22.2.1.4.2 Semantics of the service primitive

PLS_SIGNAL.indicate (SIGNAL_STATUS)

The SIGNAL_STATUS parameter can take one of two values: SIGNAL_ERROR or NO_SIGNAL_ERROR. SIGNAL_STATUS assumes the value SIGNAL_ERROR when the MII signal COL is asserted, and assumes the value NO_SIGNAL_ERROR when COL is de-asserted.

22.2.1.4.3 When generated

The PLS_SIGNAL.indicate service primitive is generated whenever SIGNAL_STATUS makes a transition from SIGNAL_ERROR to NO_SIGNAL_ERROR or vice versa.

22.2.1.5 Response to RX_ER indication from MII

If, during frame reception, both RX_DV and RX_ER are asserted, the Reconciliation sublayer shall ensure that the MAC will detect a FrameCheckError in that frame.

This requirement may be met by incorporating a function in the Reconciliation sublayer that produces a result that is guaranteed to be not equal to the CRC result, as specified by the algorithm in 3.2.8, of the sequence of nibbles comprising the received frame as delivered to the MAC sublayer. The Reconciliation sublayer must then ensure that the result of this function is delivered to the MAC sublayer at the end of the received frame in place of the last nibble(s) received from the MII.

Other techniques may be employed to respond to RX_ER, provided that the result is that the MAC sublayer behaves as though a FrameCheckError occurred in the received frame.

22.2.1.6 Conditions for generation of TX_ER

If, during the process of transmitting a frame, it is necessary to request that the PHY deliberately corrupt the contents of the frame in such a manner that a receiver will detect the corruption with the highest degree of probability, then the signal TX_ER may be generated.

For example, a repeater that detects an RX_ER during frame reception on an input port may propagate that error indication to its output ports by asserting TX_ER during the process of transmitting that frame.

Since there is no mechanism in the definition of the MAC sublayer by which the transmit data stream can be deliberately corrupted, the Reconciliation sublayer is not required to generate TX_ER.

22.2.2 MII signal functional specifications

22.2.2.1 TX_CLK (transmit clock)

TX_CLK (Transmit Clock) is a continuous clock that provides the timing reference for the transfer of the TX_EN, TXD, and TX_ER signals from the Reconciliation sublayer to the PHY. TX_CLK is sourced by the PHY.

The TX_CLK frequency shall be 25% of the nominal transmit data rate ± 100 ppm. For example, a PHY operating at 100 Mb/s must provide a TX_CLK frequency of 25 MHz, and a PHY operating at 10 Mb/s must provide a TX_CLK frequency of 2.5 MHz. The duty cycle of the TX_CLK signal shall be between 35% and 65% inclusive.

NOTE—See additional information in 22.2.4.1.5.

22.2.2.2 RX_CLK (receive clock)

RX_CLK is a continuous clock that provides the timing reference for the transfer of the RX_DV, RXD, and RX_ER signals from the PHY to the Reconciliation sublayer. RX_CLK is sourced by the PHY. The PHY may recover the RX_CLK reference from the received data or it may derive the RX_CLK reference from a nominal clock (e.g., the TX_CLK reference).

The minimum high and low times of RX_CLK shall be 35% of the nominal period under all conditions.

While RX_DV is asserted, RX_CLK shall be synchronous with recovered data, shall have a frequency equal to 25% of the data rate of the received signal, and shall have a duty cycle of between 35% and 65% inclusive.

When the signal received from the medium is continuous and the PHY can recover the RX_CLK reference and supply the RX_CLK on a continuous basis, there is no need to transition between the recovered clock reference and a nominal clock reference on a frame-by-frame basis. If loss of received signal from the medium causes a PHY to lose the recovered RX_CLK reference, the PHY shall source the RX_CLK from a nominal clock reference.

Transitions from nominal clock to recovered clock or from recovered clock to nominal clock shall be made only while RX_DV is de-asserted. During the interval between the assertion of CRS and the assertion of RX_DV at the beginning of a frame, the PHY may extend a cycle of RX_CLK by holding it in either the high or low condition until the PHY has successfully locked onto the recovered clock. Following the de-assertion of RX_DV at the end of a frame, the PHY may extend a cycle of RX_CLK by holding it in either the high or low condition for an interval that shall not exceed twice the nominal clock period.

NOTE—This standard neither requires nor assumes a guaranteed phase relationship between the RX_CLK and TX_CLK signals. See additional information in 22.2.4.1.5.

22.2.2.3 TX_EN (transmit enable)

TX_EN indicates that the Reconciliation sublayer is presenting nibbles on the MII for transmission. It shall be asserted by the Reconciliation sublayer synchronously with the first nibble of the preamble and shall remain asserted while all nibbles to be transmitted are presented to the MII. TX_EN shall be negated prior to the first TX_CLK following the final nibble of a frame. TX_EN is driven by the Reconciliation sublayer and shall transition synchronously with respect to the TX_CLK.

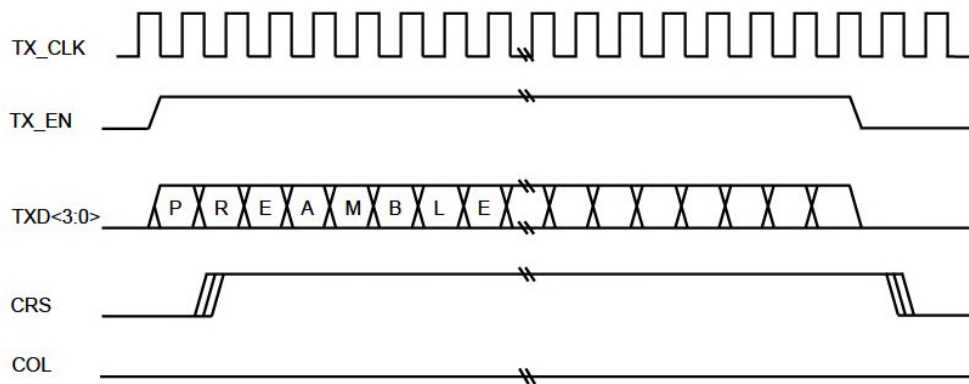Figure 22-4 depicts TX_EN behavior during a frame transmission with no collisions.

Figure 22-4—Transmission with no collision

22.2.2.4 TXD (transmit data)

TXD is a bundle of 4 data signals (TXD<3:0>) that are driven by the Reconciliation sublayer. TXD<3:0> shall transition synchronously with respect to the TX_CLK. For each TX_CLK period in which TX_EN is asserted, TXD<3:0> are accepted for transmission by the PHY. TXD<0> is the least significant bit. While TX_EN is de-asserted, TXD<3:0> shall have no effect upon the PHY.

Figure 22-4 depicts TXD<3:0> behavior during the transmission of a frame.

Table 22-1 summarizes the permissible encodings of TXD<3:0>, TX_EN, and TX_ER.

22.2.2.5 TX_ER (transmit coding error)

TX_ER shall transition synchronously with respect to the TX_CLK. When TX_ER is asserted for one or more TX_CLK periods while TX_EN is also asserted, the PHY shall emit one or more symbols that are not

Table 22-1—Permissible encodings of TXD<3:0>, TX_EN, and TX_ER

TX_EN	TX_ER	TXD<3:0>	Indication
0	0	0000 through 1111	Normal inter-frame
0	1	0000 through 1111	Reserved
1	0	0000 through 1111	Normal data transmission
1	1	0000 through 1111	Transmit error propagation

part of the valid data or delimiter set somewhere in the frame being transmitted. The relative position of the error within the frame need not be preserved.

Assertion of the TX_ER signal shall not affect the transmission of data when a PHY is operating at 10 Mb/s, or when TX_EN is de-asserted.

Figure 22-5 shows the behavior of TX_ER during the transmission of a frame propagating an error.

Table 22-1 summarizes the permissible encodings of TXD<3:0>, TX_EN, and TX_ER.
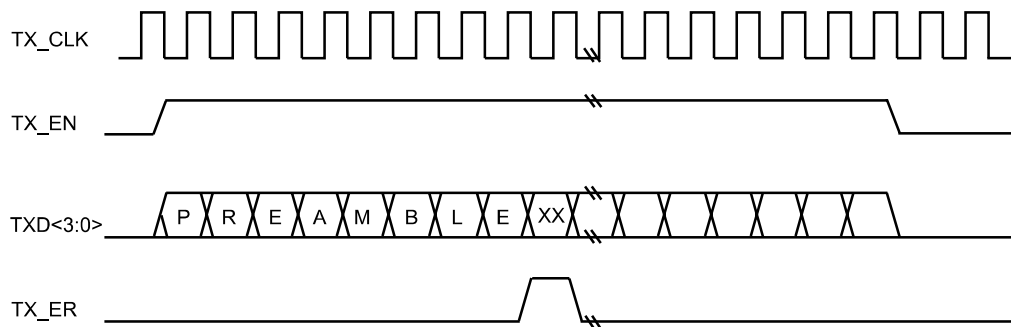

Figure 22-5—Propagating an error

The TX_ER signal shall be implemented at the MII of a PHY, may be implemented at the MII of a repeater that provides an MII port, and may be implemented in MAC sublayer devices. If a Reconciliation sublayer or a repeater with an MII port does not actively drive the TX_ER signal, it shall ensure that the TX_ER signal is pulled down to an inactive state at all times.

22.2.2.6 RX_DV (Receive Data Valid)

RX_DV (Receive Data Valid) is driven by the PHY to indicate that the PHY is presenting recovered and decoded nibbles on the RXD<3:0> bundle and that the data on RXD<3:0> is synchronous to RX_CLK. RX_DV shall transition synchronously with respect to the RX_CLK. RX_DV shall remain asserted continuously from the first recovered nibble of the frame through the final recovered nibble and shall be negated prior to the first RX_CLK that follows the final nibble. In order for a received frame to be correctly interpreted by the Reconciliation sublayer and the MAC sublayer, RX_DV must encompass the frame, starting no later than the Start Frame Delimiter (SFD) and excluding any End-of-Frame delimiter.

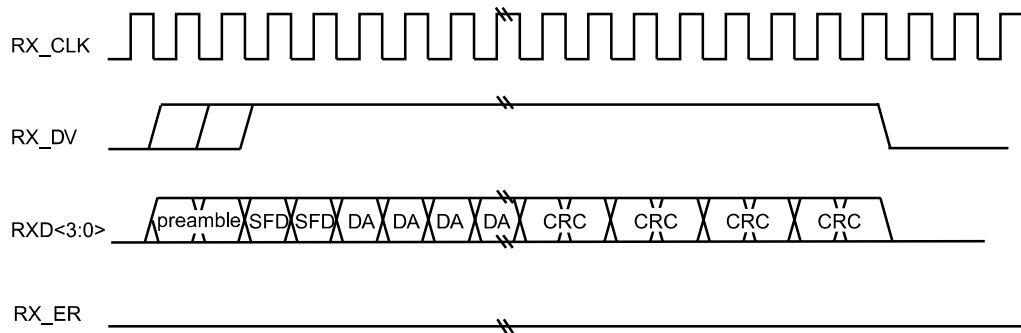Figure 22-6 shows the behavior of RX_DV during frame reception.

Figure 22-6—Reception with no errors

22.2.2.7 RXD (receive data)

RXD is a bundle of four data signals (RXD<3:0>) that transition synchronously with respect to the RX_CLK. RXD<3:0> are driven by the PHY. For each RX_CLK period in which RX_DV is asserted, RXD<3:0> transfer four bits of recovered data from the PHY to the Reconciliation sublayer. RXD<0> is the least significant bit. While RX_DV is de-asserted, RXD<3:0> shall have no effect on the Reconciliation sublayer.

While RX_DV is de-asserted, the PHY may provide a False Carrier indication by asserting the RX_ER signal while driving the value <1110> onto RXD<3:0>. See 24.2.4.4.2 for a description of the conditions under which a PHY will provide a False Carrier indication.

In order for a frame to be correctly interpreted by the MAC sublayer, a completely formed SFD must be passed across the MII. A PHY is not required to loop data transmitted on TXD<3:0> back to RXD<3:0> unless the loopback mode of operation is selected as defined in 22.2.4.1.2.

Figure 22-6 shows the behavior of RXD<3:0> during frame reception.

Table 22-2 summarizes the permissible encoding of RXD<3:0>, RX_ER, and RX_DV, along with the specific indication provided by each code.

Table 2—Permissible encoding of RXD<3:0>, RX_ER, and RX_DV

RX_DV	RX_ER	RXD<3:0>	Indication
0	0	0000 through 1111	Normal inter-frame
0	1	0000	Normal inter-frame
0	1	0001 through 1101	Reserved
0	1	1110	False Carrier indication
0	1	1111	Reserved
1	0	0000 through 1111	Normal data reception
1	1	0000 through 1111	Data reception with errors

22.2.2.8 RX_ER (receive error)

RX_ER (Receive Error) is driven by the PHY. RX_ER shall be asserted for one or more RX_CLK periods to indicate to the Reconciliation sublayer that an error (e.g., a coding error, or any error that the PHY is capable of detecting, and that may otherwise be undetectable at the MAC sublayer) was detected somewhere in the frame presently being transferred from the PHY to the Reconciliation sublayer. RX_ER shall transition synchronously with respect to RX_CLK. While RX_DV is de-asserted, RX_ER shall have no effect on the Reconciliation sublayer.

While RX_DV is de-asserted, the PHY may provide a False Carrier indication by asserting the RX_ER signal for at least one cycle of the RX_CLK while driving the appropriate value onto RXD<3:0>, as defined in 22.2.2.7. See 24.2.4.4.2 for a description of the conditions under which a PHY will provide a False Carrier indication.

The effect of RX_ER on the Reconciliation sublayer is defined in 22.2.1.5, Response to RX_ER indication from MII.

Figure 22-7 shows the behavior of RX_ER during the reception of a frame with errors.
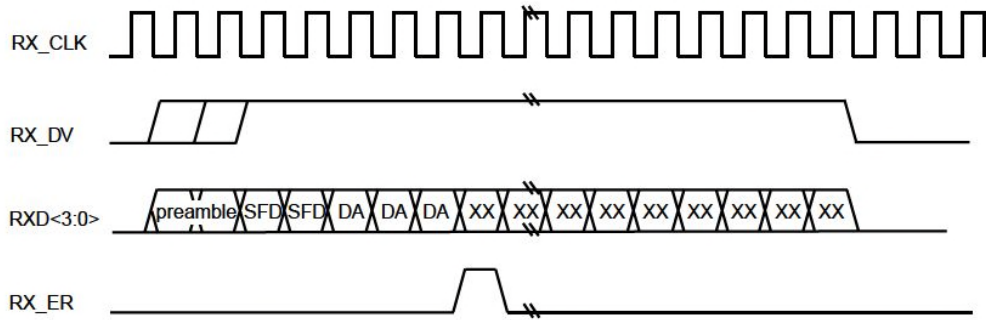

Figure 22-7—Reception with errors

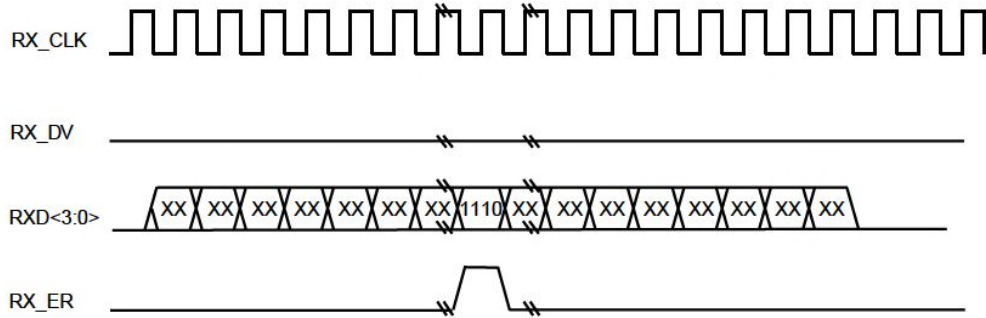Figure 22-8 shows the behavior of RX_ER, RX_DV and RXD<3:0> during a False Carrier indication.

Figure 22-8—False Carrier indication

22.2.2.9 CRS (carrier sense)

CRS shall be asserted by the PHY when either the transmit or receive medium is nonidle. CRS shall be deasserted by the PHY when both the transmit and receive media are idle. The PHY shall ensure that CRS remains asserted throughout the duration of a collision condition.

CRS is not required to transition synchronously with respect to either the TX_CLK or the RX_CLK.

The behavior of the CRS signal is unspecified when the duplex mode bit 0.8 in the control register is set to a logic one, as described in 22.2.4.1.8, or when the Auto-Negotiation process selects a full duplex mode of operation.

Figure 22-4 shows the behavior of CRS during a frame transmission without a collision, while Figure 22-9 shows the behavior of CRS during a frame transmission with a collision.

22.2.2.10 COL (collision detected)

COL shall be asserted by the PHY upon detection of a collision on the medium, and shall remain asserted while the collision condition persists.

COL shall be asserted by a PHY that is operating at 10 Mb/s in response to a *signal_quality_error* message from the PMA.

COL is not required to transition synchronously with respect to either the TX_CLK or the RX_CLK.

The behavior of the COL signal is unspecified when the duplex mode bit 0.8 in the control register is set to a logic one, as described in 22.2.4.1.8, or when the Auto-Negotiation process selects a full-duplex mode of operation.

Figure 22-9 shows the behavior of COL during a frame transmission with a collision.
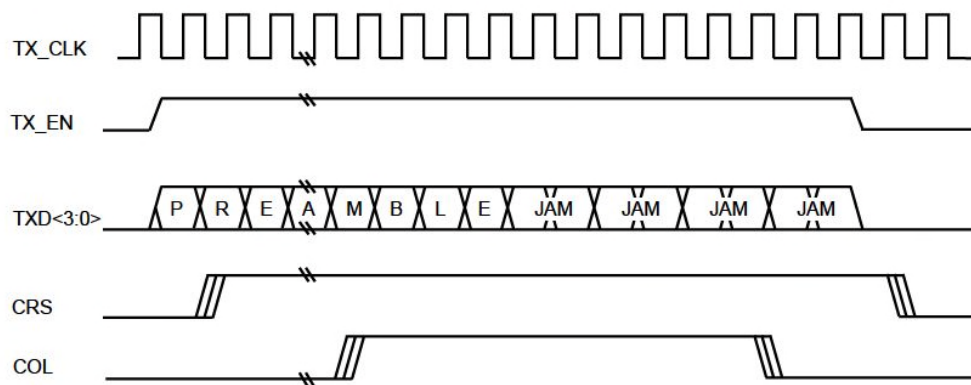

Figure 22-9—Transmission with collision

NOTE—The circuit assembly that contains the Reconciliation sublayer may incorporate a weak pull-up on the COL signal as a means of detecting an open circuit condition on the COL signal at the MII. The limit on the value of this pull-up is defined in 22.4.4.2.

22.2.2.11 MDC (management data clock)

MDC is sourced by the Station Management entity to the PHY as the timing reference for transfer of information on the MDIO signal. MDC is an aperiodic signal that has no maximum high or low times. The minimum high and low times for MDC shall be 160 ns each, and the minimum period for MDC shall be 400 ns, regardless of the nominal period of TX_CLK and RX_CLK.

22.2.2.12 MDIO (management data input/output)

MDIO is a bidirectional signal between the PHY and the STA. It is used to transfer control information and status between the PHY and the STA. Control information is driven by the STA synchronously with respect to MDC and is sampled synchronously by the PHY. Status information is driven by the PHY synchronously with respect to MDC and is sampled synchronously by the STA.

MDIO shall be driven through three-state circuits that enable either the STA or the PHY to drive the signal. A PHY that is attached to the MII via the mechanical interface specified in 22.6 shall provide a resistive pull-up to maintain the signal in a high state. The STA shall incorporate a resistive pull-down on the MDIO signal and thus may use the quiescent state of MDIO to determine if a PHY is connected to the MII via the mechanical interface defined in 22.6. The limits on the values of these pull-ups and pull-downs are defined in 22.4.4.2.

22.2.3 Frame structure

Data frames transmitted through the MII shall have the frame format shown in figure 22-10.

<inter-frame><preamble><sfd><data><efd>

Figure 22-10—MII frame format

For the MII, transmission and reception of each octet of data shall be done a nibble at a time with the order of nibble transmission and reception as shown in figure 22-11.
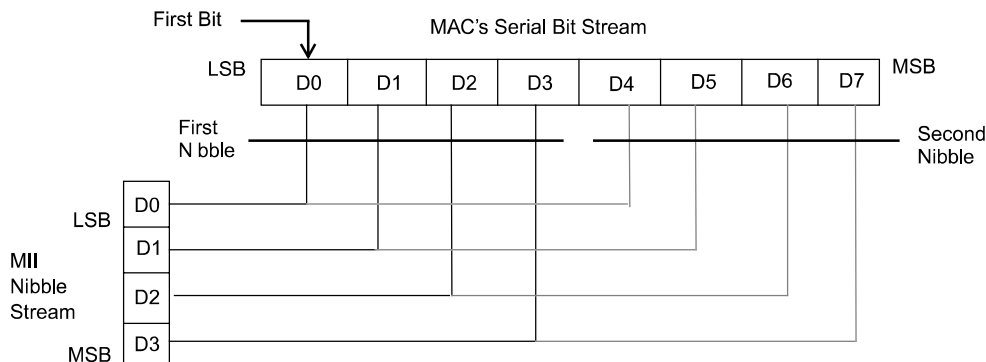

Figure 22-11—Octet/nibble transmit and receive order

The bits of each octet are transmitted and received as two nibbles, bits 0 through 3 of the octet corresponding to bits 0 through 3 of the first nibble transmitted or received, and bits 4 through 7 of the octet corresponding to bits 0 through 3 of the second nibble transmitted or received.

22.2.3.1 Inter-frame

The inter-frame period provides an observation window for an unspecified amount of time during which no data activity occurs on the MII. The absence of data activity is indicated by the de-assertion of the RX_DV signal on the receive path, and the de-assertion of the TX_EN signal on the transmit path. The MAC inter-FrameSpacing parameter defined in clause 4 is measured from the de-assertion of the CRS signal to the assertion of the CRS signal.

22.2.3.2 Preamble and start of frame delimiter

22.2.3.2.1 Transmit case

The preamble <preamble> begins a frame transmission. The bit value of the preamble field at the MII is unchanged from that specified in 7.2.3.2 and shall consist of 7 octets with the following bit values:

    10101010 10101010 10101010 10101010 10101010 10101010 10101010

In the preceding example, the preamble is displayed using the bit order it would have if transmitted serially. This means that for each octet the leftmost l value represents the LSB of the octet, and the rightmost 0 value the octet MSB.

The SFD (Start Frame Delimiter) <sfd> indicates the start of a frame and follows the preamble. The bit value of the SFD at the MII is unchanged from that specified in 7.2.3.3 and is the bit sequence:

    10101011

The preamble and SFD shall be transmitted through the MII as nibbles starting from the assertion of TX_EN as shown in table 22-3.

Table 3—Transmitted preamble and SFD

Signal	Bit values of nibbles transmitted through MII																		
TXD0	X	1*	1	1	1	1	1	1	1	1	1	1	1	1	1	1†	1	D0‡	D4§
TXD1	X	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	D1	D5
TXD2	X	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	D2	D6
TXD3	X	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	D3	D7
TX_EN	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

*1st preamble nibble transmitted.
†1st SFD nibble transmitted.
‡1st data nibble transmitted.
§D0 through D7 are the first eight bits of the data field from the Protocol Data Unit (PDU).

22.2.3.2.2 Receive case

The conditions for assertion of RX_DV are defined in 22.2.2.6.

The alignment of the received SFD and data at the MII shall be as shown in table 22-4 and table 22-5. Table 22-4 depicts the case where no preamble nibbles are conveyed across the MII, and table 22-5 depicts the case where the entire preamble is conveyed across the MII.

Table 4—Start of receive with no preamble preceding SFD

Signal	Bit values of nibbles received through MII										
RXD0	X	X	X	X	X	X	X	1*	1	D0†	D4‡
RXD1	X	X	X	X	X	X	X	0	0	D1	D5
RXD2	X	X	X	X	X	X	X	1	1	D2	D6
RXD3	X	X	X	X	X	X	X	0	1	D3	D7
RX_DV	0	0	0	0	0	0	0	1	1	1	1

*1st SFD nibble received.
†1st data nibble received.
‡D0 through D7 are the first eight bits of the data field from the PDU.

Table 5—Start of receive with entire preamble preceding SFD

Signal	Bit values of nibbles received through MII																			
RXD0	X	1*	1	1	1	1	1	1	1	1	1	1	1	1	1	1†	1	D0‡	D4§
RXD1	X	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	D1	D5
RXD2	X	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	D2	D6
RXD3	X	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	D3	D7
RX_DV	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

*1st preamble nibble received.
†1st SFD nibble received.
‡1st data nibble received.
§D0 through D7 are the first eight bits of the data field from the PDU.

22.2.3.3 Data

The data in a well formed frame shall consist of N octets of data transmitted as 2N nibbles. For each octet of data the transmit order of each nibble is as specified in figure 22-11. Data in a collision fragment may consist of an odd number of nibbles.

22.2.3.4 End-of-Frame delimiter (EFD)

De-assertion of the TX_EN signal constitutes an End-of-Frame delimiter for data conveyed on TXD<3:0>, and de-assertion of RX_DV constitutes an End-of-Frame delimiter for data conveyed on RXD<3:0>.

22.2.3.5 Handling of excess nibbles

An excess nibble condition occurs when an odd number of nibbles is conveyed across the MII beginning with the SFD and including all nibbles conveyed until the End-of-Frame delimiter. Reception of a frame containing a non-integer number of octets shall be indicated by the PHY as an excess nibble condition.

Transmission of an excess nibble may be handled by the PHY in an implementation-specific manner. No assumption should be made with regard to truncation, octet padding, or exact nibble transmission by the PHY.

22.2.4 Management functions

The management interface specified here provides a simple, two-wire, serial interface to connect a management entity and a managed PHY for the purposes of controlling the PHY and gathering status from the PHY. This interface is referred to as the MII Management Interface.

The management interface consists of a pair of signals that physically transport the management information across the MII, a frame format and a protocol specification for exchanging management frames, and a register set that can be read and written using these frames. The register definition specifies a basic register set with an extension mechanism.

The basic register set consists of two registers referred to as the Control Register (register 0) and the Status Register (register 1). The status and control functions defined here are considered basic and fundamental to 100 Mb/s PHYs. All PHYs that provide an MII shall incorporate the basic register set. Registers 2 through 7 are part of the extended register set.

The full set of management registers is listed in table 22-6.

Table 6—MII management register set

Register address	Register name	Basic/Extended
0	Control	B
1	Status	B
2,3	PHY Identifier	E
4	Auto-Negotiation Advertisement	E
5	Auto-Negotiation Link Partner Ability	E
6	Auto-Negotiation Expansion	E
7	Auto-Negotiation Next Page Transmit	E
8 through 15	Reserved	E
16 through 31	Vendor Specific	E

22.2.4.1 Control register (register 0)

The assignment of bits in the Control Register is shown in table 22-7 below. The default value for each bit of the Control Register should be chosen so that the initial state of the PHY upon power up or reset is a normal operational state without management intervention.

Table 7—Control register bit definitions

Bit(s)	Name	Description	R/W[*]
0.15	Reset	1 = PHY reset 0 = normal operation	R/W SC
0.14	Loopback	1 = enable loopback mode 0 = disable loopback mode	R/W
0.13	Speed Selection	1 = 100 Mb/s 0 = 10 Mb/s	R/W
0.12	Auto-Negotiation Enable	1 = Enable Auto-Negotiation Process 0 = Disable Auto-Negotiation Process	R/W
0.11	Power Down	1 = power down 0 = normal operation[†]	R/W
0.10	Isolate	1 = electrically Isolate PHY from MII 0 = normal operation[b]	R/W
0.9	Restart Auto-Negotiation	1 = Restart Auto-Negotiation Process 0 = normal operation	R/W SC
0.8	Duplex Mode	1 = Full Duplex[‡] 0 = Half Duplex	R/W
0.7	Collision Test	1 = enable COL signal test 0 = disable COL signal test	R/W
0.6:0	Reserved	Write as 0, ignore on Read	R/W

[*]R/W = Read/Write, SC = Self-Clearing.
[†]For normal operation, both 0.10 and 0.11 must be cleared to zero, see 22.2.4.1.5.
[‡]Specifications for full-duplex mode operation are planned for future work.

22.2.4.1.1 Reset

Resetting a PHY is accomplished by setting bit 0.15 to a logic one. This action shall set the status and control registers to their default states. As a consequence this action may change the internal state of the PHY and the state of the physical link associated with the PHY. This bit is self-clearing, and a PHY shall return a value of one in bit 0.15 until the reset process is completed. A PHY is not required to accept a write transaction to the control register until the reset process is completed, and writes to bits of the control register other than 0.15 may have no effect until the reset process is completed. The reset process shall be completed within 0.5 s from the setting of bit 0.15.

The default value of bit 0.15 is zero.

NOTE—This operation may interrupt data communication.