

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

APPLE, INC.,
Petitioner,

v.

REALTIME DATA LLC,
Patent Owner.

Case IPR2016-01365
Patent 7,181,608 B2

Before GEORGIANNA W. BRADEN, J. JOHN LEE, and
JASON J. CHUNG, *Administrative Patent Judges*.

LEE, *Administrative Patent Judge*.

DECISION
Granting Institution of *Inter Partes* Review
37 C.F.R. § 42.108

INTRODUCTION

On July 8, 2016, Petitioner Apple, Inc. filed a Petition (Paper 2, “Pet.”) requesting *inter partes* review of claims 1–31 (“the challenged claims”) of U.S. Patent No. 7,181,608 B2 (Ex. 1001, “the ’608 Patent”). Patent Owner Realtime Data, LLC timely filed a Preliminary Response (Paper 9, “Prelim. Resp.”) on October 20, 2016.

Under 35 U.S.C. § 314, an *inter partes* review may not be instituted unless the information presented in the Petition shows “there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.” *See also* 37 C.F.R. § 42.4(a) (delegating authority to the Board). Upon consideration of the Petition and Patent Owner’s Preliminary Response, and the evidence cited therein, we determine that the information presented demonstrates a reasonable likelihood that Petitioner would prevail in establishing the unpatentability of each of the challenged claims. Accordingly, we institute an *inter partes* review of the challenged claims.

A. Related Proceedings

The parties identify the following cases as related to the challenged patent: *Realtime Data, LLC v. Microsoft Corporation*, Case No. 4:14-cv-00827 (E.D. Tex.) and *Realtime Data, LLC v. Apple, Inc.*, Case No. 3:16-cv-02595 (N.D. Cal.) (transferred from *Realtime Data, LLC v. Apple, Inc.*, Case No. 6:15-cv-00885 (E.D. Tex.)). Pet. 1; Paper 8, 2.

B. The ’608 Patent

The ’608 Patent relates to “providing accelerated loading of operating system and application programs upon system boot or application launch,”

and to the use of data compression and decompression techniques for such purpose. Ex. 1001, 1:15–21. The specification discusses the limits of prior art storage devices, particularly the significant bandwidth limitations of “mass storage devices” such as hard disk drives. *Id.* at 1:39–52, 2:4–14. According to the specification,

“[A]ccelerated” data storage comprises receiving a digital data stream at a data transmission rate which is greater than the data storage rate of a target storage device, compressing the input stream at a compression rate that increases the effective data storage rate of the target storage device and storing the compressed data in the target storage device.

Id. at 5:48–54.

C. *Challenged Claims*

Petitioner challenges claims 1–31 of the ’608 Patent. Pet. 2. Claims 1, 7, 22, and 27 are independent. Claim 1 is illustrative of the challenged claims, and is reproduced below:

1. A method for providing accelerated loading of an operating system, comprising the steps of:
 - maintaining a list of boot data used for booting a computer system;
 - initializing a central processing unit of the computer system;
 - preloading the boot data into a cache memory prior to completion of initialization of the central processing unit of the computer system, wherein preloading the boot data comprises accessing compressed boot data from a boot device; and
 - servicing requests for boot data from the computer system using the preloaded boot data after completion of initialization of the central processing unit of the computer system, wherein servicing requests comprises accessing compressed boot data from the cache and decompressing the compressed boot data at a rate that increases the effective access rate of the cache.

D. Asserted Prior Art and Grounds of Unpatentability

Petitioner asserts the following grounds of unpatentability under 35 U.S.C. § 103 (Pet. 2):

Challenged Claim(s)	Asserted Prior Art
1-31	Sukegawa ¹ and Dye ²
1-31	Sukegawa, Dye, and Settsu ³
1-31	Sukegawa, Dye, and Burrows ⁴
1-31	Sukegawa, Dye, Settsu and Burrows

Additionally, Petitioner relies on the Declaration of Dr. Charles J. Neuhauser (Ex. 1003) to support its challenges.

ANALYSIS

A. Claim Construction

In an *inter partes* review, claim terms in an unexpired patent are given their broadest reasonable construction in light of the specification of the patent in which they appear. 37 C.F.R. § 42.100(b); *see Cuozzo Speed Techs., LLC v. Lee*, 136 S. Ct. 2131, 2144–46 (2016). No claim terms require express construction for purposes of this Decision. *See Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999).

¹ U.S. Patent No. 5,860,083, issued Jan. 12, 1999 (Ex. 1005, “Sukegawa”).

² U.S. Patent No. 6,145,069, filed Apr. 26, 1999, issued Nov. 7, 2000 (Ex. 1008, “Dye”).

³ U.S. Patent No. 6,374,353 B1, filed Mar. 3, 1999, issued Apr. 16, 2002 (Ex. 1006, “Settsu”).

⁴ Michael Burrows et al., *On-line Data Compression in a Log-structured File System* (1992) (Ex. 1007, “Burrows”).

B. Overview of the Asserted Prior Art

1. Sukegawa

Sukegawa relates to “a data storage system using a flash memory unit and an HDD [(hard disk drive)].” Ex. 1005, at [57]. The flash memory unit is used, for example, to store “data which is used frequently for a relatively long time period.” *Id.* Such data could include “control information necessary for starting an application program (AP) and an OS [(operating system)].” *Id.* at 2:65–3:3. Although such control information is stored on the HDD, the data may be stored also on the flash memory unit so that the OS may be started using the control information on the flash memory unit instead of the HDD. *Id.* at 6:45–54. This is advantageous because the flash memory unit has a “higher access speed,” which allows the OS to be started more quickly. *Id.* at 6:54–58.

2. Dye

Dye relates to controllers for flash or embedded memory that include data compression and decompression engines “for increased effective memory density and improved bandwidth.” Ex. 1008, 1:17–22, 2:42–46. According to Dye, such a controller enables conventional flash memory to “achieve higher bandwidth, more effective density, with less system power and noise.” *Id.* at 3:3–12, 3:23–28. The technology permits data to be “saved in either a normal or compressed format, retrieved from the Flash Memory Array for MPU [(microprocessing unit)] execution in a normal or compressed format, or transmitted and stored on a medium in a normal or compressed format.” *Id.* at 3:66–4:8.

3. *Settsu*

Settsu relates to “[a] method of booting up an information processing apparatus.” Ex. 1006, at [57]. One embodiment described in Settsu involves dividing the main body of an operating system into modules and storing each module as compressed files on a boot device. *Id.* at 14:58–63. Each of these modules is decompressed each time it is loaded into memory, and “the time required for I/O [(input/output)] processing can be reduced” as a result, which “provides an advantage of being able to further reduce the time required for booting up the information processing apparatus.” *Id.* at 14:64–15:4.

4. *Burrows*

Burrows states that it “appeared in the proceedings of the Fifth International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS-V), 12–15 October, 1992, published by ACM Press.” Ex. 1007, iv. According to Burrows, “[b]uilding a file system that compresses the data it stores on disk is clearly an attractive idea,” at least because “more data would fit on the disk” and using a “fast hardware data compressor” would “increase the effective disk transfer rate by the compression factor, thus speeding up the system.” *Id.* at 1. Burrows describes a particular type of file system utilizing data compression and reports the results of tests of that system. *See id.* at v.

C. *Alleged Obviousness in View of Sukegawa and Dye*

Petitioner contends the combination of Sukegawa and Dye teaches or suggests each element of claims 1–31. Pet. 24–67. A claim is unpatentable under 35 U.S.C. § 103 if the differences between the claimed subject matter

and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person of ordinary skill in the art. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). This determination is made in light of the relevant facts concerning: (1) the scope and content of the prior art, (2) the differences between the prior art and the claims at issue, (3) the level of ordinary skill in the pertinent art,⁵ and (4) secondary considerations, such as commercial success, long felt but unsolved needs, failure of others, etc. *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966). In addition, it may be “important to identify a reason that would have prompted a person of ordinary skill in the relevant field to combine the elements in the way the claimed new invention does.” *KSR*, 550 U.S. at 418.

1. *Independent Claim 1*

The Petition sets forth detailed contentions and supporting evidence alleging that claim 1 is obvious in light of the combined teachings of Sukegawa and Dye. Pet. 24–41. On the present record, we conclude the Petition has made an adequate showing for purposes of institution.

For the recited step of “maintaining a list of boot data used for booting a computer system,” Petitioner identifies teachings in Sukegawa relating to maintaining “control information” necessary for starting an OS or an application program. *Id.* at 25–29. For the step of “initializing” a CPU, Petitioner asserts that Sukegawa teaches a CPU and, as Dr. Neuhauser testifies, that a person of ordinary skill would have understood that the CPU

⁵ For purposes of this Decision, we determine the asserted prior art reflects the appropriate level of ordinary skill in the art. *See Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001).

must be initialized to start an OS or application program. Pet. 29–30; Ex. 1003 ¶¶ 106–07; Ex. 1005, 4:22–30, 6:19–58.

With respect to the step of “preloading the boot data into a cache memory prior to completion of initialization of the central processing unit,” Petitioner identifies teachings in Sukegawa regarding the copying of control information (e.g., for the OS) from a HDD to portions of a flash memory unit, which Sukegawa indicates is used “as a cache memory.” Pet. 30–33 (quoting Ex. 1005, 4:7–10); *see* Ex. 1005, 6:35–39, 6:45–49. Sukegawa explains that “when the OS is started at the time of the next turning-on of power, the control information necessary for starting the OS is read out not from HDD2 but from the . . . cache memory area [of the flash memory unit].” Ex. 1005, 6:49–53. According to Petitioner, these aspects of Sukegawa teach preloading boot data into a cache memory (i.e., copying control information from the HDD to the flash memory unit) prior to completion of CPU initialization (i.e., before the next time the computer is turned on), as recited in claim 1. Pet. 31–33.

As to the requirement of claim 1 that the preloading step comprises “accessing compressed boot data from a boot device,” Petitioner relies on the combination of teachings from Sukegawa and Dye. Pet. 33–35. Petitioner argues the HDD of Sukegawa teaches the recited boot device because it stores the control information necessary to boot the OS and application programs. *Id.* at 33 (citing Ex. 1005, 4:1–21, 6:19–58, Figs. 1, 4; Ex. 1001, 21:53–56). For the requirement that the boot data be compressed, Petitioner relies on Dye’s description of a memory controller using data

compression and decompression engines to compress data for storage.⁶ Pet. 33–34. Based on the testimony of its expert, Dr. Neuhauser, Petitioner argues a person of ordinary skill would have been motivated to apply these teachings of Dye to the control information of Sukegawa because Dye explicitly teaches that compression and decompression technology provides the benefits of improved memory capacity and performance, which also was well-known in the art. *Id.*; Ex. 1003 ¶¶ 63, 118–20; *see* Ex. 1008, at [57], 2:42–46.

For the step of “servicing requests for boot data from the computer system using the preloaded boot data,” Petitioner relies on Sukegawa. Pet. 35–36. Specifically, Sukegawa describes a controller that “controls the flash memory unit 1 and HDD 2, as an integrated storage system, in accordance with access requests (read/write commands) issued from the host system 4 to the HDD.” Ex. 1005, 4:26–30. As discussed above, Sukegawa describes a procedure by which control information for an OS or application program is copied from an HDD to a flash memory unit, and the control information is provided from the flash memory unit instead of the HDD for a subsequent boot-up of the computer. *Id.* at 6:45–54.

Claim 1 further requires the servicing requests step to comprise “accessing compressed boot data from the cache and decompressing the compressed boot data at a rate that increases the effective access rate of the

⁶ The Petition also relies on U.S. Patent Application No. 09/239,659 (issued as U.S. Patent No. 7,190,284 B1 (“Dye ’284,” Ex. 1009)), which Petitioner asserts is incorporated by reference into Dye. Pet. 12. Patent Owner contends Dye’s incorporation by reference of Dye ’284 is insufficient. Prelim. Resp. 17–20. For purposes of this Decision, we need not reach this issue because Petitioner has made a sufficient showing for purposes of institution even without considering Dye ’284.

cache.” As to this limitation, Petitioner argues that Dye teaches accessing and decompressing compressed data from flash memory, and that doing so increases the read access rate of the memory. Pet. 37–41. Again, Petitioner contends a person of ordinary skill would have been motivated to modify the Sukegawa system with the compression/decompression technology taught in Dye to achieve the benefits described in Dye, such as improved memory capacity and access bandwidth. *Id.* at 37, 41.

Based on the present record, we conclude Petitioner’s contentions and evidence, as discussed above, demonstrates a reasonable likelihood of prevailing as to claim 1 on the ground of unpatentability based on Sukegawa and Dye. Patent Owner’s arguments, addressed in detail below, are unpersuasive at this stage.

First, Patent Owner argues Petitioner fails to demonstrate that the asserted art teaches the “preloading” step of claim 1. Prelim. Resp. 11. To the contrary, as discussed above, Petitioner explains sufficiently at this stage how the combination of Sukegawa and Dye teaches the preloading step. *See* Pet. 30–35. Patent Owner’s arguments that Petitioner fails to show the asserted art teaches “accessing compressed boot data” and “decompressing the compressed boot data at a rate that increases the effective access rate of the cache” (Prelim. Resp. 12–13) are unpersuasive for similar reasons. *See* Pet. 33–35; 37–41.⁷

Patent Owner also argues that Petitioner fails to articulate a sufficient motivation to combine Sukegawa and Dye. *See* Prelim. Resp. 20–24. As

⁷ Several of Patent Owner’s arguments appear to be based in large part on Patent Owner’s belief that the Petition improperly relies on Dye ’284. *See, e.g.,* Prelim. Resp. 11 n.30. As discussed above, Petitioner’s showing is sufficient at this stage even if Dye ’284 is not considered.

discussed above, however, Petitioner explains that a person of ordinary skill would have been motivated to combine Sukegawa's system with Dye's compression and decompression teachings because Dye indicates those teachings lead to improved memory capacity and performance. Pet. 34, 37, 41; Ex. 1003 ¶¶ 63, 118–20; *see* Ex. 1008, at [57], 2:42–46. On this record, Petitioner has articulated sufficient reasoning with rational underpinning to combine the references as asserted, for purposes of institution.

Next, Patent Owner contends that Dye “teaches away” from the asserted combination with Sukegawa because Dye's teachings are in the context of “solid state disk and Execute In Place (‘XIP’) architectures,” which are distinguished from systems that include hard disk drives. Prelim. Resp. 25–28. At this stage, however, Patent Owner does not identify any evidence in Dye or elsewhere that criticizes, discredits, or otherwise discourages the use of compression or decompression techniques with hard disk drives. *See In re Fulton*, 391 F.3d 1195, 1201 (Fed. Cir. 2004). Merely describing how a compression/decompression technique may be advantageously used in one type of system architecture does not teach away from its use in other systems. *See id.*; *In re Gurley*, 27 F.3d 551, 554 (Fed. Cir. 1994).

In addition, Patent Owner's argument is unpersuasive that the specific configuration of the compression/decompression engine in Dye, when inserted into the system of Sukegawa, would not yield the claimed invention. Prelim. Resp. 28–29. “The test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference.” *In re Keller*, 642 F.2d 413, 425 (CCPA 1981). “Rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art.” *Id.*; *see In re Mouttet*, 686

F.3d 1322, 1332 (Fed. Cir. 2012) (citing *Keller*); *see also In re Etter*, 756 F.2d 852, 859 (Fed. Cir. 1985) (en banc) (“*Etter’s* assertions that Azure cannot be incorporated in Ambrosio are basically irrelevant, the criterion being not whether the references could be physically combined but whether the claimed inventions are rendered obvious by the teachings of the prior art as a whole.”).

Patent Owner further argues that Petitioner’s showing with respect to the step of “preloading the boot data . . . prior to completion of initialization of the [CPU]” is insufficient because Petitioner’s evidence does not support “a *de facto* inherency argument.” Prelim. Resp. 32–36. According to Patent Owner, Petitioner’s evidence only shows that the CPU of Sukegawa “may” be initialized, not that it is necessarily so, which is insufficient for inherency. *Id.* We note, however, that Petitioner’s asserted ground of unpatentability is based on obviousness, not anticipation. Moreover, Petitioner presents evidence supporting its allegation that a person of ordinary skill would have understood Sukegawa to teach that its CPU must be initialized before starting an OS or application program, including the testimony of Dr. Neuhauser. Pet. 29–30; Ex. 1003 ¶¶ 106–07; Ex. 1005, 4:22–30, 6:19–58. At this stage, Petitioner’s evidence is sufficient.

For the reasons discussed above, Petitioner has demonstrated a reasonable likelihood of prevailing as to claim 1 on the ground of obviousness in view of Sukegawa and Dye.

2. *Remaining Challenged Claims*

The Petition sets forth detailed contentions and supporting evidence alleging that claims 2–31 are obvious in light of the combined teachings of Sukegawa and Dye. Pet. 41–67. For instance, as discussed above, Sukegawa describes “control information” necessary to start an OS as well

as control information necessary to start application programs, which the Petition applies to the limitations of claims 2 and 9. *Id.* at 41–42, 53–55. With respect to the claims reciting Huffman or Lempel-Ziv encoding, Petitioner identifies disclosures in Dye that reference these encoding schemes. Pet. 59, 61, 64, 66. As for the “direct memory access” limitation of claim 13, Petitioner relies on the combination of Sukegawa’s teachings regarding accessing boot data from a HDD and Dye’s teachings regarding data compression, as well as Dr. Neuhauser’s testimony that a person of ordinary skill would have understood Sukegawa to teach direct memory access via a PCI bus (Ex. 1003 ¶¶ 260–62). Pet. 58.

For the system claims (e.g., claim 7 and 27), Petitioner identifies structures taught in Sukegawa—for example, Sukegawa’s cache system controller 3 (“digital signal processor (DSP) or controller” (claim 7)), flash memory unit 1 (“cache memory device” (claim 7), “cache memory” (claim 27)), and HDD 2 (“non-volatile memory device” (claim 7), “boot device” and “non-volatile memory” (claim 27)), and the compression/decompression engine of Dye (“data compression engine” (claim 27)). Pet. 48–49, 65–66; *see also id.* at 37–38 (arguments regarding Dye’s compression and decompression engine, which are cross-referenced in Petitioner’s arguments for claim 27), 55–58 (arguments regarding Dye’s compression and decompression engine with respect to the “data compression engine” limitations of claim 10).

Patent Owner presents the same or similar arguments for the remaining claims as it does for claim 1, which are unpersuasive on the present record for similar reasons as for claim 1. In addition, Patent Owner argues Petitioner failed to address the limitation in claim 27 of “preloading compressed boot data *associated to the list*” (emphasis added), which it

contends is different than similar language recited in claim 1. Prelim. Resp. 36–37. Petitioner relies solely on its arguments regarding the preloading step of claim 1, which it argues apply equally to this aspect of claim 27. *See* Pet. 65. At this stage, we disagree with Patent Owner’s characterization of the claim. Claim 27 recites, “maintaining a list *associated with boot data*” (emphasis added), as compared to claim 1, which recites “maintaining a list *of boot data*” (emphasis added). Neither party argues these phrases are different in scope in any respect relevant to this proceeding, nor do we perceive any such difference. The recitation in claim 27 of preloading “boot data *associated to the list*” (emphasis added) appears to be simply a reference to the previously recited “list associated with boot data,” i.e., the boot data that the list is “associated with.” Thus, at this juncture, we are not persuaded that “preloading compressed boot data associated to the list,” as recited in claim 27, is appreciably different in scope than “preloading the boot data . . . compris[ing] accessing compressed boot data,” as recited in claim 1.

Based on the evidence available at this stage of the case and the analysis presented in the Petition, Petitioner has demonstrated a reasonable likelihood of prevailing as to claims 2–31 on the ground of obviousness in view of Sukegawa and Dye.

C. Alleged Obviousness in View of Sukegawa, Dye, and Settsu and/or Burrows

For the remaining asserted grounds of unpatentability, Petitioner principally relies on the same arguments and evidence as in the ground based solely on Sukegawa and Dye, which are discussed above. Petitioner presents additional arguments relating to Settsu and Burrows as to specific

limitations in certain claims. Pet. 67–70. For example, for claim 1, Petitioner contends Settsu teaches accessing compressed operating system files on a “boot device.” *Id.* at 68; *see* Ex. 1006, 14:58–66. Settsu indicates doing so reduces the time required for booting up (Ex. 1006, 14:66–15:4), which Petitioner argues provides further motivation for a person of ordinary skill to combine the system of Sukegawa with teachings about compression/decompression, such as in Dye and Settsu. Pet. 68. Similarly, Petitioner notes Burrows teaches “that compression/decompression was well-known to increase the speed of accessing data from a hard drive,” which it contends would have further motivated a skilled artisan to combine the system of Sukegawa with the teachings of Burrows and Dye to apply compression/decompression to store the control information on the hard disk drive in compressed format. *Id.* at 69; *see id.* at 17–18 (citing Ex. 1007, 1).

In addition to its arguments relating to the asserted combination of Sukegawa and Dye, Patent Owner further argues that Petitioner’s alleged motivation to combine based on Settsu is insufficient because “Settsu does not discuss improving boot time on a system such as Sukegawa, which also claims to improve boot time using another technique,” and no evidence indicates applying Settsu to Sukegawa could further improve boot speed. Prelim. Resp. 30–31. As discussed earlier, however, “[t]he test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference.” *Keller*, 642 F.2d at 425; *see In re Mouttet*, 686 F.3d 1322, 1332 (Fed. Cir. 2012) (citing *Keller*). Patent Owner also argues Burrows does not supply sufficient evidence of a motivation to combine by merely indicating that data compression is “attractive.” Prelim. Resp. 31–32. Petitioner, however, identifies more specific and detailed portions of Burrows that support its

contentions sufficiently on this record. *See* Pet. 17–18, 69; Ex. 1007, 1 (specifying that compression would mean “more data would fit on the disk,” and the “disk transfer rate” could be increased).

Based on the present record and the analysis presented in the Petition, we are persuaded Petitioner has demonstrated a reasonable likelihood of prevailing as to claims 1–6 and 9–17 on the grounds of obviousness in view of (1) Sukegawa, Dye, and Settsu; (2) Sukegawa, Dye, and Burrows; and (3) Sukegawa, Dye, Settsu, and Burrows. With respect to independent claims 7, 22, and 27, as well as their dependent claims, however, Petitioner does not present any specific argument or evidence regarding Settsu or Burrows.⁸ Thus, we decline to institute Petitioner’s challenges to those claims based on Settsu or Burrows. *See* 37 C.F.R. § 42.108.

D. Remaining Patent Owner Arguments

Patent Owner makes several additional arguments against the Petition generally. First, Patent Owner argues the Petition violated 35 U.S.C. § 312(a)(3) and 37 C.F.R. §§ 42.22, 42.104 through the use of improper “cross-referencing, nested citations, and citations to expert declaration,” among other alleged failings. Prelim. Resp. 37–44. Aside from the table on page 71 of the Petition (*see supra* note 8), we determine the Petition is not in violation of these rules and requirements. Additionally, Patent Owner argues the Petition improperly incorporates Dr. Neuhauser’s Declaration by reference and seeks to circumvent the word limit for petitions. Prelim. Resp. 44–48. We disagree with this argument as well. Finally, Patent Owner

⁸ Although the Petition includes a table that purports to indicate which claims its “Settsu/Burrows Analysis” applies to, the table is inadequate to meet the requirements of 37 C.F.R. § 42.104(b).

urges that all grounds except obviousness in view of Sukegawa and Dye be rejected as “redundant.” *Id.* at 48–50. Although we have discretion to decline to institute on any asserted ground, including those that are duplicative of other grounds, we decline to exercise that discretion beyond as already discussed above.

CONCLUSION

For the foregoing reasons and on the present record, we determine that the information presented in the Petition demonstrates a reasonable likelihood that Petitioner would prevail in establishing the unpatentability of claims 1–31.

ORDER

Accordingly, it is

ORDERED that pursuant to 35 U.S.C. § 314, an *inter partes* review is hereby instituted on the following asserted grounds of unpatentability:

- (1) Claims 1–31 as unpatentable under 35 U.S.C. § 103(a) in view of Sukegawa and Dye;
- (2) Claims 1–6 and 9–17 as unpatentable under 35 U.S.C. § 103(a) in view of Sukegawa, Dye, and Settsu;
- (3) Claims 1–6 and 9–17 as unpatentable under 35 U.S.C. § 103(a) in view of Sukegawa, Dye, and Burrows; and
- (4) Claims 1–6 and 9–17 unpatentable under 35 U.S.C. § 103(a) in view of Sukegawa, Dye, Settsu, and Burrows;

FURTHER ORDERED that no other grounds are authorized for this *inter partes* review other than those specifically identified above; and

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FURTHER ORDERED that pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4, notice is hereby given of the institution of a trial; the trial will commence on the entry date of this decision.

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AO 120 (Rev. 08/10)

TO: Mail Stop 8 Director of the U.S. Patent and Trademark Office P.O. Box 1450 Alexandria, VA 22313-1450	REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK
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In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been filed in the U.S. District Court Eastern District of Texas, Tyler Division on the following

Trademarks or Patents. (the patent action involves 35 U.S.C. § 292.):

DOCKET NO. 6:15-cv-885	DATE FILED 10/5/2015	U.S. DISTRICT COURT Eastern District of Texas, Tyler Division
PLAINTIFF Realtime Data, LLC d/b/a IXO		DEFENDANT Apple, Inc.
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1 7,181,608	2/20/2007	Realtime Data, LLC d/b/a IXO
2 8,090,936	1/3/2012	Realtime Data, LLC d/b/a IXO
3 8,880,862	11/4/2014	Realtime Data, LLC d/b/a IXO
4 7,415,530	8/19/2008	Realtime Data, LLC d/b/a IXO
5		

In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY <input type="checkbox"/> Amendment <input type="checkbox"/> Answer <input type="checkbox"/> Cross Bill <input type="checkbox"/> Other Pleading		
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK	
1			
2			
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4			
5			

In the above—entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT

CLERK	(BY) DEPUTY CLERK	DATE
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Copy 1—Upon initiation of action, mail this copy to Director Copy 3—Upon termination of action, mail this copy to Director
 Copy 2—Upon filing document adding patent(s), mail this copy to Director Copy 4—Case file copy

AO 120 (Rev. 08/10)

TO: Mail Stop 8 Director of the U.S. Patent and Trademark Office P.O. Box 1450 Alexandria, VA 22313-1450	REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK
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In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been filed in the U.S. District Court _____ for the Eastern District of Texas _____ on the following

Trademarks or Patents. (the patent action involves 35 U.S.C. § 292.);

DOCKET NO. 4:14-cv-00827	DATE FILED 12/19/2014	U.S. DISTRICT COURT for the Eastern District of Texas
PLAINTIFF Realtime Data, LLC d/b/a IXO		DEFENDANT Microsoft Corporation, Dell Incorporated, Hewlett-Packard Company
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1 7,181,608	2/20/2007	Realtime Data, LLC
2 8,090,936	1/3/2012	Realtime Data, LLC
3 8,880,862	11/4/2014	Realtime Data, LLC
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5		

In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY <input type="checkbox"/> Amendment <input type="checkbox"/> Answer <input type="checkbox"/> Cross Bill <input type="checkbox"/> Other Pleading		
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK	
1			
2			
3			
4			
5			

In the above—entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT

CLERK	(BY) DEPUTY CLERK	DATE
-------	-------------------	------

Copy 1—Upon initiation of action, mail this copy to Director Copy 3—Upon termination of action, mail this copy to Director
 Copy 2—Upon filing document adding patent(s), mail this copy to Director Copy 4—Case file copy



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
09/776,267	02/02/2001	James J. Fallon	2855.0040003

CONFIRMATION NO. 9730

POA ACCEPTANCE LETTER

26111
STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.
1100 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005



Date Mailed: 01/26/2011

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 01/07/2011.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

/sleutchit/

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101



UNITED STATES PATENT AND TRADEMARK OFFICE

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Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
09/776,267	02/02/2001	James J. Fallon	8011-15

CONFIRMATION NO. 9730

POWER OF ATTORNEY NOTICE

1473
ROPES & GRAY LLP
PATENT DOCKETING 39/361
1211 AVENUE OF THE AMERICAS
NEW YORK, NY 10036-8704



Date Mailed: 01/26/2011

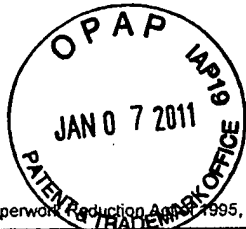
NOTICE REGARDING CHANGE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 01/07/2011.

- The Power of Attorney to you in this application has been revoked by the assignee who has intervened as provided by 37 CFR 3.71. Future correspondence will be mailed to the new address of record(37 CFR 1.33).

/sleutchit/

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101



09776267

JFW

PTO/SB/80 (11-08)

Approved for use through 11/30/2011. OMB 0651-0035
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

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POWER OF ATTORNEY TO PROSECUTE APPLICATIONS BEFORE THE USPTO

I hereby revoke all previous powers of attorney given in the application identified in the attached statement under 37 CFR 3.73(b).

I hereby appoint:

Practitioners associated with the Customer Number: 26111

OR

Practitioner(s) named below (if more than ten patent practitioners are to be named, then a customer number must be used):

Name	Registration Number	Name	Registration Number

as attorney(s) or agent(s) to represent the undersigned before the United States Patent and Trademark Office (USPTO) in connection with any and all patent applications assigned only to the undersigned according to the USPTO assignment records or assignment documents attached to this form in accordance with 37 CFR 3.73(b).

Please change the correspondence address for the application identified in the attached statement under 37 CFR 3.73(b) to:

The address associated with Customer Number: 26111

OR

<input type="checkbox"/> Firm or Individual Name			
Address			
City	State	Zip	
Country			
Telephone	Email		

Assignee Name and Address:
Realtime Data LLC DBA IXO
11 Wampus Close
Armonk, New York 10504

A copy of this form, together with a statement under 37 CFR 3.73(b) (Form PTO/SB/96 or equivalent) is required to be filed in each application in which this form is used. The statement under 37 CFR 3.73(b) may be completed by one of the practitioners appointed in this form if the appointed practitioner is authorized to act on behalf of the assignee, and must identify the application in which this Power of Attorney is to be filed.

SIGNATURE of Assignee of Record

The individual whose signature and title is supplied below is authorized to act on behalf of the assignee

Signature		Date	9/13/10
Name	James J. Fallon	Telephone	(914) 438-0233
Title	Chairman		

This collection of information is required by 37 CFR 1.31, 1.32 and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.



STATEMENT UNDER 37 CFR 3.73(b)

Atty. Docket No. 2855.0040003

Applicant/Patent Owner: Fallon et al.

Application No./Patent No.: 7,181,608 B2 Filed/Issue Date: February 20, 2007

Titled: Systems and Methods For Accelerated Loading Of Operating Systems and Application Programs

REALTIME DATA, LLC, a limited liability company

(Name of Assignee) (Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

states that it is:

- 1. [X] the assignee of the entire right, title, and interest in;
2. [] an assignee of less than the entire right, title, and interest in (The extent (by percentage) of its ownership interest is %); or
3. [] the assignee of an undivided interest in the entirety of (a complete assignment from one of the joint inventors was made)

the patent application/patent identified above, by virtue of either:

A. [X] An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel 011797, Frame 0735, or for which a copy therefore is attached.

OR

B. [] A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as follows:

1. From: To:

The document was recorded in the United States Patent and Trademark Office at Reel, Frame, or for which a copy thereof is attached.

2. From: To:

The document was recorded in the United States Patent and Trademark Office at Reel, Frame, or for which a copy thereof is attached.

3. From: To:

The document was recorded in the United States Patent and Trademark Office at Reel, Frame, or for which a copy thereof is attached.

[] Additional documents in the chain of title are listed on a supplemental sheet(s).

[X] As required by 37 CFR 3.73(b)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.

[NOTE: A separate copy (i.e., a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

Signature (Handwritten signature)

Date: 1/2/2011

Michael V. Messinger, Reg. No. 37,575

Attorney for Patentees

Printed or Typed Name

Title

This collection of information is required by 37 CFR 3.73(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
09/776,267	02/02/2001	James J. Fallon	8011-15

CONFIRMATION NO. 9730

POA ACCEPTANCE LETTER



1473
ROPES & GRAY LLP
PATENT DOCKETING 39/361
1211 AVENUE OF THE AMERICAS
NEW YORK, NY 10036-8704

Date Mailed: 04/02/2008

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 03/24/2008.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

/gbien-aime/

Office of Initial Patent Examination (571) 272-4000 or 1-800-PTO-9199



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
09/776,267	02/02/2001	James J. Fallon	8011-15

CONFIRMATION NO. 9730

POWER OF ATTORNEY NOTICE

22150
F. CHAU & ASSOCIATES, LLC
130 WOODBURY ROAD
WOODBURY, NY 11797



Date Mailed: 04/02/2008

NOTICE REGARDING CHANGE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 03/24/2008.

- The Power of Attorney to you in this application has been revoked by the assignee who has intervened as provided by 37 CFR 3.71. Future correspondence will be mailed to the new address of record(37 CFR 1.33).

/gbien-aime/

Office of Initial Patent Examination (571) 272-4000 or 1-800-PTO-9199

Electronic Acknowledgement Receipt

EFS ID:	3039284
Application Number:	09776267
International Application Number:	
Confirmation Number:	9730
Title of Invention:	SYSTEMS AND METHODS FOR ACCELERATED LOADING OF OPERATING SYSTEMS AND APPLICATION PROGRAMS
First Named Inventor/Applicant Name:	James J. Fallon
Customer Number:	22150
Filer:	Richard DeGive Allison/CindyAnne Holmes
Filer Authorized By:	Richard DeGive Allison
Attorney Docket Number:	8011-15
Receipt Date:	24-MAR-2008
Filing Date:	02-FEB-2001
Time Stamp:	12:10:51
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
------------------------	----

File Listing:

Document Number	Document Description	File Name	File Size(Bytes) /Message Digest	Multi Part /.zip	Pages (if appl.)
1	Power of Attorney	801115_Power.pdf	368805 <small>6958e36edcae66d1683ebb5928b6c709cb81b713</small>	no	2

Warnings:

Information:

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

PATENT APPLICATION

Applicants : James J. Fallon et. al.
Application No. : 09/776,267 Confirmation No. : 9730
Filed : February 2, 2001
For : SYSTEMS AND METHODS FOR ACCELERATED
LOADING OF OPERATING SYSTEMS AND
APPLICATION PROGRAMS
Art Unit : 2115
Examiner : Suresh Suryawanshi

Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

REVOCATION OF POWER OF ATTORNEY
AND NEW POWER OF ATTORNEY

Sir:

Realtime Data LLC, assignee of the above-identified United States patent application by virtue of an assignment from the inventors to Realtime Data LLC, recorded at Reel 11797, Frames 735-736, hereby revokes all powers of attorney heretofore existing in said United States patent application, and hereby appoints the attorneys and agents associated with Customer No. 1473 as its principal attorneys and agents of record in said United States patent application, with full power of substitution and revocation including the power to appoint associate attorneys and to revoke their powers, and to transact all business in the Patent and Trademark Office pertaining to said patent application.

The Patent and Trademark Office is respectfully requested to direct all correspondence to:

Customer No. 1473

and to direct all telephone calls to:

Jeffrey H. Ingerman
Tel.: (212) 596-9000.

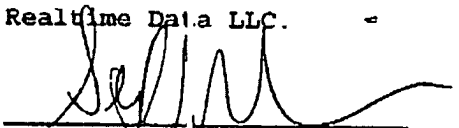
The undersigned hereby certifies that the evidentiary documents have been reviewed and, to the best of the undersigned's knowledge and belief, title is in assignee.

The undersigned hereby declares that all statements made herein of his own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Realtime Data LLC.

3/11/08
Date

By:



Stephen J. McErlain
President



APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/776,267	02/20/2007	7181608	8011-15	9730

22150 7590 01/31/2007
F. CHAU & ASSOCIATES, LLC
130 WOODBURY ROAD
WOODBURY, NY 11797

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment is 223 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site <http://pair.uspto.gov> for additional applicants):

James J. Fallon, Armonk, NY;
John Buck, Oceanside, NY;
Paul F. Pickel, Bethpage, NY;
Stephen J. McErlain, New York, NY;

01-11-07

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: **Mail** Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or **Fax** (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

22150 7590 10/16/2006

F. CHAU & ASSOCIATES, LLC
130 WOODBURY ROAD
WOODBURY, NY 11797



Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

01/11/2007 BARRAH2 00000008 061075 09776267

01 FC:2501 700.00 DA
02 FC:1504 300.00 DA
03 FC:8001 45.00 DA

Form with fields for Depositor's name, Signature, and Date.

Table with columns: APPLICATION NO., FILING DATE, FIRST NAMED INVENTOR, ATTORNEY DOCKET NO., CONFIRMATION NO.

TITLE OF INVENTION: SYSTEMS AND METHODS FOR ACCELERATED LOADING OF OPERATING SYSTEMS AND APPLICATION PROGRAMS

Table with columns: APPLN. TYPE, SMALL ENTITY, ISSUE FEE DUE, PUBLICATION FEE DUE, PREV. PAID ISSUE FEE, TOTAL FEE(S) DUE, DATE DUE

Table with columns: EXAMINER, ART UNIT, CLASS-SUBCLASS

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
 Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
 "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. Use of a Customer Number is required.

2. For printing on the patent front page, list
(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

Fish & Neave IP Group
of Ropes & Gray LLP

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE: Realtime Data LLC
(B) RESIDENCE: (CITY and STATE OR COUNTRY): New York, NY

Please check the appropriate assignee category or categories (will not be printed on the patent): Individual Corporation or other private group entity Government

4a. The following fee(s) are submitted:

Issue Fee
 Publication Fee (No small entity discount permitted)
 Advance Order - # of Copies 15

4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)

A check is enclosed.
 Payment by credit card. Form PTO-2038 is attached.
 The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number 06-1075 (enclose an extra copy of this form).

5. Change In Entity Status (from status indicated above)

a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27. b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

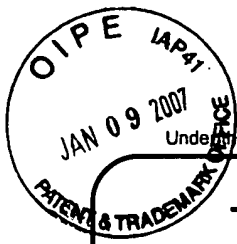
Authorized Signature: [Signature]
Typed or printed name: Jeffrey D. Mullen

Date: 1/9/07
Registration No. 52,056

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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EV620761223US



TRANSMITTAL FORM <i>(to be used for all correspondence after initial filing)</i>	Application Number	09/776,267
	Filing Date	February 2, 2001
	First Named Inventor	James J. Fallon
	Art Unit	2115
	Examiner Name	Suresh Suryawanshi
Total Number of Pages in This Submission	Attorney Docket Number	8011-15

ENCLOSURES <i>(Check all that apply)</i>				
<input type="checkbox"/> Fee Transmittal Form <input type="checkbox"/> Fee Attached <input type="checkbox"/> Amendment/Reply <input type="checkbox"/> After Final <input type="checkbox"/> Affidavits/declaration(s) <input type="checkbox"/> Extension of Time Request <input type="checkbox"/> Express Abandonment Request <input type="checkbox"/> Information Disclosure Statement <input type="checkbox"/> Certified Copy of Priority Document(s) <input type="checkbox"/> Reply to Missing Parts/ Incomplete Application <input type="checkbox"/> Reply to Missing Parts under 37 CFR 1.52 or 1.53	<input checked="" type="checkbox"/> Drawings (13 Replacement Sheets) <input type="checkbox"/> Licensing-related Papers <input type="checkbox"/> Petition <input type="checkbox"/> Petition to Convert to a Provisional Application <input type="checkbox"/> Power of Attorney, Revocation <input type="checkbox"/> Change of Correspondence Address <input type="checkbox"/> Terminal Disclaimer <input type="checkbox"/> Request for Refund <input type="checkbox"/> CD, Number of CD(s) _____ <input type="checkbox"/> Landscape Table on CD	<input type="checkbox"/> After Allowance Communication to TC <input type="checkbox"/> Appeal Communication to Board of Appeals and Interferences <input type="checkbox"/> Appeal Communication to TC (Appeal Notice, Brief, Reply Brief) <input type="checkbox"/> Proprietary Information <input type="checkbox"/> Status Letter <input checked="" type="checkbox"/> Other Enclosure(s) (please identify below) 1. Submission of Formal Drawings; 2. Thirteen Formal Drawings; 3. Issue Fee Transmittal; and 4. Return postcard.		
<table border="1" style="width: 100%;"> <tr> <td style="width: 20%;">Remarks</td> <td> Director of the United States Patent and Trademark Office is hereby authorized to charge payment of any fees required in connection with this filing to Deposit Account No. 06-1075 (Order No. 103532-0002). A duplicate copy of this Statement is transmitted herewith. </td> </tr> </table>			Remarks	Director of the United States Patent and Trademark Office is hereby authorized to charge payment of any fees required in connection with this filing to Deposit Account No. 06-1075 (Order No. 103532-0002). A duplicate copy of this Statement is transmitted herewith.
Remarks	Director of the United States Patent and Trademark Office is hereby authorized to charge payment of any fees required in connection with this filing to Deposit Account No. 06-1075 (Order No. 103532-0002). A duplicate copy of this Statement is transmitted herewith.			

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT			
Firm Name	Fish & Neave IP Group Ropes & Gray, LLP		
Signature			
Printed name	Jeffrey D. Mullen		
Date	January 9, 2007	Reg. No.	52,056

CERTIFICATE OF EXPRESS MAILING EXPRESS MAIL LABEL NO. EV620761223US			
I hereby certify that this correspondence is being facsimile transmitted to the USPTO or deposited with the United States Postal Service with sufficient postage as express mail in an envelope addressed to: Mail Stop: Issue Fee, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on the date shown below:			
Signature			
Typed or printed name	Isatta B. Smith	Date	1/9/07



PATENTS
8011-15

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

PATENT APPLICATION

Applicants : James J. Fallon et al.
 Application No. : 09/776,267 Confirmation No. : 9730
 Filed : February 2, 2001
 For : SYSTEMS AND METHODS FOR ACCELERATED
 LOADING OF OPERATING SYSTEMS AND
 APPLICATION PROGRAMS
 Group Art Unit : 2115
 Examiner : Suresh Suryawanshi

New York, New York 10020
 January 9, 2007

Mail Stop ISSUE FEE
 Hon. Commissioner for Patents
 P.O. Box 1450
 Alexandria, Virginia 22313-1450

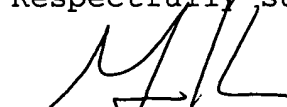
SUBMISSION OF FORMAL DRAWINGS

Sir:

Pursuant to 37 C.F.R. § 1.85, and in accordance with the requirement in the October 16, 2006 Notice of Allowability, applicants herewith furnish thirteen (13) sheets of formal drawings, to be substituted for the thirteen (13) sheets of informal drawings previously filed.

The Director is hereby authorized to charge payment of any additional fees required in connection with the paper(s) transmitted herewith, or to credit any overpayment of same, to Deposit Account No. 06-1075. A duplicate copy of this transmittal letter is transmitted herewith.

Respectfully submitted,



Jeffrey D. Mullen
Reg. No. 52,056
Agent for Applicant
FISH & NEAVE IP GROUP
ROPES & GRAY LLP
Customer No. 1473
1251 Avenue of the Americas
New York, New York 10020-1105
Tel.: (212) 596-9000

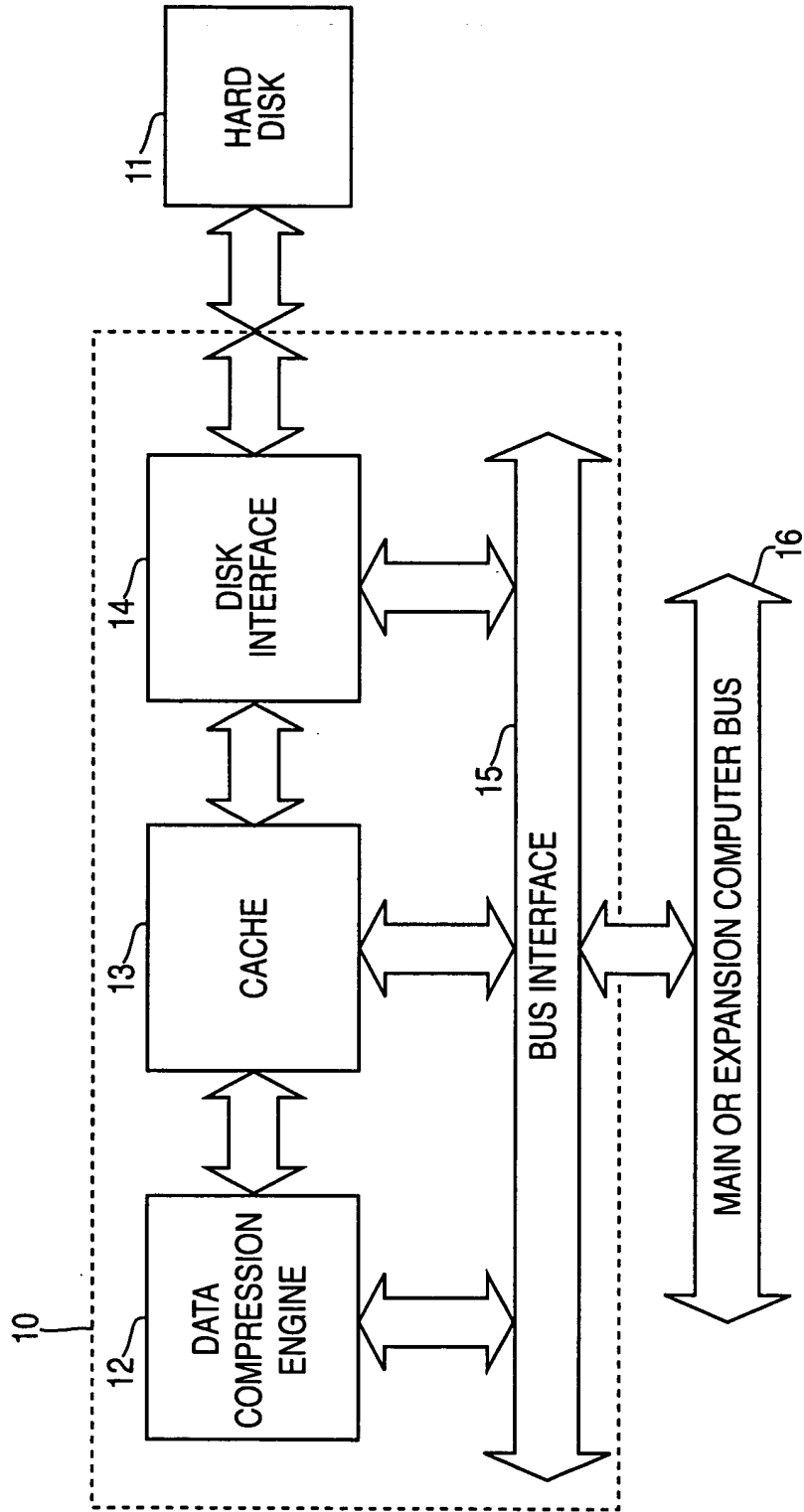


FIG. 1

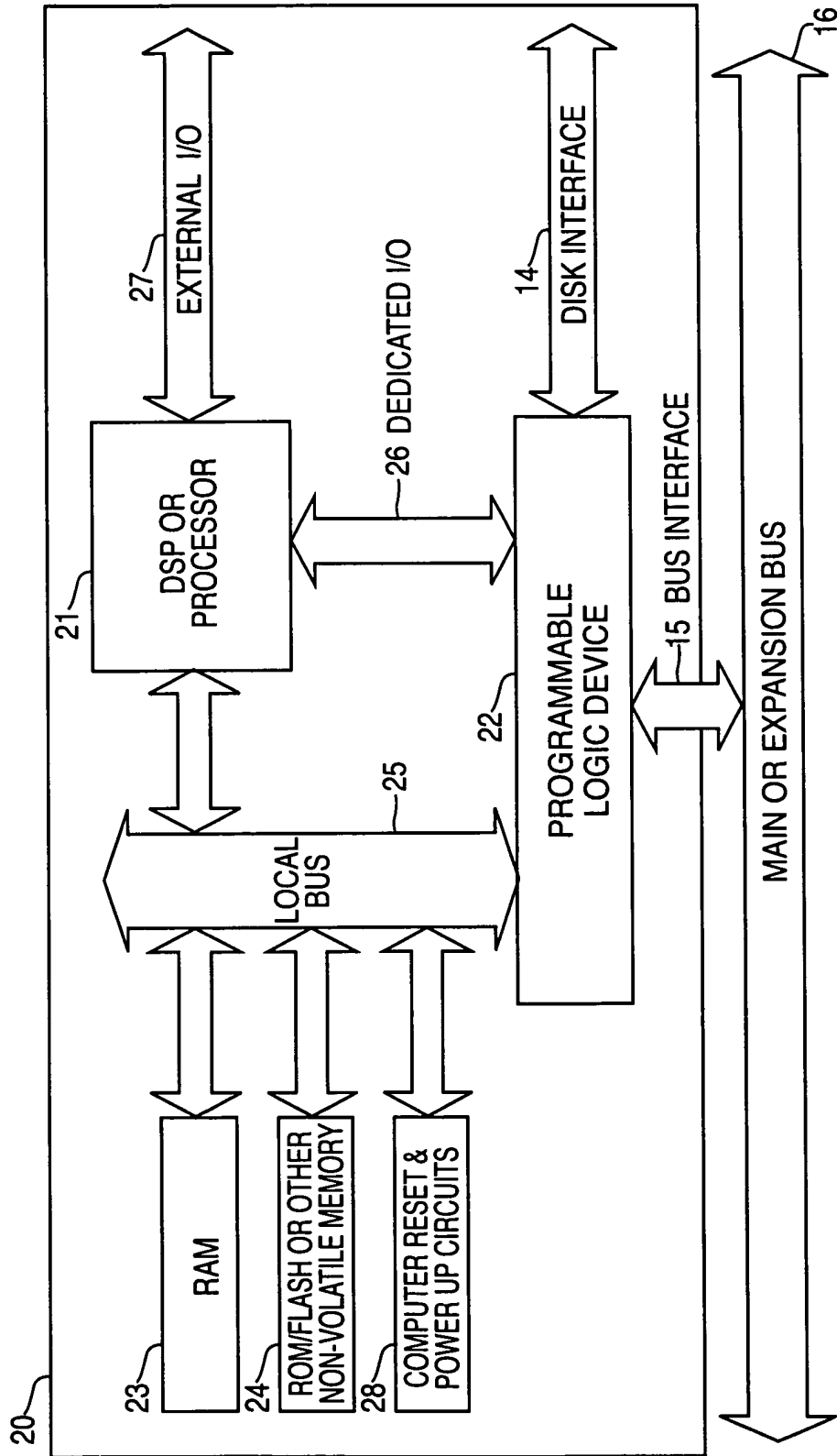


FIG. 2

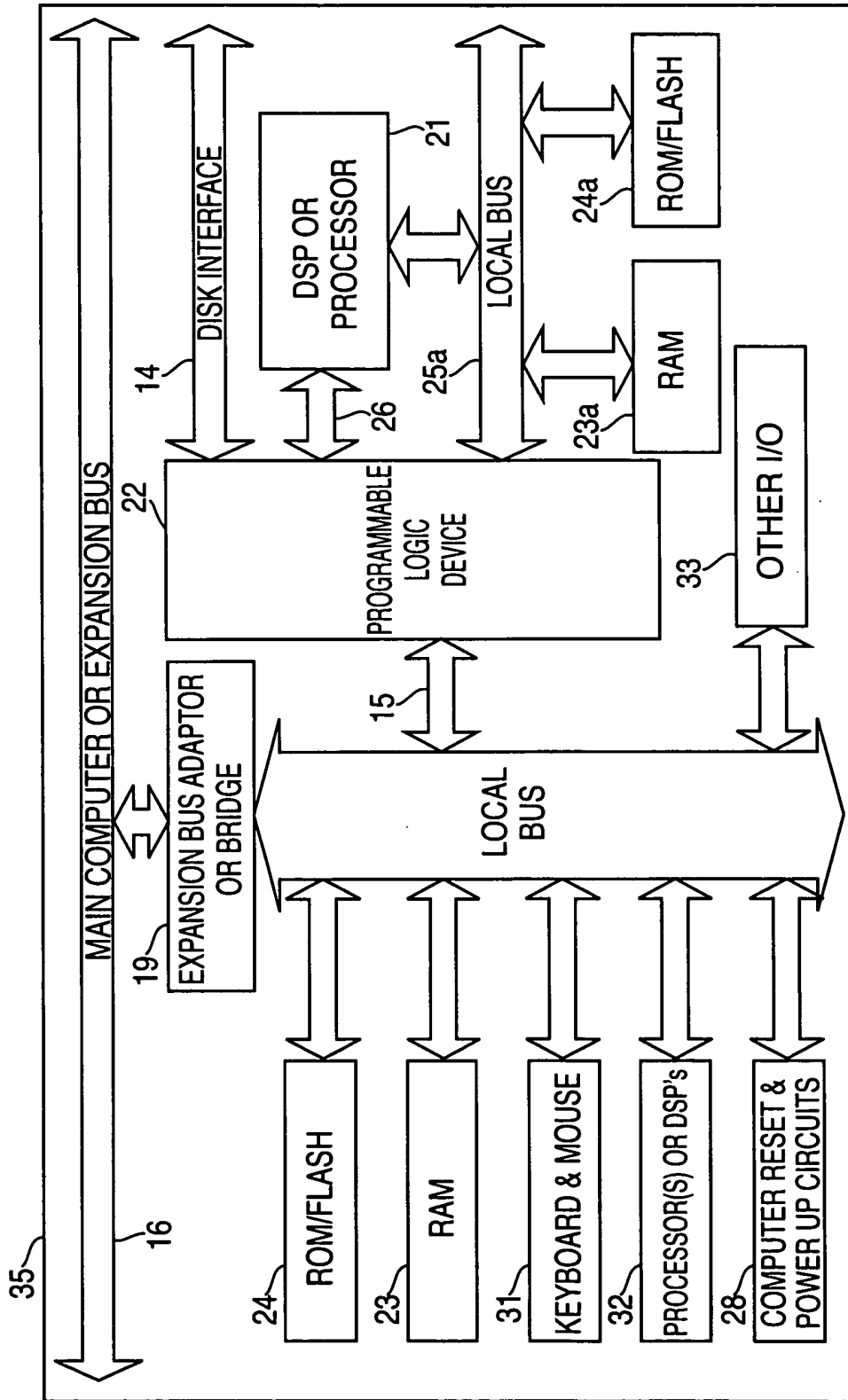


FIG. 3

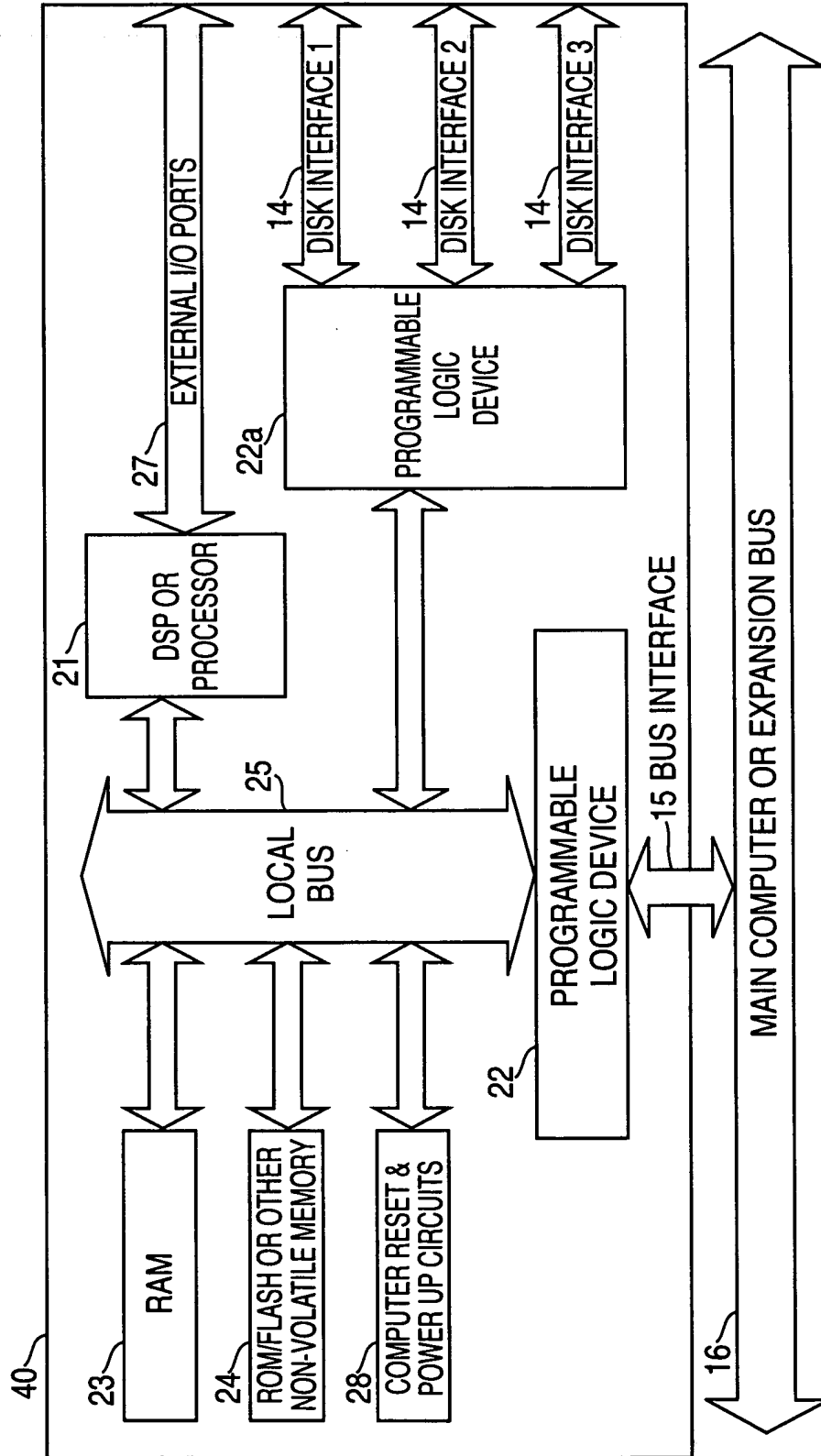


FIG. 4

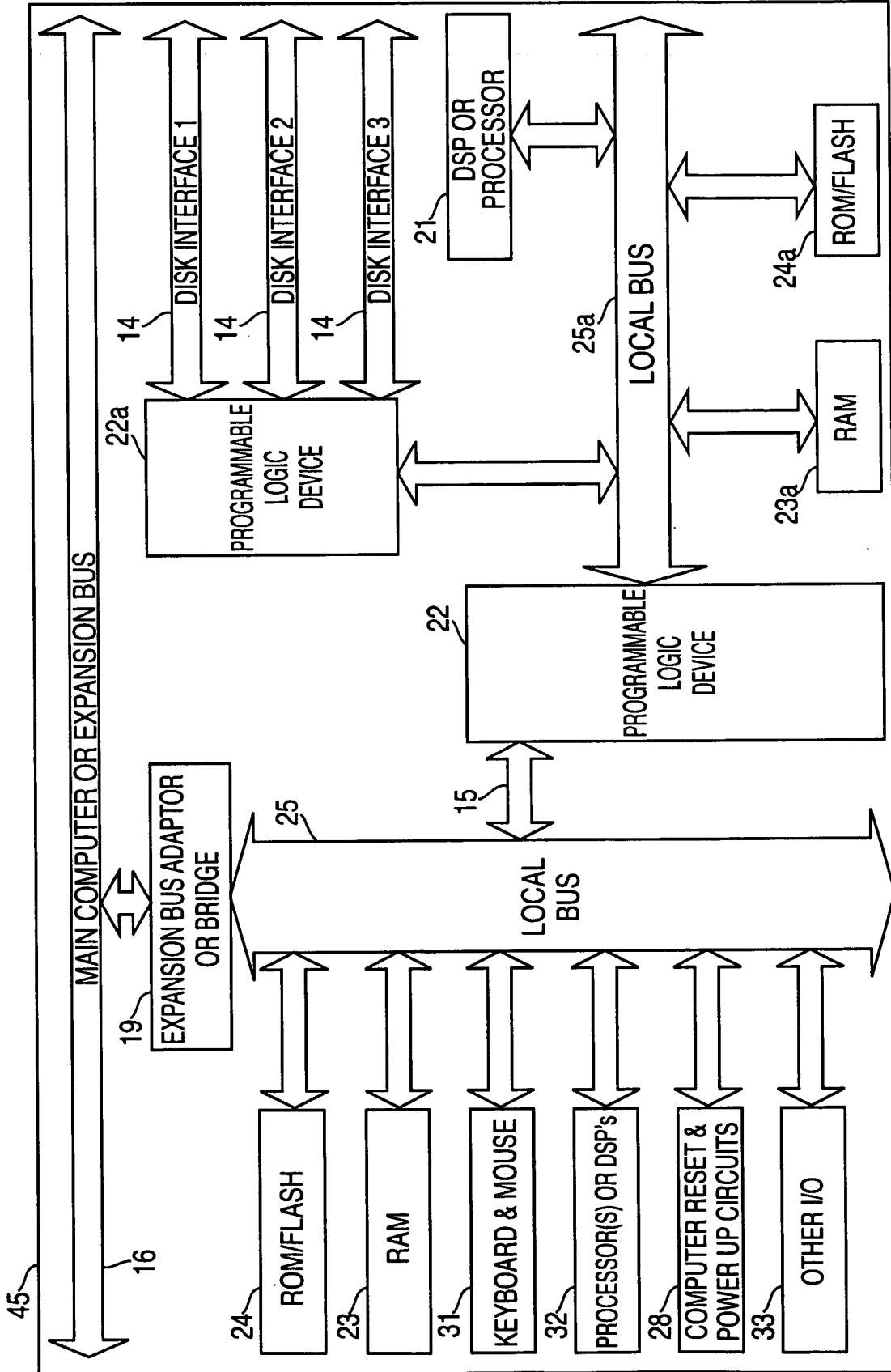


FIG. 5

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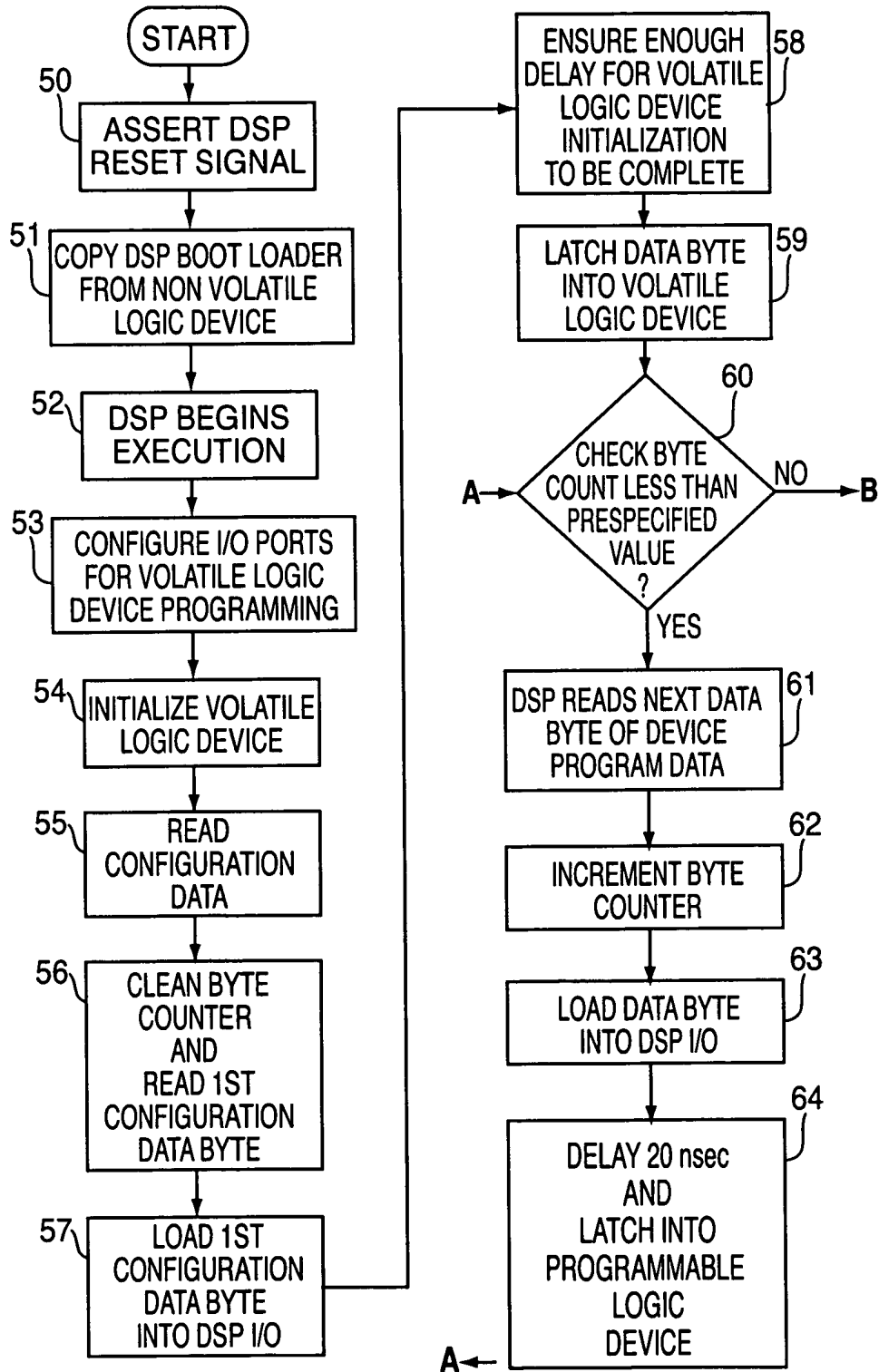


FIG. 6a

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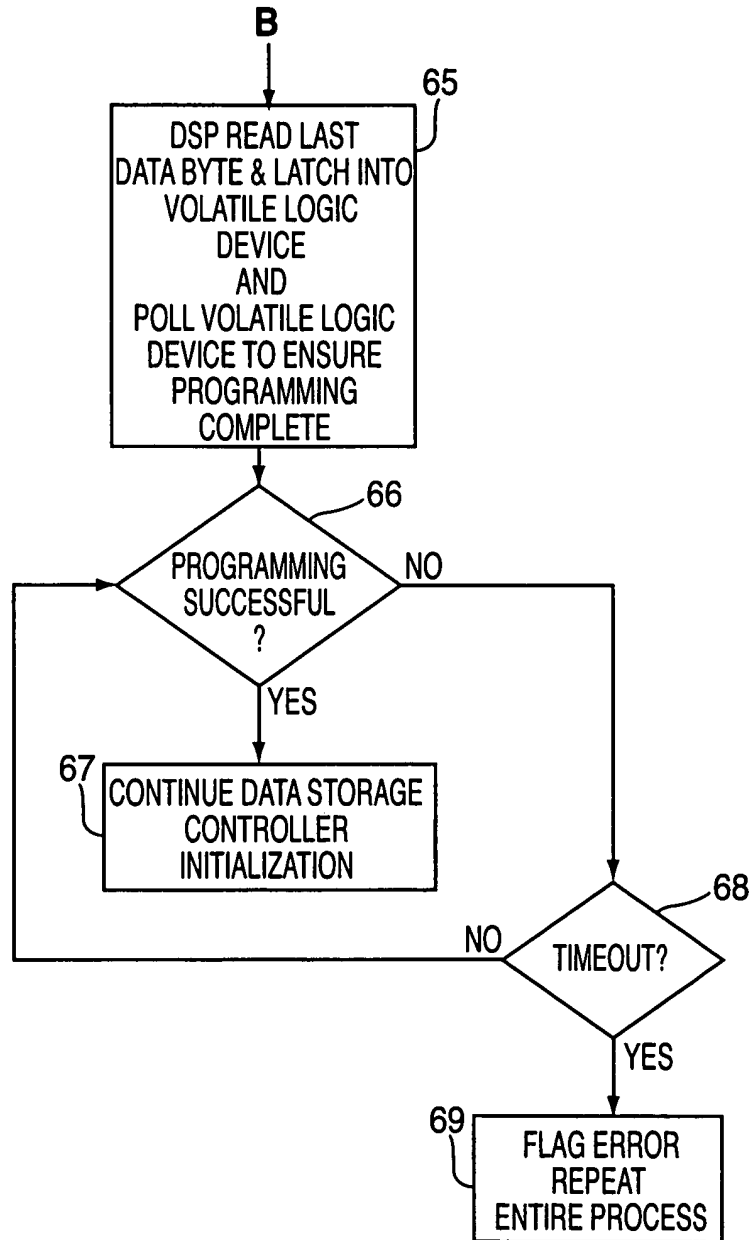


FIG. 6b

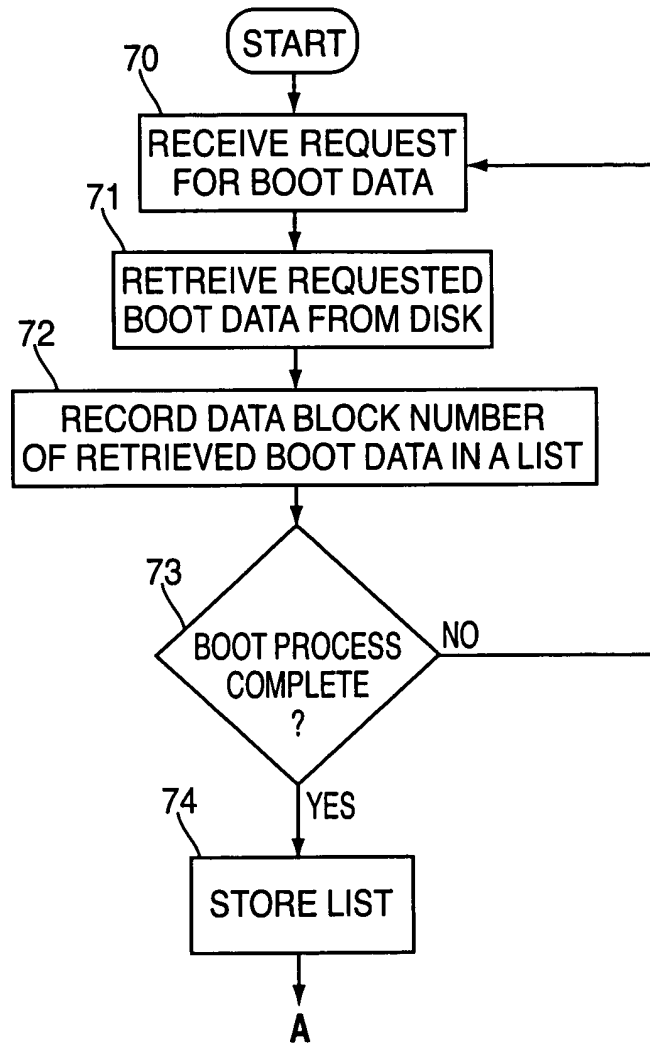


FIG. 7a

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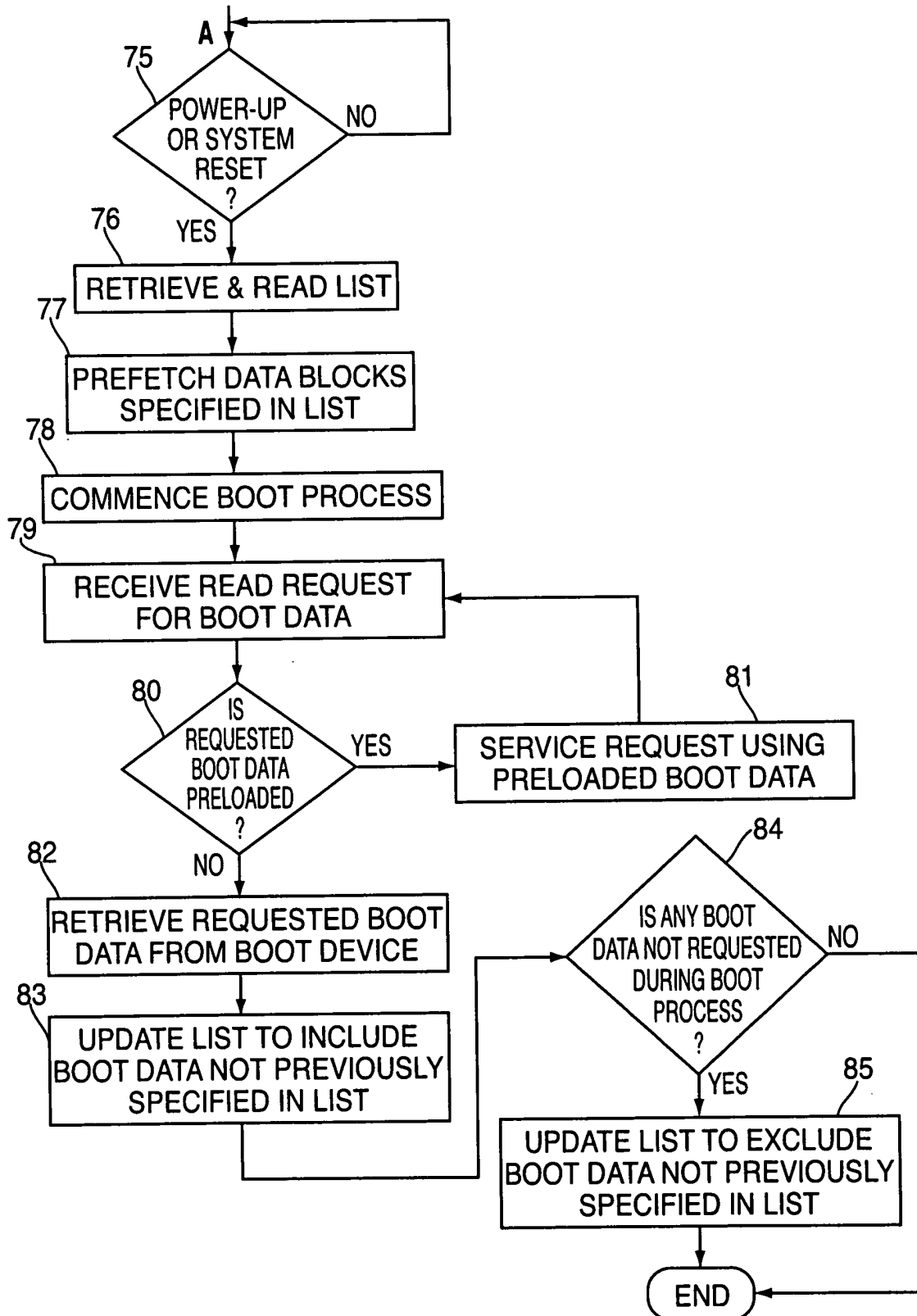


FIG. 7b

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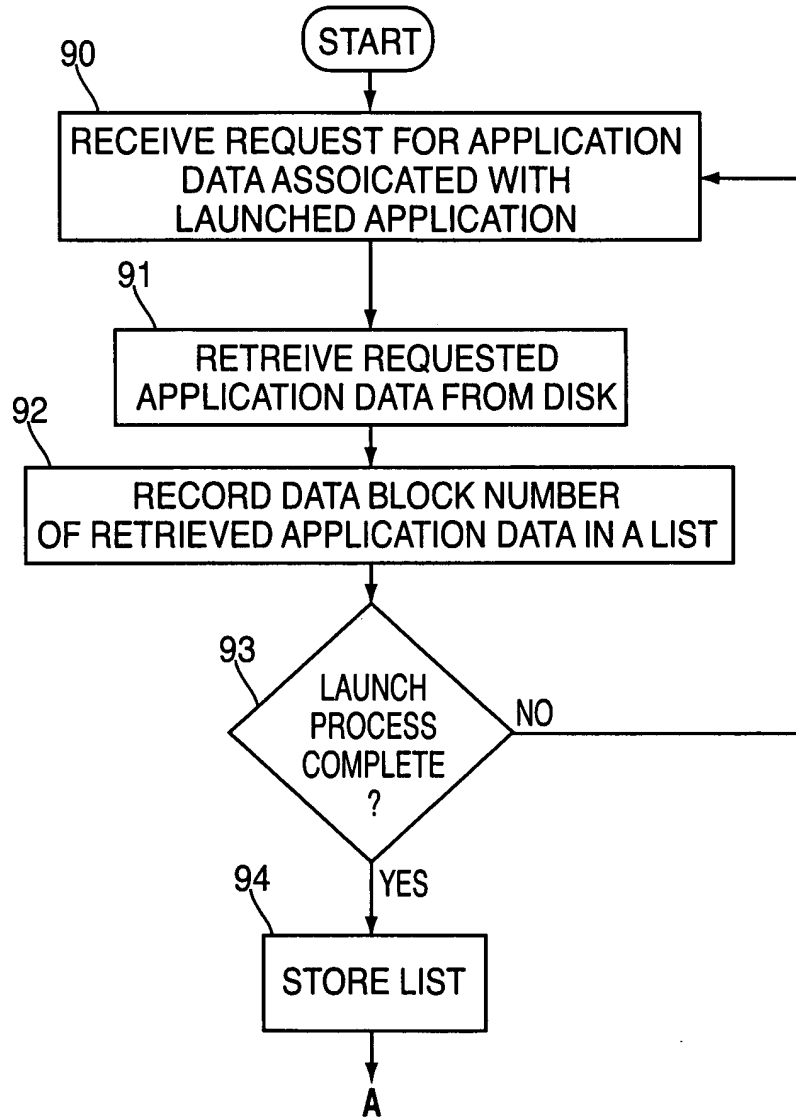


FIG. 8a

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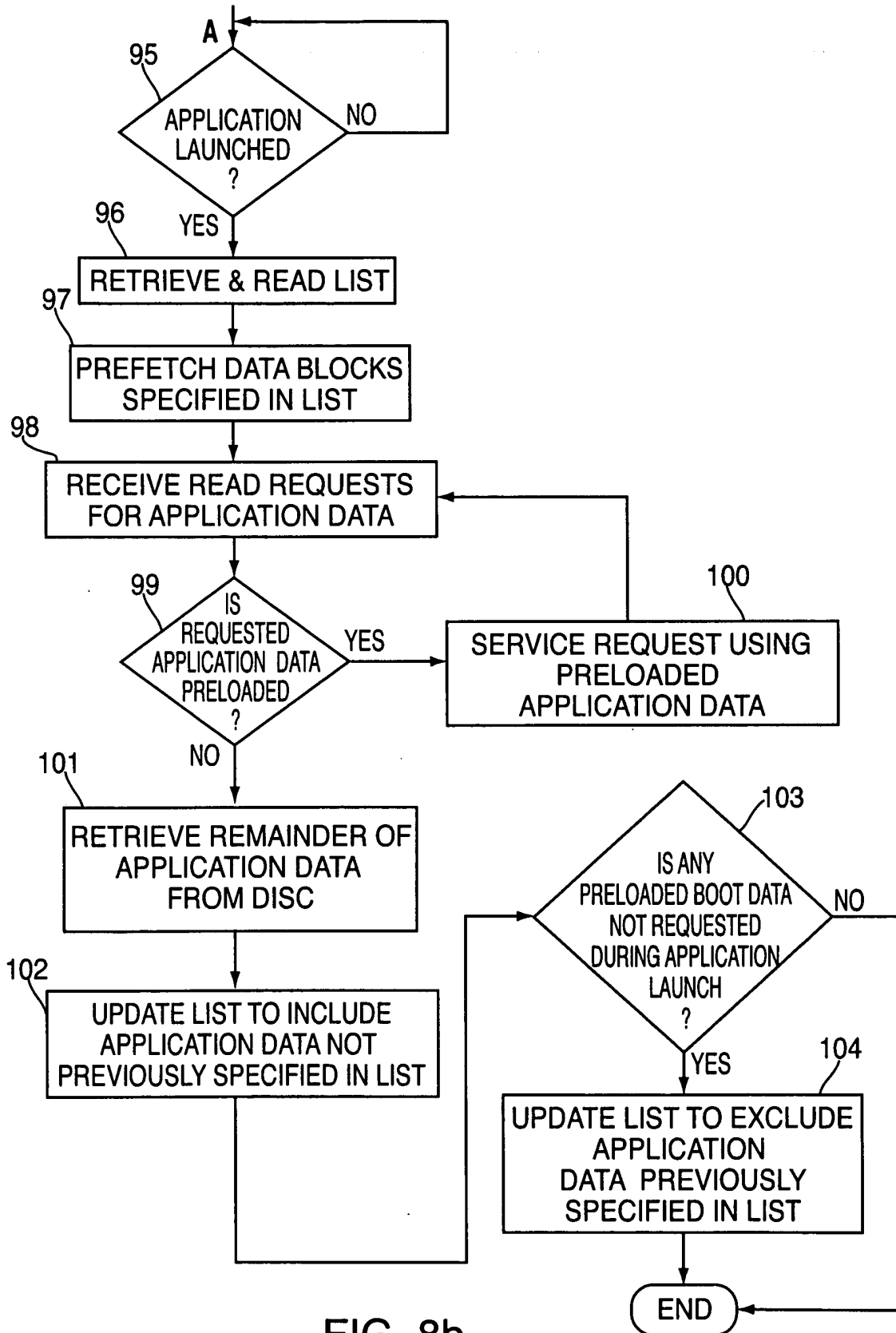


FIG. 8b

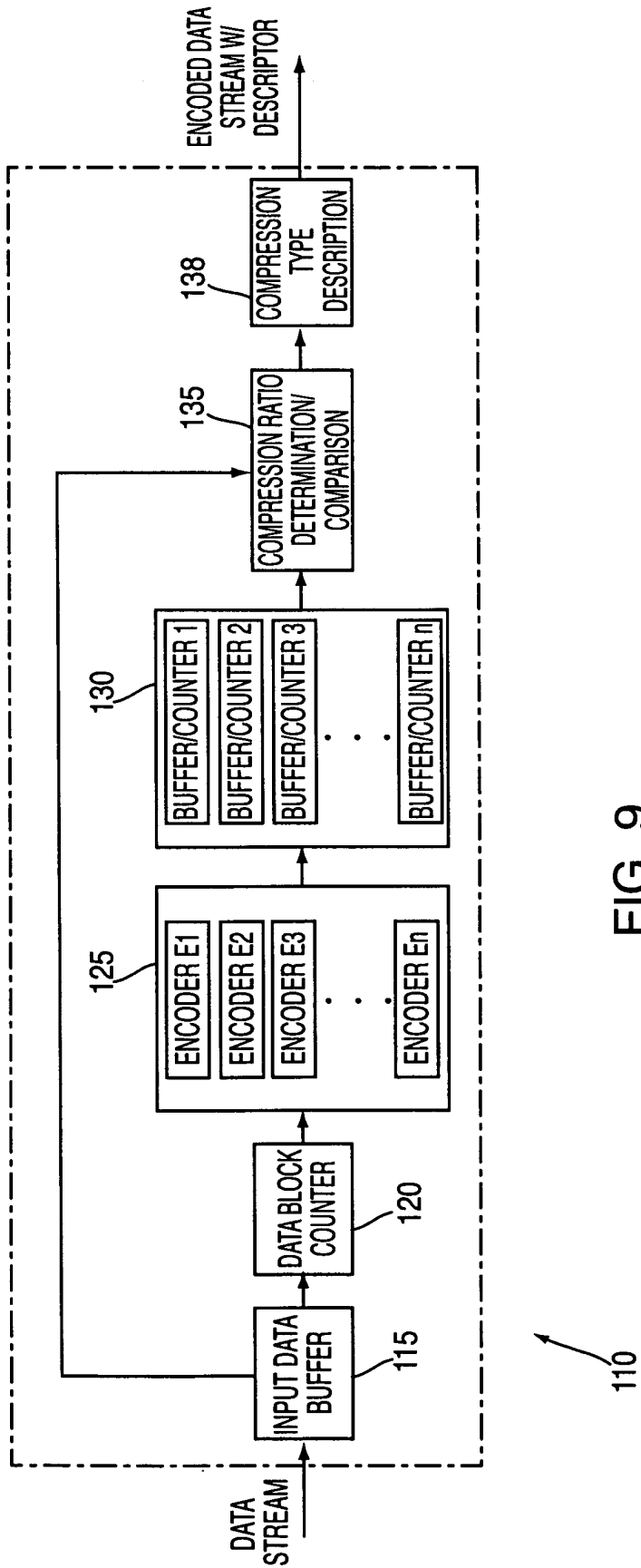


FIG. 9

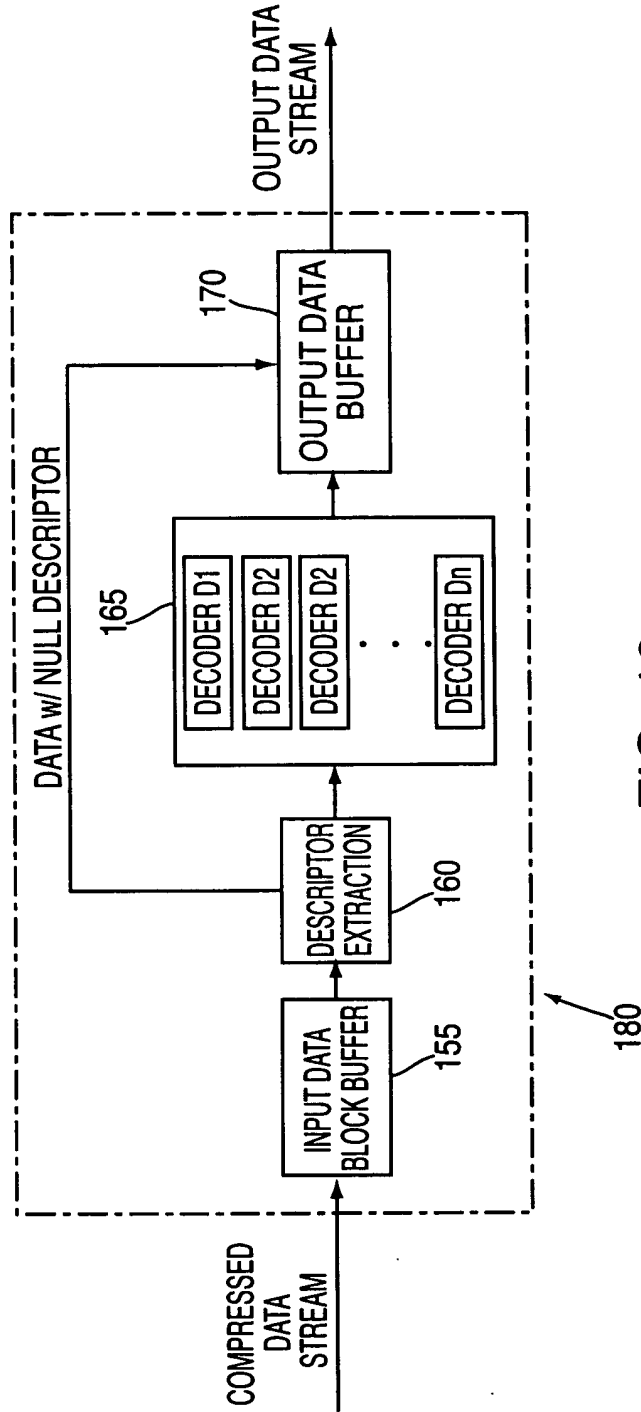


FIG. 10



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NOTICE OF ALLOWANCE AND FEE(S) DUE

22150 7590 10/16/2006

F. CHAU & ASSOCIATES, LLC
130 WOODBURY ROAD
WOODBURY, NY 11797

EXAMINER: SURYAWANSHI, SURESH
ART UNIT: 2115
PAPER NUMBER: [blank]

DATE MAILED: 10/16/2006

Table with 5 columns: APPLICATION NO., FILING DATE, FIRST NAMED INVENTOR, ATTORNEY DOCKET NO., CONFIRMATION NO.

TITLE OF INVENTION: SYSTEMS AND METHODS FOR ACCELERATED LOADING OF OPERATING SYSTEMS AND APPLICATION PROGRAMS

Table with 7 columns: APPLN. TYPE, SMALL ENTITY, ISSUE FEE DUE, PUBLICATION FEE DUE, PREV. PAID ISSUE FEE, TOTAL FEE(S) DUE, DATE DUE

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

- A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.
B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

- A. Pay TOTAL FEE(S) DUE shown above, or
B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PART B - FEE(S) TRANSMITTAL

**Complete and send this form, together with applicable fee(s), to: Mail Mail Stop ISSUE FEE
 Commissioner for Patents
 P.O. Box 1450
 Alexandria, Virginia 22313-1450
 or Fax (571)-273-2885**

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

22150 7590 10/16/2006

F. CHAU & ASSOCIATES, LLC
 130 WOODBURY ROAD
 WOODBURY, NY 11797

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/776,267	02/02/2001	James J. Fallon	8011-15	9730

TITLE OF INVENTION: SYSTEMS AND METHODS FOR ACCELERATED LOADING OF OPERATING SYSTEMS AND APPLICATION PROGRAMS

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	YES	\$700	\$300	\$0	\$1000	01/16/2007

EXAMINER	ART UNIT	CLASS-SUBCLASS
SURYAWANSHI, SURESH	2115	713-002000

<p>1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).</p> <p><input type="checkbox"/> Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.</p> <p><input type="checkbox"/> "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. Use of a Customer Number is required.</p>	<p>2. For printing on the patent front page, list</p> <p>(1) the names of up to 3 registered patent attorneys or agents OR, alternatively, _____ 1</p> <p>(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed. _____ 2</p> <p>_____ 3</p>
--	---

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE _____ (B) RESIDENCE: (CITY and STATE OR COUNTRY) _____

Please check the appropriate assignee category or categories (will not be printed on the patent) : Individual Corporation or other private group entity Government

<p>4a. The following fee(s) are submitted:</p> <p><input type="checkbox"/> Issue Fee</p> <p><input type="checkbox"/> Publication Fee (No small entity discount permitted)</p> <p><input type="checkbox"/> Advance Order - # of Copies _____</p>	<p>4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)</p> <p><input type="checkbox"/> A check is enclosed.</p> <p><input type="checkbox"/> Payment by credit card. Form PTO-2038 is attached.</p> <p><input type="checkbox"/> The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).</p>
---	--

5. Change in Entity Status (from status indicated above)

a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27. b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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Table with 5 columns: APPLICATION NO., FILING DATE, FIRST NAMED INVENTOR, ATTORNEY DOCKET NO., CONFIRMATION NO.
Row 1: 09/776,267, 02/02/2001, James J. Fallon, 8011-15, 9730
Row 2: 22150, 7590, 10/16/2006, [EXAMINER: SURYAWANSHI, SURESH], [ART UNIT: 2115, PAPER NUMBER]
Text: F. CHAU & ASSOCIATES, LLC, 130 WOODBURY ROAD, WOODBURY, NY 11797
DATE MAILED: 10/16/2006

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 266 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 266 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

Notice of Allowability	Application No.	Applicant(s)	
	09/776,267	FALLON ET AL.	
	Examiner	Art Unit	
	Suresh K. Suryawanshi	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. This communication is responsive to amendments filed on 8/14/06.
2. The allowed claim(s) is/are 1,2,4-7,13,15 and 17-39.
3. Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 - a) All b) Some* c) None of the:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

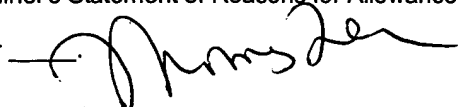
* Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

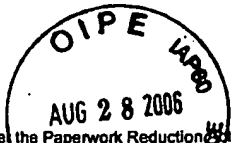
4. A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.
5. CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
 - (a) including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
 - 1) hereto or 2) to Paper No./Mail Date 2/14/06.
 - (b) including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

- | | |
|--|---|
| <ol style="list-style-type: none"> 1. <input type="checkbox"/> Notice of References Cited (PTO-892) 2. <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) 3. <input checked="" type="checkbox"/> Information Disclosure Statements (PTO/SB/08),
Paper No./Mail Date <u>See Continuation Sheet</u> 4. <input type="checkbox"/> Examiner's Comment Regarding Requirement for Deposit of Biological Material | <ol style="list-style-type: none"> 5. <input type="checkbox"/> Notice of Informal Patent Application 6. <input type="checkbox"/> Interview Summary (PTO-413),
Paper No./Mail Date _____. 7. <input type="checkbox"/> Examiner's Amendment/Comment 8. <input type="checkbox"/> Examiner's Statement of Reasons for Allowance 9. <input type="checkbox"/> Other  |
|--|---|

Continuation of Attachment(s) 3. Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date: 8/28/06,9/8/06,9/16/06.



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Substitute for form 1482A/PTO FOURTH SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)		Complete if known	
		Application Number	09/776,267
		Filing Date	February 2, 2001
		First Named Inventor	Fallon
		Art Unit	2115
		Examiner Name	Suresh K. Suryawanshi
Sheet	1	of	11
		Attorney Docket Number	8011-15

U.S. PATENT DOCUMENTS					
Examiner initials*	Cite No. ¹	Document Number Number - Kind Code ² (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Documents	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
SKS		4,127,518	11-28-1978	Coy et al.	
SKS		4,302,775	11-24-1981	Widergren et al.	
SKS		4,574,351	03-04-1986	Dang et al.	
SKS		4,593,324	06-03-1986	Ohkubo et al.	
SKS		4,682,150	07-21-1987	Mathes et al.	
SKS		4,730,348	03-08-1988	MacCrisken	
SKS		4,754,351	06-28-1988	Wright	
SKS		4,804,959	02-14-1989	Makansi et al.	
SKS		4,870,415	09-26-1989	Van Maren et al.	
SKS		4,872,009	10-03-1989	Tsukiyama et al.	
SKS		4,876,541	10-24-1989	Storer	
SKS		4,888,812	12-19-1989	Dinan et al.	
SKS		4,906,995	03-06-1990	Swanson	
SKS		4,929,946	05-29-1990	O'Brien et al.	
SKS		4,953,324	09-04-1990	Herrmann	
SKS		4,965,675	10-23-1990	Hori et al.	
SKS		5,028,922	07-02-1991	Huang	
SKS		5,045,848	09-03-1991	Fascenda	
SKS		5,045,852	09-03-1991	Mitchell et al.	
SKS		5,046,027	09-03-1991	Taafe et al.	
SKS		5,049,881	09-17-1991	Gibson et al.	
SKS		5,097,261	03-17-1992	Langdon, Jr. et al.	

Examiner Signature	Suresh K Suryawanshi	Date Considered	10/10/06
--------------------	----------------------	-----------------	----------

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.
 1 Applicant's unique citation designation number (optional). 2 Applicant is to place a check mark here if English language Translation is attached.
 This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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Substitute for form 1449A/PTO				Complete if known	
				Application Number	09/776,267
FOURTH SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Filing Date	February 2, 2001
				First Named Inventor	Fallon
				Art Unit	2115
				Examiner Name	Suresh K. Suryawanshi
(use as many sheets as necessary)				Attorney Docket Number	8011-15
Sheet	2	of	11		

Ses	5,113,522	05-12-1992	Dinwiddie, Jr. et al.	
Ses	5,121,342	06-09-1992	Szymborski	
Ses	5,150,430	09-22-1992	Chu	
Ses	5,159,336	10-27-1992	Rabin et al.	
Ses	5,175,543	12-29-1992	Lantz	
Ses	5,179,651	01-12-1993	Taaffe et al.	
Ses	5,191,431	03-02-1993	Hasegawa et al.	
Ses	5,204,756	04-20-1993	Chevion et al.	
Ses	5,212,742	05-18-1993	Normile et al.	
Ses	5,231,492	07-27-1993	Dangi et al.	
Ses	5,237,460	08-17-1993	Miller et al.	
Ses	5,237,675	08-17-1993	Hannon, Jr.	
Ses	5,243,341	09-07-1993	Seroussi et al.	
Ses	5,243,348	09-07-1993	Jackson	
Ses	5,247,638	09-21-1993	O'Brien et al.	
Ses	5,247,646	09-21-1993	Osterlund et al.	
Ses	5,263,168	11-16-1993	Toms et al.	
Ses	5,270,832	12-14-1993	Balkanski et al.	
Ses	5,287,420	02-15-1994	Barrett	
Ses	5,293,379	03-08-1994	Carr	
Ses	5,309,555	05-03-1994	Akins et al.	
Ses	5,355,498	10-11-1994	Provino et al.	
Ses	5,357,614	10-18-1994	Pattisam et al.	
Ses	5,379,036	01-03-1995	Storer	

Examiner Signature	<i>Suresh K. Suryawanshi</i>	Date Considered	<i>10/19/06</i>
-----------------------	------------------------------	--------------------	-----------------

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

1 Applicant's unique citation designation number (optional). 2 Applicant is to place a check mark here if English language Translation is attached.

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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Substitute for form 1449A/PTO				Complete if known	
				Application Number	09/776,267
FOURTH SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Filing Date	February 2, 2001
				First Named Inventor	Fallon
				Art Unit	2115
				Examiner Name	Suresh K. Suryawanshi
(use as many sheets as necessary)				Attorney Docket Number	8011-15
Sheet	3	of	11		

565	5,381,145	01-10-1995	Allen et al.	
565	5,394,534	02-28-1995	Kulakowski et al.	
565	5,396,228	03-07-1995	Garahi	
565	5,406,278	04-11-1995	Graybill et al.	
565	5,406,279	04-11-1995	Anderson et al.	
565	5,412,384	05-02-1995	Chang et al.	
565	5,414,850	05-09-1995	Whiting	
565	5,420,639	05-30-1995	Perkins	
565	5,452,287	09-19-1995	Dicecco	
565	5,461,679	10-24-1995	Normile et al.	
565	5,467,087	11-14-1995	Chu	
565	5,471,206	11-28-1995	Allen et al.	
565	5,479,587	12-26-1995	Campbell et al.	
565	5,486,826	01-23-1996	Remillard	
565	5,495,244	02-27-1996	Je-Chang et al.	
565	5,506,844	04-09-1996	Rao	
565	5,506,872	04-09-1996	Mohler	
565	5,530,845	06-25-1996	Hiatt et al.	
565	5,533,051	07-02-1996	James	
565	5,535,356	07-09-1996	Kim et al.	
565	5,537,658	07-16-1996	Bakke et al.	
565	5,557,551	09-17-1996	Craft	
565	5,557,668	09-17-1996	Brady	
565	5,557,749	09-17-1996	Norris	

Examiner Signature	Suresh K. Suryawanshi	Date Considered	01/16/06
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Substitute for form 1449A/PTO				Complete if known	
				Application Number	09/776,267
FOURTH SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Filing Date	February 2, 2001
				First Named Inventor	Fallon
				Art Unit	2115
				Examiner Name	Suresh K. Suryawanshi
(use as many sheets as necessary)				Attorney Docket Number	8011-15
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Slas	5,561,824	10-01-1996	Carreiro et al.	
Slas	5,574,952	11-12-1996	Brady et al.	
Slas	5,576,953	11-19-1996	Hugentobler	
Slas	5,583,500	12-10-1996	Allen et al.	
Slas	5,590,306	12-31-1996	Watanabe et al.	
Slas	5,596,674	01-21-1997	Bhandari et al.	
Slas	5,604,824	02-18-1997	Chui et al.	
Slas	5,606,706	02-25-1997	Takamoto et al.	
Slas	5,612,788	03-18-1997	Stone	
Slas	5,615,017	03-25-1997	Choi	
Slas	5,621,820	04-15-1997	Rynderman et al.	
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Slas	5,623,701	04-22-1997	Bakke et al.	
Slas	5,627,534	05-06-1997	Craft	
Slas	5,627,995	05-06-1997	Miller et al.	
Slas	5,629,732	05-13-1997	Moskowitz et al.	
Slas	5,630,092	05-13-1997	Carreiro et al.	
Slas	5,642,506	06-24-1997	Lee	
Slas	5,649,032	07-16-1997	Burt et al.	
Slas	5,652,795	07-29-1997	Dillon et al.	
Slas	5,652,917	07-29-1997	Maupin et al.	
Slas	5,654,703	08-05-1997	Clark, II	
Slas	5,655,138	08-05-1997	Kikinis	
Slas	5,666,560	09-09-1997	Moertl et al.	

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				Examiner Name	Suresh K. Suryawanshi
(use as many sheets as necessary)				Attorney Docket Number	8011-15
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5668,737	09-16-1997	Iler	
5,671,389	09-23-1997	Saliba	
5,675,333	10-07-1997	Boursier et al.	
5,694,619	12-02-1997	Konno	
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5,703,793	12-30-1997	Wise et al.	
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5,717,393	02-10-1998	Nakano et al.	
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5,724,475	03-03-1998	Kirsten	
5,729,228	03-17-1998	Franaszek et al.	
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5,757,852	05-26-1998	Jericevic et al.	
5,771,340	06-23-1998	Nakazato et al.	
5,778,411	07-07-1998	DeMoss et al.	
5,781,767	07-14-1998	Inoue et al.	
5,784,572	07-21-1998	Rostoker et al.	
5,787,487	07-28-1998	Hashimoto et al.	
5,799,110	08-25-1998	Israelsen et al.	
5,805,932	09-08-1998	Kawashima et al.	
5,808,660	09-15-1998	Sekine et al.	
5,809,176	09-15-1998	Yajima	
5,809,337	09-15-1998	Hannah et al.	

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				First Named Inventor	Fallon
				Art Unit	2115
				Examiner Name	Suresh K. Suryawanshi
(use as many sheets as necessary)				Attorney Docket Number	8011-15
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Slc3	5,812,789	09-22-1998	Diaz et al.	
Slc3	5,818,368	10-06-1998	Langley	
Slc3	5,818,369	10-06-1998	Withers	
Slc3	5,818,530	10-06-1998	Canfield et al.	
Slc3	5,819,215	10-06-1998	Dobson et al.	
Slc3	5,825,424	10-20-1998	Canfield et al.	
Slc3	5,832,037	11-03-1998	Park	
Slc3	5,832,126	11-03-1998	Tanaka	
Slc3	5,836,003	11-10-1998	Sadeh	
Slc3	5,838,996	11-17-1998	deCarmo	
Slc3	5,839,100	11-17-1998	Wegener	
Slc3	5,841,979	11-24-1998	Schulhof et al.	
Slc3	5,847,762	12-08-1998	Canfield	
Slc3	5,861,824	01-19-1999	Ryu et al.	
Slc3	5,861,920	01-19-1999	Mead et al.	
Slc3	5,870,036	02-09-1999	Franaszek et al.	
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Slc3	5,872,530	02-16-1999	Domyo et al.	
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Slc3	5,886,655	03-23-1999	Rust	
Slc3	5,889,961	03-30-1999	Dobbek	
Slc3	5,915,079	06-22-1999	Vondran, Jr. et al.	
Slc3	5,917,438	06-29-1999	Ando	
Slc3	5,920,326	07-06-1999	Rentschler et al.	

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FOURTH SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Filing Date	February 2, 2001
				First Named Inventor	Fallon
				Art Unit	2115
				Examiner Name	Suresh K. Suryawanshi
(use as many sheets as necessary)				Attorney Docket Number	8011-15
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SL23	5,936,616	08-10-1999	Torborg, Jr. et al.	
SL23	5,949,355	09-07-1999	Panaoussis	
SL23	5,955,976	09-21-1999	Heath	
SL23	5,960,465	09-28-1999	Adams	
SL23	5,964,842	10-12-1999	Packard	
SL23	5,968,149	10-19-1999	Jaquette et al.	
SL23	5,973,630	10-26-1999	Heath	
SL23	5,974,471	10-26-1999	Belt	
SL23	5,982,723	11-09-1999	Kamatani	
SL23	5,991,515	11-23-1999	Fall et al.	
SL23	5,996,033	11-30-1999	Chiu-Hao	
SL23	6,000,009	12-07-1999	Brady	
SL23	6,002,411	12-14-1999	Dye	
SL23	6,011,901	01-04-2000	Kirsten	
SL23	6,014,694	01-11-2000	Aharoni et al.	
SL23	6,026,217	02-15-2000	Adiletta	
SL23	6,028,725	02-22-2000	Blumenau	
SL23	6,031,939	02-29-2000	Gilbert et al.	
SL23	6,032,148	02-29-2000	Wilkes	
SL23	6,061,398	05-09-2000	Satoh et al.	
SL23	6,075,470	06-13-2000	Little et al.	
SL23	6,094,634	07-25-2000	Yahagi et al.	
SL23	6,097,520	08-01-2000	Kadnier	
SL23	6,104,389	08-15-2000	Ando	

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(use as many sheets as necessary)				Attorney Docket Number	8011-15
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863	6,105,130	08-15-2000	Wu et al.	
863	6,128,412	10-03-2000	Satoh	
863	6,141,053	10-31-2000	Saukkonen	
863	6,145,069	11-07-2000	Dye	
863	6,172,936	01-09-2001	Kitazaki	
863	6,192,082	02-20-2001	Moriarty et al.	
863	6,195,024	02-27-2001	Fallon	
863	6,253,264	06-26-2001	Sebastian	
863	6,272,627	08-07-2001	Mann	
863	6,272,628	08-07-2001	Aguilar et al.	
863	6,282,641	08-28-2001	Christensen	
863	6,309,424	10-30-2001	Fallon	
863	6,317,714	11-13-2001	Del Castillo et al.	
863	6,330,622	12-11-2001	Schaefer	
863	6,345,307	02-05-2002	Booth	
867	6,421,387	07-16-2002	Rhee	
863	6,434,168	08-13-2002	Kari	
863	6,442,659	08-27-2002	Blumenau	
863	6,449,682	09-10-2002	Toorians	
863	6,452,602	09-17-2002	Morein	
863	6,487,640	11-26-2002	Lipasti	
863	6,489,902	12-03-2002	Heath	
863	6,513,113	01-28-2003	Kobayashi	
863	6,529,633	03-04-2003	Easwar et al.	

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FOURTH SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Filing Date	February 2, 2001
				First Named Inventor	Fallon
				Art Unit	2115
				Examiner Name	Suresh K. Suryawanshi
(use as many sheets as necessary)				Attorney Docket Number	8011-15
Sheet	9	of	11		

863	6,542,644	04-01-2003	Satoh	
863	6,590,609	07-08-2003	Kitade et al.	
863	6,601,104	07-29-2003	Fallon	
863	6,604,158	08-05-2003	Fallon	
863	6,606,040	08-12-2003	Abdat	
863	6,606,413	08-12-2003	Zeineh	
863	6,618,728	09-09-2003	Rail	
863	6,624,761	09-23-2003	Fallon	
863	6,711,709	03-23-2004	York	
863	6,745,282	06-01-2004	Okada et al.	
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863	6,856,651	02-15-2005	Singh	
863	6,888,893	05-03-2005	Li et al.	
863	7,054,493	05-30-2006	Schwartz	
863	2001/ 0032128	10-18-2001	Kepecs	
863	2002/ 0037035	03-28-2002	Singh	
863	2002/ 0104891	08-08-2002	Otto	
863	2002/ 0126755	09-12-2002	Li et al.	
863	2003/ 0034905	02-20-2003	Anton et al.	
863	2003/ 0084238	05-01-2003	Okada et al.	
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				Filing Date		February 2, 2001
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				Art Unit		2115
				Examiner Name		Suresh K. Suryawanshi
(use as many sheets as necessary)				Attorney Docket Number		8011-15
Sheet	10	of	11			

FOREIGN PATENT DOCUMENTS							
Examiner Initials*	Cite No. ¹	Foreign Patent Document		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Documents	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ⁶
		Country Code ² - Number ³ - Kind Code ⁵ (if known)					
SB3		EP 0164677		12-18-1985	Texas Instruments Inc.		
SB3		EP 0185098		06-25-1986	Hitachi Ltd		
SB3		EP 0283798		09-28-1988	International Business Machines Corporation		
SB3		EP 0405572		06-29-1990	Fujitsu Limited		
SB3		EP 0493130		12-27-1991	Canon Kabushiki Kaisha		
SB3		EP 0587437		09-10-1993	International Business Machines Corporation		
SK3		EP 0595406		05-04-1994	Philips Electronics		
SB3		GB 2162025		01-22-1986	King Reginald Alfred		
SB3		JP 9188009		01-09-1996	Canon Inc.		
SB3		JP 11149376		06-02-1999	Toyo Commun Equip Co. Ltd		
SB3		WO 9414273		06-23-1994	Voxson International Pty Ltd		
SB3		WO 9429852		12-22-1994	Maxtor Corp		
SB3		WO 9502873		01-26-1995	Philips Electronics		
SB3		WO 9748212		06-03-1997	Nokia Telecommunications		

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				Attorney Docket Number	8011-15
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(use as many sheets as necessary)					

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	T ²
SB3		RICE, ROBERT F., "Some Practical Universal Noiseless Coding Techniques", Jet Propulsion Laboratory, Pasadena, California, JPL Publication 79-22, March 15, 1979.	
SB3		ANDERSON, J., et al. "Codec squeezes color teleconferencing through digital telephone lines", Electronics 1984, pp. 13-15	
SB3		VENBRUX, JACK, "A VLSI Chip Set for High-Speed Lossless Data Compression", IEEE Trans. On Circuits and Systems for Video Technology, Vol. 2, No. 44, December 1992, pp. 381-391	
SB3		"Operating System Platform Abstraction Method", IBM Technical Disclosure Bulletin, Feb. 1995, Vol. 38, Issue No. 2, pp 343-344	
SB3		MURASHITA, K., et al., "High-Speed Statistical Compression using Self-organized Rules and Predetermined Code Tables", IEEE, 1996 Data Compression Conference	
SB3		COENE, W., et al. "A Fast Route For Application of Rate-distortion Optimal Quantization in an MPEG Video Encoder" Proceedings of the International Conference on Image Processing, US., New York, IEEE, 16 September 1996, pp. 825-8286	
SB3		RICE, ROBERT, "Lossless Coding Standards for Space Data Systems", IEEE 1058-6393/97, pp. 577-585	
SB3		YEH, PEN-SHU, "The CCSDS Lossless Data Compression Recommendation for Space Applications", Chapter 16, Lossless Compression Handbook, Elsevier Science (USA), 2003, PP. 311-326.3	

Examiner Signature	Suresh K. Suryawanshi	Date Considered	12/10/06
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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

1 Applicant's unique citation designation number (optional). 2 Applicant is to place a check mark here if English language Translation is attached.

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.



Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

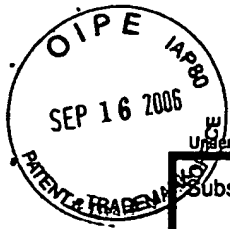
Substitute for form 1449A/PTO		SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT BY APPLICANT		Complete if known	
		Application Number	09/776,267		
		Filing Date	February 2, 2001		
		First Named Inventor	Fallon		
		Art Unit	2115		
		Examiner Name	Suresh Suyawanshi		
Sheet	1	of	1	Attorney Docket Number	8011-15

U.S. PATENT DOCUMENTS					
Examiner initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Documents	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number - Kind Code ² (if known)			
SB		4,394,774	07-19-1983	Widergren et al.	
SB		5,209,220	05-11-1993	Hiyama et al.	
SB		5,379,757	01-10-1995	Hiyama et al.	
SB		6,169,241	01-02-2001	Shimizu	
SB		6,661,839	12-09-2003	Ishida et al.	

Examiner Signature	Suresh S. Suyawanshi	Date Considered	10/10/06
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 1 Applicant's unique citation designation number (optional). 2 Applicant is to place a check mark here if English language Translation is attached.
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Express Mail
 EV620761458US




Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449/PTO SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)		Complete if known	
		Application Number	09/776,267
		Filing Date	February 2, 2001
		First Named Inventor	Fallon
		Art Unit	2115
		Examiner Name	Suresh Suyawanshi
Sheet	1	of	1
		Attorney Docket Number	8011-15

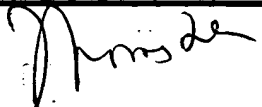
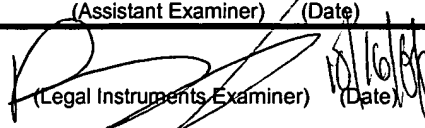
U.S. PATENT DOCUMENTS					
Examiner initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Documents	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number - Kind Code ² (if known)			
SLG		5,227,893	07-13-1993	Ett	
SLG		5,400,401	03-21-1995	Wasilewski et al.	
SLG		5,403,639	04-04-1995	Belsan et al.	
SLG		5,613,069	03-18-1997	Walker	
SLG		5,635,632	06-03-1997	Fay et al.	
SLG		5,635,932	06-03-1997	Shinagawa et al.	
SLG		5,719,862	02-17-1998	Lee et al.	
SLG		5,796,864	08-18-1998	Callahan	
SLG		5,867,167	02-02-1999	Deering	
SLG		6,182,125	01-30-2001	Borella et al.	
SLG		6,609,223	08-19-2003	Wolfgang	

Examiner Signature	Suresh K. Suyawanshi	Date Considered	10/10/06
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Issue Classification 	Application/Control No. 09/776,267	Applicant(s)/Patent under Reexamination FALLON ET AL.
	Examiner Suresh K. Suryawanshi	Art Unit 2115

ISSUE CLASSIFICATION													
ORIGINAL				INTERNATIONAL CLASSIFICATION									
CLASS		SUBCLASS		CLAIMED				NON-CLAIMED					
713		2		G	06	F	9	/24					
CROSS REFERENCES				G	06	F	9	/00					
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)			G	06	F	13	/00					
713	1							/					
711	113							/					
								/					
								/					
								/					

Suresh K Suryawanshi 10/10/06 (Assistant Examiner) (Date)	 (Primary Examiner) 10/12/06 (Date)	Total Claims Allowed: 31
 (Legal Instruments Examiner) 10/16/06 (Date)	O.G. Print Claim(s) 1	O.G. Print Fig. 1

<input type="checkbox"/> Claims renumbered in the same order as presented by applicant		<input type="checkbox"/> CPA		<input type="checkbox"/> T.D.		<input type="checkbox"/> R.1.47	
Final	Original	Final	Original	Final	Original	Final	Original
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2	2	24	32	62	92	122	152
	3	25	33	63	93	123	153
3	4	26	34	64	94	124	154
4	5	27	35	65	95	125	155
5	6	28	36	66	96	126	156
6	7	29	37	67	97	127	157
	8	30	38	68	98	128	158
	9	31	39	69	99	129	159
	10		40	70	100	130	160
	11		41	71	101	131	161
	12		42	72	102	132	162
7	13		43	73	103	133	163
	14		44	74	104	134	164
8	15		45	75	105	135	165
	16		46	76	106	136	166
9	17		47	77	107	137	167
10	18		48	78	108	138	168
11	19		49	79	109	139	169
12	20		50	80	110	140	170
13	21		51	81	111	141	171
14	22		52	82	112	142	172
15	23		53	83	113	143	173
16	24		54	84	114	144	174
17	25		55	85	115	145	175
18	26		56	86	116	146	176
19	27		57	87	117	147	177
20	28		58	88	118	148	178
21	29		59	89	119	149	179
22	30		60	90	120	150	180



SEARCHED

Class	Sub.	Date	Exmr.
713	2	1/21/04	SOS
711	1	1/24/04	SOS
712	100	1/24/04	SOS
711	113	1/29/04	SOS
711	120	1/29/04	SOS
Updated search		9/21/04 9/22/04 9/27/04 10/19/04	SOS
Updated search		6/17/05	SOS
Search updated		2/6/06	SOS
711	118	2/6/06	SOS
Search updated		10/19/06	SOS

SEARCH NOTES (INCLUDING SEARCH STRATEGY)

Exmr.	Date	Exmr.
East USPTA US-PG1US EAsy SPO D&M-TSS TTR	1/21/04 1/24/04 1/24/04 1/24/04	SOS
Updated search	9/21/04 9/22/04 9/27/04 10/19/04	SOS
Updated search	5/27/05	SOS
Updated search	2/6/06	SOS
Search updated	10/19/06	SOS

Best Available Copy

INTERFERENCE SEARCHED

Class	Sub.	Date	Exmr.
713	2	1/28/04	SOS
713	1	1/28/04	SOS
713	100	1/28/04	SOS
711	113	1/28/04	SOS
711	120	1/28/04	SOS
711	118	2/6/06	SOS
claim language searched in US-PG1US		10/19/06	SOS

(RIGHT OUTSIDE)



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COMMISSIONER FOR PATENTS
 UNITED STATES PATENT AND TRADEMARK OFFICE
 WASHINGTON, D.C. 20231
 www.uspto.gov



8b Data Sheet

CONFIRMATION NO. 9730

SERIAL NUMBER 09/776,267	FILING DATE 02/02/2001 RULE	CLASS 713	GROUP ART UNIT 2182	ATTORNEY DOCKET NO. 8011-15
APPLICANTS James J. Fallon, Armonk, NY; John Buck, Oceanside, NY; Paul F. Pickel, Bethpage, NY; Stephen J. McErlain, New York, NY;				
** CONTINUING DATA ***** THIS APPLN CLAIMS BENEFIT OF 60/180,114 02/03/2000 <i>yes SLO</i>				
** FOREIGN APPLICATIONS ***** <i>None SLO</i>				
IF REQUIRED, FOREIGN FILING LICENSE GRANTED ** 03/09/2001		** SMALL ENTITY **		
Foreign Priority claimed <input type="checkbox"/> yes <input checked="" type="checkbox"/> no	35 USC 119 (a-d) conditions met <input type="checkbox"/> yes <input type="checkbox"/> no <input type="checkbox"/> Met after Allowance	STATE OR COUNTRY NY	SHEETS DRAWING 13	TOTAL CLAIMS 30 18 12
Verified and Acknowledged	Examiner's Signature <i>SLO</i> Initials			INDEPENDENT CLAIMS 2 4 SLO 1/11/06
ADDRESS Frank Chau, Esq. F. CHAU & ASSOCIATES, LLP Suite 501 1900 Hempstead Turnpike East Meadow, NY 11554				
TITLE Systems and methods for accelerated loading of operating systems and application programs				
FILING FEE RECEIVED 420	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:	<input type="checkbox"/> All Fees <input type="checkbox"/> 1.16 Fees (Filing) <input type="checkbox"/> 1.17 Fees (Processing Ext. of time) <input type="checkbox"/> 1.18 Fees (Issue) <input type="checkbox"/> Other _____ <input type="checkbox"/> Credit _____		

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	1	pre\$1load\$3 near2 boot adj data near5 cache	USPAT	OR	OFF	2006/10/10 13:20
S2	2	pre\$1load\$3 near2 boot adj data near5 cache	US-PGPUB	OR	OFF	2006/10/10 13:25
S3	0	pre\$1load\$3 near2 boot adj data near5 cache	EPO; JPO; IBM_TDB	OR	OFF	2006/10/10 13:26
S5	2	load\$3 near3 boot adj data near5 cache	USPAT	OR	OFF	2006/10/10 13:27
S6	1	load\$3 near3 boot adj data near5 cache	US-PGPUB	OR	OFF	2006/10/10 13:28
S7	0	load\$3 near3 boot adj data near5 cache	EPO; JPO; IBM_TDB	OR	OFF	2006/10/10 13:28
S8	0	compressed adj boot adj data	USPAT	OR	OFF	2006/10/10 13:29
S9	0	compressed adj boot adj data	US-PGPUB	OR	OFF	2006/10/10 13:30
S10	0	compressed adj boot adj data	EPO; JPO; IBM_TDB	OR	OFF	2006/10/10 13:30
S11	0	compress\$3 near2 boot adj data	USPAT	OR	OFF	2006/10/10 13:31
S12	0	compress\$3 near2 boot adj data	US-PGPUB	OR	OFF	2006/10/10 13:31
S13	0	compress\$3 near2 boot adj data	EPO; JPO; IBM_TDB	OR	OFF	2006/10/10 13:31
S14	0	increas\$3 near3 access adj rate near3 cache	USPAT	OR	OFF	2006/10/10 13:34
S15	0	increas\$3 near3 access adj rate near3 cache	US-PGPUB	OR	OFF	2006/10/10 13:34
S16	0	increas\$3 near3 access adj rate near3 cache	EPO; JPO; IBM_TDB	OR	OFF	2006/10/10 13:34
S17	1	preloaded adj boot adj data	USPAT	OR	OFF	2006/10/10 13:36
S18	4	preloaded adj boot adj data	US-PGPUB	OR	OFF	2006/10/10 13:36
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S21	5	("4394774" "5209220" "5379757" "6169241" "6661839").pn.	USPAT	OR	OFF	2006/10/10 13:43

EAST Search History

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S23	24	("5113522" "5121342" "5150430" "5159336" "5175543" "5179651" "5191431" "5204756" "5212742" "5231492" "5237460" "5237675" "5243341" "5243348" "5247638" "5247646" "5263168" "5270832" "5287420" "5293379" "5309555" "5355498" "5357614" "5379036").pn.	USPAT	OR	OFF	2006/10/10 13:51
S24	24	("5381145" "5394534" "5396228" "5406278" "5406279" "5412384" "5414850" "5420639" "5452287" "5461679" "5467087" "5471206" "5479587" "5486826" "5495244" "5506844" "5506872" "5530845" "5533051" "5535356" "5537658" "5557551" "5557668" "5557749").pn.	USPAT	OR	OFF	2006/10/10 13:59
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S26	24	("5668737" "5671389" "5675333" "5694619" "5696927" "5703793" "5715477" "5717393" "5717394" "5721958" "5724475" "5729228" "5748904" "5757852" "5771340" "5778411" "5781767" "5784572" "5787487" "5799110" "5805932" "5808660" "5809176" "5809337").pn.	USPAT	OR	OFF	2006/10/10 14:07
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S30	14	("6542644" "6590609" "6601104" "6604158" "6606040" "6606413" "6618728" "6624761" "6711709" "6745282" "6748457" "6856651" "6888893" "7054493").pn.	USPAT	OR	OFF	2006/10/10 14:28
S31	7	"20010032128" "20020037035" "20020104891" "20020126755" "20030034905" "20030084238" "20030142874"	US-PGPUB	OR	OFF	2006/10/10 14:30
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S33	75	buck.in. with john	USPAT	OR	OFF	2006/10/10 16:19
S34	0	buck.in. with john and realtime.as.	USPAT	OR	OFF	2006/10/10 16:20
S35	0	buck.in. with john and boot adj data	USPAT	OR	OFF	2006/10/10 16:20
S36	1	pickel.in. with paul	USPAT	OR	OFF	2006/10/10 16:21
S37	0	McErlain.in. with stephen	USPAT	OR	OFF	2006/10/10 16:22
S38	0	McErlain.in.	USPAT	OR	OFF	2006/10/10 16:22
S39	0	mcerlain.in.	USPAT	OR	OFF	2006/10/10 16:23
S40	0	stephen.in. and realtime.as.	USPAT	OR	OFF	2006/10/10 16:23
S41	2	stephen.in. and boot adj data	USPAT	OR	OFF	2006/10/10 16:23
S42	2441	713/2	USPAT	OR	OFF	2006/10/10 16:26
S43	0	713/2.ccls. and pre\$1load\$3 near2 boot adj data near5 cache	USPAT	OR	OFF	2006/10/10 16:32
S44	2	713/2.ccls. and load\$3 near3 boot adj data near5 cache	USPAT	OR	OFF	2006/10/10 16:33
S45	0	713/2.ccls. and compressed adj boot adj data	USPAT	OR	OFF	2006/10/10 16:33
S46	0	713/2.ccls. and preloaded adj boot adj data	USPAT	OR	OFF	2006/10/10 16:34
S47	1535	713/1.ccls.	USPAT	OR	OFF	2006/10/10 16:34

EAST Search History

S48	0	713/1.ccls. and pre\$1load\$3 near2 boot adj data near5 cache	USPAT	OR	OFF	2006/10/10 16:39
S49	0	713/1.ccls. and load\$3 near3 boot adj data near5 cache	USPAT	OR	OFF	2006/10/10 16:40
S50	0	713/1.ccls. and compressed adj boot adj data	USPAT	OR	OFF	2006/10/10 16:40
S51	0	713/1.ccls. and preloaded adj boot adj data	USPAT	OR	OFF	2006/10/10 16:40
S52	837	711/113.ccls.	USPAT	OR	OFF	2006/10/10 16:43
S53	0	711/113.ccls. and pre\$1load\$3 near2 boot adj data near5 cache	USPAT	OR	OFF	2006/10/10 16:48
S54	2	711/113.ccls. and load\$3 near3 boot adj data near5 cache	USPAT	OR	OFF	2006/10/10 16:49
S55	0	711/113.ccls. and compressed adj boot adj data	USPAT	OR	OFF	2006/10/10 16:49
S56	0	711/113.ccls. and preloaded adj boot adj data	USPAT	OR	OFF	2006/10/10 16:50

9-18-06 IFW 2115/8



PATENTS
Attorney Docket No. 8011-15

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants : James J. Fallon et al.
Application No. : 09/776,267 Confirmation No. : 9730
Filing Date : February 2, 2001
Title : SYSTEMS AND METHODS FOR ACCELERATED LOADING OF OPERATING SYSTEMS AND APPLICATION PROGRAMS
Art Unit : 2115
Examiner : Suresh Suyawanshi

New York, New York 10020
September 15, 2006

Hon. Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

EXPRESS MAIL CERTIFICATION

Sir:

"Express Mail" mailing label number EV669635044US

Date of Deposit September 15, 2006

I hereby certify that the papers and fees identified below are being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 C.F.R. § 1.10 on the date indicated above and are addressed to Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

- Supplemental Information Disclosure Statement (in duplicate);
- Form PTO/SB/08A (in duplicate); and,
- Return Postcard.


ROSE MARIE DHANRAJ



PATENTS
8011-15

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants : James J. Fallon et al.
Application No. : 09/776,267 Conf. No.: 9730
Filed : February 2, 2001
For : SYSTEMS AND METHODS FOR ACCELERATED LOADING
OF OPERATING SYSTEMS AND APPLICATION
PROGRAMS
Art Unit : 2115
Examiner : Suresh Suyawanshi

Commissioner for Patents
P.O. Box 1450 New York, New York 10020
Alexandria, VA 22313-1450 September 15, 2006

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Sir:

Pursuant to 37 C.F.R. §§ 1.56 and 1.97, applicants hereby make the following documents of record in the above-identified patent application:

U.S. Patent Documents

5,227,893	Ett	07-13-1993
5,400,401	Wasilewski et al.	03-21-1995
5,403,639	Belsan et al.	04-04-1995
5,613,069	Walker	03-18-1997
5,635,632	Fay et al.	06-03-1997
5,635,932	Shinagawa et al.	06-03-1997
5,719,862	Lee et al.	02-17-1998
5,796,864	Callahan	08-18-1998
5,867,167	Deering	02-02-1999

09/19/2006 RHEBRAHT 00000016 061075 09776267

01 FC:1806 180.00 DA

6,182,125 Borella et al.
6,609,223 Wolfgang

01-30-2001
08-19-2003

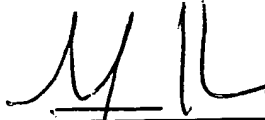
The aforementioned documents, which are listed on the accompanying Form SB/08A (submitted in duplicate), were cited in U.S. Patent Application No. 10/434,305 in the Office Action mailed on September 13, 2006.

It is respectfully requested that these documents be: (1) fully considered by the Patent and Trademark Office during the examination of this application; and (2) printed on any patent which may issue on this application. Applicants request that a copy of Form SB/08A, as considered and initialed by the Examiner, be returned with the next communication.

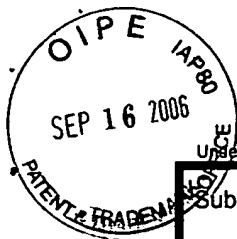
This Statement is submitted after the mailing of a first Office Action on the merits. In accordance with 37 C.F.R. §197 (c)(2), submission of this Statement requires a fee of \$180.00. The Director is hereby authorized to charge payment of \$180.00 and any other fees required in connection with this paper, or credit any overpayment of the same, to Deposit Account No. 06-1075, Order No. 103532-0002. A duplicate copy of this paper is being submitted herewith.

An early and favorable action is respectfully
requested.

Respectfully submitted,



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Substitute for form 1449A/PTO SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)				Complete if known		
				Application Number	09/776,267	
Sheet		1	of	1	Examiner Name	Suresh Suyawanshi
					Attorney Docket Number	8011-15

U.S. PATENT DOCUMENTS					
Examiner initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Documents	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number - Kind Code ² (if known)			
		5,227,893	07-13-1993	Ett	
		5,400,401	03-21-1995	Wasilewski et al.	
		5,403,639	04-04-1995	Belsan et al.	
		5,613,069	03-18-1997	Walker	
		5,635,632	06-03-1997	Fay et al.	
		5,635,932	06-03-1997	Shinagawa et al.	
		5,719,862	02-17-1998	Lee et al.	
		5,796,864	08-18-1998	Callahan	
		5,867,167	02-02-1999	Deering	
		6,182,125	01-30-2001	Borella et al.	
		6,609,223	08-19-2003	Wolfgang	

Examiner Signature		Date Considered	
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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

¹ Applicant's unique citation designation number (optional). ² Applicant is to place a check mark here if English language Translation is attached. This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

09-11-06

IFW 2115#



PATENTS
8011-15

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants : James J. Fallon et al.

Application No. : 09/776,267 Conf. No.: 9730

Filed : February 2, 2001

For : SYSTEMS AND METHODS FOR ACCELERATED LOADING
OF OPERATING SYSTEMS AND APPLICATION
PROGRAMS

Art Unit : 2115

Examiner : Suresh Suyawanshi

Commissioner for Patents
P.O. Box 1450 New York, New York 10020
Alexandria, VA 22313-1450 September 8, 2006

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Sir:

Pursuant to 37 C.F.R. §§ 1.56 and 1.97, applicants
hereby make the following documents of record in the above-
identified patent application:

U.S. Patent Documents

4,394,774	Widergren et al.	07-19-1983
5,209,220	Hiyama et al.	05-11-1993
5,379,757	Hiyama et al.	01-10-1995
6,169,241	Shimizu	01-02-2001
6,661,839	Ishida et al.	12-09-2003

The aforementioned patent documents are listed on the
accompanying Form SB/08A (submitted in duplicate).

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09/12/2006 HVUONG1 00000006 061075 09776267

01 FC:1806 180.00 DA

The aforementioned documents were cited in U.S. Patent Application No. 10/628,795 in the Notice of Allowability mailed on August 29, 2006.

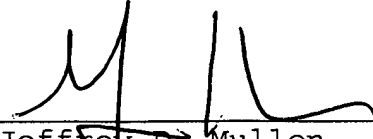
Documents identified in the aforementioned Notice of Allowability that are not being cited herewith are already of record in the present application.

It is respectfully requested that these documents be: (1) fully considered by the Patent and Trademark Office during the examination of this application; and (2) printed on any patent which may issue on this application. Applicants request that a copy of Form SB/08A, as considered and initialed by the Examiner, be returned with the next communication.

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An early and favorable action is respectfully
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Respectfully submitted,



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Submitted under 37 C.F.R. § 1.34
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PATENTS
Attorney Docket No. 8011-15

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants : James J. Fallon et al.
Application No. : 09/776,267 Confirmation No. : 9730
Filing Date : February 2, 2001
Title : SYSTEMS AND METHODS FOR ACCELERATED LOADING
OF OPERATING SYSTEMS AND APPLICATION PROGRAMS
Art Unit : 2115
Examiner : Suresh Suryawanshi

New York, New York 10020
September 8, 2006

Hon. Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

EXPRESS MAIL CERTIFICATION

Sir:

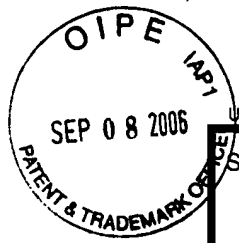
"Express Mail" mailing label number EV620761458US

Date of Deposit September 8, 2006

I hereby certify that the papers and fees identified below are being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 C.F.R. § 1.10 on the date indicated above and are addressed to Hon. Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Supplemental Information Disclosure Statement (in duplicate);
PTO Form SB/08A (in duplicate); and,
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ROSE MARIE DHANRAJ



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Substitute for form 1449A/PTO SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)				Complete if known			
				Application Number	09/776,267		
Sheet		1	of	1	Filing Date	February 2, 2001	
					First Named Inventor	Fallon	
					Art Unit	2115	
					Examiner Name	Suresh Suyawanshi	
					Attorney Docket Number	8011-15	

U.S. PATENT DOCUMENTS					
Examiner initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Documents	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number - Kind Code ² (if known)			
		4,394,774	07-19-1983	Widergren et al.	
		5,209,220	05-11-1993	Hiyama et al.	
		5,379,757	01-10-1995	Hiyama et al.	
		6,169,241	01-02-2001	Shimizu	
		6,661,839	12-09-2003	Ishida et al.	

Examiner Signature		Date Considered	
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8-30-06

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PATENTS
Attorney Docket No. 8011-15

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants : James J. Fallon et al.
Application No. : 09/776,267 Confirmation No. : 9730
Filing Date : February 2, 2001
Title : SYSTEMS AND METHODS FOR ACCELERATED LOADING
OF OPERATING SYSTEMS AND APPLICATION PROGRAMS
Art Unit : 2115
Examiner : Suresh Suryawanshi

New York, New York 10020
August 28, 2006

Hon. Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

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Date of Deposit August 28, 2006

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Supplemental Information Disclosure Statement (in duplicate);
PTO Form SB/08A (in duplicate);
Copies of Cited Foreign Patent Documents;
Copies of Cited Non Patent Literature Documents; and,
Return Postcard.


Isatta B. Smith



PATENTS
8011-15

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : James J. Fallon et al.

Application No. : 09/776,267 Conf. No.: 9730

Filed : February 2, 2001

For : SYSTEMS AND METHODS FOR ACCELERATED LOADING
OF OPERATING SYSTEMS AND APPLICATION
PROGRAMS

Art Unit : 2115

Examiner : Suresh K. Suryawanshi

Commissioner for Patents
P.O. Box 1450 New York, New York 10020
Alexandria, VA 22313-1450 August 28, 2006

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Sir:

Pursuant to 37 C.F.R. §§ 1.56 and 1.97, applicant hereby make the following documents of record in the above-identified patent application:

U.S. Patent Documents

4,127,518	Coy et al.	11-28-1978	
4,302,775	Widergren et al.	11-24-1981	(18)
4,574,351	Dang et al.	03-04-1986	
4,593,324	Ohkubo et al.	06-03-1986	(10)
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08/30/2006 SFELEKE1 00000055 061075 09776267

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Page 86 of 964

4,872,009	Tsukiyama et al.	10-03-1989	
4,876,541	Storer	10-24-1989	(18)
4,888,812	Dinan et al.	12-19-1989	(13,14)
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5,237,460	Miller et al.	08-17-1993	
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5,379,036	Storer	01-03-1995	
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6,104,389	Ando	08-15-2000	(13,14)
6,105,130	Wu et al.	08-15-2000	(21)
6,128,412	Satoh	10-03-2000	(18)
6,141,053	Saukkonen	10-31-2000	(2)
6,145,069	Dye	11-07-2000	(12)
6,172,936	Kitazaki	01-09-2001	(21)
6,192,082	Moriarty et al.	02-20-2001	(20)
6,195,024	Fallon	02-27-2001	(3,7,24)
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6,282,641	Christensen	08-28-2001	(21)
6,309,424	Fallon	10-30-2001	(7)
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6,449,682	Toorians	09-10-2002	(21)
6,452,602	Morein	09-17-2002	(22)
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6,489,902	Heath	12-03-2002	(3)
6,513,113	Kobayashi	01-28-2003	(21)
6,529,633	Easwar et al.	03-04-2003	(8)
6,542,644	Satoh	04-01-2003	(18)
6,590,609	Kitade et al.	07-08-2003	(10)
6,601,104	Fallon	07-29-2003	(14)
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6,606,413	Zeineh	08-12-2003	(18)
6,618,728	Rail	09-09-2003	(22)
6,624,761	Fallon	09-23-2003	(15)
6,711,709	York	03-23-2004	(16,17)
6,745,282	Okada et al.	06-01-2004	(12,22)
6,748,457	Fallon	06-08-2004	(14)
6,856,651	Singh	02-15-2005	(18)
6,888,893	Li et al.	05-03-2005	(18)
7,054,493	Schwartz	05-30-2006	(10)
2001/ 0032128	Kepecs	10-18-2001	(20)
2002/ 0037035	Singh	03-28-2002	(18)
2002/ 0104891	Otto	08-08-2002	(18)
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Copies of the aforementioned non-U.S. patent
documents and non-patent documents, which are listed on the
accompanying Form SB/08A (submitted in duplicate), are enclosed
herewith.

The above-identified documents marked with the
numeral one, (1), were cited in U.S. Patent Application No.
09/210,491 in the Office Action mailed on May 19, 2000.

The above-identified document marked with the numeral
two, (2), was cited in U.S. Patent Application No. 10/705,446
in the Office Action mailed on April 10, 2001.

The above-identified documents marked with the
numeral three, (3), were cited in U.S. Patent Application No.
09/579,221 in the Notice of Allowance mailed on February 28,
2003.

The above-identified documents marked with the numeral four, (4), were cited in U.S. Patent Application No. 09/266,394 in the Office Action mailed on February 1, 2002.

The above-identified document marked with the numeral five, (5), was cited in the U.S. Patent Application No. 09/266,394 in the Notice of Allowance mailed on July 29, 2002.

The above-identified documents marked with the numeral six, (6), were cited in the U.S. Patent Application No. 09/481,243 in the Office Action mailed on June 26, 2002.

The above-identified documents marked with the numeral seven, (7), were cited in the U.S. Patent Application No. 10/016,355 in the Office Action mailed on November 22, 2002.

The above-identified document marked with the numeral eight, (8), was cited in the U.S. Patent Application No. 10/016,355 in the Notice of Allowance mailed on April 18, 2003.

The above-identified documents marked with the numeral nine, (9), were cited in the U.S. Patent Application No. 09/775,905 in the Office Action mailed on April 23, 2003.

The above-identified documents marked with the numeral ten, (10), were cited in the U.S. Patent Application No. 10/628,801 in the Office Action mailed on March 17, 2005.

The above-identified documents marked with the numeral eleven, (11), were cited in the U.S. Patent Application No. 10/628,795 in the Office Action mailed on November 12, 2004.

The above-identified documents marked with the numeral twelve, (12), were cited in the U.S. Patent Application No. 10/306,581 in the Office Action mailed on June 29, 2004.

The above-identified documents marked with the numeral thirteen, (13), were cited in the U.S. Patent Application No. 10/076,013 in the Office Action mailed on May 24, 2005.

The above-identified documents marked with the numeral fourteen, (14), were cited in the U.S. Patent Application No. 10/076,013 in the Office Action mailed on February 27, 2006.

The above-identified document marked with the numeral fifteen, (15), was cited in the U.S. Patent Application No. 10/668,768 in the Office Action mailed on February 20, 2004.

The above-identified document marked with the numeral sixteen, (16), was cited in the U.S. Patent Application No. 10/668,768 in the Office Action mailed on July 28, 2005.

The above-identified documents marked with the numeral seventeen, (17), were cited in the U.S. Patent Application No. 10/668,768 in the Notice of Allowance mailed on May 1, 2006.

The above-identified documents marked with the numeral eighteen, (18), were cited in the U.S. Patent Application No. 09/969,987 in the Office Action mailed on January 26, 2005.

The above-identified document marked with the numeral nineteen, (19), was cited in the U.S. Patent Application No. 09/969,987 in the Office Action mailed on September 12, 2005.

The above-identified documents marked with the numeral twenty, (20), were cited in the U.S. Patent Application No. 09/969,987 in the Office Action mailed on June 19, 2006.

The above-identified documents marked with the numeral twenty-one, (21), were cited in the U.S. Patent Application No. 09/775,897 in the Office Action mailed on December 24, 2003.

The above-identified documents marked with the numeral twenty-two, (22), were cited in the U.S. Patent Application No. 10/306,581 in the Office Action mailed on July 24, 2006.

The above-identified documents marked with the numeral twenty-three, (23), were cited in an International Search Report ("ISR") in PCT Application No. PCT/US01/03712. A copy of this ISR is being submitted herewith.

The above-identified documents marked with the numeral twenty-four, (24), were cited in an International Search Report ("ISR") in PCT Application No. PCT/US00/42018. A copy of this ISR is being submitted herewith.

Documents included in the above-identified Office Actions and Search Report that are not being cited herewith are already of record in the present application.

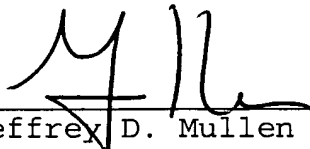
It is respectfully requested that these documents be: (1) fully considered by the Patent and Trademark Office during the examination of this application; and (2) printed on any patent which may issue on this application. Applicant requests that a copy of Form SB/08A, as considered and initialed by the Examiner, be returned with the next communication.

This Statement is submitted after the mailing of a first Office Action on the merits. In accordance with 37 C.F.R. §197(c)(2), submission of this Statement requires a fee of \$180.00. The Director is hereby authorized to charge payment of \$180.00 and any other fees required in connection

with this paper, or credit any overpayment of the same, to
Deposit Account No. 06-1075, Order No. 103532-0002. A
duplicate copy of this paper is being submitted herewith.

An early and favorable action is respectfully
requested.

Respectfully submitted,



Jeffrey D. Mullen

Registration No. 52,056

Agent for Applicant

Submitted under 37 C.F.R. § 1.34

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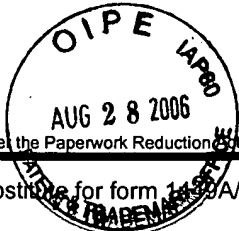
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Substitute for form 1485A/PTO FOURTH SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)				Complete if known	
Application Number		09/776,267			
Filing Date		February 2, 2001			
First Named Inventor		Fallon			
Art Unit		2115			
Examiner Name		Suresh K. Suryawanshi			
Attorney Docket Number		8011-15			
Sheet	1	of	11		

U.S. PATENT DOCUMENTS					
Examiner initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Documents	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number - Kind Code* (if known)			
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Examiner Signature		Date Considered	
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 1 Applicant's unique citation designation number (optional). 2 Applicant is to place a check mark here if English language Translation is attached.
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Substitute for form 1449A/PTO				Complete if known	
				Application Number	09/776,267
FOURTH SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Filing Date	February 2, 2001
				First Named Inventor	Fallon
(use as many sheets as necessary)				Art Unit	2115
				Examiner Name	Suresh K. Suryawanshi
Sheet	2	of	11	Attorney Docket Number	8011-15

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				Application Number	09/776,267
FOURTH SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Filing Date	February 2, 2001
				First Named Inventor	Fallon
				Art Unit	2115
				Examiner Name	Suresh K. Suryawanshi
(use as many sheets as necessary)				Attorney Docket Number	8011-15
Sheet	3	of	11		

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				Application Number	09/776,267
FOURTH SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Filing Date	February 2, 2001
				First Named Inventor	Fallon
(use as many sheets as necessary)				Art Unit	2115
				Examiner Name	Suresh K. Suryawanshi
Sheet	4	of	11	Attorney Docket Number	8011-15

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Substitute for form 1449A/PTO				Complete if known	
				Application Number	09/776,267
FOURTH SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Filing Date	February 2, 2001
				First Named Inventor	Fallon
(use as many sheets as necessary)				Art Unit	2115
				Examiner Name	Suresh K. Suryawanshi
Sheet	5	of	11	Attorney Docket Number	8011-15

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Examiner Signature		Date Considered	
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FOURTH SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Filing Date	February 2, 2001
				First Named Inventor	Fallon
				Art Unit	2115
				Examiner Name	Suresh K. Suryawanshi
(use as many sheets as necessary)				Attorney Docket Number	8011-15
Sheet	6	of	11		

		5,812,789	09-22-1998	Diaz et al.	
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FOURTH SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Filing Date	February 2, 2001
				First Named Inventor	Fallon
				Art Unit	2115
				Examiner Name	Suresh K. Suryawanshi
(use as many sheets as necessary)				Attorney Docket Number	8011-15
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(use as many sheets as necessary)				Attorney Docket Number	8011-15
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Examiner initials*	Cite No. ¹	Foreign Patent Document		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Documents	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ⁶
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Sheet	11	of	11	Attorney Docket Number	8011-15

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Examiner initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	T ²
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Radio device with signal compression.

A digital radio device (2) for *inter alia* mobile radio or cordless telephony is proposed with signal compression (12) for base band signals and/or hard-limiting at RF (6) an/or IF (10) stages. Such an architecture allows for a high level of integration with less complexity than known digital radio devices, and is thus cost saving. In an embodiments of the present invention the signal compression (12) can be carried out by a true logarithmic amplifier or by a compression device (13, 14) having a sine-shaped transfer characteristic. In successive signal processing (24) of digitised base band signals, digital signal decompression can be carried out by using the samples of the base band signal as addresses to a decompression lookup-table.

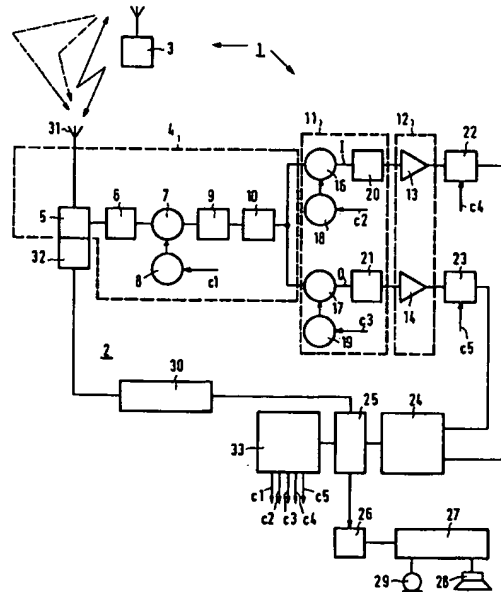


FIG.1

EP 0 595 406 A1

The present invention relates to a digital radio device comprising an analog receiving part for receiving phase or frequency modulated radio frequency signals coupled to base band conversion means for converting the radio frequency signals to at least one base band signal, analog to digital conversion means for sampling the at least one base band signal, and digital processing means for processing samples of the at least one base band signal. Such digital radio devices, which can be transceivers if also a transmitting part and switchover means for switching over between transmission and reception are comprised therein, can be used in mobile radio systems, in cordless telephony systems, and in paging systems inter alia.

A digital radio device of this kind is known from the German patent application DE-OS 39 25 305. In the known digital radio device signal compression and signal limiting is carried out before base band conversion and base band converted radio frequency quadrature signals are sampled by means of analog to digital converters. After analog to digital conversion digital samples are further processed in the known digital radio device. In the known radio device, e.g. to be used in a cellular radio system such as a so-called GSM-system (Groupe Special Mobile), a pan-European mobile radio system, signal compression is carried out to achieve dynamics compression of the radio frequency signal which may vary 100 dB at an antenna input of the radio device, in order to relieve analog to digital conversion of the quadrature base band signals. Without compression a 20 bit A/D-converter would be necessary for achieving the necessary number of significant bits at very small signal strength, i.e. such an A/D-converter would become very expensive. A disadvantage of the known signal limiting and compression is that when interfering signals are present the compression means introduce intermodulation products that one cannot get rid of during subsequent processing of the baseband samples. Bandpass filtering is therefore required before limiting and compression, implemented for example by a separate device like a SAW-filter (Surface Acoustic Wave).

It is an object of the present invention to provide a digital radio device in which inexpensive analog to digital converters are used, not having the disadvantages of the known digital radio device.

To this end a digital radio device according to the present invention is characterised in that the digital radio device comprises a smooth-non-linear arrangement coupled between the base band conversion means and the analog to digital conversion means for compressing larger signals at an input thereof more than smaller signals. By signal

smoothing after base band conversion the smoothing arrangement consumes less power than the logarithmic compression in the known device, due to the lower frequency operating range, whereas limiting at RF and/or IF can at least substantially be avoided. Due to the base band smoothing no separate SAW-filter would be necessary, whereas the base band smoothing can be integrated with further functions, thus reducing costs by achieving a simplified device. It is to be realized that the dynamic range of an analog to digital converter is proportional to cost, IC surface area, and power consumption, or, otherwise stated, every extra bit doubles the complexity of an analog to digital converter.

In an embodiment of a digital radio device according to the present invention the smooth-non-linear arrangement is a logarithmic amplifier. By using a logarithmic amplifier, which should be of the so-called true logarithmic amplifier type which compresses the amplitude of an input signal while retaining information about its sign, very large amplitude range signals can be coped with.

In another embodiment of a digital radio device according to the present invention the smooth-non-linear arrangement is an arrangement having a sine-shaped transfer characteristic. Also with a sine-shaped transfer characteristic input signals with a larger amplitude are compressed with respect to smaller signals whilst hard limiting on base band signals is avoided. It is to be realised that hard limiting of base band signals would lead to phase errors and thus to an unacceptable increase of the BER (Bit Error Rate) of demodulated digital signals.

In a further embodiment of a digital radio device according to the present invention the digital radio device comprises at least one signal limiting arrangement in the analog receiving part. The limiting can be at higher signal levels not leading to substantial performance degradation in the base band processing due to interference caused by the presence of unwanted signals. By also adding some limiting at radio frequency and/or intermediate frequency maximum signal control for analog to digital conversion is achieved. The limiting can be done by means of hard limiting or by means of AGC (Automatic Gain Control). Fading signals can only demodulated correctly (by an equalizer) if amplitude information is preserved. However fading are only to be expected up to a certain field strength. Higher strengths are encountered when one is near a transmitter, and then one radio propagation path from the transmitter to the receiver tends to dominate, and fading is less significant. Under these circumstances of very high signal strength the signal amplitude can be limited without seriously affecting performance. This limiting is best done at r.f. or at an i.f. In order to avoid

distortion of the signal phase that would occur with baseband limiting, and to reduce the dynamic range required in the later parts of the receiver.

In a further embodiment of a digital radio device according to the present invention the digital radio device comprises at least one low pass filter for filtering the at least one base band signal. It is achieved that unwanted signals are removed and that less demand is imposed on passband filtering. Also filtering at lower frequencies eases integration thereof on an IC (Integrated Circuit).

In a further embodiment of a digital radio device according to the present invention the digital radio device comprises at least one band pass filter before the at least one signal limiting arrangement. Band pass filtering, which can be carried out on radio frequency signals and/or intermediate frequencies, removes unwanted signals. Thus, filter effort can be distributed over various frequency bands, i.e. at radio frequency, at intermediate frequency, or at low frequency. Low pass filtering before the logarithmic amplifier can be dimensioned such that closest neighbour channel signals are attenuated such that a rest signal thereof has negligible effect on the dynamics compression.

In a further embodiment of a digital radio device according to the present invention, the digital processing means are arranged for correcting the samples of the at least one base band signal so as to decompress for compression by means of the smooth-non-linear arrangement. In this way a quasi linear result is achieved in which fine quantisation is achieved for very small signals, where noise plays a greater role, while greater quantisation steps are used for stronger fading signals, where less accuracy is required.

In a further embodiment of a digital radio device according to the present invention, the processing means are arranged for correcting the samples by using the samples as addresses for a correction lookup-table which outputs decompressed sample values. Use of a lookup-table allows for a fast software correction of digitised base band signals.

The present invention will now be described, by way of example, with reference to the accompanying drawings, wherein

Fig. 1 schematically shows a radio communication system with a digital radio device according to the present invention,

Fig. 2 diagrammatically shows an embodiment of a signal compression device for use in the digital radio device, and

Fig. 3 shows simulation results of bit error rates versus signal levels in a radio device according to the present invention under various conditions.

Figure 1 schematically shows a radio communication system 1 with a digital radio device 2 according to the present invention, and at least one radio base station of which a radio base station 3 is shown. The radio base station 3 communicates with the digital radio device 2, which comprises a receiving and a transmitting part, e.g. using a TDMA communication method such as used in GSM. It is pointed out in figure 1 by means of a solid line for a direct path and broken lines for reflected paths between the radio base station 3 and the digital radio device 2 that signals transmitted and received signals are subject to multipath propagation due to reflections *inter alia*, i.e. delayed replica of transmitted signals are received. Furthermore, for mobile digital radio devices, the radio signals are subject to fading of 40 dB or more, causing a very rapidly fluctuating signal strength at receiver side. It is thus important that the digital receiver 2 can cope with these kind of problems. The digital radio receiver 2 comprises an analog receiving part 4 for receiving phase or frequency modulated signals, e.g. quadrature GMSK (Gaussian Minimum Shift Keying) modulated signals. The analog receiving part 4 comprises an RF-input-stage 5 which can be coupled to a signal limiting arrangement 6 in an embodiment of a digital radio device according to the present invention. The received and at choice limited signal is fed to an intermediate mixer which is coupled with a local oscillator 8. Although only one mixing stage 7 is shown, frequency down conversion may be carried out via several mixing stages. The mixer 7 is coupled to an intermediate stage 9 comprising a band pass filter which can be coupled to a further limiting arrangement 10. It has been shown that no further limiting than for signal levels above -40 dBm, preferably distributed over various intermediate frequencies, will not substantially degrade the performance of the digital radio device as to BER (Bit Error Rate). E.g. for GSM, GSM recommendation 05.05, version 3.5.0, Transmission and Reception, 1.3.89, assumes a static channel condition for RF signal levels between -10 dBm and -40 dBm, for the purpose of BER-measurements. Assuming RF signals with a maximum signal level of -10 dBm in a GSM system, in an embodiment of the present invention input RF signals are hard limited above -40 dBm, in RF and/or IF receiver stages, such a hard limiting being permissible. Hard limiting should be avoided below the signal level of the strongest interferer. The down converted received radio frequency signal is fed to base band conversion means 11 for obtaining base band signals, which are fed to a smooth-non-linear arrangement 12 for achieving base band signal compression in accordance to the present invention. The smooth-non-linear arrangement 12 can comprise true loga-

rithmic amplifiers 13 and 14 for compressing respective quadrature base band signals I and Q, i.e. an in-phase and quadrature signal respectively. Such a true logarithmic amplifier can be a circuit as in an IC with type number SL531C (Plessey), or any other true logarithmic amplifier. Instead of logarithmic amplifiers 13 and 14 the smooth-non-linear arrangement 12 may comprise circuits with a different transfer characteristic, such as a sine-shaped transfer characteristic. The base band conversion means 11 comprise respective base band converters 16 and 17 which are coupled to sine and cosine local oscillators 18 and 19 respectively. The base band conversion means may further comprise respective low pass filters 20 and 21 for low pass filtering the quadrature signals I and Q. After signal compression the base band signals are fed to analog to digital conversion means such as A/D-converters 22 and 23 for obtaining samples of the same. The samples are fed to digital processing means 24 for base band processing. The processed signals, e.g. representing speech signals, are fed via interface logic 25 to a PCM (Pulse Code Modulation) Bus Interface 26 to an handset in which conversion from digital to analog signals is carried out. In case of a speech communication, an analog speech signal is fed to a speaker 28. In opposite direction, in full duplex mode, an analog speech signal picked-up by a microphone is fed to the digital processing means 24 via the interfaces 26 and 25, and is modulated and converted to a radio frequency signal in transmitting means 30 which deliver an signal to an antenna 31 via a diplexer 32. The interface logic is further coupled to a device control unit 33 for generating various control signals within the digital radio device, such as TDMA control. Shown are control signals c1, c2, c3, c4, and c5 for respective control of the local oscillators 8, 18, and 19, and the analog to digital converters 22 and 23. For a more detailed description of a known GSM receiver referred is to an article, "Architektur eines Mobilfunkgerätes für das Netz D", P. Schöffel et al., Philips Innovation 1/1991, pp. 132-139.

Fig. 2 diagrammatically shows an embodiment of a signal compression device 13 or 14 for use in the digital radio device 2 having a sine-shaped transfer characteristic sine from $-\pi/2$ to $+\pi/2$, indicated by an input-output relation U_o/U_i of the devices 13 and 14. Such a transfer characteristic sine can be realised and approximated by a number cascaded and/or cascoded amplifier stages having a non-linear transfer characteristic, the resulting transfer characteristic being a polynomial approximation of a sine-shaped transfer characteristic. In applying such a sine-shaped characteristic, lower level input signals are approximately linearly amplified whereas higher level input signals are

compressed, and such a compression favours lower level noisy signals as to quantisation in the A/D-converters 22 and 23.

Fig. 3 shows simulation results of bit error rates BER versus signal levels slev in dBm, in a radio device 2 according to the present invention under various channel conditions. The simulations were carried out for a receiver architecture with IF hard limiting above -40 dBm, base band signal compression, and A/D-conversion using 6 bit A/D-converters. Signal compression was done in a signal range between -84 dBm and -40 dBm. Specification masks M11, M12 at -100 dBm, and M21, M22 at higher signal levels are shown. For a test channel behaving like a typical fading channel the BER should not exceed M11 and M21 respectively, and for a test channel like a static test channel the BER should not exceed M12 and M22 respectively. Simulation results for the typical fading channel, indicated with curves simf1 and simf2, and for the static channel, indicated with sims1 and sims2, show that the particular receiver architecture complies with the BER-specifications M11, M12, and M21, M22. Though signal compression increases the BER, the increased BER still complies with the specifications. The receiver architecture according to the present invention allows for a cost saving high level of integration, i.e. from the limiting arrangement 10 circuits can be integrated within one integrated circuit, whereas the signal limiting arrangement 6, the mixer 7, and the local oscillator 8 can be integrated within another integrated circuit, for even more integration.

The digital processing means 24, e.g. a signal processor with RAM and ROM memory with software etc., can be arranged for decompressing the compressed signal, i.e. for correcting the base band samples. In an embodiment the software comprises a lookup-table addressed by the base band signal samples from the A/D-converters 22 and 23, the lookup-table outputting decompressed sample values. Thus, a quasi-linear result is achieved, with a higher quantisation level for lower level noisy signals than for higher level signals.

Claims

1. A digital radio device (2) comprising an analog receiving part (4) for receiving phase or frequency modulated radio frequency signals coupled to base band conversion means (11) for converting the radio frequency signals to at least one base band signal, analog to digital conversion means (22, 23) for sampling the at least one base band signal, and digital processing means (24) for processing samples of the at least one base band signal, characterised in that the digital radio device (2) com-

prises a smooth-non-linear arrangement (12) coupled between the base band conversion means (11) and the analog to digital conversion means (22, 23) for compressing larger signals at an input thereof more than smaller signals. 5

2. A digital radio device (2) as claimed in claim 1, wherein the smooth-non-linear arrangement (12) is a logarithmic amplifier. 10
3. A digital radio device (2) as claimed in claim 1, wherein the smooth-non-linear arrangement (12) is an arrangement (13, 14) having a sine-shaped transfer characteristic. 15
4. A digital radio device (2) as claimed in claims 1, 2 or 3, wherein the base band signals are quadrature signals. 20
5. A digital radio device (2) as claimed in claims 1, 2, 3 or 4, comprising at least one signal limiting arrangement (6, 10) in the analog receiving part (4). 25
6. A digital radio device (2) as claimed in claim 5, comprising at least one low pass filter (20, 21) for filtering the at least one base band signal.
7. A digital radio receiver (2) as claimed in claims 5 or 6, comprising at least one band pass filter (5, 9) before the at least one signal limiting arrangement (6, 10). 30
8. A digital radio device (2) as claimed in any one of the preceding claims, wherein the digital processing means (24) are arranged for correcting the samples of the at least one base band signal so as to decompress for compression by means of the smooth-non-linear arrangement (12). 35 40
9. A digital radio device (2) as claimed in claim 8, wherein the processing means (24) are arranged for correcting the samples by using the samples as addresses for a correction lookup-table which outputs decompressed sample values. 45

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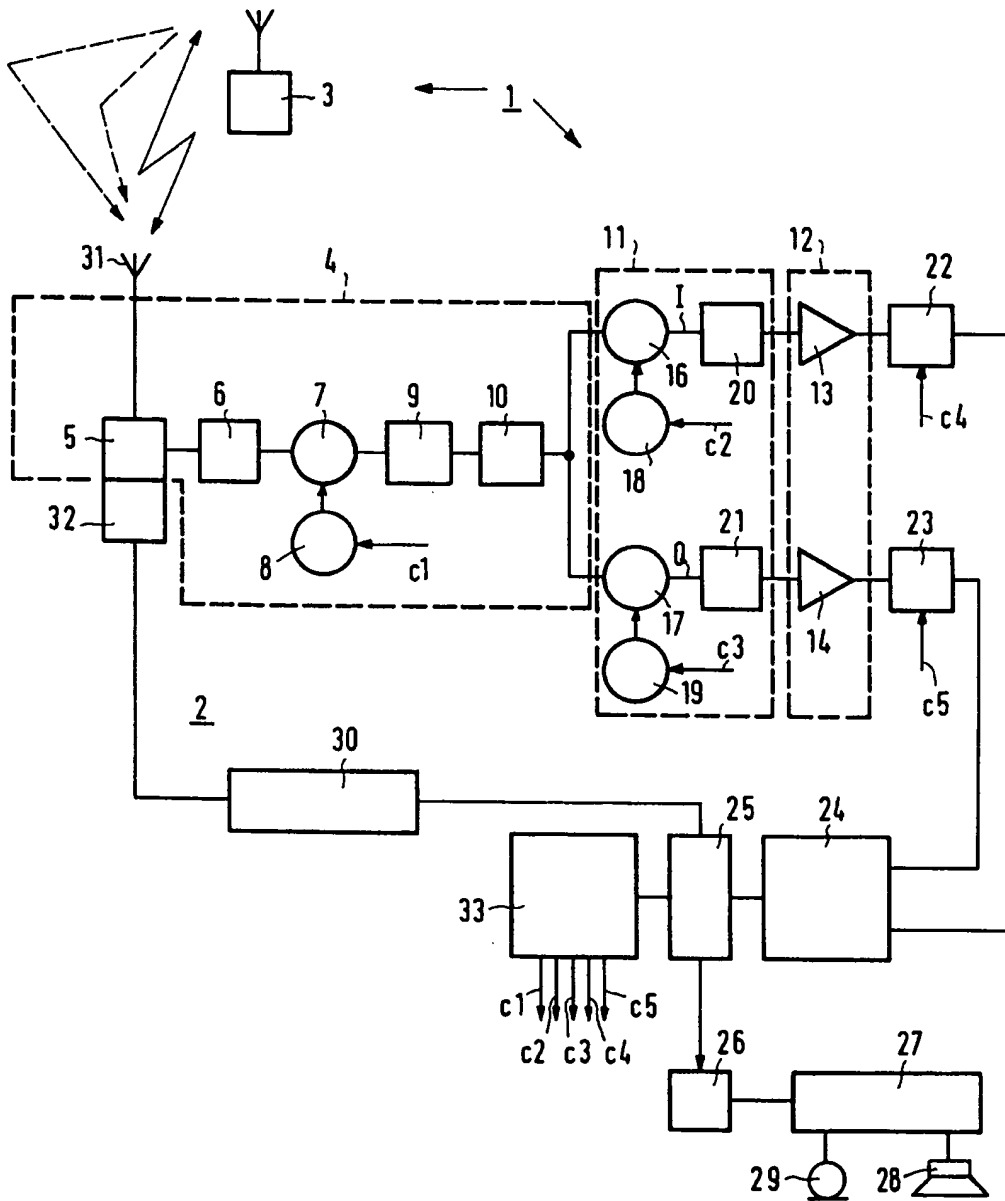


FIG. 1

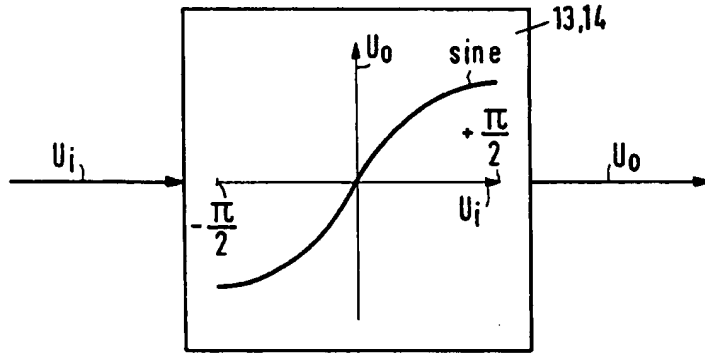


FIG.2

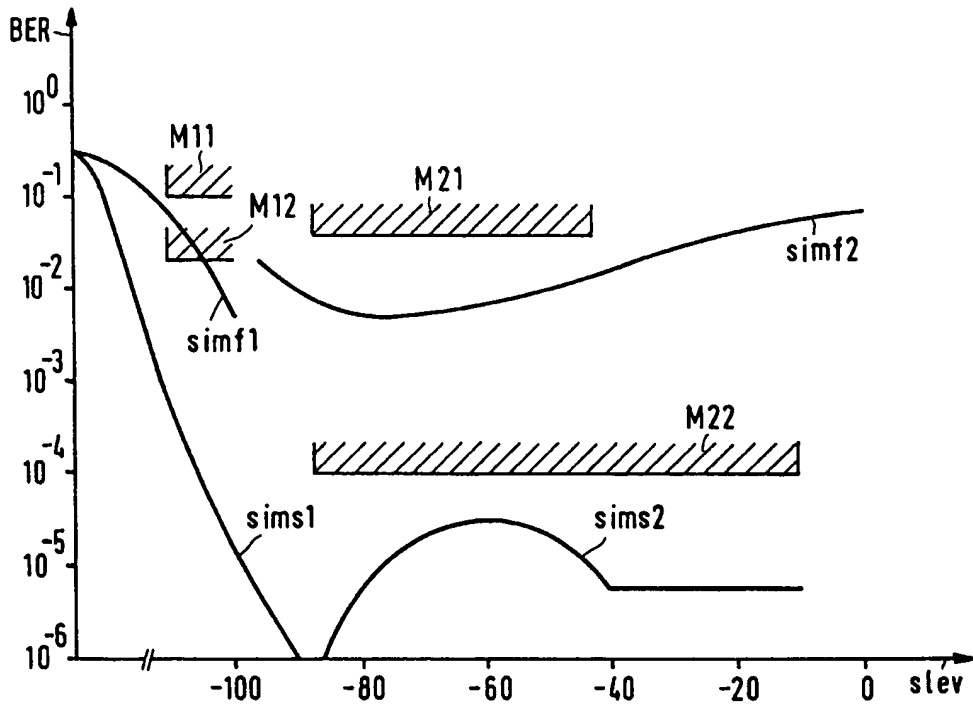


FIG.3



DOCUMENTS CONSIDERED TO BE RELEVANT		
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim
D,A	DE-A-39 25 305 (PHILIPS) * abstract * * column 2, line 33 - line 53 * * column 3, line 66 - column 4, line 25 * * column 4, line 40 - column 5, line 1 * * figures 1,2 * ---	1,2,4,5
A	GB-A-2 210 741 (ANT NACHRICHTENTECHNIK) * page 1, line 13 - line 20 * * page 2, line 19 - page 3, line 16 * * page 4, line 12 - line 24 * * figure 1 * -----	1,8
		TECHNICAL FIELDS SEARCHED (Int.Cl.5)
		H04B H03G
The present search report has been drawn up for all claims		
Place of search	Date of completion of the search	Examiner
THE HAGUE	4 February 1994	Lydon, M
CATEGORY OF CITED DOCUMENTS		
X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document		T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application I : document cited for other reasons ----- & : member of the same patent family, corresponding document

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(72) Inventor Reginald Alfred King	

(54) Waveform encoding method

(57) An analogue waveform, such as a speech waveform, is converted into a digital data stream by known methods, such as Pulse Code Modulation or Delta Modulation. To achieve a reduction in the bit rate, the digital data stream is divided into a number of successive equal time periods and stored. Time encoded symbols are also derived for the digital data stored in each time period and stored. The distributions of each symbol in successive time periods are then determined and compared. The digital data stored in respect of any time period is transmitted or substituted by digital data derived from the data stored in one or more of the preceding time periods in dependence upon the results of the comparison between the symbols derived from that time period and the one or more preceding time periods.

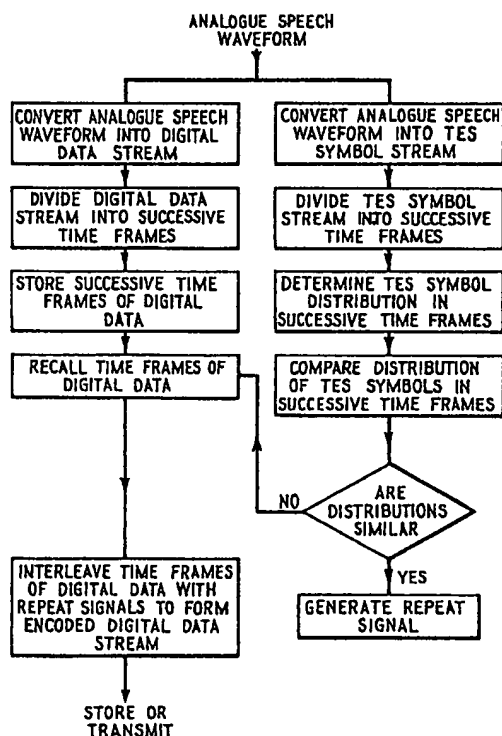


FIG. 1

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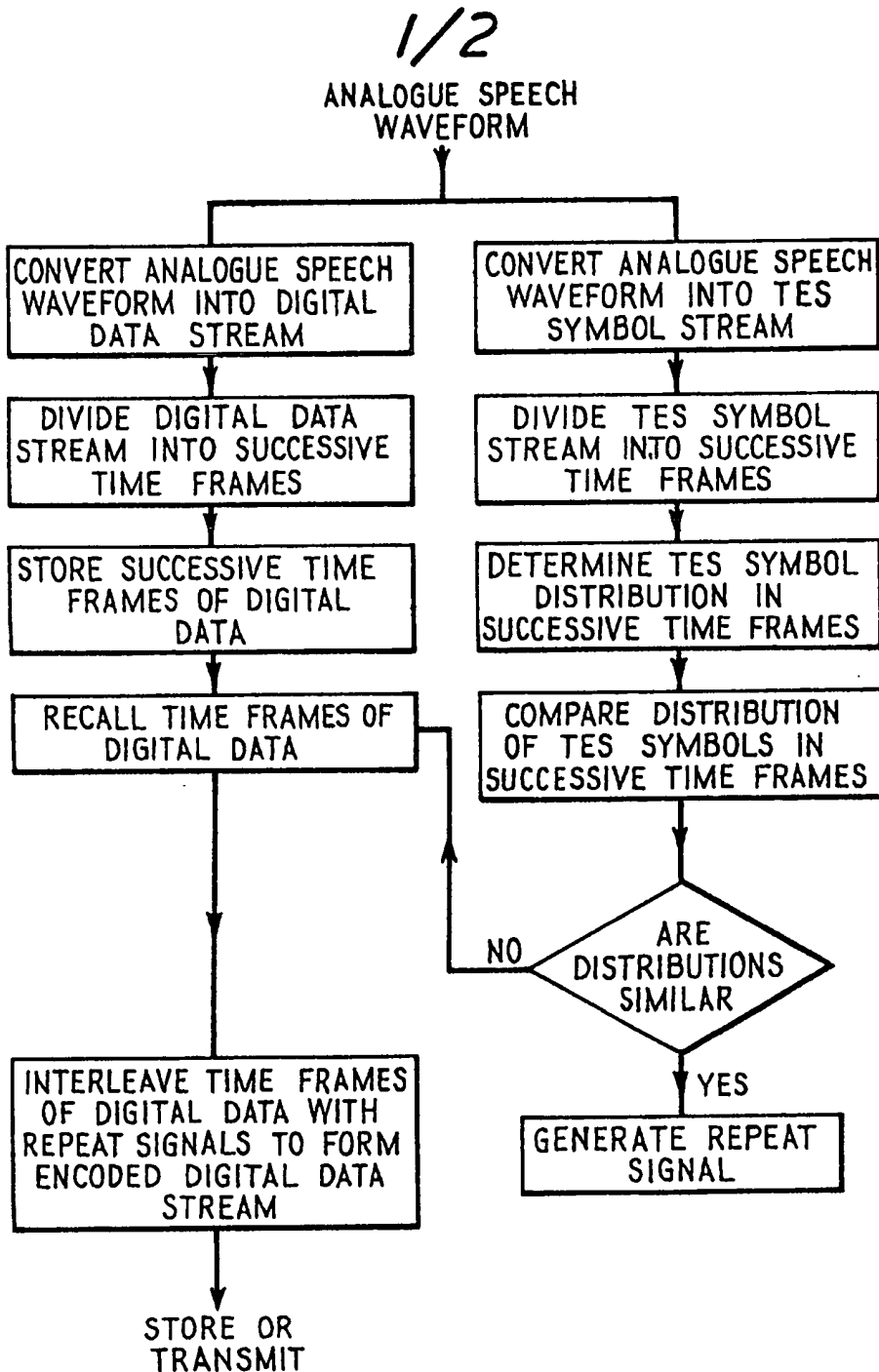


FIG. 1

2/2

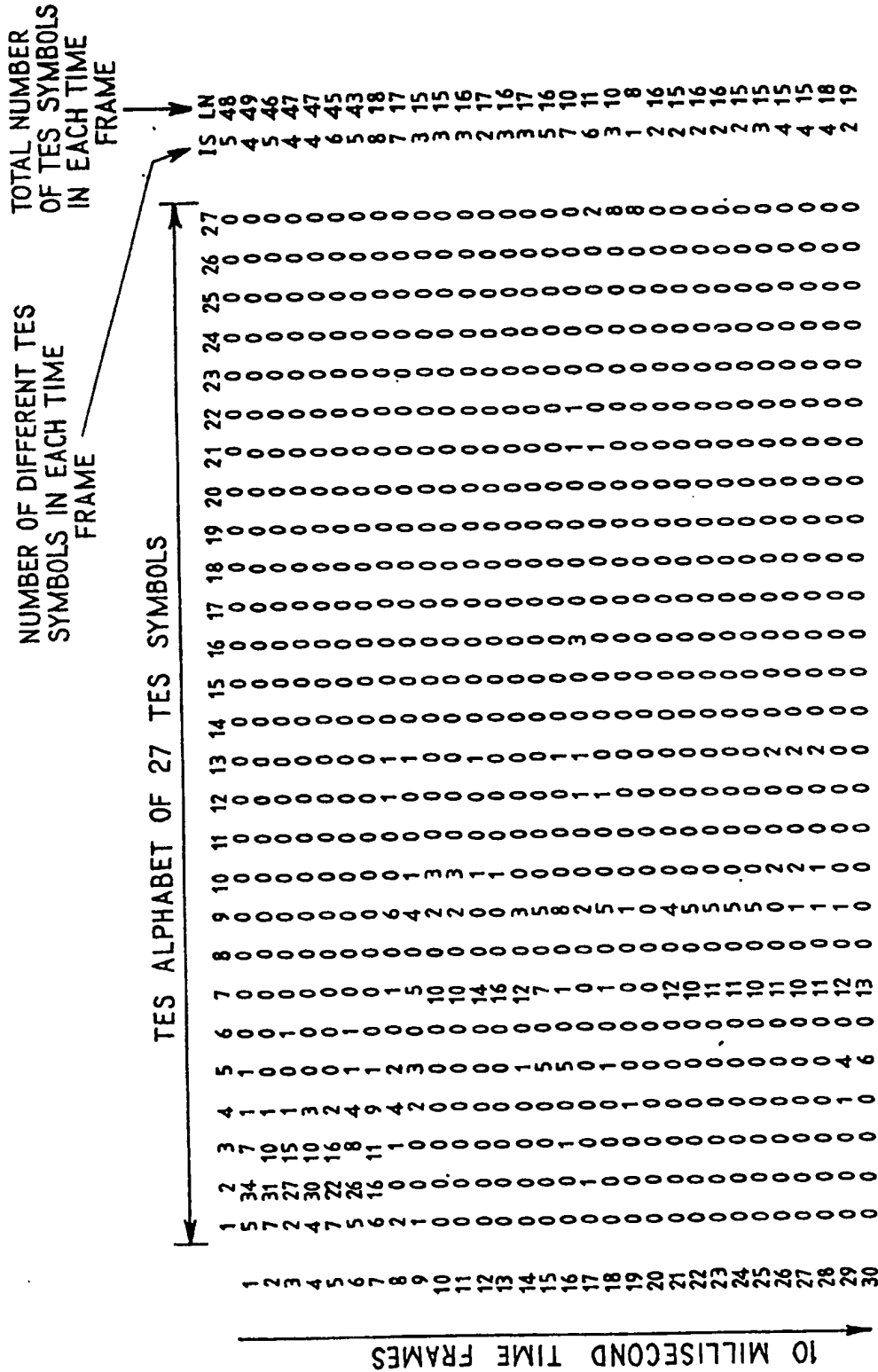


FIG. 2.

SPECIFICATION

Encoding method

5 The present invention relates to an encoding method for an analogue waveform, and in particular, but not exclusively, to an encoding method for an analogue waveform representing speech.

Electrical waveforms derived from human speech
10 are complex in character, having significant components extending from below 300 Hz, to above 3kHz and a wide dynamic range. Such waveforms may be converted into streams of digital data by known methods such as Pulse Code Modulation (PCM), Delta
15 Modulation or Time Encoding. In PCM, the analogue speech waveform is sampled and a digital code is assigned to each sample to indicate the instantaneous amplitude of the analogue waveform at the time the sample was taken. However, to obtain acceptable
20 quality the sampling rate must be at least double the bandwidth of the waveform. Furthermore, the digital code indicating amplitude normally comprises at least an 8 bit code. Hence, assuming a bandwidth of 3kHz for the speech waveform, it can be seen that the digital
25 data stream will contain 48 k bits/second. In most commercial applications 64 k bits/second are generated as the bandwidth is taken as 4 kHz.

In Delta Modulation the analogue speech waveform is sampled, as with PCM. A single bit descriptor code is
30 then assigned to each sample in order to describe the amplitude of the sample with respect to the preceding sample. However, as a single bit descriptor code is used it is necessary to use a higher sample rate than PCM and, for commercial applications, a sample rate
35 of at least 32 k bits/second is necessary. Hence, the digital data stream generated will contain 32 k bits/second.

In Time Encoding, the locations of the real zeros in the analogue waveform are determined by quantising
40 in the time domain. The shape of the waveform between successive zeros is then determined by studying the number of events, e.g. maxima or minima, in the waveform between successive real zeros. A series of coded symbols is generated by
45 grouping the successive zeros with their associated events. These symbols are known as TES symbols, and the analogue speech waveform can be reconstructed from them.

Since the analogue speech waveform is of restricted
50 bandwidth only a limited number of coded symbols are necessary. For example, in a speech waveform having a bandwidth of 300 Hz to 3.3 kHz with a sampling rate of 20k samples/second, only a limited variation in half cycle durations can occur. At the
55 highest frequency, 3.3 kHz, the half cycle duration is approximately 3 quanta, at the lowest frequency, 300 Hz, the half cycle duration is approximately 34 quanta. By applying mapping logic it has been found that an alphabet of about 27 TES symbols can be used to
60 define the analogue speech waveform. As there are fewer than 32 symbols, a 5 bit constant length (linear) binary word may be allocated to represent each TES

symbol. Hence, the TES symbol stream is represented by a digital data stream of 5 bit constant length (linear) data words. In practice, however, additional data may be included, such as amplitude information so that
70 each symbol would be represented by a (5 + n) bit constant length (linear) data word, where n is normally a 1 to 3 bit code word. The principles of Time Encoded Speech (TES) are described in detail in UK Patent No. 2020517. By adopting Time Encoding it is
75 possible to represent an analogue speech waveform by a digital data stream having a bit rate of approximately 12k bits/second, whilst maintaining acceptable quality.

It is often desirable to store digitally encoded speech
80 but it can be seen that, with existing methods of encoding, large memories are required to store relatively short periods of speech because of the number of bits of digital information to be stored per second of the analogue speech waveform. In order to
85 reduce memory requirements, a reduction in the bit rate of the digital data stream is both desirable and necessary.

It is an object of the present invention to provide a method of encoding data whereby the bit rate of the digital data stream representing the data is reduced
90 substantially from that obtained with existing methods. The method of the present invention is, therefore, particularly applicable when it is required to store speech in digital form. Furthermore, in transmission by line or radio the lower bit rate means that a
95 narrower bandwidth is required for transmission. If a narrower bandwidth is not adopted the time required to transmit a given quantity of data is reduced, which may be particularly advantageous when the data is to
100 be transmitted by telephone line link.

According to the present invention there is provided an encoding method for an analogue waveform, the method comprising deriving a digital data stream from the analogue waveform, dividing the digital data
105 stream into a number of successive time frames of equal time period, storing the digital data in respect of successive time frames, deriving a stream of time encoded symbols from the analogue waveform, dividing the stream of time encoded symbols into
110 successive time frames corresponding to the successive time frames of the digital data stream, storing the time encoded symbols for successive time frames, determining and comparing the distribution of the time encoded symbols for successive time frames,
115 and reconstructing a digital data stream from the digital data stored and derived digital data which is dependent upon the results of the comparison of the time encoded symbols for successive time frames.

Preferably the time frames are of 10 to 20 mil-
120 lisecond time period.

The digital data derived from that stored in respect of one or more time frames may comprise digital data stored in the immediately preceding time frame.

The reconstructed digital data stream may be
125 stored.

The reconstructed digital data stream may be transmitted.

The digital data stream may be derived from the analogue waveform by pulse code modulation.

The digital data stream may be derived from the analogue waveform by delta modulation.

- 5 The digital data stream may be derived from the analogue waveform by time encoding.

The digital data stream may be derived from the analogue waveform by any other method of digital encoding,

- 10 The present invention will now be described, by way of example, with reference to the accompanying drawings in which:—

Figure 1 shows a flow chart illustrating an encoding method in accordance with the present invention, and

- 15 Figure 2 shows a table illustrating the distribution of time encoded symbols representing a short period of speech.

- Referring to the drawings, an analogue waveform, for example an analogue speech waveform, is digitized into a digital data stream by any known method such as for example Pulse Code Modulation, Delta Modulation, or Time Encoding. The digital data stream is then divided into a number of successive time frames of equal time period and stored. In this example a 10 millisecond time period has been chosen but time periods of longer or shorter duration may also be adopted. Any store suitable for storing quantities of digital information may be used to store the time frames of digital data. The division of the digital data stream into the successive time frames may be achieved by gating at the required 10 millisecond time intervals.

- The analogue speech waveform is also time encoded into a stream of TES symbols. Apparatus suitable for this purpose is described in UK Patent 2020517. The stream of TES symbols is also divided into a number of successive time frames of equal time period and stored such that the time frames stored in respect of the TES symbol stream correspond both in time and duration to the time frames stored in respect of the digital data stream.

- The distributions of the TES symbols stored in respect of successive time frames are now determined and compared. As previously mentioned the TES alphabet may consist of 27 TES symbols and hence, each stored TES symbol may be represented by a 5 bit binary word. The identity of each TES symbol stored in respect of successive time frames can, therefore, be determined easily by reading the stored 5 bit binary words. The frequency with which any TES symbol occurs may then be determined by incrementing a counter each time a particular 5 bit binary word is recognised. In this way a table can be formulated which shows, for successive time frames, the distribution of the stored TES symbols. The information contained in the table can be generated and stored in any apparatus suitable for this purpose, such as a computer.

- Figure 2 illustrates the information which could be contained in such a table. Figure 2 shows clearly the distribution of the TES symbols in any time frame. In time frame 1 for example, which represents the TES symbols generated by time encoding 10 milliseconds of speech, it can be seen that only TES symbols 1 to 5 were derived and that TES symbol 2 occurred most

frequently.

- The distribution of the TES symbols in successive time frames is now compared. It can be seen from Figure 2 that there is a little change in the frequency with which the TES symbols occur in time frames 1 to 7 and hence there is a little change in the distribution of the TES symbols in these time frames. This restricted change in distribution indicates that, in the speech waveform from which the TES symbols were derived, there was little change in the character of the speech which occurred in time frames 1 to 7. However, it will be seen that the TES symbol distribution in time frames 8 and 9 differ from the preceding time frames and from each other which indicates a transition from one speech sound to another. Time frame 11 is identical to that of time frame 10 which indicates that the character of the speech was essentially constant for this 20 millisecond period. Although the TES symbols stored in respect of time frames 10 and 11 are identical, the digital data stored in respect of the same time frames of the digital data stream produced for example by Pulse Code Modulation may differ greatly in view of the sampling rate and the binary codes allocated for each sample.

- It has been determined by analysing segmented TES symbol streams derived from speech that the TES symbol distribution may remain substantially constant through several 10 millisecond time periods indicating the occurrence of considerable repetition redundancy and the encoding method of the present invention proposes to reconstruct the digital data stream in dependence upon the results of the comparison between the TES symbols stored in respect of successive time frames of the TES symbol stream to eliminate a proportion of this repetition redundancy.

- The digital data stream is reconstructed by recalling the digital data stored in respect of the successive time frames. However, the digital data stored in respect of any particular successive time frame is not recalled until the distribution of the TES symbols stored in respect of that time frame has been compared with the distribution of the TES symbols stored in respect of one or more preceding time frames. The results of this comparison then determine whether the digital data in the particular time frame is recalled to form part of the reconstructed digital data stream or whether the digital data in that time frame is substituted by other digital data, for example a repeat signal to indicate that the repetition of a previous time frame, with a similar TES symbol distribution may be substituted. This repeated digital data may consist of the digital data stored in respect of a preceding time frame if the TES symbol distribution between the two time frames is substantially identical or it may consist of digital data which is derived from the digital data stored in respect of several preceding time frames if the difference in the TES symbol distribution in these preceding time frames is within pre-determined limits.

- This procedure may be seen more clearly with reference to Figure 2.

- Referring firstly to time frames 10 and 11, if a comparison is made between the TES symbol distribution in these frames it will be recognised that the distributions for the two time frames are identical. As

a result of this comparison the digital data stored in respect of time frame 11 would not be recalled and a repeat signal would be generated indicating that the digital data stored in respect of time frame 10 is to be repeated to replace the data stored in respect of time frame 11.

This repeat signal would replace the data stored in respect of time frame 11 and hence, the bit rate of the encoded digital data stream would be reduced in comparison to the bit rate of the digital data stream derived from digitizing the analogue speech waveform by known methods, such as PCM.

Referring now to time frames 1 to 7 shown in figure 2, if a comparison is made between the TES symbol distribution it can be seen there is little change between time frames 1 to 7. However, as there are several time frames having similar TES symbol distribution it may not be possible to repeat any one of these time frames seven times without affecting the character of the speech reconstructed from the encoded data. Hence, the reconstructed or encoded data stream could consist of the repetition of the digital data stored in respect of a selected smaller number of these time frames with a repeat signal generated to indicate when the repetition of a selected time frame is to occur. In this manner the repeated time frames are substituted in the encoded data stream by the repeat signals thereby effecting a reduction in the bit rate of the data stream whilst maintaining the character of any speech reconstructed from the data.

With regard to time frames 7, 8 and 9 in Figure 2, it can be seen that these frames differ considerably from each other and therefore, a repeat strategy would not be adopted for these frames since the comparison of the TES symbol distribution in these frames would not show sufficient similarity.

With reference to time frames 21 to 30 in Figure 2 it can be seen that the TES symbol distribution in time frames 21 to 25 is almost identical, there being minor variations in the frequency of TES symbols 7 and 9. As a result, the digital data stored in respect of time frames 21 to 25 would not be recalled and could be substituted in the reconstructed digital data stream by repeat signals indicating when a selected time frame is to be repeated, as previously described in relation to time frames 1 to 7. A similar procedure may be applied to segments 26 to 28 and segments 29 and 30 as the variations in TES symbol distribution in these time frames are also slight. The digital data which is substituted into the reconstructed digital data stream may be derived according to predetermined guidelines which enable the maximum possible reduction in the bit rate whilst maintaining acceptable quality in the reconstructed speech.

Therefore, by adopting the method of the present invention the analogue speech waveform is encoded into a stream of digital data which may comprise sections of digital data derived directly by known methods such as PCM interleaved with frames of digital data derived in dependence upon the results of the comparison made on the TES symbol distribution stored in respect of successive time frames.

The reconstructed digital data stream may be either transmitted or stored for subsequent transmission by

known methods.

The method of the present invention is also applicable when the digital data stream comprises a TES digital data stream. In this case the presence of repeat signals may preferably indicate that, for example, selected TES symbols or groups of TES symbols may be omitted throughout the time frames being compared to reduce the transmission bit rate. On reception or reconstruction the remaining TES symbols or groups of TES symbols may be repeated to replace those symbols or groups of symbols selected for omission in order to reconstruct an acceptable version of the original speech waveform.

Furthermore, the present invention has been described with reference to first order probability distribution but it should be understood that higher order probability distribution or alternative probability distribution may equally be used to advantage with the present invention.

CLAIMS

1. An encoding method for an analogue waveform, the method comprising deriving a digital data stream from the analogue waveform, dividing the digital data stream into a number of successive time frames of equal time period, storing the digital data in respect of successive time frames, deriving a stream of time encoded symbols from the analogue waveform, dividing the stream of time encoded symbols into successive time frames corresponding to the successive time frames of the digital data stream, storing the time encoded symbols for successive time frames, determining and comparing the distribution of the time encoded symbols for successive time frames, and reconstructing a digital data stream from the digital data stored and derived digital data which is dependent upon the results of the comparison of the time encoded symbols for successive time frames.

2. A method according to claim 1 wherein the derived digital data comprises a repeat signal for indicating that, when the reconstructed data stream is to be decoded, the digital data stored in respect of any time frame is to be repeated.

3. A method according to claim 1 wherein the derived digital data for a particular time frame comprises the digital data stored in respect of the time frame immediately preceding the particular time frame.

4. A method according to claim 1 wherein the derived digital data comprises digital data which is derived from the digital data stored in respect of one or more time frames.

5. A method according to any one of the preceding claims wherein the time frames are of 10 to 20 millisecond time period.

6. A method according to any one of the preceding claims wherein the reconstructed digital data stream is stored.

7. A method according to any one of claims 1 to 5 wherein the reconstructed digital data stream is transmitted.

8. A method according to claim 2 wherein the digital data stream derived from the analogue waveform comprises a stream of time encoded symbols and the repeat signal is for indicating that selected time encoded symbols or groups of symbols in the

digital data stream are to be omitted or repeated in the reconstructed digital data stream.

9. A method according to any one of claims 1 to 7 wherein the digital data stream is derived from the analogue waveform by pulse code modulation.

10. A method according to any one of claims 1 to 7 wherein the digital data stream is derived from the analogue waveform by delta modulation.

11. A method according to any one of the preceding claims wherein the analogue waveform comprises a speech waveform.

12. An encoding method substantially as hereinbefore described with reference to the accompanying drawings.

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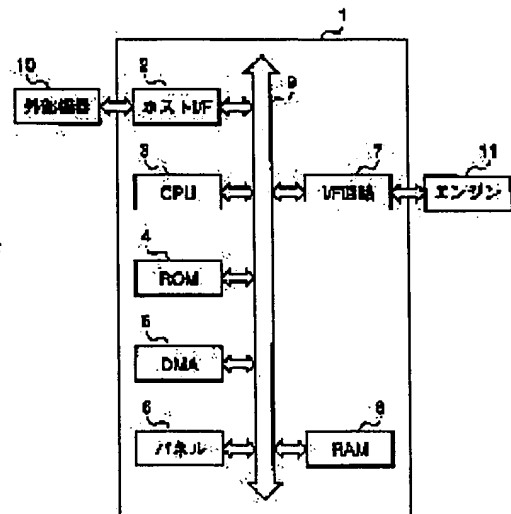
(21)Application number : 08-018068 (71)Applicant : CANON INC
(22)Date of filing : 09.01.1996 (72)Inventor : WAKANA TORU

(54) PRINTER AND DATA COMPRESSING METHOD THEREIN

(57)Abstract:

PROBLEM TO BE SOLVED: To provide a printer capable of enhancing a compression ratio by selecting a compression method fitted to data from a plurality of compression methods to perform compression and the data compressing method in the printer.

SOLUTION: A laser beam printer is equipped with an ROM 4 storing a plurality of preset compression methods and a CPU 3 having a data kind discriminating function analyzing the command of received data and discriminating the kind of data on the basis of the analytical result, a compression method selecting function selecting the compression method fitted to the kind of the discriminated data from a plurality of the compression methods stored in the ROM 4 and data compressing function compressing the data on the basis of the selected compression method.



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[Date of final disposal for application]

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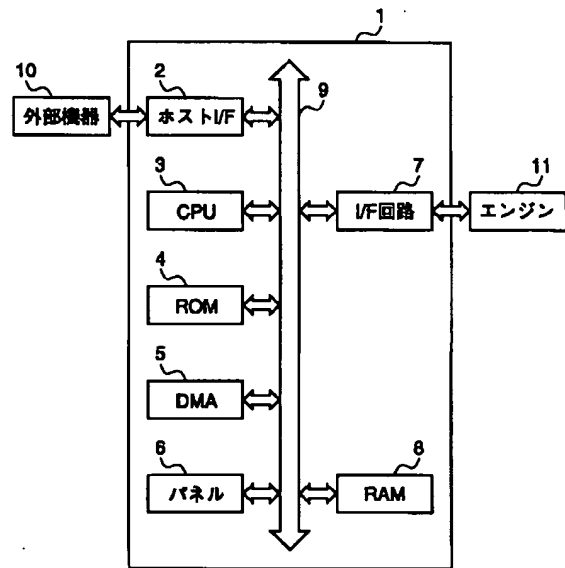
(21)出願番号	特願平8-18068	(71)出願人	000001007 キヤノン株式会社 東京都大田区下丸子3丁目30番2号
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		(74)代理人	弁理士 渡部 敏彦

(54)【発明の名称】 印刷装置及び印刷装置におけるデータ圧縮方法

(57)【要約】

【課題】 複数の圧縮方法の中からデータに適合した圧縮方法を選択して圧縮を行うことにより圧縮率を向上させることを可能とした印刷装置及び印刷装置におけるデータ圧縮方法を提供する。

【解決手段】 レーザビームプリンタは、予め設定された複数の圧縮方法を記憶したROM4と、受信したデータのコマンドを解析すると共に当該解析結果に基づきデータの種別を判別するデータ種別判別機能、判別したデータの種別に適合した圧縮方法をROM4に記憶された複数の圧縮方法から選択する圧縮方法選択機能、及び選択した圧縮方法に基づきデータの圧縮を行うデータ圧縮機能を有するCPU3とを具備する。



【特許請求の範囲】

【請求項1】 外部機器等から受信したデータの圧縮を行うようにした印刷装置において、

予め設定された複数の圧縮方法を記憶した圧縮方法記憶手段と、受信したデータのコマンドを解析すると共に当該解析結果に基づきデータの種別を判別するデータ種別判別手段と、判別したデータの種別に適合した圧縮方法を前記圧縮方法記憶手段に記憶された複数の圧縮方法から選択する圧縮方法選択手段と、選択した圧縮方法に基づきデータの圧縮を行うデータ圧縮手段とを具備することを特徴とする印刷装置。

【請求項2】 外部機器等から受信したデータの圧縮を行うようにした印刷装置において、

予め設定された複数の圧縮方法を記憶した圧縮方法記憶手段と、受信したデータを展開してオブジェクトを生成するオブジェクト生成手段と、生成したオブジェクトの形態をサーチすると共に当該サーチしたオブジェクトの形態に適合した圧縮方法を前記圧縮方法記憶手段に記憶された複数の圧縮方法から選択する圧縮方法選択手段と、選択した圧縮方法に基づきデータの圧縮を行うデータ圧縮手段とを具備することを特徴とする印刷装置。

【請求項3】 外部機器等から受信したデータの圧縮を行うようにした印刷装置におけるデータ圧縮方法において、

受信したデータのコマンドを解析すると共に当該解析結果に基づきデータの種別を判別するデータ種別判別工程と、判別したデータの種別に適合した圧縮方法を予め設定された複数の圧縮方法から選択する圧縮方法選択工程と、選択した圧縮方法に基づきデータの圧縮を行うデータ圧縮工程とを有することを特徴とする印刷装置におけるデータ圧縮方法。

【請求項4】 外部機器等から受信したデータの圧縮を行うようにした印刷装置におけるデータ圧縮方法において、

受信したデータを展開してオブジェクトを生成するオブジェクト生成工程と、生成したオブジェクトの形態をサーチすると共に当該サーチしたオブジェクトの形態に適合した圧縮方法を予め設定された複数の圧縮方法から選択する圧縮方法選択工程と、選択した圧縮方法に基づきデータの圧縮を行うデータ圧縮工程とを有することを特徴とする印刷装置におけるデータ圧縮方法。

【発明の詳細な説明】

【0001】

【発明の属する技術分野】本発明は、印刷装置及び印刷装置におけるデータ圧縮方法に係り、更に詳しくは、外部機器等から受信したデータを当該データに適合した圧縮方法で圧縮することにより圧縮率の向上を図る場合に好適な印刷装置及び印刷装置におけるデータ圧縮方法に関する。

【0002】

【従来の技術】従来、コンピュータ等の外部機器へ接続されるプリンタ等の印刷装置としては、外部機器から接続ケーブル等を介して受信した多数のデータをまとめてファイル全体の量を減らす、いわゆる圧縮（データ圧縮）機能を有する印刷装置がある。この種の印刷装置においては、外部機器から受信した何等かのデータに対して圧縮を行う場合、予め決定されている圧縮方法を用いてデータの圧縮を行っていた。

【0003】

【発明が解決しようとする課題】しかしながら、従来の印刷装置においては、上述した如く外部機器から受信したデータの圧縮は予め決定されている圧縮方法を用いて行っているため、データの種別やデータの形式によっては、圧縮を行った場合でも圧縮率がそれほど上がらないデータも存在するという問題があった。

【0004】本発明は、上述した点に鑑みなされたものであり、複数の圧縮方法の中からデータに適合した圧縮方法を選択して圧縮を行うことにより圧縮率を向上させることを可能とした印刷装置及び印刷装置におけるデータ圧縮方法を提供することを目的とする。

【0005】

【課題を解決するための手段】上記目的を達成するため、請求項1の発明は、外部機器等から受信したデータの圧縮を行うようにした印刷装置において、予め設定された複数の圧縮方法を記憶した圧縮方法記憶手段と、受信したデータのコマンドを解析すると共に当該解析結果に基づきデータの種別を判別するデータ種別判別手段と、判別したデータの種別に適合した圧縮方法を前記圧縮方法記憶手段に記憶された複数の圧縮方法から選択する圧縮方法選択手段と、選択した圧縮方法に基づきデータの圧縮を行うデータ圧縮手段とを具備することを特徴とする。

【0006】上記目的を達成するため、請求項2の発明は、外部機器等から受信したデータの圧縮を行うようにした印刷装置において、予め設定された複数の圧縮方法を記憶した圧縮方法記憶手段と、受信したデータを展開してオブジェクトを生成するオブジェクト生成手段と、生成したオブジェクトの形態をサーチすると共に当該サーチしたオブジェクトの形態に適合した圧縮方法を前記圧縮方法記憶手段に記憶された複数の圧縮方法から選択する圧縮方法選択手段と、選択した圧縮方法に基づきデータの圧縮を行うデータ圧縮手段とを具備することを特徴とする。

【0007】上記目的を達成するため、請求項3の発明は、外部機器等から受信したデータの圧縮を行うようにした印刷装置におけるデータ圧縮方法において、受信したデータのコマンドを解析すると共に当該解析結果に基づきデータの種別を判別するデータ種別判別工程と、判別したデータの種別に適合した圧縮方法を予め設定された複数の圧縮方法から選択する圧縮方法選択工程と、選

択した圧縮方法に基づきデータの圧縮を行うデータ圧縮工程とを有することを特徴とする。

【0008】上記目的を達成するため、請求項4の発明は、外部機器等から受信したデータの圧縮を行うようにした印刷装置におけるデータ圧縮方法において、受信したデータを展開してオブジェクトを生成するオブジェクト生成工程と、生成したオブジェクトの形態をサーチすると共に当該サーチしたオブジェクトの形態に適合した圧縮方法を予め設定された複数の圧縮方法から選択する圧縮方法選択工程と、選択した圧縮方法に基づきデータの圧縮を行うデータ圧縮工程とを有することを特徴とする。

【0009】

【発明の実施の形態】以下、本発明の実施の形態を図面を参照して説明する。

【0010】(1)第1の実施の形態

先ず、第1の実施の形態に係る印刷装置としてのレーザビームプリンタ(以下LBPと略称)の内部構成を図2に基づき説明する。LBPは、LBP本体21と、操作パネル22と、プリンタ制御ユニット23と、レーザドライバ24と、半導体レーザ25と、回転多面鏡26と、反射鏡27と、静電ドラム28と、現像ユニット29と、用紙カセット30と、給紙ローラ31と、搬送ローラ32と、搬送ローラ33とを備える構成となっている。LBPは、データ源(図示略)から文字パターンの登録や定型書式(フォームデータ)等の登録を行うことができるようになっている。

【0011】上記各部の構成及び機能を詳述すると、LBP本体21は、LBPの外部に接続されているホストコンピュータ(図1参照)から供給される文字情報(文字コード)、フォーム情報、マクロ命令等を入力して記憶すると共に、これらの情報に基づき対応する文字パターンやフォームパターン等を作成し、記録媒体である記録紙上に像を形成する。操作パネル22は、操作者が各種操作を行うためのスイッチや、メッセージ等を表示する例えばLED表示器等の表示部を備えている。プリンタ制御ユニット23は、LBP本体21の全体を制御するものであり、ホストコンピュータから供給される文字情報等を解析し、主に文字情報を対応する文字パターンのビデオ信号に変換してレーザドライバ24へ出力する。

【0012】レーザドライバ24は、半導体レーザ25を駆動するための回路であり、プリンタ制御ユニット23から入力されたビデオ信号に応じて半導体レーザ25から発射されるレーザ光Hのオン/オフ切り替えを行う。半導体レーザ25は、レーザドライバ24による駆動に基づき回転多面鏡26へ向けてレーザ光Hを発射する。回転多面鏡26は、半導体レーザ25から発射されたレーザ光Hを水平方向へ振ることによりレーザ光Hを反射鏡27へ入光させる。反射鏡27は、回転多面鏡2

6を介して入光されたレーザ光Hを反射し、静電ドラム28の表面に照射する。静電ドラム28は、回転多面鏡26及び反射鏡27を介して照射されたレーザ光Hが当該静電ドラム28上に走査されることにより、当該静電ドラム28上には文字パターンの静電潜像が形成される。

【0013】現像ユニット29は、静電ドラム28の周囲に配置されており、静電ドラム28上に形成された静電潜像を現像するものであり、現像された静電潜像は記録紙へ転写される。用紙カセット30は、LBP本体21に着脱自在に装着されており、複数枚のカットシート記録紙が収納されるものである。給紙ローラ31は、用紙カセット30に収納されているカットシート記録紙を1枚ずつLBP本体21の内部へ取り込む。搬送ローラ32及び搬送ローラ33は、給紙ローラ31によりLBP本体21内部へ取り込まれたカットシート記録紙を静電ドラム28へ供給する。

【0014】次に、第1の実施の形態に係るLBPのプリンタコントローラを中心とした構成を図1に基づき説明する。プリンタコントローラ1は、上述したプリンタ制御ユニット23に装備されており、ホストI/F(インタフェース)2と、CPU3と、ROM4と、DMA(Direct Memory Acces)5と、パネル部6と、I/F(インタフェース)回路7と、RAM8と、アドレスデータバス9とを備える構成となっている。また、プリンタコントローラ1には、ホストコンピュータ等の外部機器10とエンジン11とが接続されている。

【0015】上記各部の構成及び機能を詳述すると、ホストI/F2は、受信バッファ部を備えており、外部機器10とデータの送受を行う。CPU3は、プログラムに基づきプリンタコントローラ1各部を制御する。ROM4は、プリンタコントローラ制御等を行うプログラムや、後述する複数の圧縮方法(圧縮方法1, 2, 3)に係るデータを格納している。DMA5は、CPU3に制御される。パネル部6は、上述した操作パネル22のスイッチやLED表示器に接続されている。I/F回路7は、エンジン11へ送出するデータを格納しておくための出力バッファ部を備えている。RAM8は、各種データを記憶する。アドレスデータバス9は、上記各部の信号の伝送が行われる。

【0016】次に、第1の実施の形態に係るデータ圧縮処理を図3のフローチャートに基づき説明する。

【0017】外部機器10がLBPのプリンタコントローラ1へ所定のデータを送信すると(ステップSA1)、プリンタコントローラ1のCPU3はホストI/F2の受信バッファ部を介してデータを受信し(ステップSA2)、受信したデータの命令の解析を行う(ステップSA3)。この場合、前記命令にはデータの種類の分別が可能な命令が含まれているものとする。尚、データの種類とは、例えば文字データ、多値

データ、2値データ等を指している。

【0018】プリンタコントローラ1のCPU3は上記データのコマンドの解析を行った後、当該解析結果に基づきデータの種別を判定し(ステップSA4)、後述するようにデータの種別に応じて圧縮方法を分ける。本実施の形態では、データの種別としては文字データ、多値データ、2値データのみを扱うものとするが、これに限定されるものではない。

【0019】プリンタコントローラ1のCPU3は上記ステップSA4においてデータの種別が文字データであると判定した場合は、ROM4に予め設定記憶されている複数の圧縮方法の中から文字データに有効な圧縮方法を検索し(ステップSA5)、文字データの圧縮方法として圧縮方法1を選択する(ステップSA6)。

【0020】また、プリンタコントローラ1のCPU3は上記ステップSA4においてデータの種別が多値データであると判定した場合は、ROM4に予め設定記憶されている複数の圧縮方法の中から多値データに有効な圧縮方法を検索し(ステップSA7)、多値データの圧縮方法として圧縮方法2を選択する(ステップSA8)。

【0021】また、プリンタコントローラ1のCPU3は上記ステップSA4においてデータの種別が2値データであると判定した場合は、ROM4に予め設定記憶されている複数の圧縮方法の中から2値データに有効な圧縮方法を検索し(ステップSA9)、2値データの圧縮方法として圧縮方法3を選択する(ステップSA10)。

【0022】そして、プリンタコントローラ1のCPU3はデータの種別が文字データである場合は、上記ステップSA6で選択した圧縮方法1を用いて文字データの圧縮を行い、データの種別が多値データである場合は、上記ステップSA8で選択した圧縮方法2を用いて多値データの圧縮を行い、データの種別が2値データである場合は、上記ステップSA10で選択した圧縮方法3を用いて2値データの圧縮を行い(ステップSA11)、本処理を終了する(ステップSA12)。

【0023】尚、第1の実施の形態では、圧縮方法として3つの圧縮方法(圧縮方法1、2、3)を例に上げたが、圧縮方法は3つに限定されるものではなく任意の個数とすることができる。

【0024】上述したように、第1の実施の形態によれば、LBPは、予め設定された複数の圧縮方法を記憶したROM4と、受信したデータのコマンドを解析すると共に当該解析結果に基づきデータの種別を判別するデータ種別判別機能、判別したデータの種別に適合した圧縮方法をROM4に記憶された複数の圧縮方法から選択する圧縮方法選択機能、及び選択した圧縮方法に基づきデータの圧縮を行うデータ圧縮機能を有するCPU3とを具備しているため、データに適合した圧縮方法を選択して圧縮を行うことが可能となり、圧縮率を向上させるこ

とができる。これにより、従来の如く、データの種別や形式によっては圧縮を行った場合に圧縮率がそれほど上がらないデータが存在するといった不具合を解消することができる。

【0025】(2)第2の実施の形態

第2の実施の形態に係るLBPは、上記第1の実施の形態と同様に、LBP本体21と、操作パネル22と、プリンタ制御ユニット23と、レーザドライバ24と、半導体レーザ25と、回転多面鏡26と、反射鏡27と、静電ドラム28と、現像ユニット29と、用紙カセット30と、給紙ローラ31と、搬送ローラ32と、搬送ローラ33とを備える構成となっている(上記図2参照)。

【0026】また、第2の実施の形態に係るプリンタコントローラ1は、上記第1の実施の形態と同様に、ホストI/F2と、CPU3と、ROM4と、DMA5と、パネル部6と、I/F回路7と、RAM8と、アドレスデータバス9とを備える構成となっている。プリンタコントローラ1には、ホストコンピュータ等の外部機器10とエンジン11とが接続されている(上記図1参照)。上記各部の詳細構成については、上記第1の実施の形態と同様であるため説明は省略する。

【0027】次に、第2の実施の形態に係るデータ圧縮処理を図4のフローチャートに基づき説明する。

【0028】外部機器10がLBPのプリンタコントローラ1へ所定のデータを送信すると(ステップSB1)、プリンタコントローラ1のCPU3はホストI/F2の受信バッファ部を介してデータを受信し(ステップSB2)、受信したデータのコマンドを解析すると共に当該コマンドに応じたデータ処理を行う(ステップSB3)。この場合、前記データにはコマンド等が含まれているものとする。

【0029】プリンタコントローラ1のCPU3は上記データ処理を行った後、データを展開してオブジェクト(データの値とそれに関する手続きを合わせたもの)を生成する(ステップSB4)。この場合、オブジェクトには文字データ、多値データ、2値データ等が含まれているものとする。

【0030】プリンタコントローラ1のCPU3は上記オブジェクトの生成を行った後、当該生成したオブジェクトの形態をサーチし、サーチしたオブジェクトの形態に適切な圧縮方法を判定する(ステップSB5)。この場合、圧縮方法は、ROM4に複数記憶されており、或るパターンに対していかなる圧縮方法が有効であるかが予め決定されているものとする。尚、オブジェクトの形態のサーチの仕方は問わない。

【0031】プリンタコントローラ1のCPU3は上記ステップSB5においてサーチしたオブジェクトの形態に適切な圧縮方法が圧縮方法1であると判定した場合は、当該圧縮方法1を選択する(ステップSB6)。

【0032】また、プリンタコントローラ1のCPU3は上記ステップSB5においてサーチしたオブジェクトの形態に適切な圧縮方法が圧縮方法2であると判定した場合は、当該圧縮方法2を選択する（ステップSB7）。

【0033】また、プリンタコントローラ1のCPU3は上記ステップSB5においてサーチしたオブジェクトの形態に適切な圧縮方法が圧縮方法Nであると判定した場合は、当該圧縮方法3を選択する（ステップSB8）。

【0034】そして、プリンタコントローラ1のCPU3は、上記ステップSB6または上記ステップSB7または上記ステップSB8で選択した圧縮方法を用いてデータの圧縮を行い（ステップSB9）、本処理を終了する（ステップSB10）。

【0035】尚、第2の実施の形態では、オブジェクトの種類としては3つの場合を例に上げたが、これに限定されるものではなく、オブジェクトの種類は任意の個数とすることができる。また、オブジェクトと圧縮方法を1対1に対応させているが、これに限定されるものではない。また、オブジェクトの形態をサーチする方法としては、オブジェクトの一部分をサーチする方法或いはオブジェクトの全部をサーチする方法の何れでもよい。

【0036】上述したように、第2の実施の形態によれば、LBPは、予め設定された複数の圧縮方法を記憶したROM4と、受信したデータを展開してオブジェクトを生成するオブジェクト生成機能、生成したオブジェクトの形態をサーチすると共に当該サーチしたオブジェクトの形態に適合した圧縮方法をROM4に記憶された複数の圧縮方法から選択する圧縮方法選択機能、及び選択した圧縮方法に基づきデータの圧縮を行うデータ圧縮機能を有するCPU3とを具備しているため、データを展開したオブジェクトの形態に適合した圧縮方法を選択して圧縮を行うことが可能となり、圧縮率を向上させることができる。これにより、従来の如く、データの種類や形式によっては圧縮を行った場合に圧縮率がそれほど上がらないデータが存在するといった不具合を解消することができる。

【0037】尚、本発明は、複数の機器から構成されるシステムに適用しても、1つの機器からなる装置に適用しても良い。また、本発明は、システム或は装置にプログラムを供給することによって達成される場合にも適用できることは言うまでもない。この場合、本発明を達成するためのソフトウェアによって表されるプログラムを格納した記憶媒体を該システム或は装置に読み出すことによって、そのシステム或は装置が、本発明の効果を享受することが可能となる。

【0038】

【発明の効果】以上説明したように、請求項1の発明によれば、印刷装置は、予め設定された複数の圧縮方法を

記憶した圧縮方法記憶手段と、受信したデータのコマンドを解析すると共に解析結果に基づきデータの種類を判別するデータ種類判別手段と、判別したデータの種類に適合した圧縮方法を複数の圧縮方法から選択する圧縮方法選択手段と、選択した圧縮方法に基づきデータの圧縮を行うデータ圧縮手段とを具備しているため、データに適合した圧縮方法を選択して圧縮を行うことが可能となり、圧縮率を向上させることができる。これにより、従来の如く、データの種類や形式によっては圧縮を行った場合に圧縮率がそれほど上がらないデータが存在するといった不具合を解消することができる。

【0039】請求項2の発明によれば、印刷装置は、予め設定された複数の圧縮方法を記憶した圧縮方法記憶手段と、受信したデータを展開してオブジェクトを生成するオブジェクト生成手段と、生成したオブジェクトの形態をサーチすると共にサーチしたオブジェクトの形態に適合した圧縮方法を複数の圧縮方法から選択する圧縮方法選択手段と、選択した圧縮方法に基づきデータの圧縮を行うデータ圧縮手段とを具備しているため、データを展開したオブジェクトの形態に適合した圧縮方法を選択して圧縮を行うことが可能となり、圧縮率を向上させることができる。これにより、従来の如く、データの種類や形式によっては圧縮を行った場合に圧縮率がそれほど上がらないデータが存在するといった不具合を解消することができる。

【0040】請求項3の発明によれば、印刷装置におけるデータ圧縮方法は、受信したデータのコマンドを解析すると共に解析結果に基づきデータの種類を判別するデータ種類判別工程と、判別したデータの種類に適合した圧縮方法を予め設定された複数の圧縮方法から選択する圧縮方法選択工程と、選択した圧縮方法に基づきデータの圧縮を行うデータ圧縮工程とを有しているため、データに適合した圧縮方法を選択して圧縮を行うことが可能となり、圧縮率を向上させることができる。これにより、従来の如く、データの種類や形式によっては圧縮を行った場合に圧縮率がそれほど上がらないデータが存在するといった不具合を解消することができる。

【0041】請求項4の発明によれば、印刷装置におけるデータ圧縮方法は、受信したデータを展開してオブジェクトを生成するオブジェクト生成工程と、生成したオブジェクトの形態をサーチすると共にサーチしたオブジェクトの形態に適合した圧縮方法を予め設定された複数の圧縮方法から選択する圧縮方法選択工程と、選択した圧縮方法に基づきデータの圧縮を行うデータ圧縮工程とを有しているため、データを展開したオブジェクトの形態に適合した圧縮方法を選択して圧縮を行うことが可能となり、圧縮率を向上させることができる。これにより、従来の如く、データの種類や形式によっては圧縮を行った場合に圧縮率がそれほど上がらないデータが存在するといった不具合を解消することができる。

【図面の簡単な説明】

【図1】本発明の第1及び第2の実施の形態に係るレーザビームプリンタのプリンタコントローラを中心とした構成を示すブロック図である。

【図2】本発明の第1及び第2の実施の形態に係るレーザビームプリンタの内部構成を示す断面図である。

【図3】本発明の第1の実施の形態に係るデータ圧縮処理の流れを示すフローチャートである。

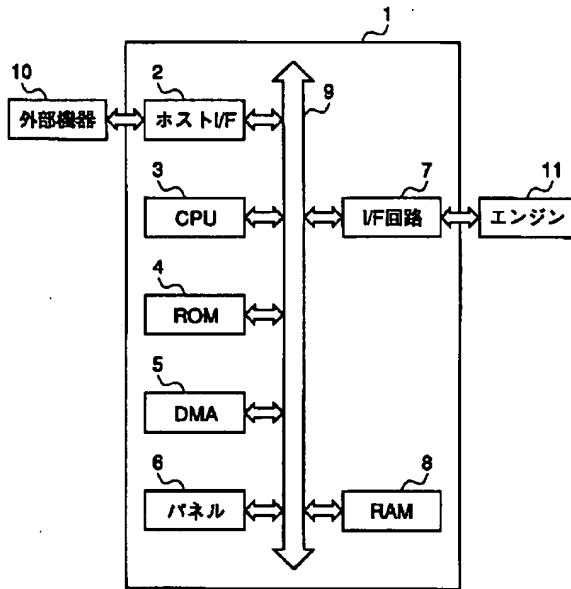
【図4】本発明の第2の実施の形態に係るデータ圧縮処

理の流れを示すフローチャートである。

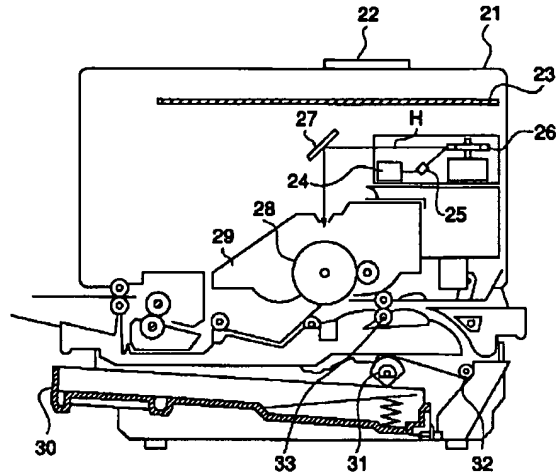
【符号の説明】

- 1 プリンタコントローラ
- 3 CPU (データ種類判別手段、圧縮方法選択手段、オブジェクト生成手段、データ圧縮手段)
- 4 ROM (圧縮方法記憶手段)
- 10 外部機器
- 21 LBP本体 (印刷装置)

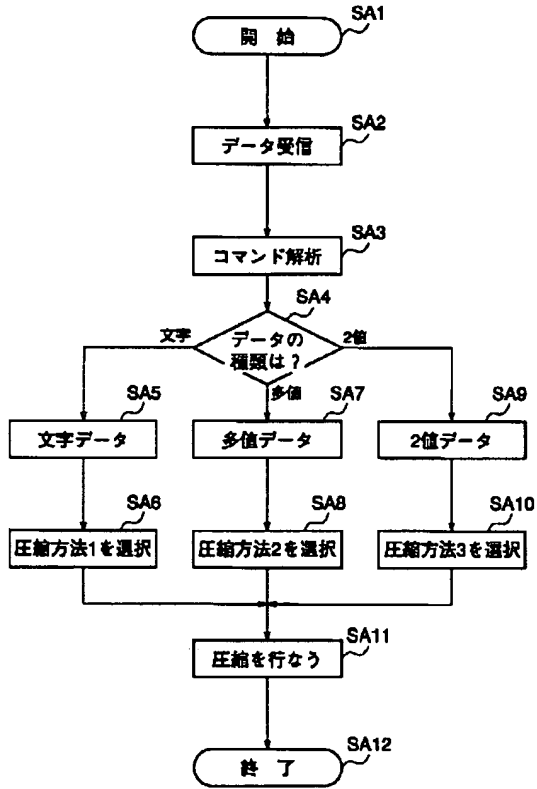
【図1】



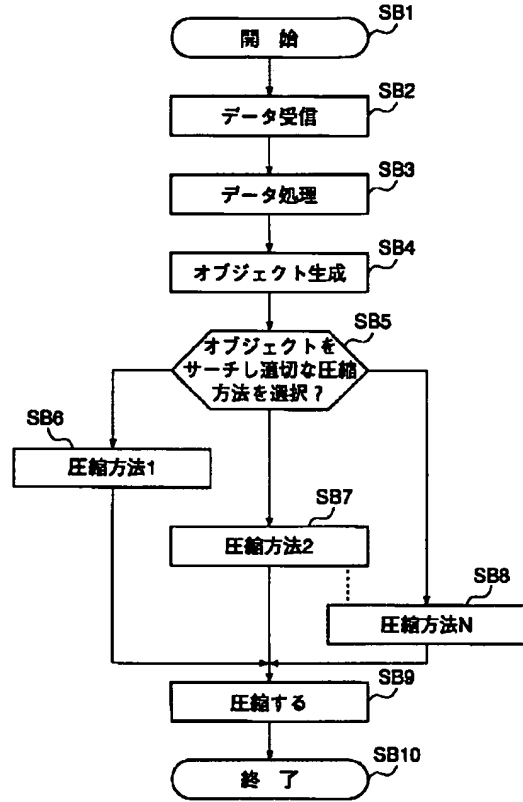
【図2】



【図3】



【図4】



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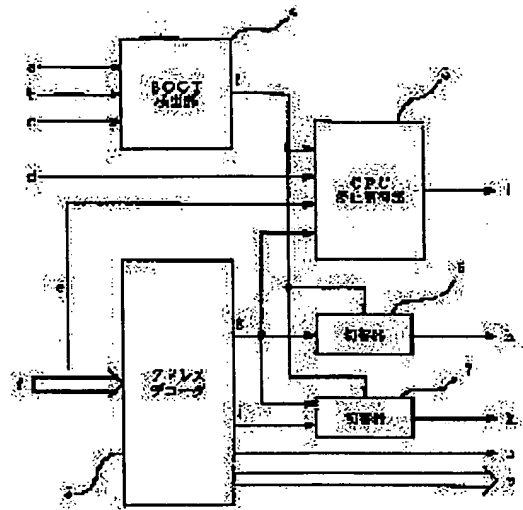
(21)Application number : 09-330983 (71)Applicant : TOYO COMMUN EQUIP CO LTD
 (22)Date of filing : 14.11.1997 (72)Inventor : TAKASE YASUHIRO

(54) BOOT LOADER CIRCUIT

(57)Abstract:

PROBLEM TO BE SOLVED: To provide a more flexible software development environment by realizing the same function with a circuit mounting an Initial Program Loader ROM in circuit constitution of a smaller scale.

SOLUTION: A BOOT loader circuit is provided with a BOOT detection part 4 for detecting whether a system becomes a BOOT mode or not, an address decoder 5 for generating a selection signal for each device, switch parts 6 and 7 for selecting ROM and the external input interface and a CPU stop control part 8 for instructing the stop of CPU various conditions.



LEGAL STATUS

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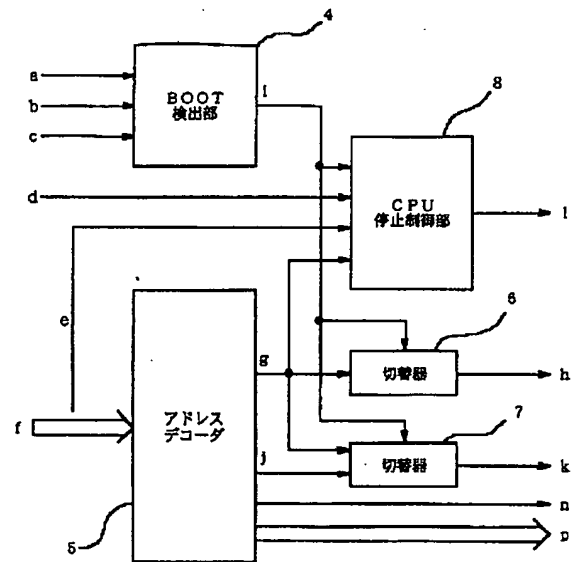
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(54)【発明の名称】 BOOTローダー回路

(57)【要約】

【課題】 電子機器は、通常CPUと、実装後に書き込み可能なROMと、外部入力インターフェースを備えた制御装置を搭載しており、さらに前記ROMとは別にIPL-ROMを搭載している。別のROMが必要な制御装置が有する欠点を除去するためになされたものであって、同等の機能をより小規模の回路構成で実現し、より柔軟な開発環境を提供することを課題とする。

【解決手段】 本発明によるBOOTローダー回路は、BOOTモードに入るかどうかを検出するBOOT検出部4と、各デバイスの選択信号を作るアドレスデコーダ5と、ROMや外部入力インターフェースを選択する切替部6、7と、各種条件でCPUの停止を指示するCPU停止制御部8とにより構成する。



【特許請求の範囲】

【請求項1】CPUと、実装後書き込み可能な不揮発性メモリ（以下ROMと称する）と、CPUの作業用RAMと、外部通信インターフェース手段を持つ制御装置において、プログラムが記憶されていない状態のROMを実装した場合又はプログラム更新のために旧プログラムに上書きする必要がある場合に、ROMの内容に依存せずに外部通信インターフェース手段を通して直接CPUに命令を与えて動作させ前記制御装置がプログラムを持っていなくてもROMに書き込むことができるように構成したことを特徴とするBOOTローダー回路。

【請求項2】CPUがROMから命令を読み出すことを検出した後にCPUが応答の遅いメモリをアクセスする時のWAIT時間を使用して、外部通信インターフェース手段を介して得たデータを命令として実行させることを特徴とする請求項1記載のBOOTローダー回路。

【請求項3】CPUがROMから命令を読み出す際CPUの動作クロックを停止させ、外部通信インターフェース手段に入力があった時点でクロックを再動作させてCPUにROMのデータの代わりに外部通信インターフェースで得たデータを命令として実行させることを特徴とする請求項1記載のBOOTローダー回路。

【発明の詳細な説明】

【0001】

【発明の属する技術分野】本発明はBOOTローダー回路に関し、特に外部通信インターフェース手段を持つ制御装置において、そのためのプログラムを保持することなくROMの書き込みを可能にしたBOOTローダー回路に関する。

【0002】

【従来の技術】例えば携帯電話等、非常に小型な電子機器においては、より小型化、軽量化にするための構成、方法が思案されている。上記電子機器には、通常CPUと、フラッシュROM等の実装後に書き込み可能なROMと、外部入力インターフェースを備えた制御装置を搭載しており、この制御装置にはさらに前記ROMとは別にIPL-ROMを搭載している。IPL-ROMとはイニシャル・プログラム・ローダーROMのことであり、前記ROMにプログラムが全く記憶されていない場合、又はプログラムを新しいバージョンに更新する場合に、CPUを動作させるために必要なプログラムを記憶しておくROMのことである。前記IPL-ROMに記憶すべきプログラムを他のプログラムを保持するためのROMに記憶させた場合は、ROMの書き込み作業中は同ROMに書かれたプログラムが実行できなくなるため、このプログラムをRAMに一旦格納してRAM上で書き換えプログラムを実行する必要があり、もし書き換える途中で動作が中断するなどの不慮の事故が起きた場合に、復旧できなくなる可能性があるため、このような不具合を解消するためにもIPL-ROMが使用されて

いる。図4は、従来のIPL-ROMを使用する回路構成の代表例を示すブロック図である。同図において1はBOOT検出又は切替スイッチ部であって、IPL-ROMで起動するか、前記ROMで起動するかを選択するための機構であり、手動の切替スイッチや、制御信号を用いた自動操作による切り替え等を行い、結果を信号bでアドレスデコーダ2に伝達する。アドレスデコーダ2は、CPUの制御信号群a及び前記信号bによりアドレスをデコードしてIPL-ROM選択信号c、実装後書き込み可能なROMの選択信号d及びその他の選択信号eを出力し、3は前記IPL-ROMである。

【0003】

【発明が解決しようとする課題】しかしながら、前記制御装置では、IPL-ROMを必要とするから、部品点数が増加する。又、ROM内蔵の1チップCPUの場合には普段ほとんど使われない機能のために高速アクセスが可能な内臓ROMを占有するという欠点があった。本発明は上述したように従来のBOOTローダー回路の欠点を除去するためになされたものであって、同等の機能をより小規模の回路構成で実現し、より柔軟な開発環境を備えたBOOTローダー回路を提供することを目的とする。

【0004】

【課題を解決するための手段】上述の課題を達成するため本発明は、CPUと、実装後書き込み可能なROMと、CPUの作業用RAMと、外部通信インターフェース手段を持つ制御装置において、プログラムが記憶されていない状態のROMを実装した場合、又は、プログラム更新のために旧プログラムに上書きする必要がある場合に、ROMの内容に依存せずに外部通信インターフェース手段を通して直接CPUに命令を与えて動作させ前記制御装置がプログラムを持っていなくてもROMに書き込むことができるように構成したことを特徴とする。又、前記制御装置は、CPUがROMから命令を読み出すことを検出した後にCPUが応答の遅いメモリをアクセスする時のWAIT時間機能を使用して、外部通信インターフェース手段を介して得たデータを命令として実行させることを特徴とする。又、前記制御装置は、CPUがROMから命令を読み出す際CPUの動作クロックを停止させ、外部通信インターフェース手段に入力があった時点で、クロックを再動作させてCPUにROMのデータの代りに外部通信インターフェースで得たデータを命令として実行させることを特徴とする。

【0005】

【発明の実施の形態】以下、本発明を図面に示した実施例に基づいて詳細に説明する。図1は本発明によるBOOTローダー回路の概略構成例を示す図である。図1に示す回路は、当該装置がBOOTモードとなることを検出する機能をもつBOOT検出部4と、その結果を受けてCPUの動作を停止するCPU停止制御部8と、各デ

バイスの選択信号を生成するアドレスデコーダ5と、BOOTモードの選択条件を設定する切替器6及び切替器7とを備えている。この構成において動作を説明する。まず、当該BOOTローダー回路を搭載した装置において、装置がBOOTモード状態に移行するか否かは、BOOT検出部4がBOOTモードに入るかどうかの検出を行い、制御信号aのBOOTモード移行要求をリセット信号cにより保持することで決定する。選択信号bは、BOOTモードの解除要求としてBOOTモードから通常モードに戻るのに使用する。制御信号fは、CPUのバス接続による信号を示し、制御信号eのCPUリード信号を含み、アドレスデコーダ5によって各デバイスの選択信号を作る。選択信号gは、ROMの内部選択信号を示し、選択信号gと制御信号eとによってROMのリードが検出できる。hは、ROMの外部選択信号であり、切替器6によって制御信号iのBOOTモード信号が通常モードの時、選択信号gと同じようにBOOTモードでは非選択になる。jは、外部入力インターフェースの内部選択信号を示し、切替器7によって制御信号iが通常モードの時、外部入力インターフェースの外部選択信号kは、選択信号jと同じようにBOOTモードの時選択信号gと同じになって前記ROMの代りに選択される。CPU停止制御部8は、制御信号iがBOOTモードにおいて、選択信号gはROM選択を、又、制御信号eはリード中を、更に制御信号dの外部入力インターフェースの入力完了信号は未完了の場合のみ制御信号lでCPU停止を指示する。この時制御信号dが完了信号となり次第CPUは動作を再開して前記外部入力インターフェースのデータを読み込み実行する。選択信号kはRAMの選択信号、選択信号lはその他の選択信号とし、制御装置において必要なものを作る。制御信号aによりBOOTモードにした後、外部入力インターフェースからCPUがROMから読み込むのと同じ順番によりデータを入力すればCPUに期待通りの動作をさせられる。例えば、最初にCPUがROM（実際は外部入力インターフェース）からRAMにデータ転送後、RAMにジャンプしてRAMのプログラム（ROM書き込みプログラム等）を実行するようなプログラムを送れば、RAMの容量内で実行可能なプログラムを実行することができる。又、RAMの容量に余裕がない場合には、実行速度は劣るが最後まで外部通信インターフェースを使ってROMの書き込みをすることも可能である。

【0006】図2に本発明に係るBOOTローダー回路の動作フローチャートの1例を示す。制御装置のリセットが解除されCPUが起動する前にスイッチ又は決められた制御信号によって通常モードか、BOOTモードに設定されるかを決定する。通常モードとは、CPUが普通にROMを読み出して動作するモードである。BOOTモードとは、CPUがROMを読み出そうとした時に限って以下に説明する操作を施し、CPUのその他の動

作に関しては通常モードと同じ動作をするモードである。BOOTモードで、且つCPUがROMを読み出そうとした事を検出した場合に、本発明はCPUがROMの読み出しを完了する前にCPUを止めて外部通信インターフェースにデータが入力されるまで待つ。更に、入力されたデータをROMのデータの代りにCPUのデータバスに出力した後、CPUの動作を再開させる。そこで、CPUに外部通信インターフェースのデータを命令として実行させる事によって、IPL-ROM無しでCPUを動作させることを目的としている。そして、これを応用することによりROMの書き込みが可能となる。

【0007】外部通信インターフェースには大別してパラレルインターフェースとシリアルインターフェースとがあるが、このインターフェース以降の動作は同様であり、以下の例ではシリアルインターフェースにより説明する。図3は本発明を内蔵した制御装置の外部通信インターフェースをRS232Cのシリアルインターフェースによりパソコンと接続してROMにプログラムを書き込む時の実施例を示す概略構成図である。同図は、制御装置のCPUを動作させるプログラムを送るパソコン9と、本発明を利用した制御装置10とで構成し、その他装置に必要な回路群11は本発明の説明とは無関係な部分をまとめたものである。パソコン9と制御装置10はRS232C規格のシリアルインターフェースmにより接続し、レベル変換部12においてRS232Cの電圧レベルを制御装置の電圧レベルに変換し、シリアル受信インターフェース13において入力データaをパラレルデータに変換してBOOTモードの時は前記パラレルデータを制御信号fのCPUバスの中のデータバスに出力する。BOOTローダー回路14は本発明によるものであり、信号線を表す記号は図1と対応させている。この例ではシリアル入力データaをシステムリセット回路15によるリセット信号cのタイミングで保持して、入力データが0の時BOOTモード、1の時通常モードになるものとする。kはシリアルインターフェースの選択信号、dはシリアルインターフェースの受信フラグ、lはCPU16の停止信号、nはRAM17の選択信号、hはROM18の選択信号、pは制御装置の選択信号である。又、この例ではCPUリード信号eとRAM選択信号kによりBOOTモード解除信号bを作っており、CPU16がRAM17を読み込もうとした時にBOOTモードを解除するようになっているが、他の条件で解除信号bを作ってもよい。

【0008】CPU16の停止信号mをCPU16のWAIT信号にした例を請求項2に示し、停止可能なCPUクロックにした例を請求項3に示す。ROM18を書き込むためには、パソコン9からブレイク・キャラクタの送信などの手段により信号aを0にした状態において、制御装置10の電源を入れるか、又はシステムリセット回路15においてリセットすることで制御装置10

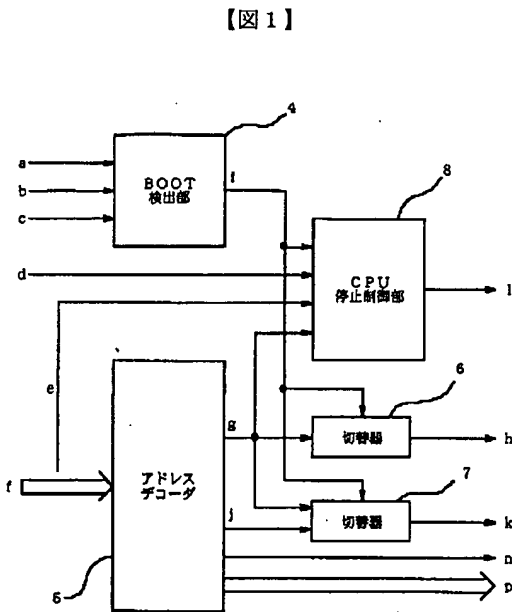
は前述のようにBOOTモードになる。そこで、CPU 16がROM 18からデータを読み込むのと同じ順序でパソコン9から制御信号mを通してIPLプログラムをRAM 17に書き込むプログラムを送り、最後にRAM 17に書いたプログラムの実行アドレスにジャンプする命令を送る。更に、CPU 16はRAM 17上のプログラムをリードして実行しようとするので、この時点においてRAMリードが発生しBOOTモードが解除されてRAM 17のプログラムが動き出す。後はRAM 17上のプログラムでROM 18にプログラムを書き込むことができる。

【0009】

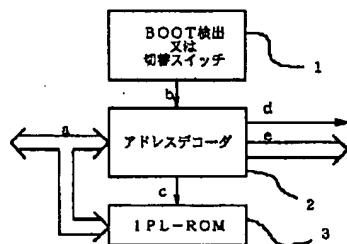
【発明の効果】本発明は以上説明した如く構成するものであるから、回路規模の縮小化やソフトウェア開発手段の多様化を実現する上で著しい効果を発揮する。

【図面の簡単な説明】

【図1】本発明によるBOOTローダー回路の1例を示す概略構成図



【図4】



【図2】本発明による動作フローチャートの1例を示す構成図

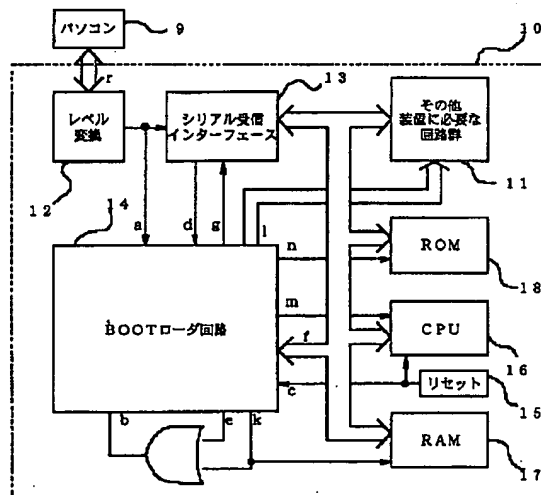
【図3】本発明によるBOOTローダー回路をシリアルインターフェースに適用した場合の1実施例を示す概略構成図

【図4】従来のIPL-ROMを内蔵する回路例を示す構成図

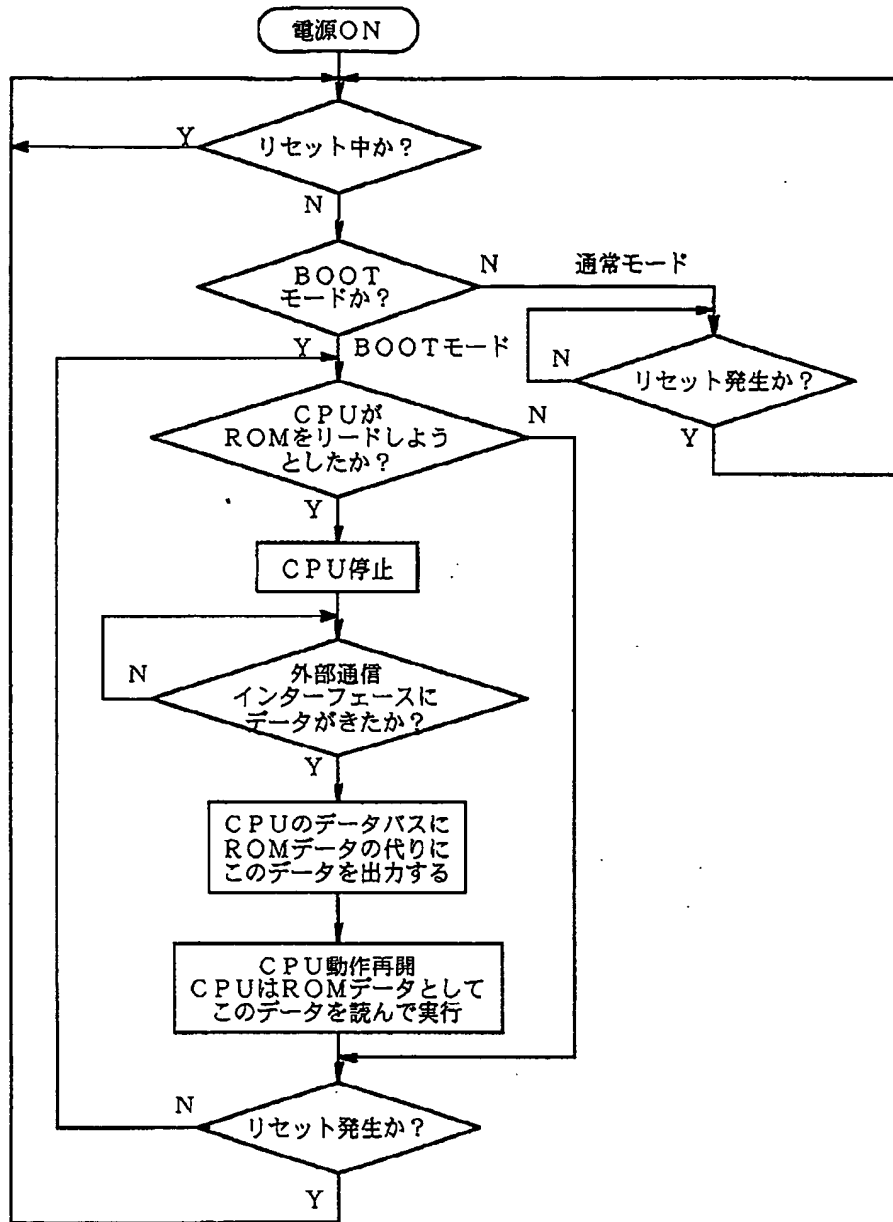
【符号の説明】

- 1・・・BOOT検出又は切替スイッチ部、
- 2・・・アドレスデコーダ、
- 3・・・IPL-ROM、
- 4・・・BOOT検出部、
- 5・・・アドレスデコーダ、
- 6・・・切替部、
- 7・・・切替部、
- 8・・・CPU停止制御部、
- 9・・・パソコン、
- 10・・・制御装置、
- 11・・・その他装置に必要な回路群、
- 12・・・レベル変換部、
- 13・・・シリアル受信インターフェース、
- 14・・・BOOTローダー回路、
- 15・・・システムリセット回路、
- 16・・・CPU、
- 17・・・RAM、
- 18・・・ROM

【図3】



【図2】



⑫ **EUROPEAN PATENT SPECIFICATION**

- ⑬ Date of publication of patent specification: 18.10.89 ⑭ Int. Cl.⁴: **G 10 L 9/18**
⑮ Application number: **85106852.8**
⑯ Date of filing: **27.01.81**
⑰ Publication number of the earlier application in accordance with Art. 76 EPC: **0 033 510**

⑱ **Speech synthesis system.**

<p>⑲ Priority: 04.02.80 US 118139 04.02.80 US 118366 04.02.80 US 118156 04.02.80 US 118155 04.02.80 US 118255 04.02.80 US 118367 04.02.80 US 118138</p> <p>⑳ Date of publication of application: 18.12.85 Bulletin 85/51</p> <p>㉑ Publication of the grant of the patent: 18.10.89 Bulletin 89/42</p> <p>㉒ Designated Contracting States: DE FR GB IT NL</p> <p>㉓ References cited: DE-A-2 804 721 DE-A-2 917 161 GB-A-2 014 765</p>	<p>㉔ Proprietor: TEXAS INSTRUMENTS INCORPORATED 13500 North Central Expressway Dallas Texas 75265 (US)</p> <p>㉕ Inventor: Henderson, Alva E. 5610 70th Street Lubbock, Texas 79424 (US) Inventor: Wiggins, Richard H. 6931 Mill Falls Dallas, Texas 75248 (US)</p> <p>㉖ Representative: Leiser, Gottfried, Dipl.-Ing. et al Patentanwälte Prinz, Leiser, Bunke & Partner Manzingerweg 7 D-8000 München 60 (DE)</p> <p>㉗ References cited: JOURNAL OF THE ACOUSTICAL SOCIETY OF AMERICA, vol. 56, supplement, 1974, page S15, abstract H3, New York, US; R. VISWANATHAN et al.: "Towards a minimally redundant linear predictive vocoder" IEEE TRANSACTIONS ON ACOUSTICS, SPEECH, AND SIGNAL PROCESSING, vol. ASSP-25, no. 4, August 1977, pages 322-330, New York, US; S. CHANDRA et al.: "Linear prediction with a variable analysis frame size"</p>
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Courier Press, Leamington Spa, England.

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Description

This application is a division from patent application EP—A—33 510.

The invention described herein relates to a speech synthesis system as defined in the pre-characterizing part of claim 1. More specifically, this invention relates to the following aspects of a speech synthesis system:

interpolation circuitry utilized to increase the effective data rate in speech synthesis circuits; and data frame rate control in speech synthesis circuits.

Several techniques are known in the prior art for digitizing human speech. For example, pulse code modulation, differential pulse code modulation, adaptive predictive coding, delta modulation, channel vocoders, cepstrum vocoders, formant vocoders, voice excited vocoders, and linear predictive coding techniques of speech digitization are known. The techniques are briefly explained in "Voice Signals; Bit by Bit" on pages 28—34 of the October, 1973 issue of IEEE Spectrum.

In certain applications and particularly those in which digitized speech is to be stored in a memory, most researchers tend to use the linear predictive coding technique because it produces a very high quality speech using rather low data rates. A speech synthesis system employing the linear predictive coding technique would typically utilize frames of data which are comprised of digital representations of pitch, energy, and certain linear predictive coefficients which are utilized to control a digital filter. High quality synthetic human speech may be produced by such a speech synthesis system at a relatively low data rate, such as 1,200 bits per second, utilizing a fixed rate of data frame entry. It will be appreciated that a more accurate representation of human speech may be obtained by increasing the frame rate to a significantly higher level. However, such an increase in the frame rate is accompanied by a corresponding increase in the number of bits which must be stored in memory to synthesize a given quantity of human speech. Further, because certain aspects of human speech are quite redundant, accurate synthesization of such redundant human speech can be achieved by utilizing a data rate significantly lower than that which would be normally employed. An ideal solution to the aforementioned problem, would require a speech synthesis system capable of synthesizing human speech from frames of data which change rapidly during those complex periods of human speech and change slowly during redundant periods, thereby minimizing the required bit storage.

A problem encountered in attempting to utilize variable frame rate data in speech synthesis circuits occurs when interpolation calculation is utilized between frames of data to enhance data rate capability. A fixed interpolation system wherein eight interpolation calculations take place between each frame of data is adequate for fixed frame rate systems; however, a variable frame rate system requires much more sophistication in interpolation circuitry. Specifically, during slowly changing periods of speech data, a more accurate portrayal of the human speech waveform may be achieved by increasing the number of interpolation steps between frames. Conversely, during rapidly changing aspects of human speech, few or no interpolations between frames of data are required to accurately synthesize human speech. Thus, in order to solve the aforementioned problem, a speech synthesis circuit must be able to vary the number of interpolation calculations taken between successive frames of speech data. Further, it has been discovered that in certain aspects of synthesis of human speech, the interpolation between frames of data may more accurately portray human speech if interpolated linearly, or in other circumstances, non-linear interpolation may provide greater accuracy.

In accordance with one aspect of the invention, a speech synthesis system is constructed with a linear predictive filter utilizing coded reflection coefficients to produce digital signals representative of human speech. A variable interpolation circuit within the linear predictive filter allows a variable number of interpolation steps to be calculated between successive values of reflection coefficients. Additionally, a user programmable option allows the user to select a linear, nonlinear, or combination form of interpolation.

As previously described, speech synthesis if carried out at an increased data rate would typically require a corresponding increase in the number of bits to be stored in a memory to synthesize a given quantity of human speech. To reduce the bit storage requirements of the memory while maintaining the capability of speech synthesis at a relatively high data rate is the subject of two papers delivered at the 1977 IEEE Conference on Acoustics, Speech and Signal Processing, and published in the record thereof. One attempted solution was suggested in "Variable-to-Fixed Rate Conversion of Narrowband LPC Speech" by E. Blackman, R. Viswanathan and J. Makhoul. The aforementioned solution required transmission of pitch, gain and reflection coefficients in three separate variable rates, with separate transmission criterion and a three bit header code to distinguish transmissions. Additionally, transmit and receive buffers were necessary in that system to convert the transmission back into a fixed rate signal. The second attempted solution was documented in a paper entitled "The Application of a Functional/Perceptual Model of Speech to Variable-Rate LPC Systems" by R. Viswanathan, J. Makhoul and R. Wicks. This second solution involved the transmission of pitch and gain information at a fixed frame rate, and utilizing a variable frame rate for transmission of reflection coefficients.

The above described problems are overcome in a speech synthesis system of the type defined in the pre-characterizing part of claim 1 by incorporating the features of the characterizing part thereof.

The novel features believed characteristic of the invention are set forth in the appended claims. The

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invention itself, however, as well as a preferred mode of use, further objects and advantages thereof, will best be understood by reference to the following detailed description of an illustrative embodiment when read in conjunction with the accompanying drawings, wherein:

5 Figure 1a is a view of an electronic learning aid which is a suitable structure for enclosing the speech synthesizer system;

Figure 1b is a generalized block diagram of a speech synthesis system;

Figures 2a and 2b form a detailed block diagram of the speech synthesizer;

Figure 3 is a logic diagram of the input data register and frame control PLA;

Figure 4 is a logic diagram of the interpolation counter circuitry;

10 Figure 5 is a detailed logic diagram of the speak latch circuitry and status latch circuitry.

Figure 6 is a detailed logic diagram of the instruction decoder circuitry.

Figure 7 is a detailed logic diagram of the parameter load control circuitry.

Figures 8a and 8b form a composite block diagram of the array multiplier;

15 Figures 9a—9d are detailed logic diagrams of the blocks which form the array multiplier.

Figures 10a—10c are detailed logic diagrams of the recoding logic;

Figure 11 is a detailed logic diagram of the filter adder;

Figure 12 is a detailed logic diagram of one call of the B-Stack, PPC, Y Latch register;

Figure 13 is a detailed logic diagram of multiplex 58 and register 66;

Figures 14a and 14b are detailed logic diagrams of the digital-to-analog and output circuitry.

20 Referring to Figure 1a, there is shown an electronic learning aid which may serve as a suitable structure for enclosing the speech synthesis system of the present invention. Figure 1b shows a generalized block diagram of the major components which make up such a learning aid. Keyboard 16 may be a standard matrix keyboard such as the type disclosed in U.S. Patent No. 4,074,055. Various algorithms required to implement the desired modes of operation of an electronic learning aid, electronic language translator or other applications may be programmed into the microprocessor in a manner well known in the art. An example of one such algorithm may be seen in US—A—4 209 836.

Data ROM 12 is a standard non-volatile Read Only Memory such as is described in US—A—4 209 836. The coded or uncoded filter parameters which are utilized to control synthesizer 10 are stored therein. Synthesizer 10 is a linear predictive filter type synthesizer such as is described in DE—A 28 26 570; however, improvements in the synthesizer circuitry which result in higher quality speech, lower data rates and smaller circuit size are incorporated herein. Synthesizer 10 is controlled by microprocessor 14, and generates synthetic speech at speaker 18 by utilization of certain filter parameters stored in ROM 12. While synthesizer 10 is shown being controlled by microprocessor 14, it will be understood by those skilled in the art that any digital control mechanism may control synthesizer 10. In an embodiment disclosed herein, in which synthesizer 10 is implemented in complementary MIS, such as CMOS, it is preferable that microprocessor 14 also be implemented in CMOS to permit both devices to be operated from a single low voltage source, such as a battery. The linear predictive filter utilized in synthesizer 10 is a single multiplier, lattice type filter similar to the filter described in DE—A—28 26 570. The reader is encouraged to read the aforementioned German Patent Application to familiarize himself with the basic operation of this complex circuitry.

Referring to Figures 2a and 2b, there is shown a detailed block diagram of synthesizer 10. Most of the blocks of Figures 2a and 2b are shown in greater detail in later figures.

Speech data, comprising either coded or uncoded filter coefficients, is received by synthesizer 10 from ROM 12 at the Data In pad of input register 22, input register 22 is a ten bit register latch which accepts the speech data serially and outputs the data in parallel to frame control PLA 30.

45 Input/output pads 1, 2, 4 and 8 accept control data from microprocessor 14, and input the control data to instruction decoder 20. Input/output pads 1, 2, 4 and 8 are bidirectional lines and microprocessor 14 is therefore able to access speech data out of input register 22 as in an alternate embodiment wherein a control mechanism may be utilized to examine such data. Instruction decoder 20 is utilized to decode the instructions which microprocessor 14 inputs to synthesizer 10. Instruction decoder 20 also set speak latch 24 and parameter load control 26. Speak latch 24 generates logic signals which are utilized throughout synthesizer 10 to indicate that synthetic speech is being generated. Parameter load control 26 is utilized to control the loading of data into input register 22. In addition to instruction control of parameter load control 26, the status latch 28 is also capable of controlling the input of data to input register 22 by detecting certain special states of input data which will later be described in detail.

Frame control PLA 30 is utilized to decode the aforementioned special states of input data which in turn set the special state latches in status latch 28. Frame control PLA 30 also decodes special states of the input data which control how many interpolation steps take place between each frame of data, thereby allowing synthesizer 10 to vary the rate at which data is applied. Interpolation counter 34 is utilized to generate a signal which controls the number of interpolation steps which will be calculated between adjacent frames.

Code RAM 32 is a twelve by ten bit RAM utilized to store an entire frame of data. An entire frame of data will include a pitch parameter, an energy parameter and ten filter parameters. The maximum length of an uncoded parameter is ten bits, and twelve parameters are normally required for each frame.

65 In one mode of operation, synthesizer 10 generates synthetic speech from uncoded parameters. These parameters are transferred from code RAM 32 to the ROM/RAM load, parallel/serial converter 38, to be

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serially loaded out to the linear predictive filter. In the alternative mode of operation the coded parameters are utilized by address PLA 36 to generate an address for the appropriate uncoded parameter stored in parameter ROM 40. The uncoded parameters from ROM 40 are inputted to converter 38 and then serially loaded out to the linear predictive filter.

5 The parameters outputted from converter 38 are coupled into array multiplier/interpolator 50. Array multiplier/interpolator 50 functions similarly to the array multiplier of US—A—4 209 844, with the additional capability of conducting interpolation steps. Array multiplier/interpolator 50 is coupled to filter adder 54, which is utilized to perform the additions and subtractions necessary to implement the filter function. The output of adder 54 is coupled to B stack, PPC register and Y latch register 56 and to
10 multiplexer 58. Register 56 serves as a temporary store for those intermediate values necessary to perform the filter calculations, and storing the pitch period count (PPC). Register 56 also serves to drive D to A converter 64 with appropriate output values. D to A converter 64 converts the output of the filter to analog signals which drive speaker 18. Multiplexer 58 serves to couple information back up into multiplier/interpolator 50 through recoding logic 52 from adder 54 or the multipurpose shift register 66.

15 Shift register 66 is a multipurpose shift register utilized to couple excitation data or scale data from ROM 78 into multiplier/interpolator 50 through multiplexer 58 and recoding logic 52. Scale data is utilized by multiplier/interpolator 50 to perform interpolation. Additionally, shift register 66 couples pitch period counter (PPC) information which is utilized to address excitation data in ROM 78. Pitch period counter information is coupled through multiplex 70 to address register 72 where it is utilized to address excitation
20 data in ROM 78. Unvoiced address generator 76 is utilized during unvoiced periods of speech to randomly address one of two excitation values, utilized during unvoiced speech, which are stored in ROM 78.

Tri-state buffer 68, in an alternative embodiment of the present invention, it utilized to control the excitation input to shift register 66. Synthesizer 10 may be utilized as a residually excited synthesizer, in a vocoder application, for example. In such an alternative embodiment a residual excitation signal is applied
25 to residual input pin 80, and tri-state buffer 68 is disabled by a control signal at residual control pin 82. In this alternative embodiment, parameters are inputted to multiplier/interpolator 50 from an external source, rather than through converter 38.

The synthesizer 10 is preferably implemented using precharged conditional discharge type logics. Thus, four clock signals, $\emptyset 1$ — $\emptyset 4$ are appropriate for use in such precharge, conditional discharge logic.
30 There are two main clock phases ($\emptyset 1$ and $\emptyset 2$) and two precharge clock phases ($\emptyset 3$ and $\emptyset 4$). Phase $\emptyset 3$ goes high during the first half of phase $\emptyset 1$ and serves as a precharge therefor. Phase $\emptyset 4$ goes high during the first half of phase $\emptyset 2$ and serves as a precharge therefor. A set of clocks $\emptyset 1$ — $\emptyset 4$ is required to clock one bit of data, and thus correspond to one time period.

Timing signals, labelled T1—T22, each having a period on the order of 4.5 microseconds are utilized
35 throughout the system. Selecting a time period on the order of 4.5 microseconds permits data to be outputted from synthesizer 10 at a 10 kilohertz rate (i.e. at a 100 microsecond period) which provides for a frequency response of 5 kilohertz in the digital-to-analog converter 64. It will be appreciated by those skilled in the art, however, that depending upon the frequency response desired, the number of reflection coefficients utilized and the type of logics utilized, the periods or frequencies of the clocks and clock phases
40 may be substantially altered.

Thirteen parameter count (PC) signals are also utilized in the depicted embodiment of the invention. The first twelve of these, PC=0 through PC=11 correspond to the times when the energy, pitch, and K1—K10 reflection coefficients are available in parallel-serial converter 38. Each of the first twelve
45 parameter counts comprise two cycles, referred to as the A and B cycles. Each cycle, whether A or B, begins at T18 and ends at the next T18. During each parameter count the value in parallel-serial converter 38 is utilized as a target value for interpolation with an existing value stored in a recirculating portion of multiplier interpolator 50. During the A cycle, the appropriate existing parameter is withdrawn from the recirculating portion of multiplier/interpolator 50, and during the B cycle the newly interpolated value is reinserted.

50 The thirteenth parameter count, PC=12, is provided for timing purposes so that all twelve parameters are interpolated once each 2.5 millisecond, and for indicating that period of time during which variable frame rate data is inputted.

As was discussed earlier with respect to interpolation, the synthesizer of the present invention is capable of performing from zero to one hundred twenty seven interpolations between each frame of
55 parameters inputted. A new interpolation count signal is available from interpolation counter 34 every 2.5 milliseconds, and is utilized to address a scale value in excitation/scale ROM 78. Thus the period for interpolation remains constant at 2.5 milliseconds, regardless of the number of interpolation steps between two values.

60 New parameters may be inputted to synthesizer 10 at a fifty hertz frame rate. It will be seen subsequently that in multiplier/interpolator 50, the pitch data, energy data and reflection coefficients are utilized as ten bit binary numbers. If each of the twelve parameters were updated with a ten bit binary number at a fifty hertz rate, a $12 \times 10 \times 50$, or 6,000 hertz bit rate would result. Therefore, in order to lower the bit rate, the data compression scheme of US—A—4 209 836 may be utilized. In Figure 6 of US—A—4 209 836, there is shown pictorially a representation at four different lengths of data frames. One frame, labelled
65 "voiced frame" has a length of 49 bits, while another labelled "unvoiced frame", has a length of 28 bits. A

"repeat frame" has only ten bits and a "zero energy" frame has only 4 bits. In an alternative embodiment, a direct, uncoded, ten bit binary number may be loaded for each parameter. The input circuitry of synthesizer 10 is capable of accepting either format.

5 Various portions of synthesizer 10 will now be described in detail with reference to Figures 3 through 14, which depict in detail the logic circuits which implement synthesizer 10. Certain well known sections of the block diagram depicted in Figures 2a and 2b are not included in Figures 3—14. The following discussion, with reference to Figures 3—14, refers to logic signals available at many points in the circuit. Synthesizer 10, in this embodiment disclosed, is implemented in complementary MIS, such as CMOS. It must be remembered that in CMOS devices, a logic zero corresponds to a zero voltage, that is Vss. Further, the P channel devices depicted in the aforementioned figures are conductive when a logic zero is applied to their respective gates. Also, a logic one in CMOS devices corresponds to a positive voltage, +3V in the embodiment disclosed (Vdd). Therefore, the N channel devices depicted are conductive when a logic one is applied to their respective gates. When a logic signal is referred to which is unbarred, the signal is to be interpreted as "True" logic, that is, a binary one indicates the presence of Vdd and a binary zero indicates the presence of Vss. Logic signals which are barred indicate "False" logic and the aforementioned relationships are reversed. It should also be understood that a numeral in a clocked gate indicates which of the clock phases is utilized, as a precharge clock. The letter "S" in a gate indicates the gate is statically operated.

20 Referring to Figure 3, there is shown a logic diagram of input data register 22. Input data register 22 is a ten stage register, the first stage of which is shown within the detail marked A. Input data register 22 is ten stages in length to allow synthesizer 10 to accommodate uncoded parameters up to ten bits long, or, in an alternative embodiment, coded parameters of the type utilized in US—A—4 209 836.

25 Certain signals are utilized to control input data register 22. A clear signal (CLR) is generated by parameter load control 26, and is utilized to clear input data register 22 at time T22, during speech. The IO, ROM control signal, is delayed to form IOD, which is utilized to clock bits of data into input data register 22. An optional control signal, HC, is utilized as a modified Huffman code. This signal is utilized during variable frame rate operation to control the receipt of the Huffman code, which, those skilled in the art will recall, is a variable length code.

30 Frame control PLA 30 is shown in Figure 3. PLA 30 is a programmable PLA, and is therefore shown without gates. PLA 30 is utilized to detect certain special states which occur in the input data. Among those special states are those which effect the length of each individual frame, including: the Repeat state (RPT); the "Energy equal zero" state (E=0); the "Pitch equal zero" state (P=0); and the "End of File" or "Energy equal fifteen" state (E=15).

35 Additionally, the lower half of PLA 30 also decodes the Huffman code mentioned earlier, or a standard binary code, either of which may be utilized during variable frame rate operation. The decoded variable frame rate data is utilized to generate the signals ICP6—ICP0, which are in turn utilized to control interpolation counter 34. The parameters in input data register 22 are also passed through PLA 30 to the parameter RAM 32. These signals are shown in D10—D19.

40 Interpolation counter 34 is shown in detail in Figure 4. Previous attempts at variable frame rate voice synthesis have had difficulty due to the problem of varying lengths of time between each frame, and the question of interpolation therein. Interpolation counter 34 is capable of utilizing the variable frame length data to control the number of interpolation steps between each frame. Thus, during rapidly changing speech, few or no interpolations take place between data frames. However, during slowly changing speech, up to one hundred twenty seven interpolations may take place.

45 Register 343 is a seven stage shift register, which is initially set by the signals ICP6—ICP0. The first stage of register 343 is shown within the detail marked "A". The signals ICP6—ICP0 initially set register 343 to some number, the interpolation count, which is between zero and one hundred twenty seven. The interpolation count initially set into register 343 is clocked out and around through a series of inverters which generate an appropriate amount of delay. Gates 344 are utilized to selectively increment the interpolation count after each interpolation. The new interpolation count is then shifted back into register 50 343, whose gate 341 is utilized to detect the "interpolation count equal zero" (IC=0) state. When the IC=0 state is detected, gates 342 are utilized to latch this condition. The IC=0 condition is utilized throughout synthesizer 10 to indicate the end of interpolation, and allow the entry of new data. The interpolation count is outputted from interpolation counter 34 to be utilized as part of the address in excitation/scale ROM 78.

55 Figure 5 shows a detailed logic diagram of speak latch 24. Speak latch 24 consists of four latch circuits utilized to set and hold signals which indicate synthesizer 10 is generating speech. Gates 241 form a latch which has SPK as its input. SPK is generated by instruction decoder 20 in response to an input command which causes speech to be generated utilizing coded speech parameters. Instruction decoder 20 may also generate SPKEXT in response to an input command which causes speech to be generated utilizing 60 uncoded, ten bit, binary parameters, as discussed earlier with respect to an alternate method of operation. The SPK command is utilized to generate the "speak enable" (SPKE) command out of gates 241, and to set latch 242 to generate SPKL. The SPKEXT command will set a latch 244 comprised of gates 243, which in turn will set latch 244 and generate SPKEXTL. The occurrence of either SPKEXTL or SPKL will in turn generate the TALK signal. Gate 245 is utilized to reset the latches comprised of gates 241 and 243 during a power up, or after a reset signal. The speak reset (SPRST) command is generated by gate 246 by receipt of 65

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an "end of file" or "Energy equal fifteen" (E=15) code. Additionally, gate 247 is utilized to latch out a "talk status" signal which indicates synthesizer 10 is generating speech. Thus, the logic signals outputted by speak latch 24 are utilized throughout synthesizer 10 to indicate the generation of speech.

Status Latches 28 are also shown in detail in Figure 5. The function of the various status latches is identical to the function described in US—A—4 209 836, and will only be described briefly herein.

Latching signal LATCH 1 is generated by gate 281 at the beginning of a frame of data, the inputs to gate 281 all signifying a frame start. The LATCH 1 signal will strobe any SPKEXTL or SPKL signal at latch 244 or 242 in the speak latch 24, and will additionally strobe the output of latches 289 (the "Pitch equal zero" (P=0 latch) and 290 (the "Energy equal zero" (E=0) latch) into latches 284 and 285 to generate Old E=0 and Old P=0. The contents of latches 284 and 285 are utilized in conjunction with the P=0 signal to generate the INHIBIT signal. As in the synthesizer of US—A—4 209 836 the INHIBIT signal is utilized to inhibit interpolations in certain conditions. During transition from voiced to unvoiced speech, or unvoiced to voiced speech, it is advantageous to insert new parameters directly, without interpolations. Also, interpolations are not desirable when transitioning from silence to speech.

As was explained in detail in US—A—4 209 836 it has been determined that fewer parameters are required to accurately represent unvoiced speech. Therefore, gate 288 is utilized to generate a "zero parameter" (ZPAR) signal during unvoiced speech (Old pitch equal zero) after the parameter count has reached five (PC 5). Gate 288 also zeroes all parameters during non-speaking periods, by utilizing the TALK signal and the TALKD signal generated by latch 283.

Referring to Figure 6, there is shown a detailed logic diagram of instruction decoder 20. Instructions from microprocessor 14 are input to synthesizer 10 on I/O pins I/O1, I/O2 and I/O4. The instructions are clocked in each time a Processor Data Clock (PDC) signal is generated. The instructions are decoded by PLA 202. Many of the instructions are identical to those utilized by the synthesizer of US—A—4 209 836. A brief description of each instruction and its function is listed below.

The "Reset" (RST) instruction is a software reset instruction which is utilized by gate 201 in conjunction with the synthesizer "power up clear" (PUC) signal to form PUC+RST. This instruction is then utilized to reset speak latch 24.

The "Read" (READ) instruction is a signal from microprocessor 14 telling synthesizer 10 to access one data bit from ROM 12.

The "Load Address" (LA) instruction is an instruction which requires two PDC signals to execute. On the first PDC, the LA instruction is latched into latch 203. Latch 203 disables PLA 202 so that no command is decoded. On the second PDC, gate 205 is enabled, causing instruction decoder 20 to output an I1 signal to ROM 12. The I1 signal instructs ROM 12 to load four bits of address.

The "Speak" (SPK) instruction causes synthesizer 10 to begin synthesizing speech utilizing coded speech parameters. The SPK instruction is utilized throughout synthesizer 10.

The "Speak External" (SPKEXT) instruction causes synthesizer 10 to begin synthesizing speech utilizing direct, uncoded, parameter loading, as in the alternate embodiment discussed herein.

The "Read and Branch" (R+B) instruction is an instruction to ROM 12 to internally read data and load the data back into its address register, to allow indirect addressing.

The "Test Talk" (TTALK) instruction and the "output" (OUTPUT) instruction both require three PDC signals to execute. The TTALK instruction sets latch 206 and disables PLA 202 through gate 240. On the next PDC, the output of latch 206 is clocked through gate 208 to generate signal C2. Signal C2 is utilized to control the buffer between I/O8 and IR9, allowing the "talk status" (TALKST) signal to be output on I/O8. Thus, microprocessor 14 can determine whether synthesizer 10 is talking. The next PDC signal shuts off the C2 signal and resets latch 206. The OUTPUT instruction also requires three PDC signals to execute. Latch 207 and gate 209 interact in the same manner as latch 206 and gate 208. However, in the case of the OUTPUT instruction, a C1 signal is generated which enables the buffer to all of the I/O pads. In this manner, microprocessor 14 can access data in ROM 12, through synthesizer 10.

Detail diagrams of the buffers for the I/O pads are also shown in Figure 6b.

Parameter load control 26 is shown in detail in Figure 7. Parameter load control 26 generates the I0 signal to ROM 12. The I0 signal and the I1 signal, generated by instruction decoder 20, control ROM 12 in the manner described in US—A—4 209 836. The I0 signal is utilized to clock data out of ROM 12.

Gate 261 is utilized to generate the Parameter Load Enable (PLEN) signal which allows parameters to be written into code RAM 32. PLEN is generated unless one of three conditions exist at the input of gate 261. When a repeat (RPT) bit is detected, the PLEN signal stops. A RPT bit is utilized when old parameters are to be repeated, thus no new parameters should be loaded. When the Energy parameter is zero (E=0), indicating silence, the PLEN signal is disabled. Lastly, as described in US—A—4 209 836, during unvoiced speech the system utilizes fewer parameters to accurately represent speech. Thus, when the pitch parameter is equal zero (P=0) and the parameter count indicates that the first six parameters have been loaded (PC>5), PLEN is disabled.

Gate 262 is utilized during variable frame rate operation to allow the frame rate data to be loaded (at PC=12) despite a condition which would preclude loading parameters. Gate 266 is utilized to set latch 263, the output of which is utilized in conjunction with the even clock times (TEVEN) by gate 264 to generate I0 signals. Gate 266 is utilized to distinguish between loading coded or direct parameters, since in the embodiment disclosed coded parameters consist of two to seven bits and direct parameters consist of ten

bits. Gate 265 is utilized to reset latch 263. Gate 267 is utilized to generate the CLR signal which clears the input register.

Recoding logic 52 couples the outputs of multiplexor 58 to multiplier/interpolator 50. Recoding logic 52 is shown in detail in Figures 10a—d. Recoding logic 52 consists of six stages, three of which are identical, as seen in Figure 10b. The first stage of recoding logic 52 (labelled REL 20) generates signals for the first two stages of multiplier/interpolator 50. The subscripts on each control signal indicate to which stage of multiplier/interpolator 50 it is coupled. The third stage of multiplier/interpolator 50 and the seventh stage require additional control signals due to the interpolation function therein. The INT signal discussed in the interpolation section is generated in the section of reading logic 52 labelled REL 30 in Figure 10a, and the T18 signal for the seventh stage is generated by the stage labelled REL 50 in Figure 10c. Recoding logic 52 outputs $+2$, -2 , $+1$ and -1 to each stage of multiplier/interpolator 50 with the exception of stage one which receives only $+1$, -1 , and -2 outputs. Effectively, as seen in US—A—4 209 836, recoding logic 52 permits multiplier/interpolator 50 to process, in each stage thereof, two bits of information in lieu of one, by utilizing Booth's Algorithm. Booth's Algorithm is explained in "Theory and Application of Digital Signal Processing", published by Prentice-Hall 1975, at pp. 517-18.

A block diagram of multiplier/interpolator 50 is formed by the composite of Figures 8a and 8b. Multiplier/interpolator 50 is an array multiplier. Array multipliers are sometimes referred to as "Pipeline Multipliers". For example, see "Pipeline Multiplier" by Granville Ott, published by the University of Missouri. Multiplier/interpolator 50 has seven stages, stage 1 through 7 and operates similar to the array multiplier disclosed in the aforementioned US—A—4 209 844. The equations in Table I herein represent the operation of the digital filter wherein multiplier/interpolator 50 and filter adder 54 are utilized to solve these equations.

The inputs to multiplier/interpolator 50 are the target values for new parameters, input at the PROMOUT terminal of the first stage, the aforementioned $+1$, -1 , $+2$ and -2 signals from recoding logic 52, and the INT and TPAR signals from recoding logic 52. The outputs of multiplier/interpolator 50, MULT 0—MULT 13 and PITCH 0—PITCH 9 are applied to filter adder 54. The blocks which make up individual sections of each stage are labelled A-1, B-1 through B-5, C-1 through C-3 and D-1 and D-2. The detailed logic diagrams of each block section are shown in Figures 9a—9d. The operation of multiplier/interpolator 50 is identical to that of the multiplier in US—A—4 209 836, with the exception of additional interpolation circuitry which will be explained with reference to Figures 8a and 8b and also 9a—9d.

The first stage of multiplier/interpolator 50 is comprised of nine A-1 blocks, with an additional bit of storage in the two inverters on its input and are thus responsive to the TPAR signal and to -1 , $+1$, -2 signals output from recoding logic 52. When multiplications occur in multiplier/interpolator 50, the most significant bit is always maintained in the left most column elements while the partial sums are continuously shifted toward the right. Inasmuch as each stage of multiplier/interpolator operates on two binary bits, the partial sums, labelled E are each shifted to the right two places. Thus, a total capacity of ten bits is available. As explained earlier, whether coded or direct parameters are utilized, the parameters utilized in multiplier/interpolator 50 are ten bits in length, due to the decoding of any coded values by address PLA 36 and ROM 40. The ten bit parameters which are loaded into multiplier/interpolator 50 represent the target values for current calculations. As the interpolation calculations reach these target values, the target values become current values, and new target values are loaded into multiplier/interpolator 50 at the PROMOUT point.

Current values for filter parameters are stored within multiplier/interpolator 50 in recirculating shift registers contained in all but the most significant bit of each stage. The recirculating shift registers circulate out of B terminals of each block and into the A terminals of the block below. At the bottom or seventh stage, the values are circulated back up through the D terminals into the C terminals. The current values shifted into the A terminals of each block are the multiplicands. The multipliers are the values input to multiplier/interpolator 50 by recoding logic 52.

The recirculating shift registers within multiplier/interpolator 50 form an eleven bit shift register, with each parameter shifting by each eleven time periods. There are twenty-two time periods, and each parameter K1—K9 is utilized twice during filter calculations. Thus eighteen time periods are required for these nine parameters. The K10 value and the energy value, as disclosed in US—A—4 209 836, are each utilized once in filter calculations, and are therefore swapped or exchanged, in the seventh stage of multiplier/interpolator 50. This requires two additional time periods. Of the two remaining time periods, one is utilized during interpolation, and the other is not utilized.

In Figure 9d, there is shown a detailed logic diagram of blocks D2 and D1. In each of the D type blocks, there is shown a group of gates labelled 501. The leftmost, latch 501a is a recirculating latch wherein either K10 or the energy value is stored. The multiplex gate 501b, in gates 501, is controlled by the signals labelled P' and E' which determine whether the signal outputted at the D terminal is the input from terminal A, or the contents of latch 501a. When the input signal at terminal A is the K10 parameter, it is stored in latch 501a and the previous contents of latch 501a is output through multiplexer 501b. The output of multiplex gate 501b is coupled to terminal D through a transmission gate controlled by the signal labelled F.

As discussed above, multiplier/interpolator 50 contains a recirculating shift register formed by vertical contacts between stages. The energy and K1—K10 parameters, which represent the current values, are recirculating through this register, occupying twenty of the possible twenty-two time periods. In order to

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perform interpolation, the current value of any given parameter must be captured and presented in the stage of multiplier/interpolator 50 to determine the difference between that current value and the target value being input at the appropriate time. Interpolation must take place when each target value is inputted, and not necessarily when the current value has circulated up to the proper position. The new current value
5 (V_{n+1}) represents the sum of the old current value (V_n) plus some scale factor (N) times the difference between the old current value (V_n) and the target value (V_T). N , the scale value is some fractional number stored in ROM 78 and utilized during variable interpolation. Thus the interpolation formula may be expressed:

$$10 \quad (1) \quad V_{n+1} = V_n + N(V_T - V_n)$$

The sample of any given current value must therefore be stored until the unused time period which is utilized for interpolation. Each block in the seventh stage of multiplier/interpolator 50 has a storage latch 502, wherein the current value is temporarily stored. When a parameter to be interpolated circulates into
15 the seventh stage D block, it passes through multiplex 501b and out through the D terminal, the value is also sampled through the transmission gate controlled by the signal N , and placed in storage latch 502. Storage latch 502 has a two input NOR gate on its recirculation line, the other input of which is the ZPAR signal utilized to zero parameters in specific states discussed above. Thus, the current value of the parameter to be interpolated is temporarily stored in storage latch 502. At the appropriate time period (T_7
20 in the embodiment disclosed) the control signal labelled G is generated, and the contents of storage latch 502 is output to the D terminal. Therefore, the recirculating shift registers in multiplier/interpolator 50 contain the parameters K_1 — K_9 an exchanged value representing K_{10} or Energy, and the about to be interpolated value of one of the parameters. The value to be interpolated is shifted up to the second stage of multiplier/interpolator 50 and, at the same time, the target value for that particular parameter is serially
25 shifted into the first stage. Recoding logic 52 provides a $\overline{1}$ signal to the second stage, which operates on the value to be interpolated, the result of which is then added to the target value, which generates $V_T - V_n$, for output at the Σ output terminal.

The third through sixth stage of multiplier/interpolator 50 act as an eight by ten bit multiplier during the interpolation time period for multiplying the difference between the target value and the current value
30 ($V_T - V_n$) times the scale value N . The various values for N are stored in ROM 78 and inputted to multiplier/interpolator 50 through recoding logic 52, from multiplex 58 and shift register 66 (as shown in Figure 2b).

The third stage of multiplier/interpolator 50 is different from other stages due to the fact that the sum out of the second stage during interpolation is not merely added to the next calculation. In the interpolation
35 operation, it is required that $V_T - V_n$ be utilized as the multiplicand in order to be multiplied by scale factor N . Thus, the $V_T - V_n$ value must be substituted for the multiplicands which are normally inputted on the A terminal from the B terminal above, in the normal recirculating shift register operation described above. In order to accomplish this exchange, each of the C blocks of multiplier/interpolator 50, shown in Figure 9c,
40 has a multiplex gate 503, controlled by the signal INT , which operates during the interpolation mode. When a $V_T - V_n$ value is present in the second stage of multiplier/interpolator 50, the INT signal controls gates 503 so that the signal at the E input terminal is selected by gate 503 and $V_T - V_n$ is inserted into the recirculating shift register to be utilized as the multiplicand. The $V_T - V_n$ value is inserted during one of the two unused
45 time periods discussed above and therefore has no effect on the recirculating current parameter values. Since during interpolation, the third stage of multiplier/interpolator 50 is utilized as the first stage of an eight by ten bit multiplier, as discussed above, the input on the H terminal must be forced to zero. This is also accomplished by the INT signal coupling V_{ss} into each C block at the H terminal.

The $V_T - V_n$ value is thus forced into the multiplicand position, and multiplied by the scale value N . Therefore the output of the sixth multiplier stage is the value $N(V_T - V_n)$. The seventh stage of
50 multiplier/interpolator 50 is utilized to add the current value of a parameter to the recently calculated $N(V_T - V_n)$ value. As shown in the detail of the D blocks in Figure 9d, at time T_{18} , the normal S input terminal is disabled and the E input is enabled through the bank of transmission gates depicted. T_{18} also enables a transmission gate which allows the contents of storage latch 502 to be coupled to full adder 504. Thus the
55 output of full adder 504 is the solution to Equation (1) or $V_n + N(V_T - V_n)$. The output of full adder 504 is coupled through a transmission gate controlled by the signal labelled I and coupled into storage latch 502. This is necessary since the newly interpolated value is always available at T_{19} , due to the requirement that
60 all interpolation calculations take place during the aforementioned window or open spot which occurs in the recirculating shift register. At the appropriate time, the contents of storage latch 502 is forced back into the recirculating shift register through a transmission gate controlled by the signal labelled G . A special case occurs at the last interpolation prior to achieving the target value, or as described earlier herein, the
65 $IC=0$ state. To avoid the problems generated by slight errors which may cause the interpolated value to be slightly over or under the target value, a special case is utilized for the last interpolation or interpolation count equal zero state ($IC=0$). As in normal interpolation, the current value of a particular parameter is captured and inserted into the interpolation time period in the recirculating shift register. However, rather than being operated upon by the $\overline{1}$ signal from recoding logic 52, the current value is zeroed and then
65 subtracted from the target value. The target value is then circulated down to the seventh stage of

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multiplier/interpolator 50 where it is input on the A terminal. The signal is then shifted through multiplier 501b in each block of the seventh stage, and inserted into storage latch 502 directly by way of a transmission gate controlled by a signal labelled H. Thus, rather than a newly interpolated value, during the last interpolation the target value itself is inserted into storage latch 502. Again as above, at the appropriate time the contents of storage latch 502 is inserted into the recirculating shift register to replace the old current value. This progress is repeated, and a new parameter is interpolated.

A slightly different operation is utilized for interpolation of the pitch value. After a target value for pitch is input to multiplier/interpolator 50, it is circulated down through the recirculating shift register discussed above. Entering the seventh stage at the A terminal, it is passed through multiplex gate 501b and stored in storage latch 502. If the value in storage latch 502 is a pitch value, it is stored in pitch latch 505. Each block of the seventh stage of multiplier/interpolator 50 has a latch 505 for storing one bit of the pitch value. The pitch latch 505 is controlled by the signals labelled M and N in Figure 9d. Pitch latch 505 then stores the pitch value until the appropriate time, when the control signal labelled L allows the pitch value to be outputted.

The outputs of multiplier/interpolator 50 include PITCH 0—PITCH 9, representative of the pitch value stored in the pitch latch formed by gates 505, and MULT 0—MULT 13 which represents the intermediate products generated during filter operation. As shown in Figure 8b, the least significant bit of the MULT output (MULT 0) is forced to the value of the sign bit (MULTSN). This transaction is utilized to prevent the negative drift which normally results from simple truncation of a two's complement number. By forcing the least significant bit to the value of the sign bit, truncation is always toward zero. Those skilled in the art will appreciate that this truncation scheme will help avoid the "limit cycle" problem.

Filter adder 54 is shown in Figure 11. The tenth and fourteenth block of filter adder 54 are shown in detail. Filter adder 54 is utilized to perform the additions and subtractions necessary to solve the equations listed in Table I. There are twenty additions or subtractions required to implement a ten pole filter, utilizing twenty of the twenty-two time periods. During the free time periods, filter adder 54 increments a pitch period counter signal and compares it to the pitch value inputted from multiplier/interpolator 50. The pitch period counter (PPC) is utilized to address periodic or voiced excitation values in ROM 78. When the PPC signal is equal to the pitch value, it is zeroed and begins incrementing again. A more detailed description of the PPC signal operation is listed below.

B stack 56 is a temporary storage facility utilized to temporarily store those intermediate values or "b" values which are necessary to solve the equations listed in Table I. B stack 56 is shown in detail in Figure 12. B stack 56 also provides temporary storage for the aforementioned PPC signal and the YLATCH signal which represents the output of the filter formed by multiplier/interpolator 50 and filter adder 56. The YLATCH output is coupled to the digital to analog converter and is utilized to generate analog signals representative of human voice. The PPC signal is output to multipurpose shift register 66 where it is utilized to address excitation values.

The multipurpose shift register 66 and multiplex 58 are shown in Figure 13, and two of the stages are shown in detail therein. Referring to the block diagram of Figure 2b and the equations of Table I will facilitate an understanding of the interworkings of the filter output circuitry. The MULT outputs from multiplier/interpolator 50 represent intermediate products required to solve the equations of Table I. Such products may be a K value times a b value, or a K value times a Y value. Filter adder 56 then adds or subtracts the intermediate product from a Y value or a b value to obtain a Y value or a b value. B stack 56 is utilized to store these b values, since each b value is utilized in filter adder 56 to calculate the next b value. The PPC signal from B stack 56 is input to shift register 66 and output to multiplex 70. Multiplex 70, not shown in detail, utilizes the PPC signal to address voiced excitation values stored in ROM 78. Any conventional address scheme may be utilized. The values stored in ROM 78 represent a chirp function, as in US—A—4 209 836, and it has been found that a chirp function closely models vocal cord excitation. Multipurpose shift register 66 also receives the aforementioned excitation values, or scale values addressed by an interpolation count signal from ROM 78 which are multiplexed out as MR signals to recoding logic 52.

The scale values stored in ROM 78 are chosen by the operator to generate any desired type of interpolation. As previously discussed, the IC or interpolation count may be any number from one to one hundred twenty seven. The IC count is utilized to address scale factors in ROM 78, thus, in the embodiment disclosed, up to one hundred twenty seven custom scaling values may be stored in ROM 78. A mask programmable option, or programmable type memory will allow easy substitution of scale values or excitation values. Scale values are typically fractional values utilized during interpolation of speech data and may be linearly or nonlinearly related.

Another important feature of the excitation signals provided by ROM 78 concerns the capability of scaling unvoiced excitation. In previous speech synthesis systems, such as disclosed in US—A—4 209 836 the unvoiced excitation is characterized as white noise. Such an input may be generated in many ways, such as a constant value with a pseudorandom sign bit. This solution is quite adequate; however, the inability to scale the unvoiced excitation to the voiced excitation results in unbalanced excitation signals. ROM 78, in the embodiment disclosed, also stores two unvoiced excitation signals, of approximately equal value, and opposite sign. A random bit is generated by unvoiced address generator 76 and is utilized as one bit in the address of the two aforementioned unvoiced excitation signals. This allows great resolution of the level of the unvoiced excitation, and further, allows the operator to change the level or value to balance

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excitation signals. Although ROM 78 is disclosed in the present embodiment as a Read Only Memory, those skilled in the art will appreciate that a Random Access Memory will provide an easier method of value changing than the mask programmable method required by a Read Only Memory.

5 An alternate form of excitation is also available through tristate buffer 68, shown in Figure 2b. This gate allows synthesizer 10 to be utilized as a residually excited synthesizer, in a vocoder application for example.

Multiplex 58 is utilized to couple the newly calculated "b" values or Y values to recoding logic 52. Multiplex 58 may also couple excitation values or scale values to recoding logic 52, the former for filter calculations, and the latter for interpolations. The outputs of multiplexer 58 are labelled MR0—MR12 and MRSN (for sign bit).

10 The digital-to-analog converter herein described is particularly well suited to low voltage applications and may be implemented in complementary MIS, such as CMOS, and may be integrated on a common semiconductor substrate with the CMOS synthesizer described above.

Digital-to-Analog converter 64 receives the YLATCH output signal from B stack 56 in a nine bit, two's complement notation, and converts the YLATCH signal into an analog signal representative of human
15 speech. A detail description of Digital-to-Analog converter 64 is seen in Figures 14a and b.

In Figure 14a, there is shown a PLA 641 with inputs YLATCH3, YLATCH4 and YLATCH5. Another input is the signal CLIPP from gate 642. Gate 642 and Gate 643 form a clipping circuit. A nine bit two's complement signal has a range from -256 to +255. It has been demonstrated that the larger values of a speech waveform convey little intelligence and may be clipped without loss of essential intelligence. Gates
20 642 and 643 examine the two most significant bits of the YLATCH signal (YLATCH6 and YLATCH7) and the sign bit YLATCHSN to determine if the absolute value of the incoming value exceeds 64, a CLIPP or CLIPN signal is generated.

Shift register 640 is a controllable register triggered off gate 644. Gate 644 generates a leading edge of the time periods T18 through T3 or T7 through T14, when synthesizer 10 is generating speech. Gate 644
25 may be disabled by the CLIPN signal, thus preventing a pulse from shifting into register 640. Assuming a large negative value is not present, the leading edge propagates down register 640, to an extent controlled by PLA 641. The YLATCH values input to PLA 641 will determine how far down register 640 the pulse propagates. It should be noted that in the event of a large positive value, CLIPP will cause the pulse to propagate to the end of register 640. The output gate 644 is coupled directly to gate 645, as are the
30 complemented outputs of the eight stages of register 640. Therefore, if gate 644 is enabled, gate 645 will act as an OR function, and at point X there will be generated a variable width pulse, ranging from one to eighth time periods in length. Additionally, the composite signal comprised of TALK, and T18 through T3 or T7 through T14 is delayed by gates 646 to form TCOMP4, a delayed signal. The TCOMP4 signal is further
35 delayed to form a signal called WINDOW. Gates 647 are shown providing the additional half bit of delay; however, for additional accuracy, the WINDOW signal may be finely adjusted utilizing high speed clock signals. The WINDOW signal is required to remove the PULGEN, minimum pulse width, when all inputs are zero. The PULGEN signal is required to charge the logics in the programmable delay shown in Figure 14b.

In Figure 14b is shown a detailed logic diagram of a three stage programmable delay 648 and the output speaker drive circuitry. The programmable delay shown in Figure 14 has three stages. Each stage
40 has a positive or P type device and a negative or N type device above and below it. A zero at point X will turn on the P device in stage 1, the N device in stage two and the P device in stage 3, causing PW to be a logic one or VDD. Thus a positive pulse out of gate 645 (Figure 14a) will be propagated through programmable delay 648 statically. When the pulse ends, or X goes to a logic one, the P device in stage one
45 shuts off and the N device conducts. Following this, the output of stage one will go to Vss, or logic zero, conditionally, base upon the clock gates contained between the P device and N device. The clocked gates in stage one are thus capable of extending the pulse-width seen at PW. Stage one is clocked to provide either one half of a time period of delay, or no additional delay. Similarly, stage two can provide either one fourth of a time period delay, or no additional delay. Stage three also operates similarly; however, a special high
50 speed clock $\emptyset 800$ is utilized to provide a delay of one eighth of a time period. Thus, the output at PW is either zero, when large negative numbers cause gate 644 to be disabled, or a pulse from one to eight and seven-eighths time period in length, with one eighth time period resolution.

The PW signal is still expressed in two's complement notation, and must therefore be converted to sign magnitude data for negative numbers. Gates 649 and 650 are utilized to generate complementary sign
55 magnitude, pulse width modulated signals. The positive numbers are generated by gate 650 (YLATCHSN equal zero) with PW and WINDOW, to eliminate the PULGEN pulses. PW is inverted to effectively convert negative numbers (YLATCHSN equal one) to sign magnitude data through gate 649.

The two pulsewidth modulated values SPK1 and SPK2 are then applied to a push/pull output circuit 651. Circuit 651 is utilized since it possesses no DC power component, and will effectively drive speaker 18.

60

65

TABLE I

	Equation	Stage
5	$Y_{10}(i) = Y_{11}(i) - K_{10}b_{10}(i-1)$	10
	$Y_9(i) = Y_{10}(i) - K_9b_9(i-1)$ $b_{10}(i) = b_9(i-1) + K_9Y_9(i)$	9 9
10	$Y_8(i) = Y_9(i) - K_8b_8(i-1)$ $b_9(i) = b_8(i-1) + K_8Y_8(i)$ $Y_7(i) = Y_8(i) - K_7b_7(i-1)$ $b_8(i) = b_7(i-1) + K_7Y_7(i)$	8 8 7 7
15	$Y_6(i) = Y_7(i) - K_6b_6(i-1)$ $b_7(i) = b_6(i-1) + K_6Y_6(i)$	6 6
20	$Y_5(i) = Y_6(i) - K_5b_5(i-1)$ $b_6(i) = b_5(i-1) + K_5Y_5(i)$ $Y_4(i) = Y_5(i) - K_4b_4(i-1)$ $b_5(i) = b_4(i-1) + K_4Y_4(i)$	5 5 4 4
25	$Y_3(i) = Y_4(i) - K_3b_3(i-1)$ $b_4(i) = b_3(i-1) + K_3Y_3(i)$	3 3
	$Y_2(i) = Y_3(i) - K_2b_2(i-1)$ $b_3(i) = b_2(i-1) + K_2Y_2(i)$	2 2
30	$Y_1(i) = Y_2(i) - K_1b_1(i-1)$ $b_2(i) = b_1(i-1) + K_1Y_1(i)$	1 1
	$b_1(i) = Y_1(i)$	

35

Claims

1. A speech synthesis system comprising:
 - input means (22—Figure 2a) for receiving frames of speech data, said frames of speech data comprising binary representations of speech-determinative data, wherein each said frame of speech data is defined by a binary representation including pitch data, energy data, and filter coefficient data,
 - interpolation means (50—Figure 2b) coupled to said input means for interpolating between adjacent frames of said speech data,
 - synthesizer means (50, 52, 54, 56, 58—Figure 2b) coupled to said input means and to said interpolation means for selectively converting said speech data and interpolated values thereof into signals representative of human speech, and
 - means (64, 18—Figure 2b) coupled to said synthesizer means for producing audible sound characterized in that said frames of speech data as received by said input means include coded frame rate data indicative of a variable time interval between the start of a current frame of speech data and the start of the next successive frame of speech data, and by decoding means (48—Figure 2a) coupled to said input means for decoding said frame rate data, said interpolation means being also coupled to said decoding means for providing a variable number of interpolation calculations to define interpolated speech values between adjacent frames of speech data from last implemented speech data in which the number of interpolation calculations and the time interval between the respective starts of adjacent frames of speech data in a given instance are determined by said frame rate data such that successive frames of speech data as respectively defined by a binary representation including pitch data, energy data, and filter coefficient data are sequentially delivered to said input means with a time interval therebetween which varies in accordance with the decoder value of said coded frame rate data accompanying the speech-determinative data of each speech data frame.
2. A speech synthesis system as set forth in claim 1, further characterized by frame control means (30—Figure 2a) coupled to said decoding means and said input means for controlling the rate at which new frames of speech data are provided to said input means.
3. A speech synthesis system as set forth in claim 2, further characterized in that said frame control means is effective for controlling the rate at which new frames of speech data are received by said input means in response to frame rate data included in a current frame of speech data, the time interval between

the receipt of successive new frames of speech data by said input means being variable and being determined by said frame rate data.

4. A speech synthesis system as set forth in either of claims 2 or 3, further characterized in that said interpolation means, is also coupled to said frame control means and is responsive to said frame rate data for providing the variable number of interpolation calculations between adjacent frames of speech data.

5. A speech synthesis system as set forth in any preceding claim, further characterized by memory means (12—Figure 1b) for storing selectable speech data, and controller means (14—Figure 1b) operably associated with said memory means for controlling the selective accessing of said speech data from said memory means, said input means being coupled to said memory means for receiving selected frames of speech data as accessed under control of said controller means.

6. A speech synthesis system as set forth in claim 5, further characterized by switch means (16—Figure 1b) operably associated with said controller means and responsive to operator commands, said controller means being responsive to said switch means for controlling the selective accessing of said speech data from said memory means in accordance with said operator commands.

7. A speech synthesis system as set forth in claim 6, further characterized in that said switch means comprises a keyboard having a plurality of operator actuatable key switches.

8. A speech synthesis system as set forth in any preceding claim, further characterized in that said variable number of interpolation calculations is $2 \times n$ where n is an integer less than one hundred.

9. A speech synthesis system as set forth in any preceding claim, further characterized in that said speech synthesis system comprises a portable learning aid.

10. A speech synthesis system as set forth in any of claims 1 to 8, further characterized in that said speech synthesis system comprises a portable calculator device.

11. A speech synthesis system as set forth in any of claims 1 to 8, further characterized in that said speech synthesis system comprises a portable language translator device.

12. A speech synthesis system as set forth in any preceding claim, further characterized in that said synthesizer means is effective for selectively converting said speech data into digital signals representative of human speech, and said means for producing audible sound comprising digital to analog converter means (64—Figure 2b) coupled to said synthesizer means for converting said digital signals representative of human speech into analog signals, and audio means (18—Figure 2b) coupled to said converter means for converting said analog signals into audible sound.

13. A speech synthesis system as set forth in claim 12, further characterized in that said audio means comprises a speaker.

14. A speech synthesis system as set forth in claim 12, further characterized in that said audio means includes amplifier means coupled to a speaker.

Patentansprüche

1. Sprachsynthesesystem mit

—Eingangsmitteln (22—Fig. 2a) für den Empfang von Sprachdatenrahmen, die aus binären Darstellungen sprachbestimmender Daten bestehen, wobei jeder Rahmen der Sprachdaten durch eine binäre Darstellung mit Tonhöhendaten, Energiedaten und Filterkoeffizientendaten definiert ist,

—Interpolationsmitteln (50—Fig. 2b), die mit den Eingangsmitteln gekoppelt sind und dem Interpolieren zwischen benachbarten Rahmen der Sprachdaten dienen,

—Synthesermitteln (50, 52, 54, 56, 58—Fig. 2b), die mit den Eingangsmitteln und den Interpolationsmitteln gekoppelt sind und die Sprachdaten sowie deren interpolierte Werte selektiv in Signale umsetzen, die menschliche Sprache präsentieren, und

—Mitteln (64, 18—Fig. 2b), die mit den Synthesermitteln gekoppelt sind und hörbare Töne erzeugen, dadurch gekennzeichnet, daß die Sprachrahmendaten, wie sie von den Eingangsmitteln empfangen werden, codierte Rahmenratendaten enthalten, die ein variables Zeitintervall zwischen dem Beginn eines gerade vorliegenden Sprachdatenrahmens und dem Beginn des nächstfolgenden Sprachdatenrahmens

angeben, wobei Decodiermittel (48—Fig. 2a) vorgesehen sind, die mit den Eingabemitteln gekoppelt sind und die Rahmenratendaten decodieren, wobei die Interpolationsmittel ebenfalls mit den Decodiermitteln verbunden sind, damit eine variable Anzahl von Interpolationsberechnungen zur Definition interpolierter Sprachwerte zwischen benachbarten Sprachdatenrahmen aus zuletzt erzeugten Sprachdaten definiert werden, bei denen die Anzahl der Interpolationsberechnungen und das Zeitintervall zwischen den jeweiligen Anfängen benachbarter Sprachdatenrahmen in einem gegebenen Zeitpunkt durch die Sprachratendaten so bestimmt werden, daß aufeinanderfolgende Sprachdatenrahmen, die jeweils durch eine binäre Darstellung durch Tonhöhendaten, Energiedaten und Filterkoeffizientendaten definiert sind, nacheinander an die Eingabemittel mit einem dazwischenliegenden Zeitintervall geliefert werden, das sich

entsprechenden dem codierten Wert der Rahmenratendaten verändert, die die sprachbestimmenden Daten jedes Sprachdatenrahmens leiten.

2. Sprachsynthesesystem nach Anspruch 1, gekennzeichnet durch Rahmensteuermittel (30—Fig. 2a), die mit den Decodiermitteln und den Eingangsmitteln verbunden sind und die Rate steuern, mit der neue Sprachdatenrahmen an die Eingangsmittel geliefert werden.

3. Sprachsynthesesystem nach Anspruch 2, dadurch gekennzeichnet, daß die Rahmensteuermittel die

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Rate, mit der neue Sprachdatenrahmen von den Eingangsmitteln empfangen werden, in Abhängigkeit von den Rahmenratendaten steuern, die in einem gerade vorliegenden Sprachdatenrahmen enthalten sind, sowie das Zeitintervall zwischen dem Empfang aufeinanderfolgender neuer Sprachdatenrahmen durch die Eingangsmittel veränderlich ist und von den Rahmenratendaten bestimmt wird.

5 4. Sprachsynthesystem nach Anspruch 2 oder 3, dadurch gekennzeichnet, daß die Interpolationsmittel ebenfalls mit den Rahmensteuermitteln verbunden sind und abhängig von den Rahmenratendaten die variable Anzahl der Interpolationsberechnungen zwischen benachbarten Sprachdatenrahmen liefern.

10 5. Sprachsynthesystem nach einem der vorhergehenden Ansprüche, gekennzeichnet durch Speichermittel (12—Fig. 1b) zum Speichern auswählbarer Sprachdaten und Steuermitteln (14—Fig. 1b), die den Speichermitteln wirkungsmäßig zugeordnet sind und den selektiven Zugriff auf die Sprachdaten aus den Speichermitteln steuern, wobei die Eingangsmittel mit den Speichermitteln gekoppelt sind, damit sie ausgewählte Sprachdatenrahmen entsprechend dem Zugriff unter der Steuerung durch die Steuermittel empfangen.

15 6. Sprachsynthesystem nach Anspruch 5, gekennzeichnet durch Schaltermittel (16—Fig. 1b), die den Steuermitteln wirkungsmäßig zugeordnet sind und abhängig von Bedienerbefehlen arbeiten, wobei die Steuermittel in Abhängigkeit von den Schaltermitteln das selektive Umgreifen auf die Sprachdaten aus den Speichermitteln gemäß den Bedienerbefehlen steuern.

7. Sprachsynthesystem nach Anspruch 6, dadurch gekennzeichnet, daß die Schaltermittel aus einer Tastatur bestehen, die mehrere von einem Bediener betätigbare Tastenschalter aufweist.

20 8. Sprachsynthesystem nach einem der vorhergehenden Ansprüche, dadurch gekennzeichnet, daß die variable Anzahl von Interpolationsberechnungen $2 \times n$ beträgt, wobei n eine ganze Zahl kleiner als Hundert ist.

9. Sprachsynthesystem nach einem der vorhergehenden Ansprüche, dadurch gekennzeichnet, daß das Sprachsynthesystem eine tragbare Lernhilfe ist.

25 10. Sprachsynthesystem nach einem der Ansprüche 1 bis 8, dadurch gekennzeichnet, daß das Sprachsynthesystem ein tragbares Rechenggerät ist.

11. Sprachsynthesystem nach einem der Ansprüche 1 bis 8, dadurch gekennzeichnet, daß das Sprachsynthesystem ein tragbares Sprachübersetzungsgerät ist.

30 12. Sprachsynthesystem nach einem der vorhergehenden Ansprüche, dadurch gekennzeichnet, daß die Synthesizermittel die Sprachdaten selektiv in digitale Signale umsetzen, die menschliche Sprache repräsentieren, und daß die Mittel zum Erzeugen hörbarer Töne Digital-Analog-Umsetzermittel (64—Fig. 2b) sind, die mit den Synthesizermitteln verbunden sind und die menschliche Sprache repräsentierenden digitalen Signale in analoge Signale umsetzen, wobei Tonmittel (18—Fig. 2b) mit den Umsetzermitteln zum Umsetzen der analogen Signale in hörbare Töne verbunden sind.

35 13. Sprachsynthesystem nach Anspruch 12, dadurch gekennzeichnet, daß die Tonmittel einen Lautsprecher umfassen.

14. Sprachsynthesystem nach Anspruch 12, dadurch gekennzeichnet, daß die Tonmittel einen mit dem Lautsprecher verbundenen Verstärker enthalten.

40 Revendications

1. Système de synthèse de la parole comportant:

45 —des moyens d'entrée (22-figure 2a) pour recevoir des trames de données de parole, lesdites trames de données de parole consistant en des représentations binaires de données déterminant la parole, dans lesquelles chacune desdites trames de données de parole est définie par une représentation binaire comprenant des données de hauteur, des données d'énergie et des données de coefficients de filtre,

—des moyens d'interpolation (50-figure 2b) couplés avec lesdits moyens d'entrée pour l'interpolation entre des trames voisines desdites données de parole,

50 —des moyens de synthétiseur (50, 52, 54, 56, 58-figure 2b) couplés avec lesdits moyens d'entrée et lesdits moyens d'interpolation pour convertir sélectivement lesdites données de parole et leurs valeurs interpolées en des signaux représentant la parole humaine, et

—des moyens (64, 18-figure 2b) couplés avec lesdits moyens de synthétiseur pour produire un son audible

55 caractérisé en ce que lesdites trames de données de parole, telles que reçues par lesdits moyens d'entrée, comprennent des données de fréquence de trames codées indiquant un intervalle de temps variable entre le début d'une trame en cours des données de parole et le début de la trame qui suit immédiatement des données de parole, et par des moyens de décodage (48-figure 2a) couplés avec lesdits moyens d'entrée pour décoder lesdites données de fréquence en trame, lesdits moyens d'interpolation étant également couplés avec lesdits moyens de décodage pour produire un nombre variable de calculs d'interpolation pour définir des valeurs de parole interpolées entre les trames voisines des données de parole, à partir des dernières données de parole réalisées dans lesquelles le nombre des calculs d'interpolation et l'intervalle de temps entre les débuts respectifs de trames voisines des données de parole dans un cas donné sont déterminés par lesdites données de fréquence de trame de manière que des trames successives de données de parole telles que définies respectivement par une représentation binaire 65 comprenant des données de hauteur, des données d'énergie et des données de coefficients de filtre soient

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délivrées séquentiellement auxdits moyens d'entrée avec un intervalle de temps entre elles qui varie en fonction de la valeur décodée desdites données de fréquence de trame codées accompagnant les données de détermination de parole de chaque trame de données de parole.

5 2. Système de synthèse de parole selon la revendication 1, caractérisé en outre par des moyens de commande de trame (30-figure 2a) couplés avec lesdits moyens de décodage et lesdits moyens d'entrée pour commander la fréquence à laquelle des nouvelles trames de données de parole sont produits pour lesdits moyens d'entrée.

10 3. Système de synthèse de parole selon la revendication 2, caractérisé en outre en ce que lesdits moyens de commande de trame ont pour fonction de commander la fréquence à laquelle des nouvelles trames des données de parole sont reçues par lesdits moyens d'entrée en réponse aux données de fréquence de trames incluses dans une trame en cours de données de parole, l'intervalle de temps entre la réception de nouvelles trames successives de données de parole par lesdits moyens d'entrée étant variable étant déterminé par lesdites données de fréquence de trame.

15 4. Système de synthèse de parole selon la revendication 2 ou 3, caractérisé en outre en ce que lesdits moyens d'interpolation sont également couplés avec lesdits moyens de commande de trame et réagissent auxdites données de fréquence de trame en produisant le nombre variable de calcul d'interpolation entre des trames voisines de données de parole.

20 5. Système de synthèse de parole selon l'une quelconque des revendications précédentes, caractérisé en outre par des moyens de mémoire (12-figure 1b) pour mémoriser des données de parole pouvant être sélectionnées et des moyens de commande (14-figure 1b) associés en fonctionnement avec lesdits moyens de mémoire pour commander l'accès sélectif desdites données de parole dans lesdits moyens de mémoire, lesdits moyens d'entrée étant couplés avec lesdits moyens de mémoire pour recevoir des trames sélectionnées de données de parole, accédées à la commande desdits moyens de commande.

25 6. Système de synthèse de parole selon la revendication 5, caractérisé en outre par des moyens de commutation (16-figure 1b) associés en fonctionnement avec lesdits moyens de commande et réagissant à des commandes de l'opérateur, lesdits moyens de commande réagissant auxdits moyens de commutation en commandant l'accès sélectif desdites données de parole dans lesdits moyens de mémoire en fonction desdites commandes de l'opérateur.

30 7. Système de synthèse de parole selon la revendication 6, caractérisé en outre en ce que lesdits moyens de commutation comprennent un clavier avec plusieurs commutateurs à touches pouvant être actionnés par un opérateur.

8. Système de synthèse de parole selon l'une quelconque des revendications précédentes, caractérisé en outre en ce que ledit nombre variable des calculs d'interpolation est $2 \times n$, où n est un entier inférieur à cent.

35 9. Système de synthèse de parole selon l'une quelconque des revendications précédentes, caractérisé en outre en ce que ledit système de synthèse de parole consiste en une aide portative à l'enseignement.

10. Système de synthèse de parole selon l'une quelconque des revendications 1 à 8, caractérisé en outre en ce que ledit système de synthèse de parole consiste en un dispositif calculateur portatif.

40 11. Système de synthèse de parole selon l'une quelconque des revendications 1 à 8, caractérisé en outre en ce que ledit système de synthèse de parole consiste en un dispositif portatif de traduction de langage.

45 12. Système de synthèse de la parole selon l'une quelconque des revendications précédentes, caractérisé en outre en ce que lesdits moyens synthétiseurs ont pour fonction de convertir sélectivement lesdites données de parole en des signaux numériques représentant une parole humaine, et lesdits moyens de production de son audible consistant en des moyens de convertisseur numérique-analogique (64-figure 2b) couplés avec lesdits moyens synthétiseurs pour convertir lesdits signaux numériques représentant une parole humaine en des signaux analogiques, et des moyens de son (18-figure 2b) couplés avec lesdits moyens convertisseurs pour convertir lesdits signaux analogiques en un son audible.

50 13. Système de synthèse de parole selon la revendication 12, caractérisé en outre en ce que lesdits moyens de son comprennent en un haut-parleur.

14. Système de synthèse de la parole selon la revendication 12, caractérisé en outre en ce que lesdits moyens de son comprennent des moyens d'amplificateur couplés avec un haut-parleur.

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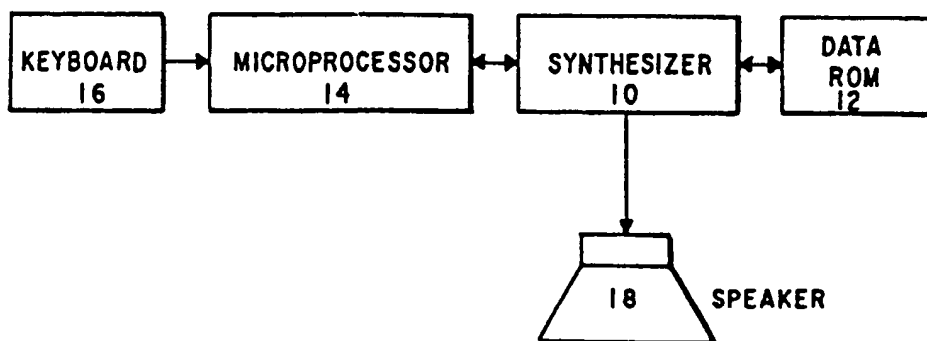
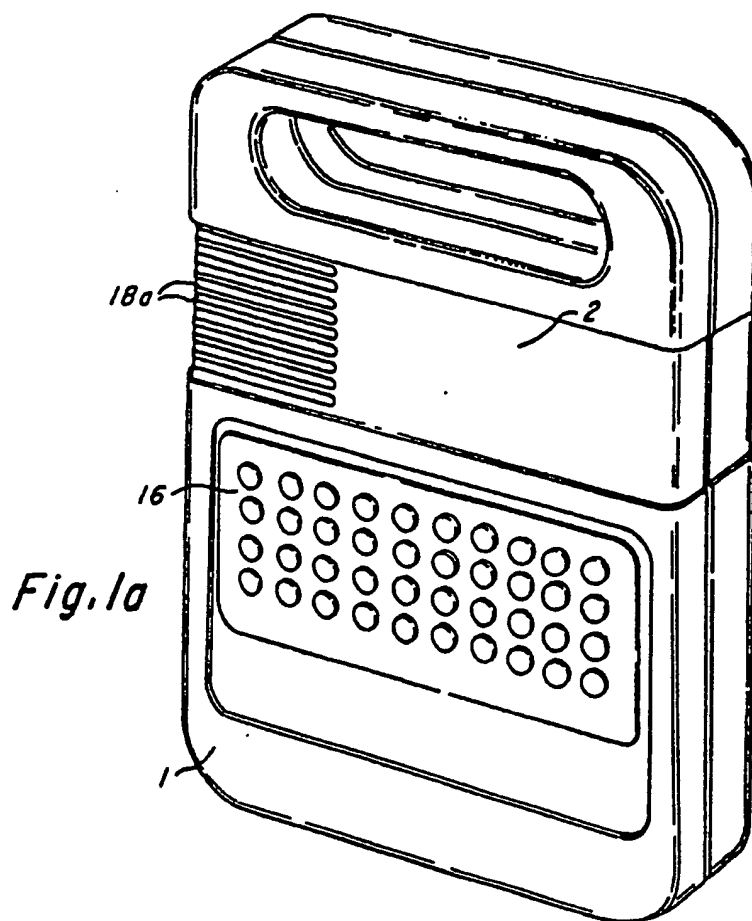
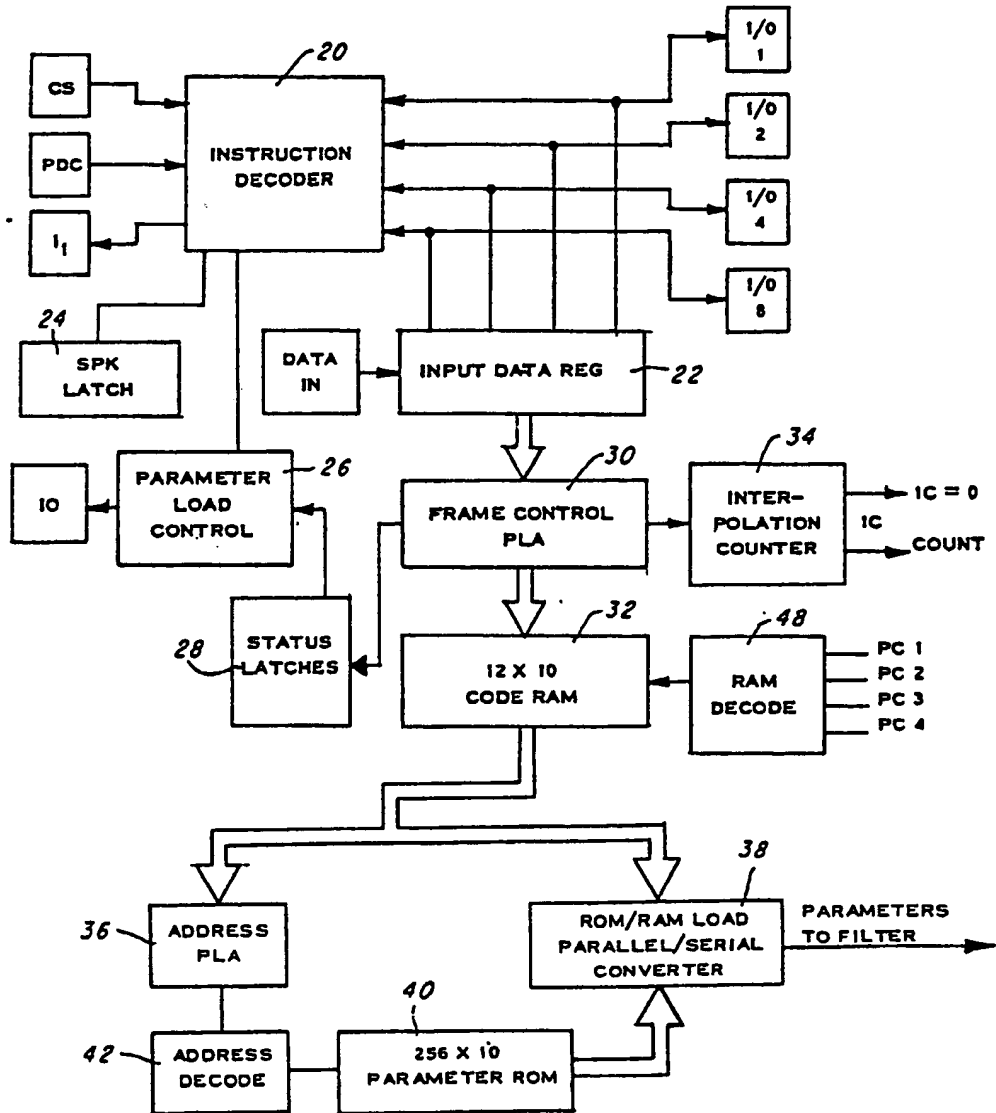


Fig. 1b

Fig.2a



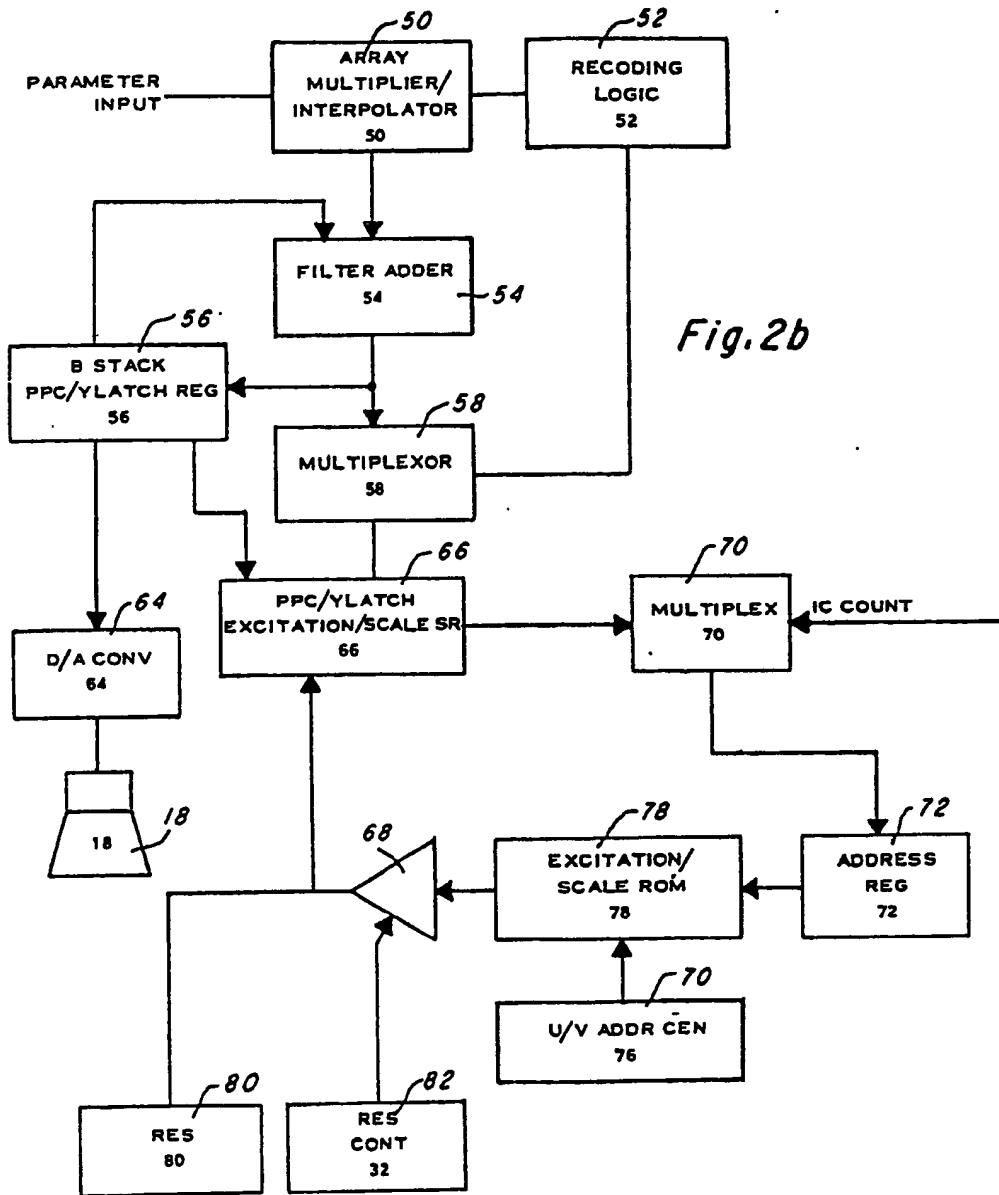
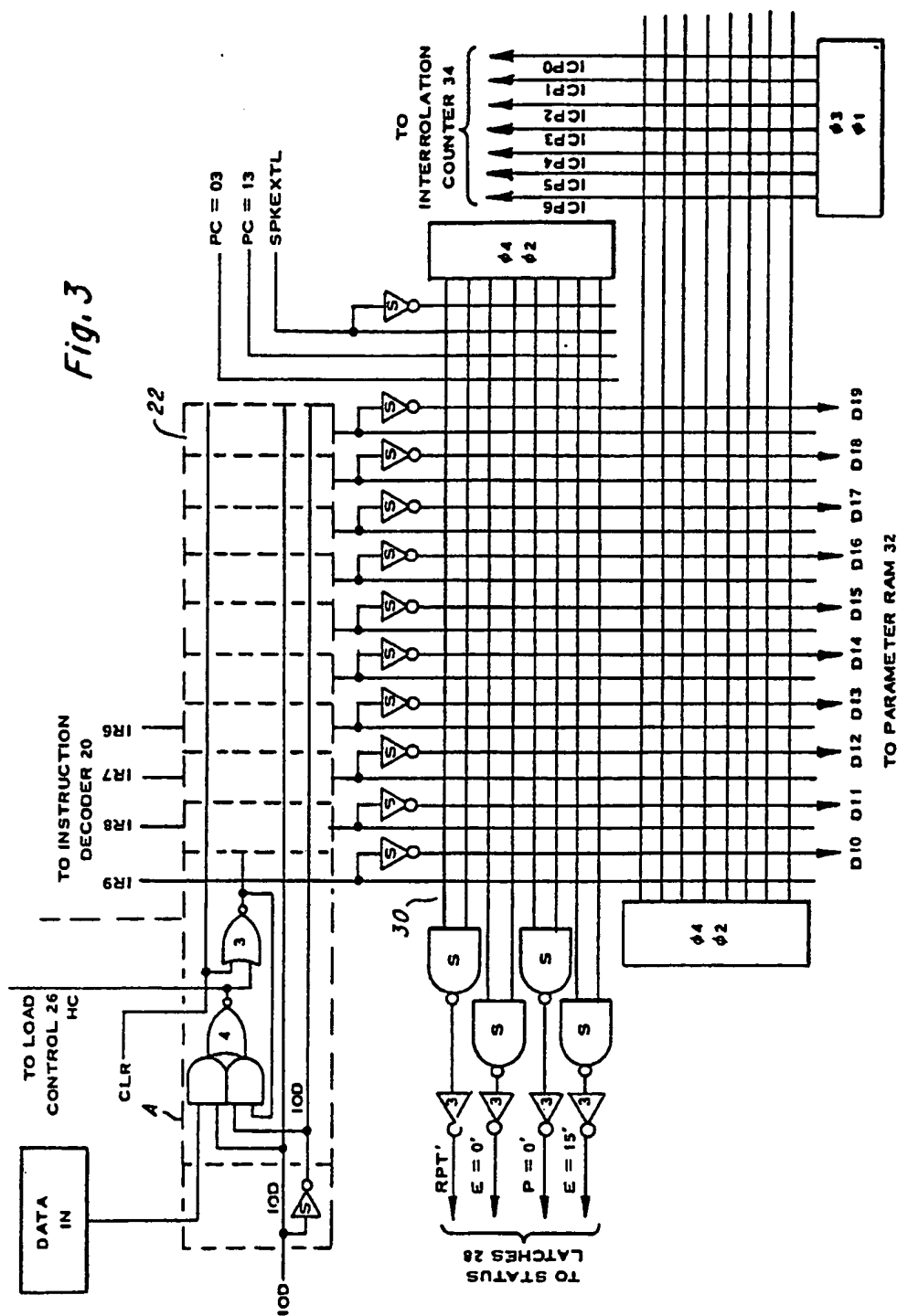


Fig. 3



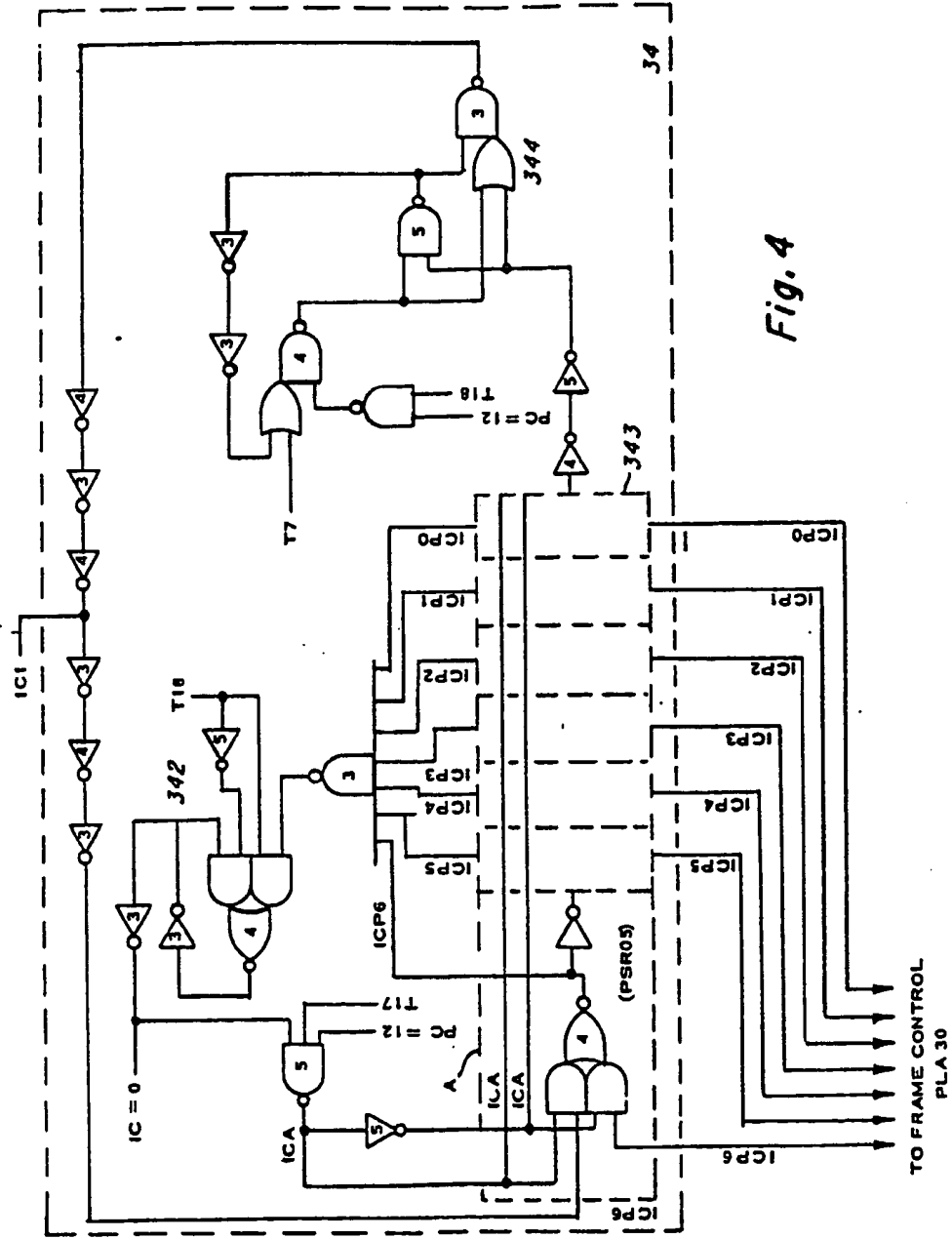


Fig. 4

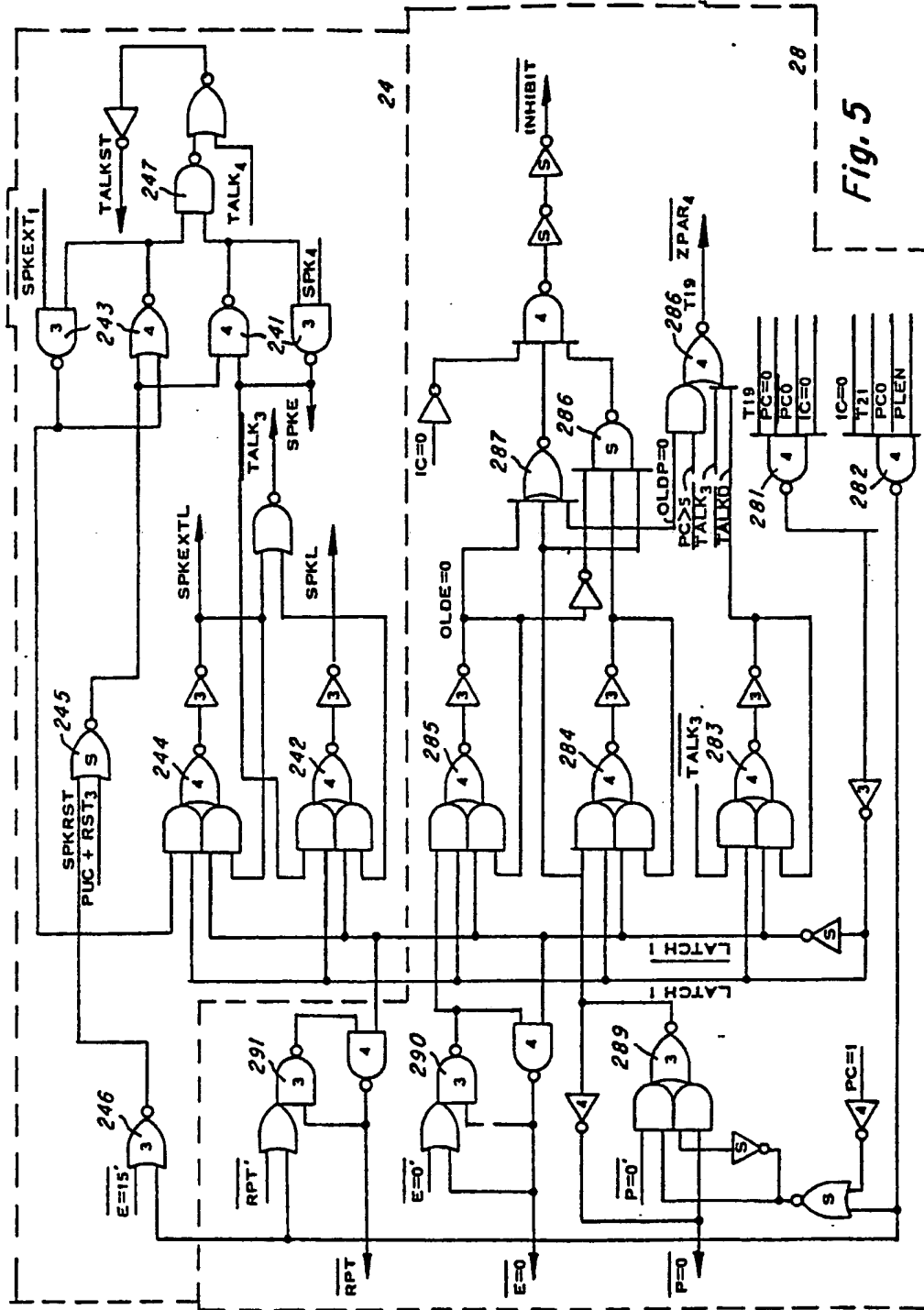


Fig. 5

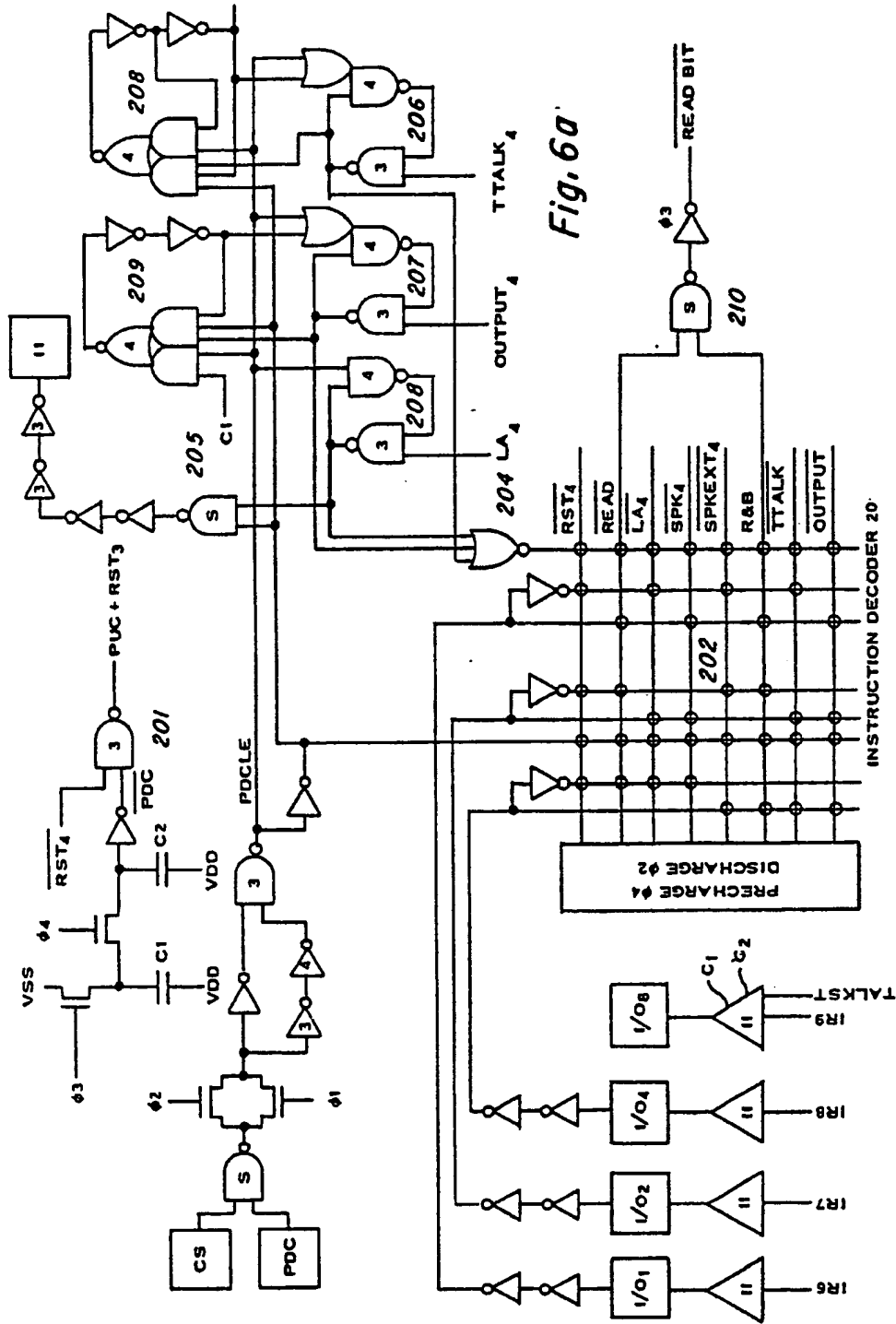
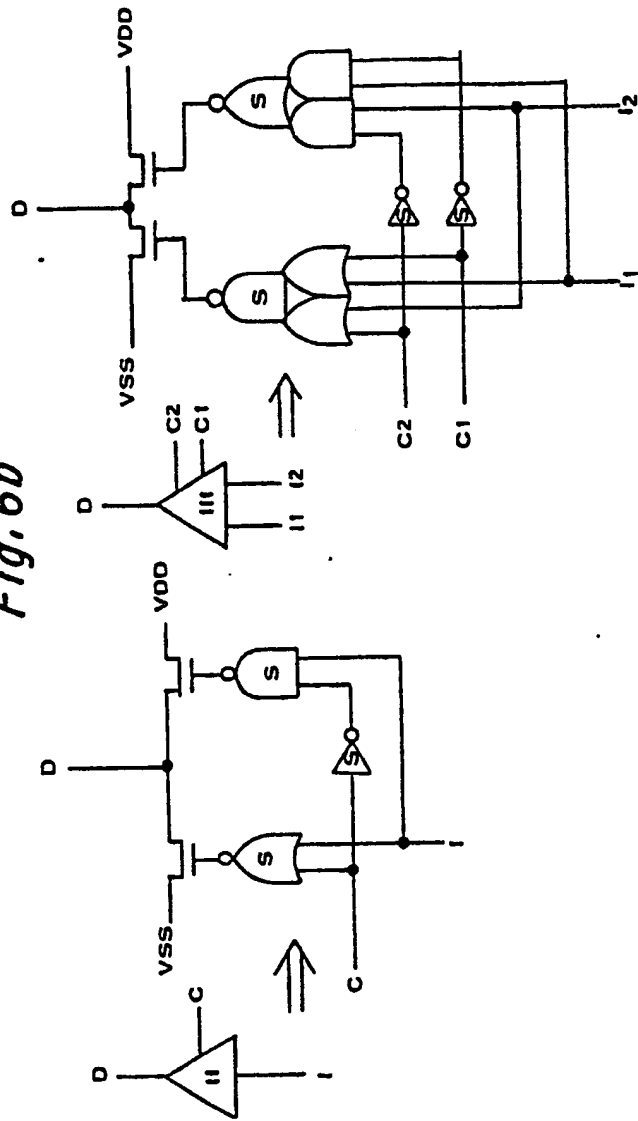


Fig. 6a

Fig. 6b



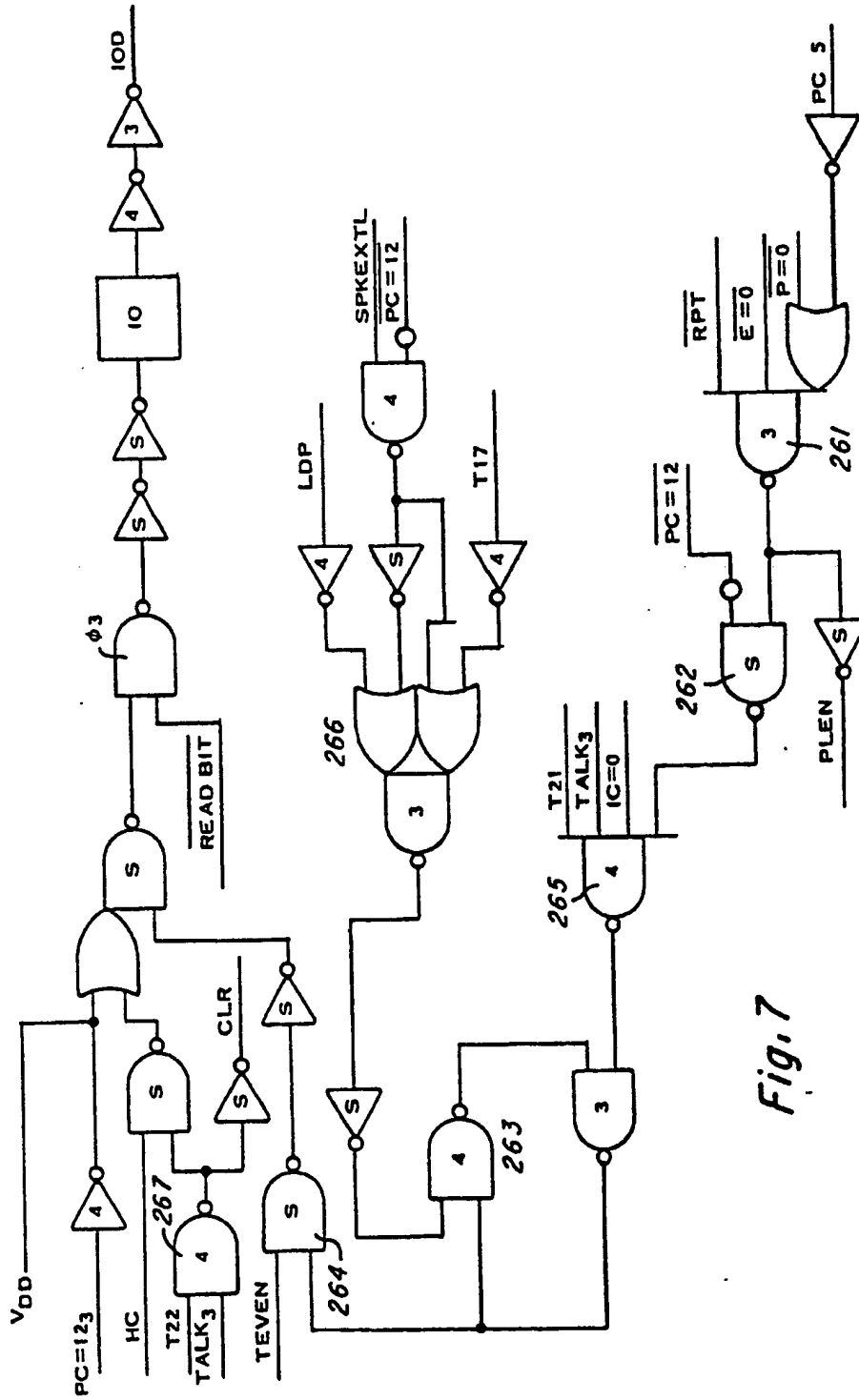


Fig. 7

Fig. 8a

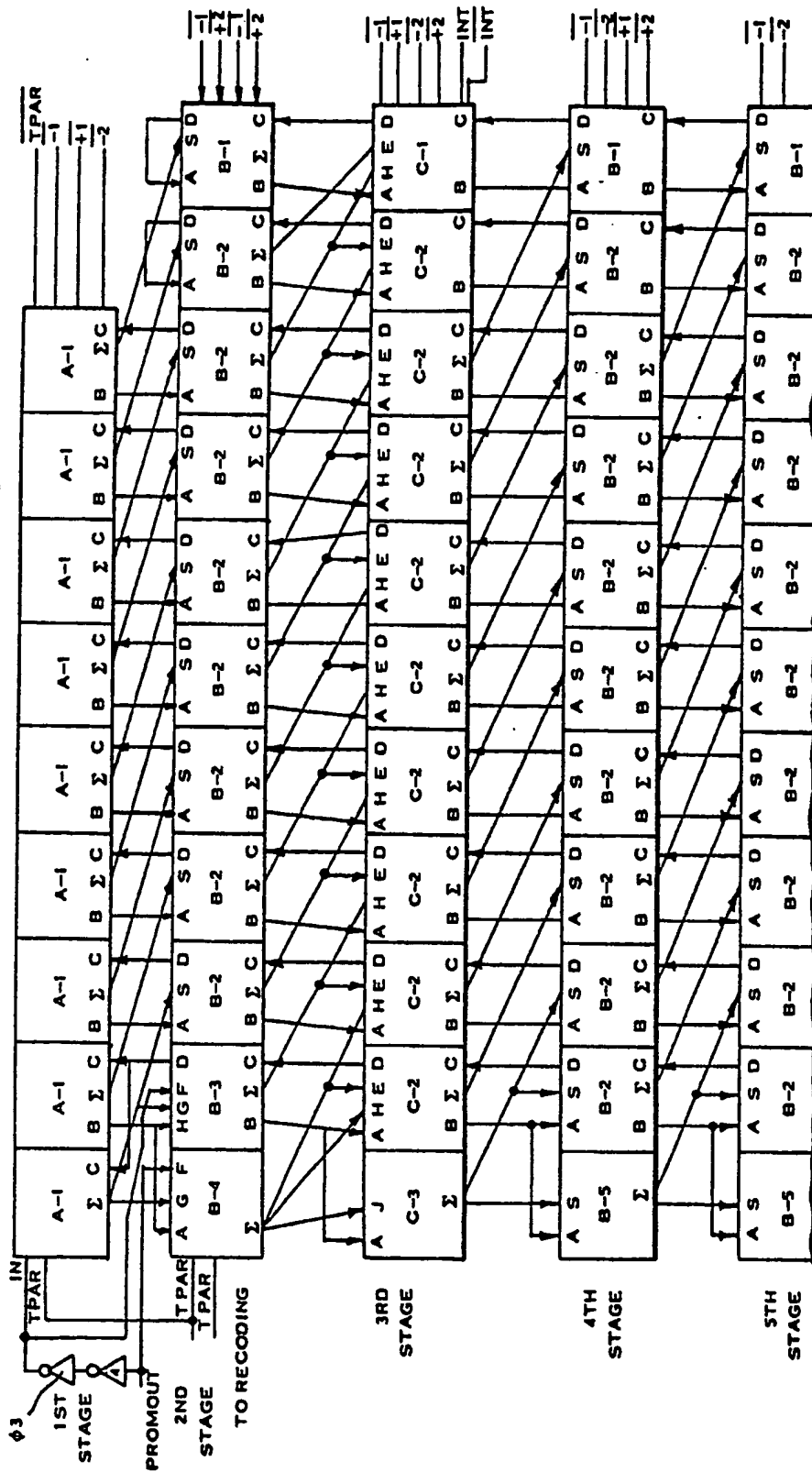
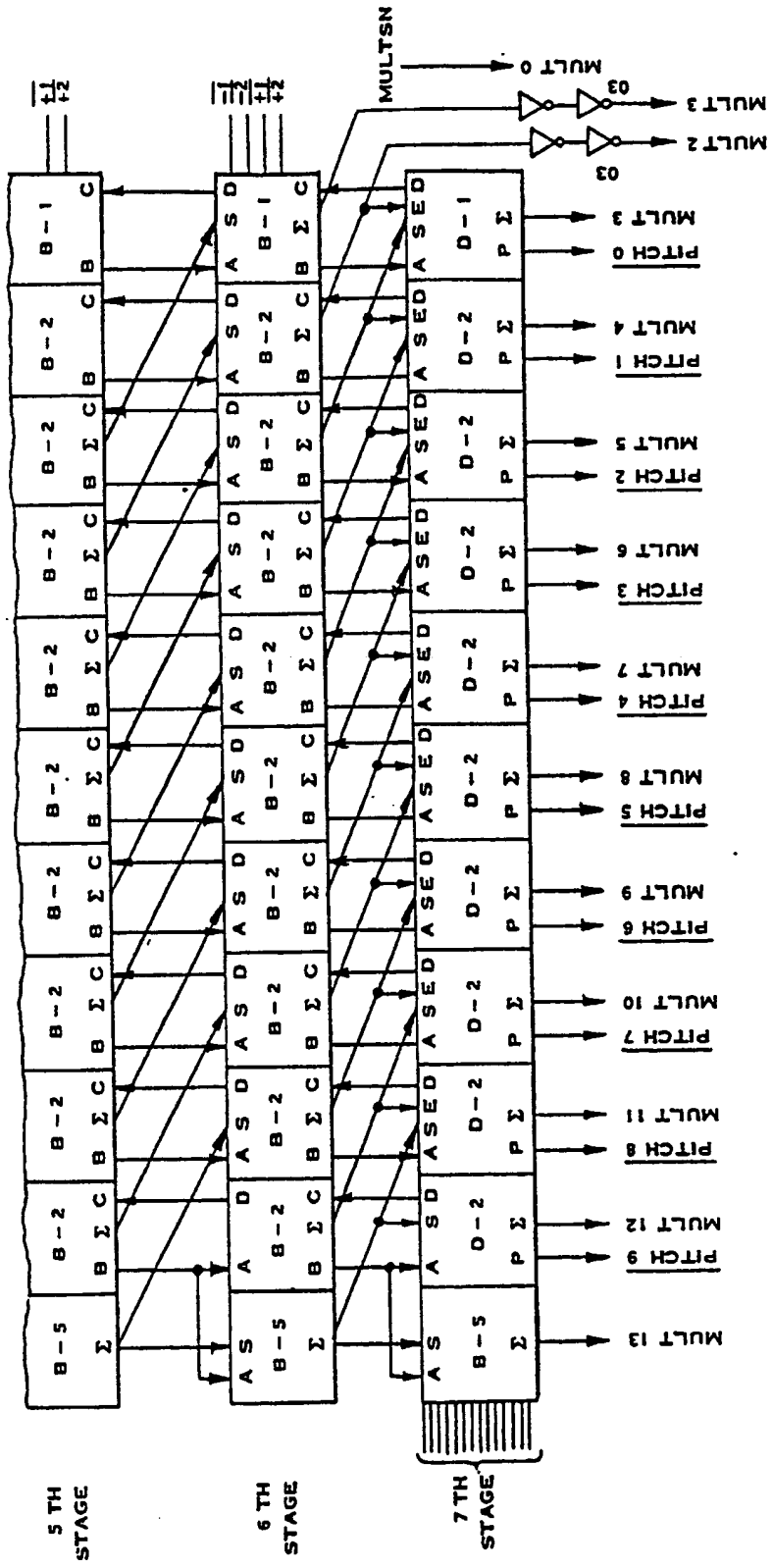


Fig. 8b



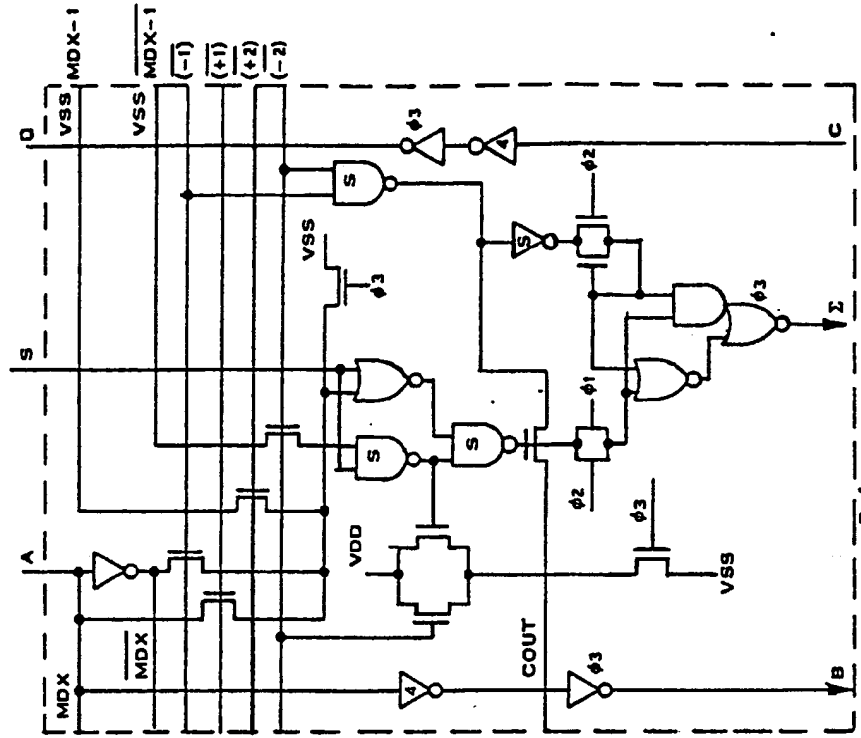


Fig. 9ab

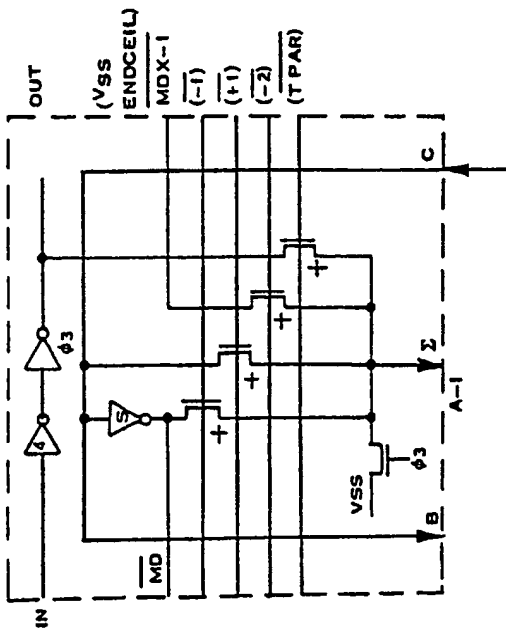
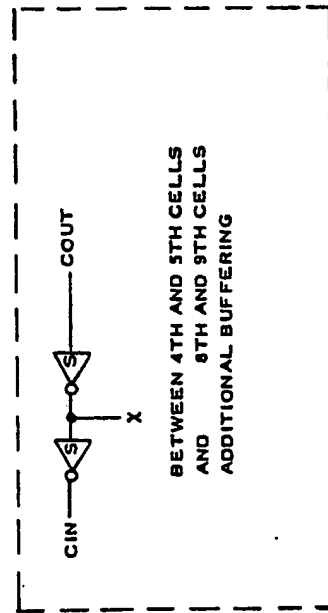
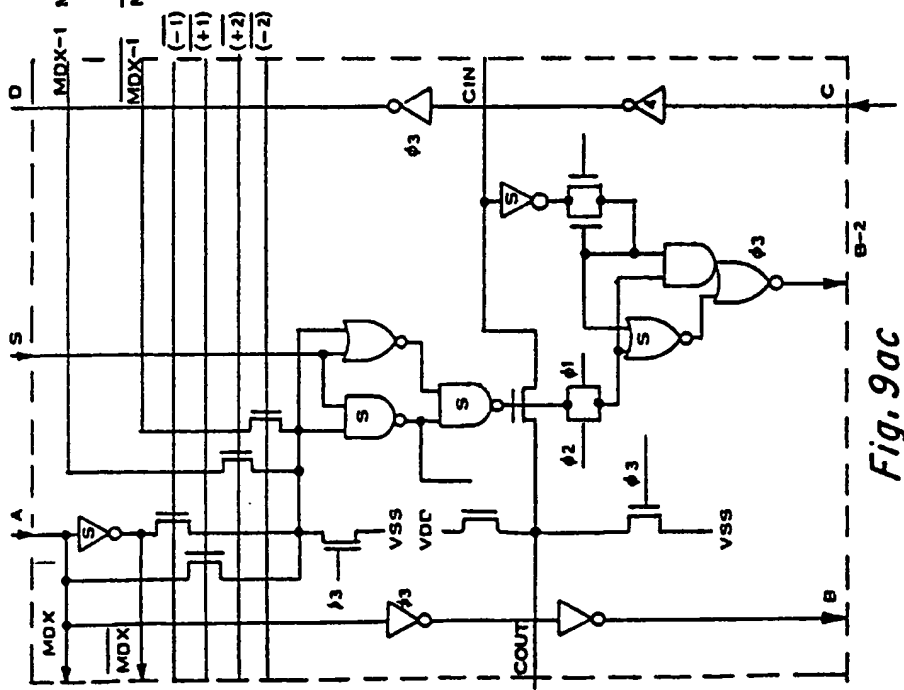
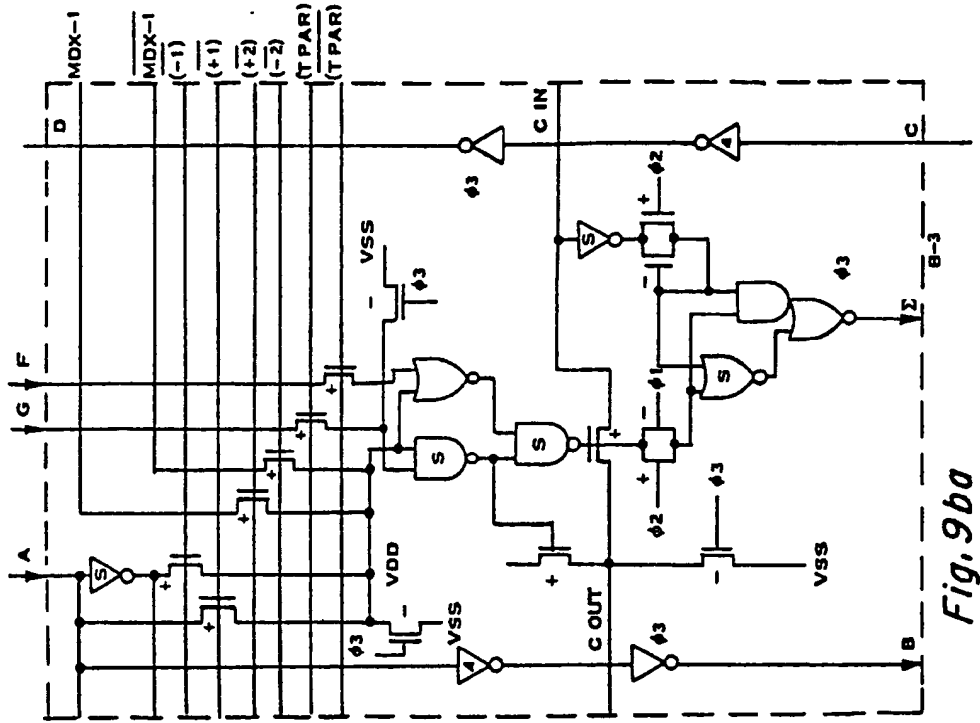


Fig. 9aa



NOTE A



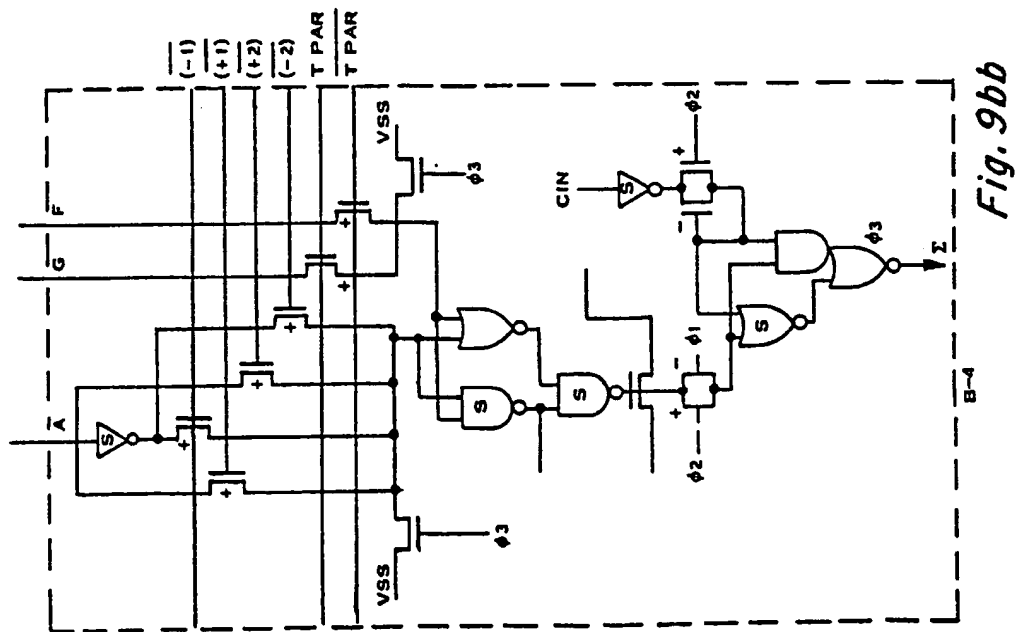
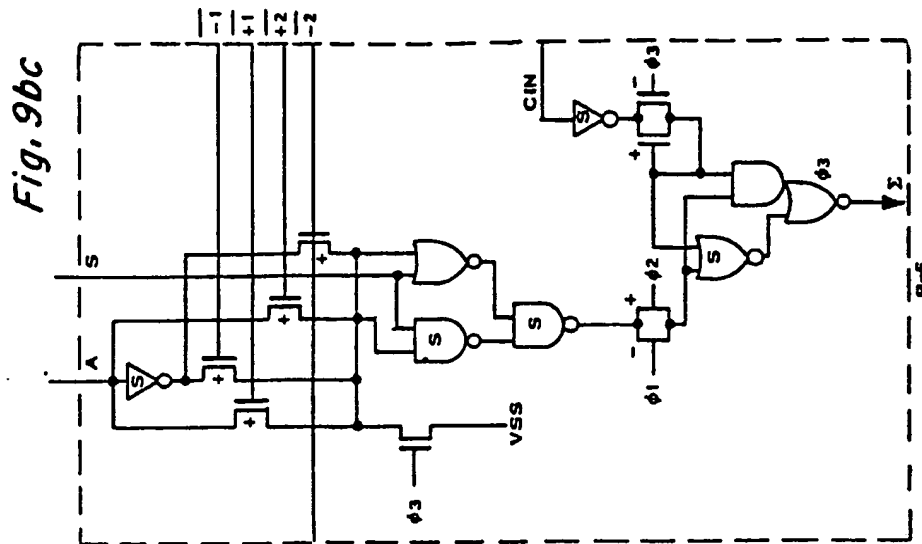


Fig. 9ca

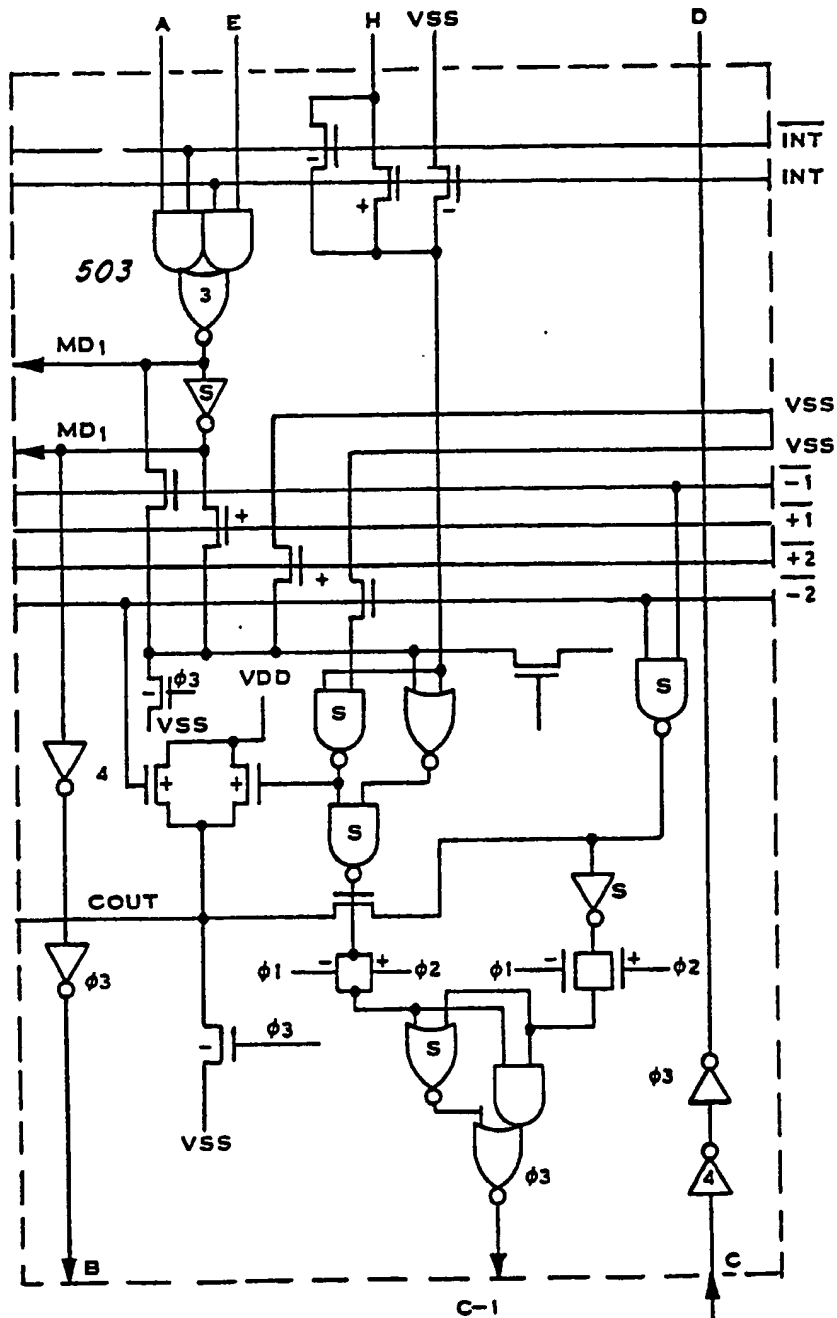


Fig. 9cb

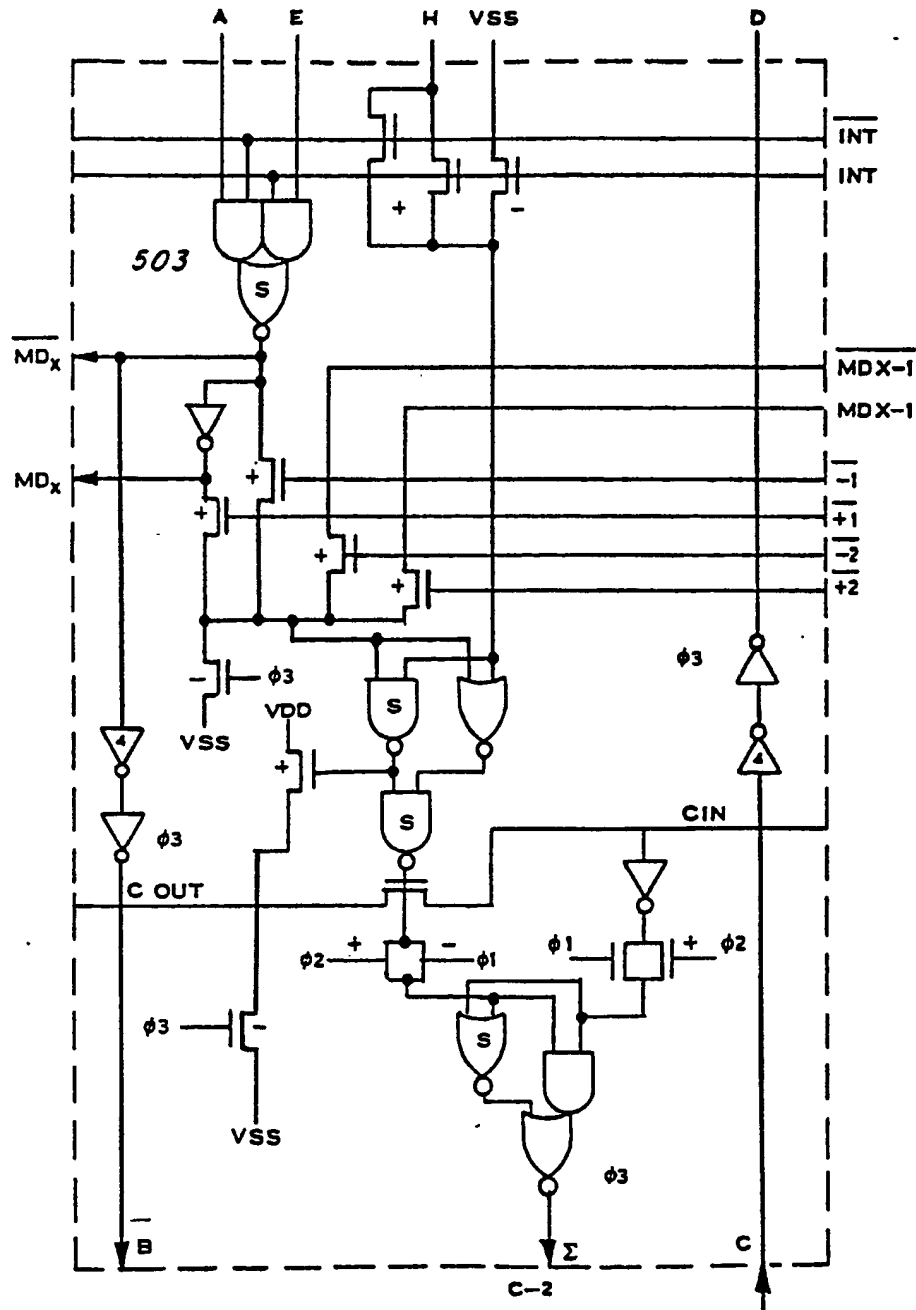


Fig. 9cc

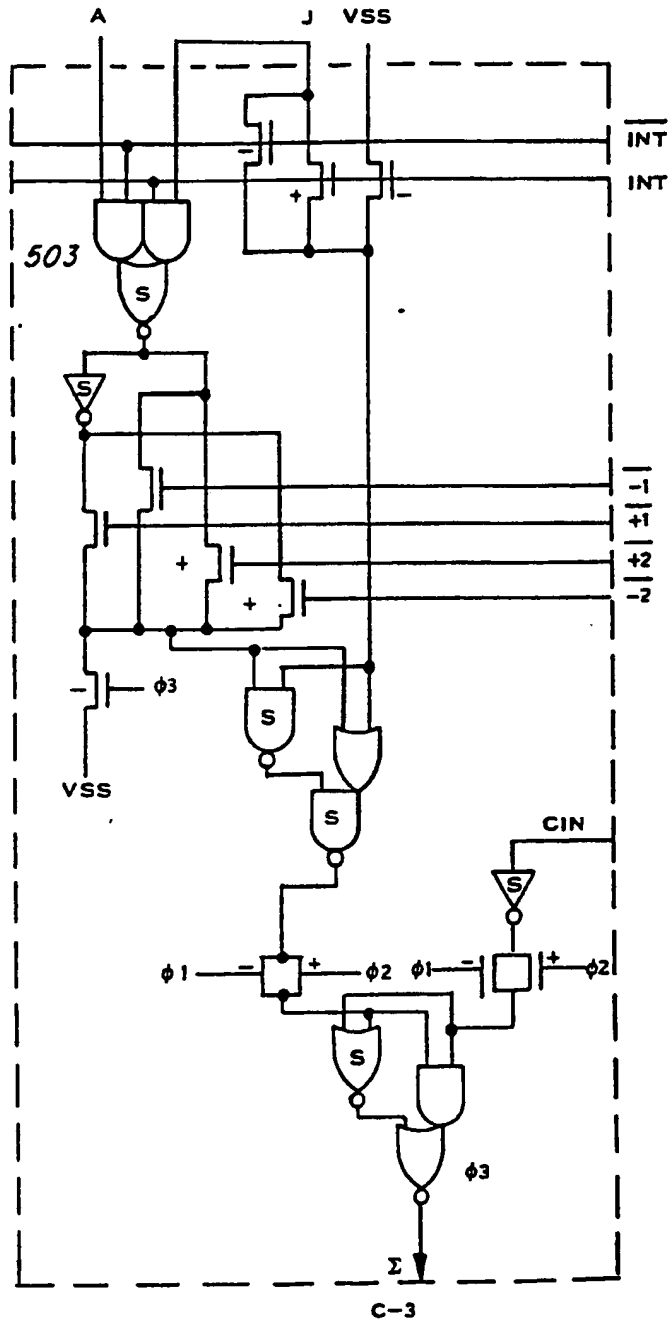


Fig. 9da

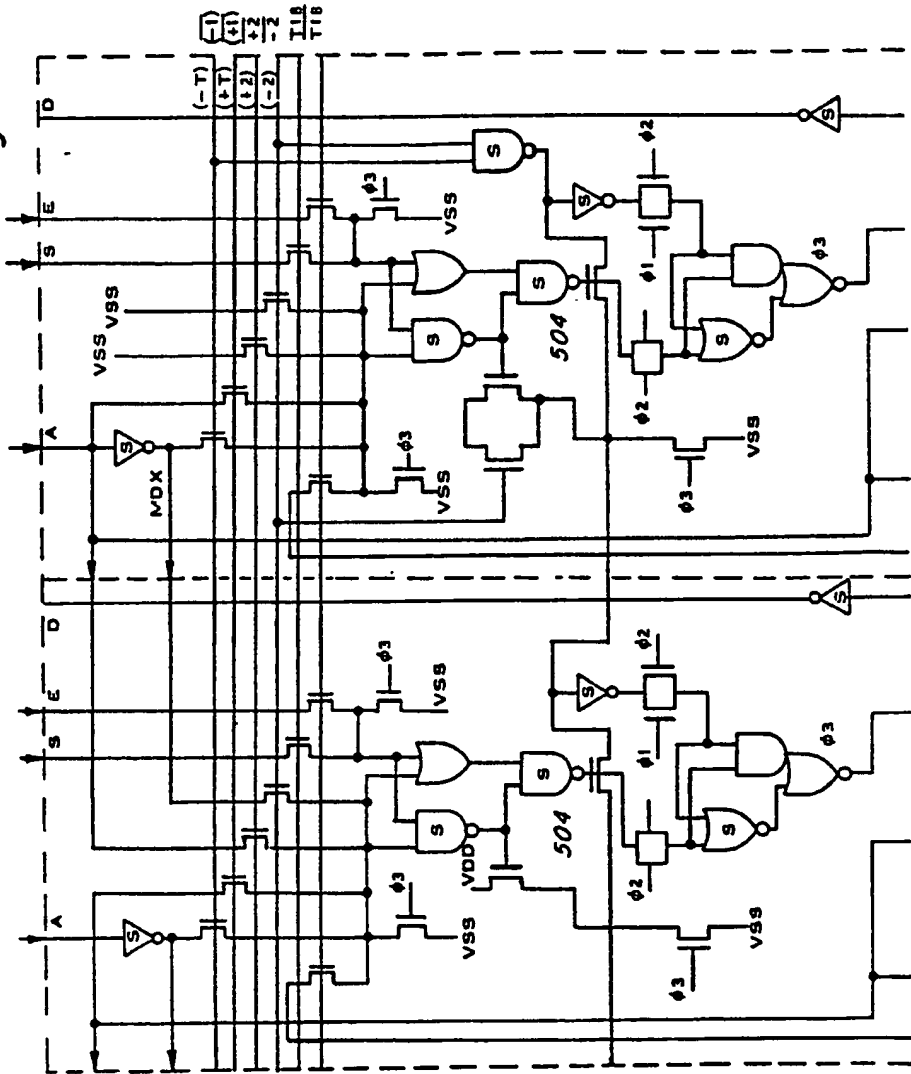
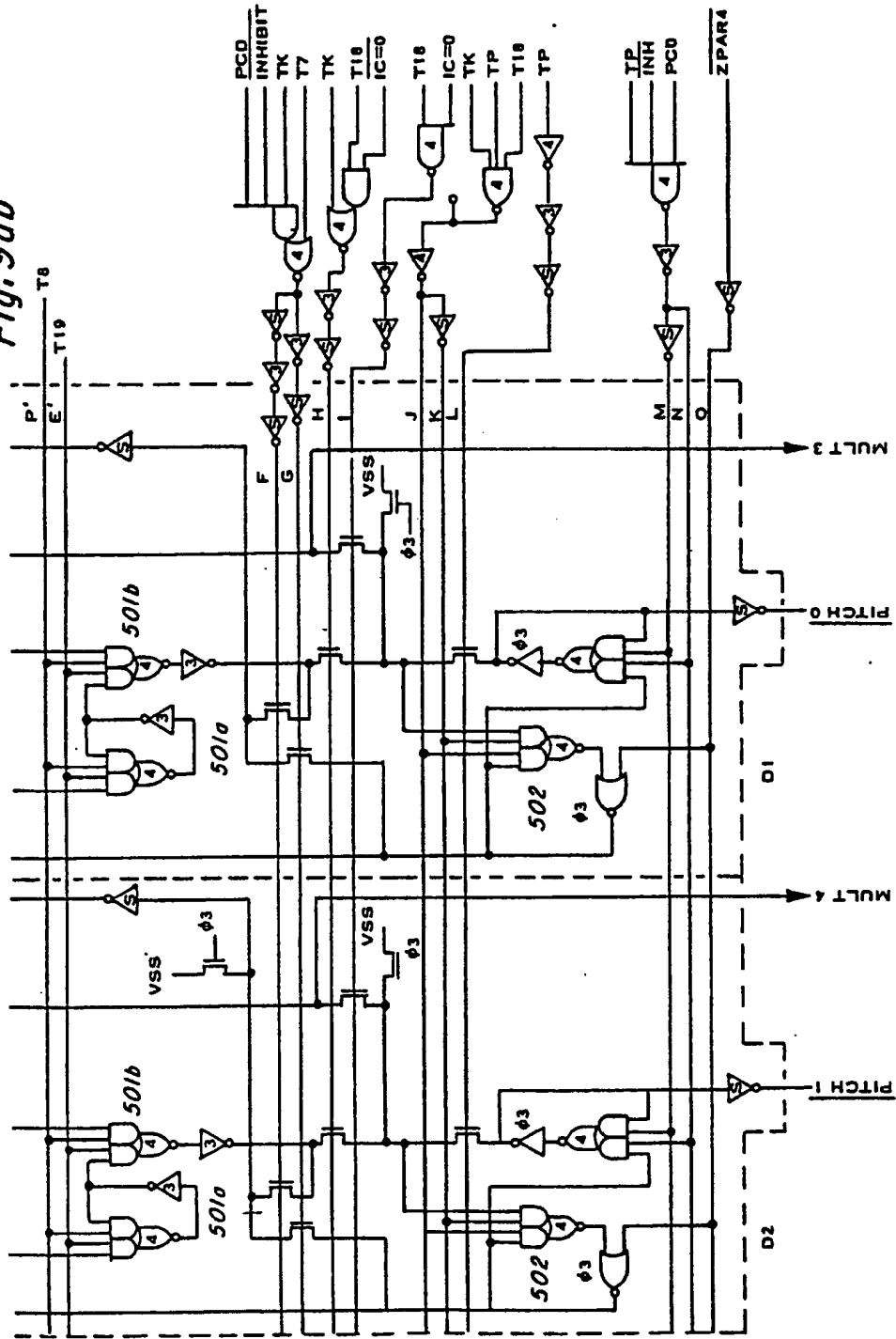


Fig. 9db



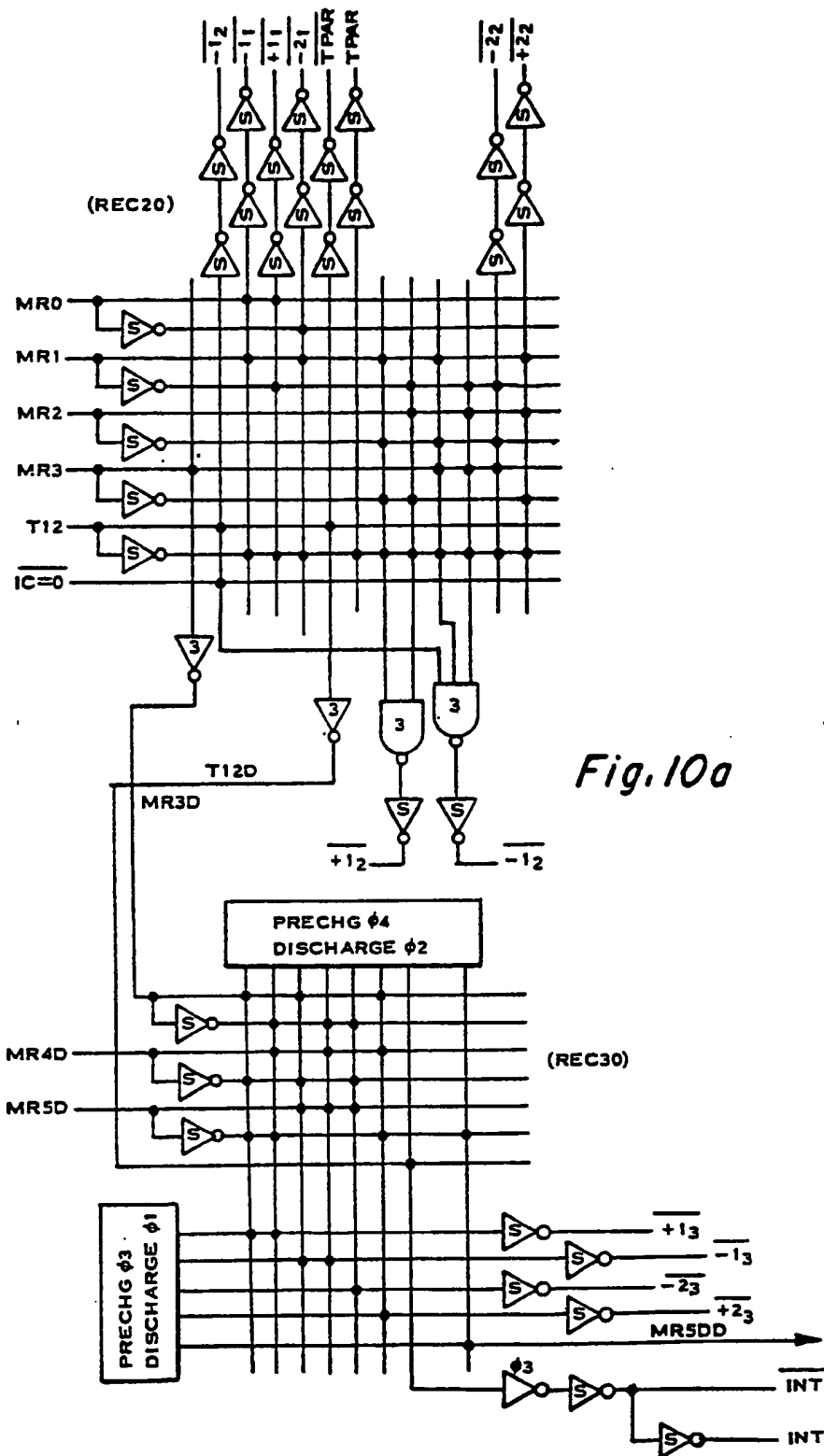


Fig. 10a

Fig. 10b

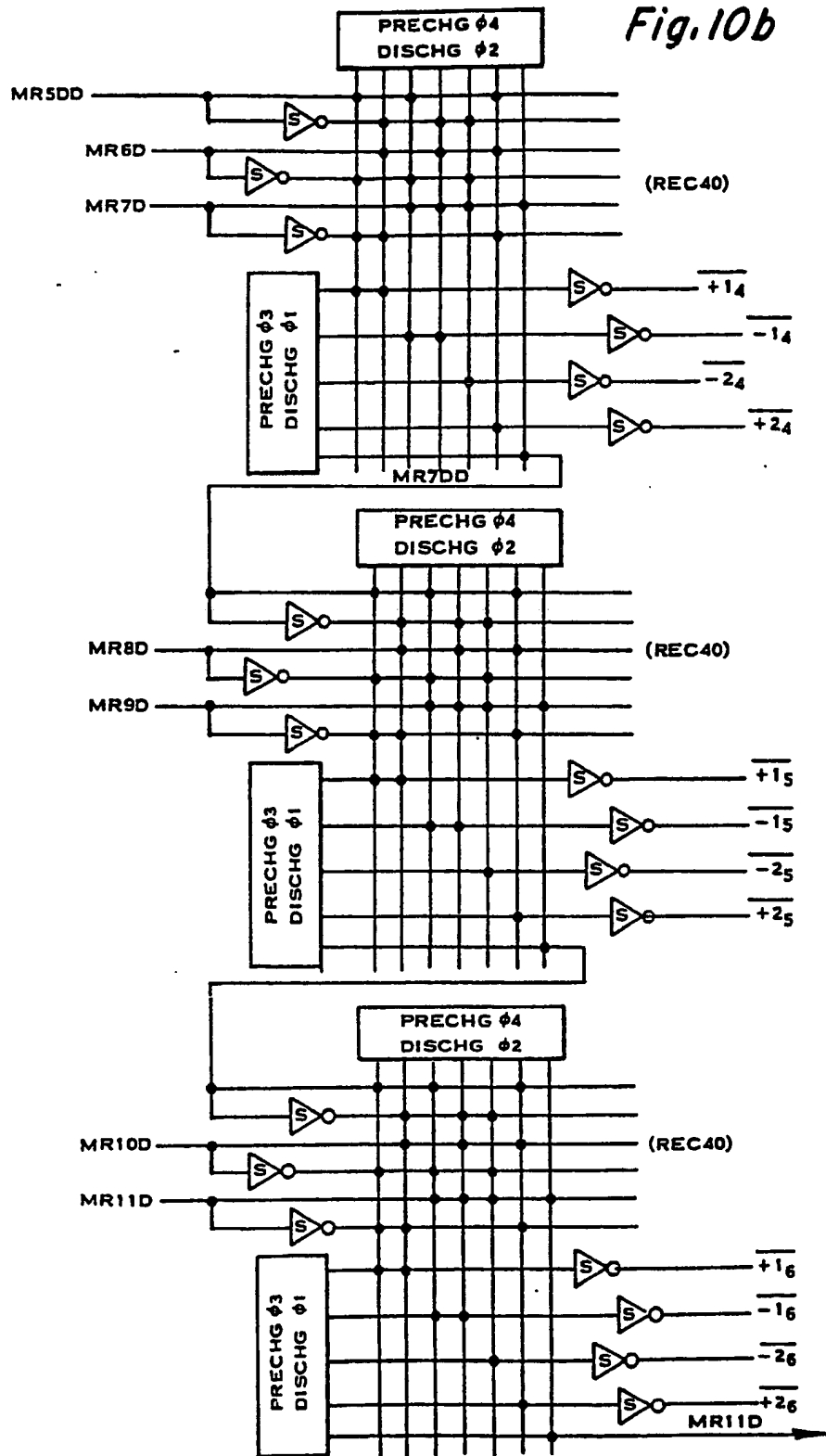
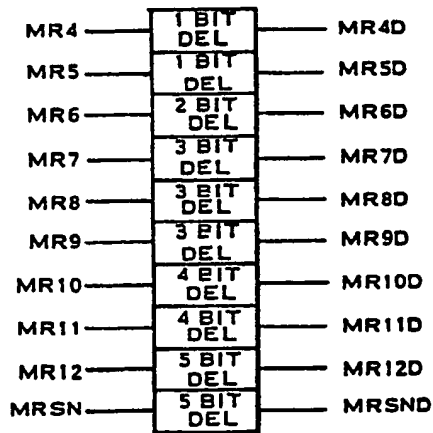
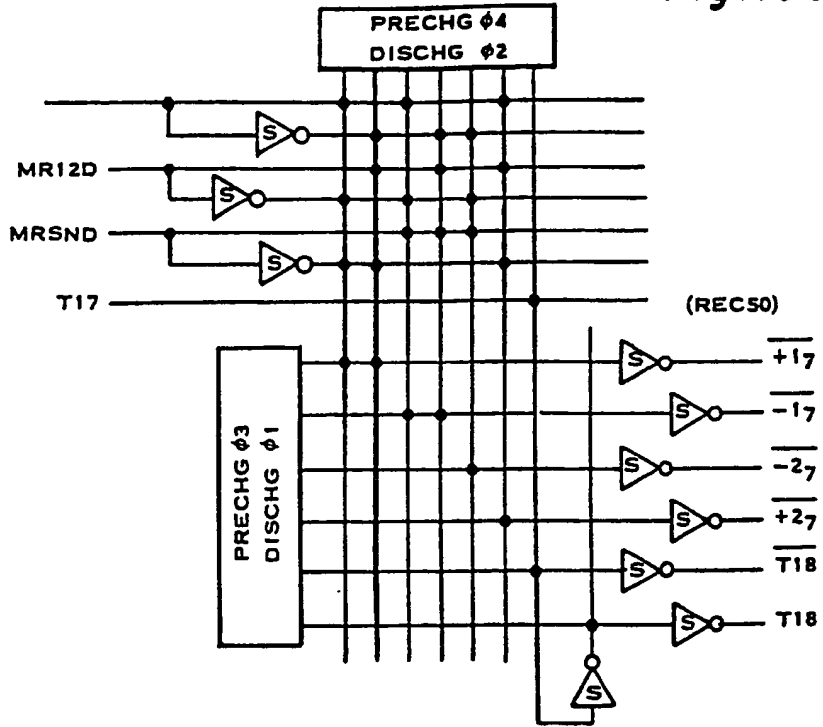


Fig. 10c



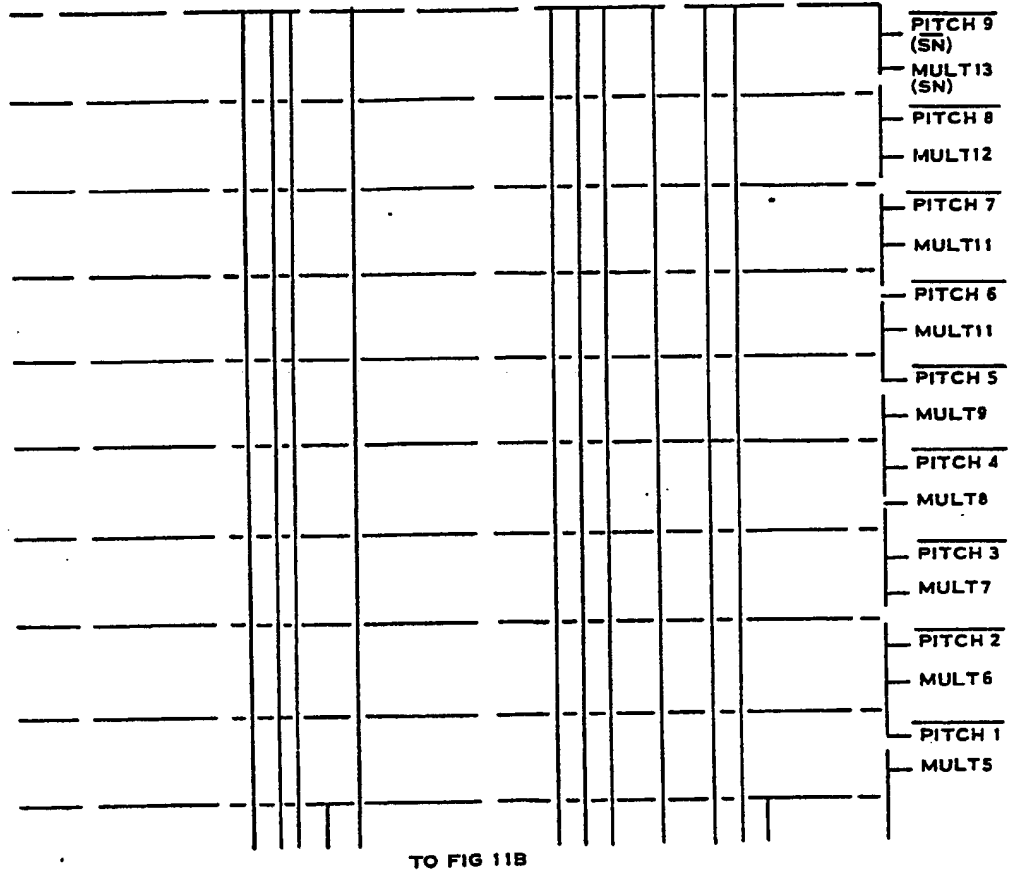


Fig. 11a

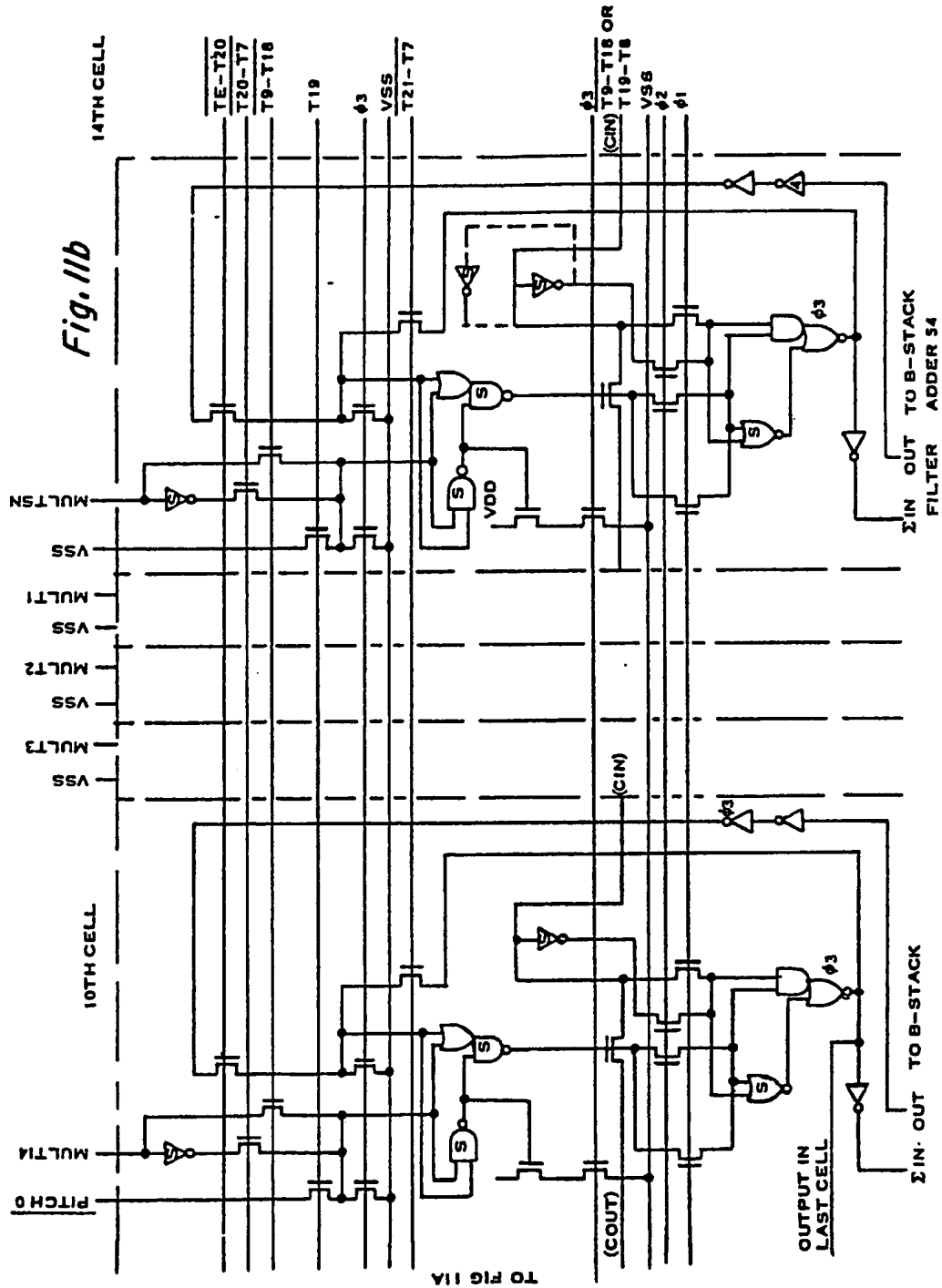


Fig. 12a

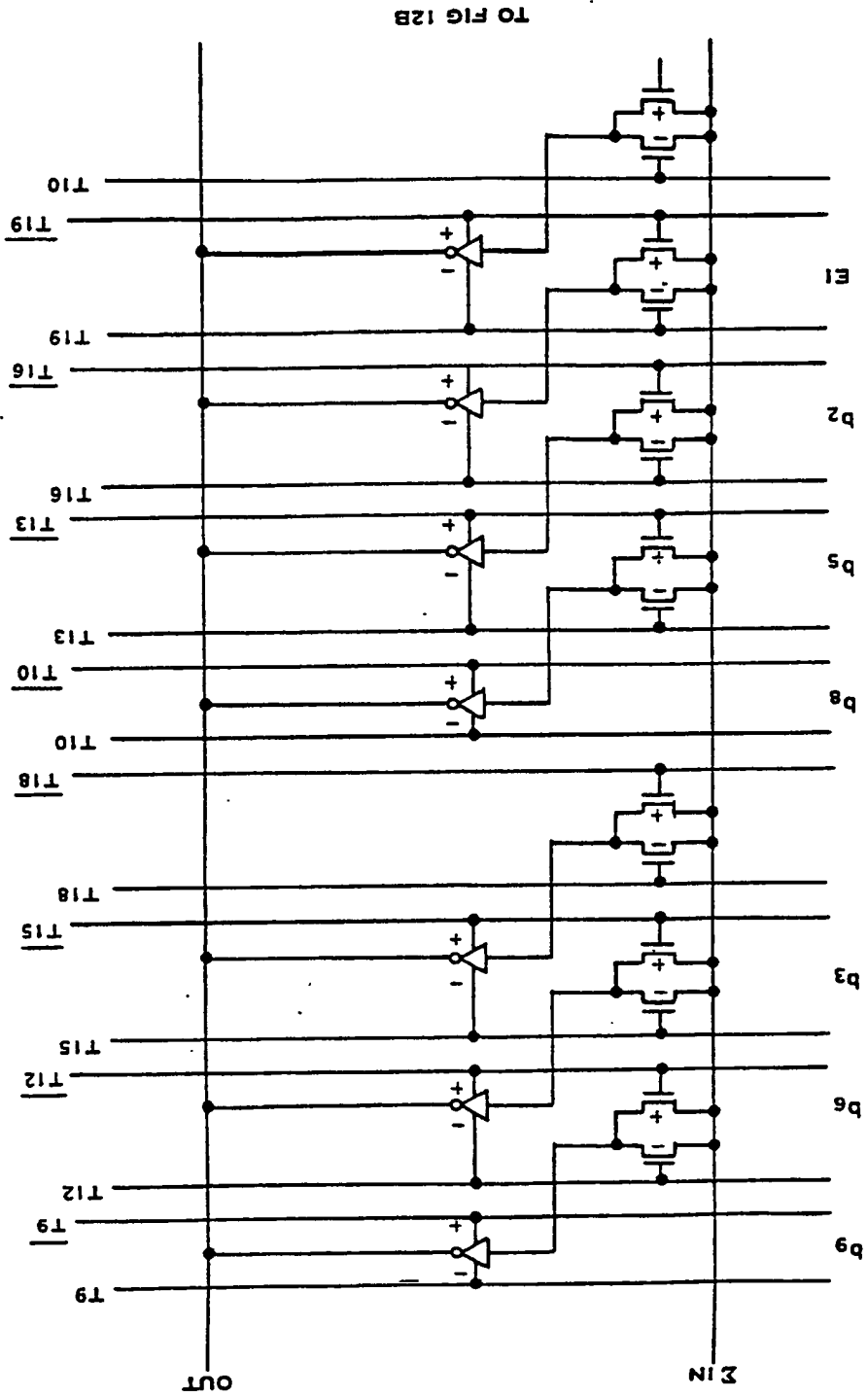
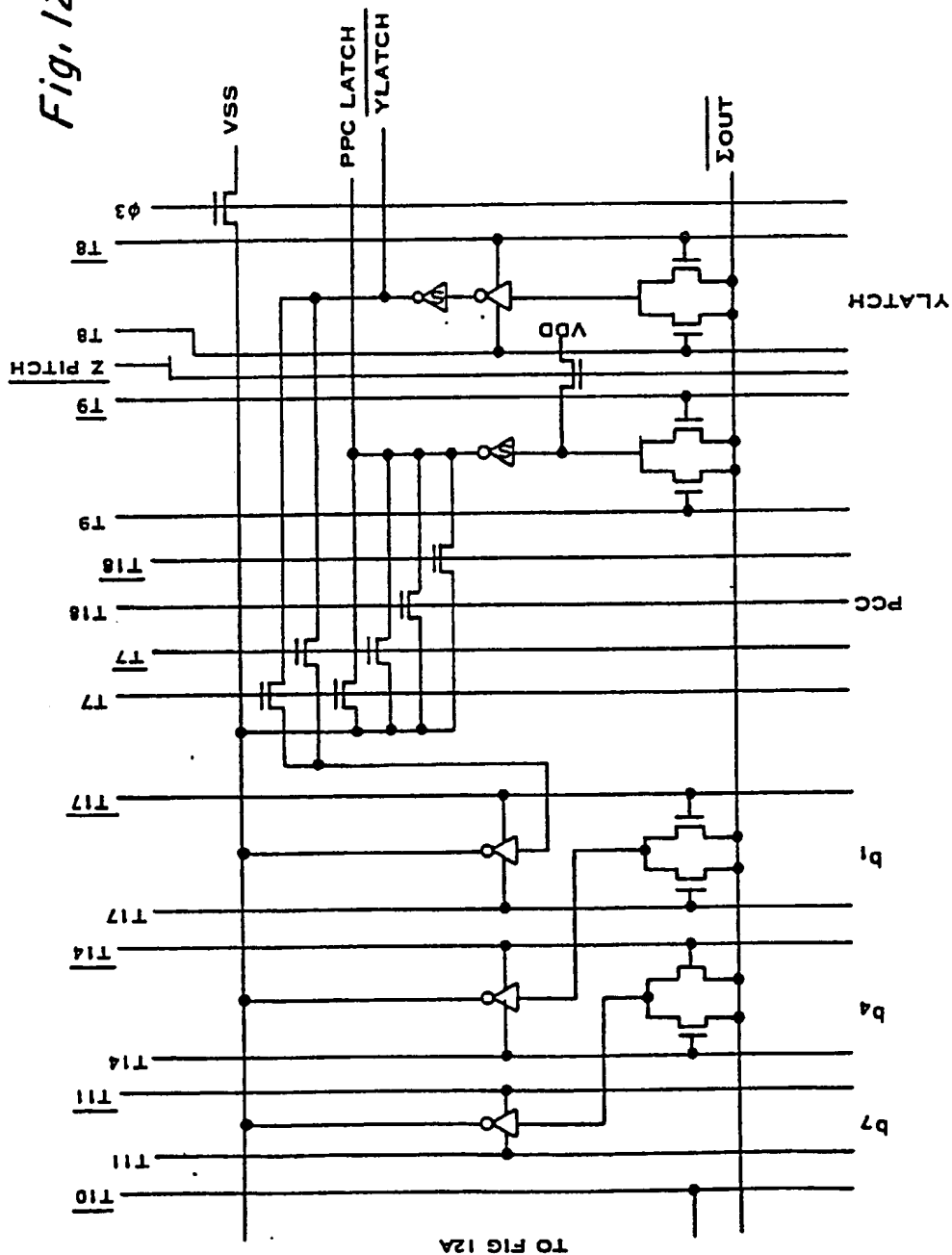


Fig. 12b



TO FIG 12A

Fig. 13a

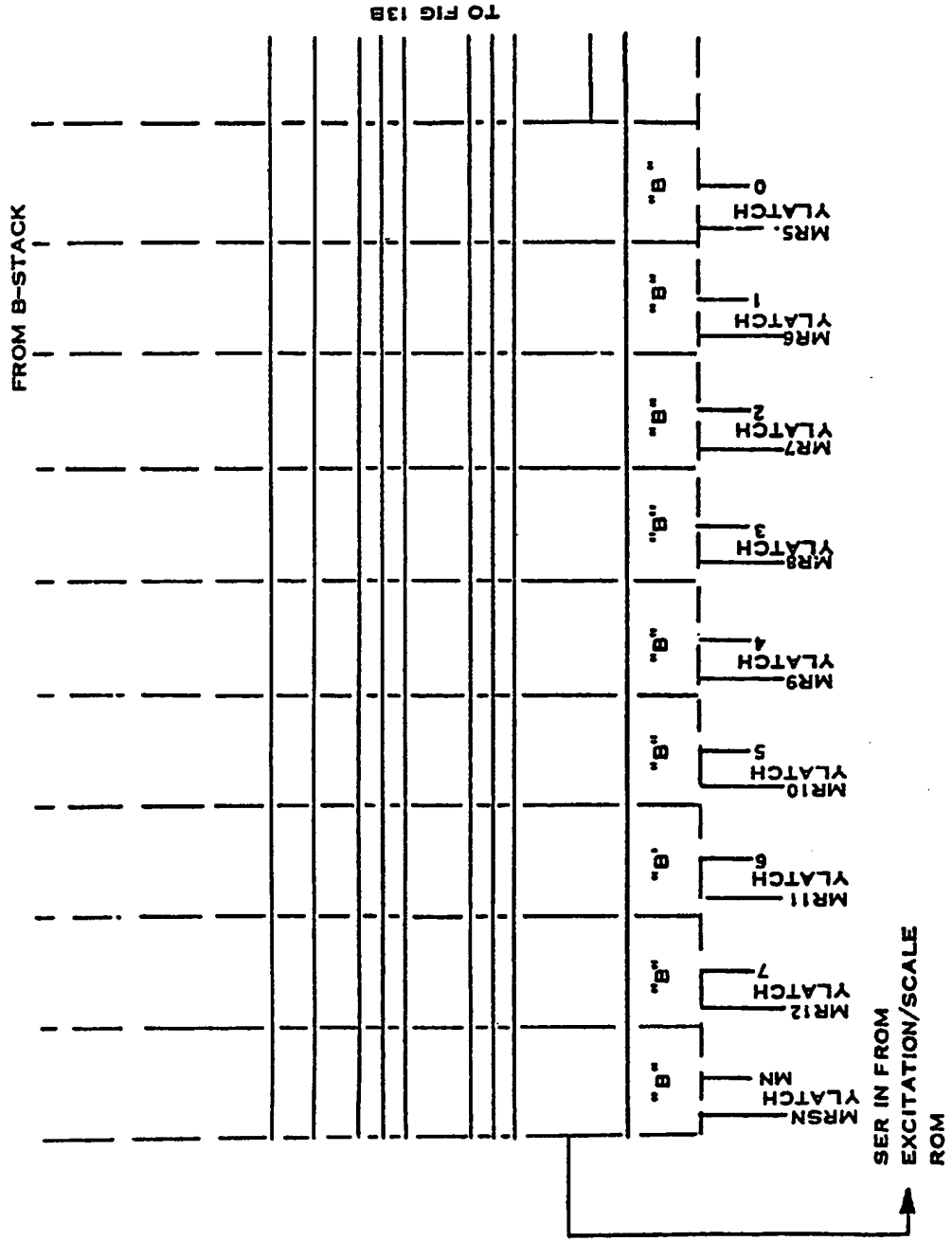
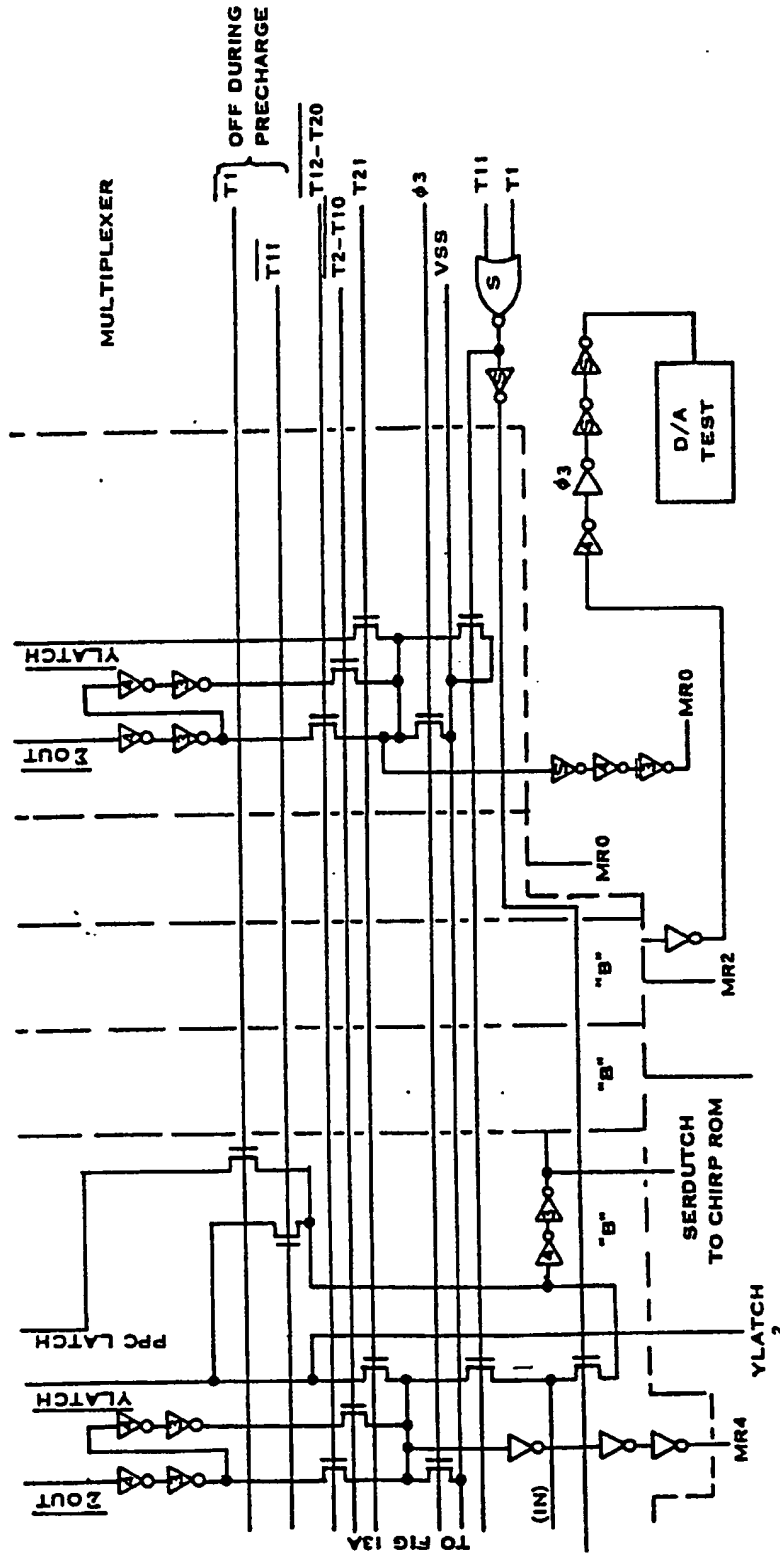
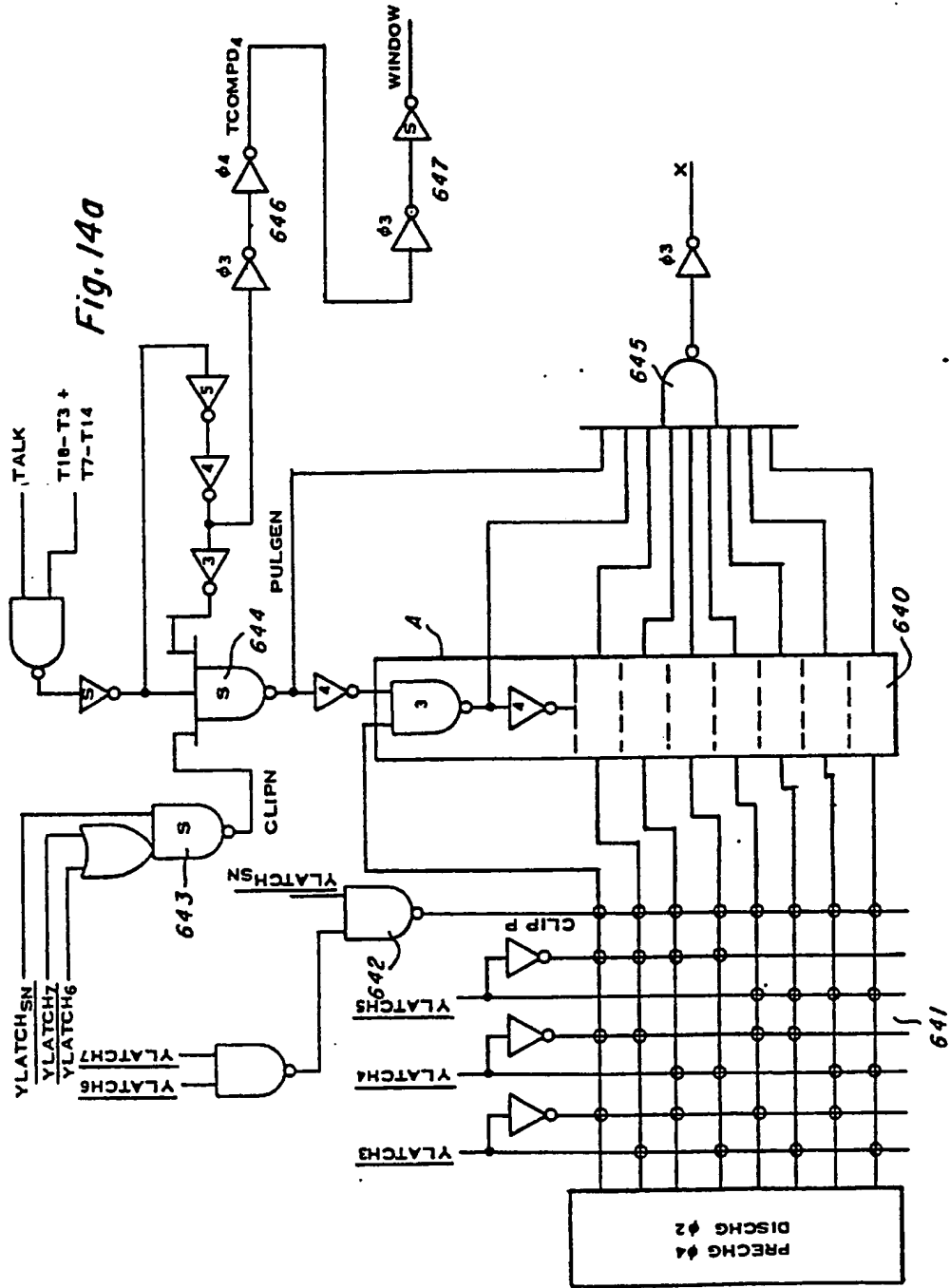


Fig. 13b



PC/LATCH/
EXCITATION/SCALE REGISTER 66



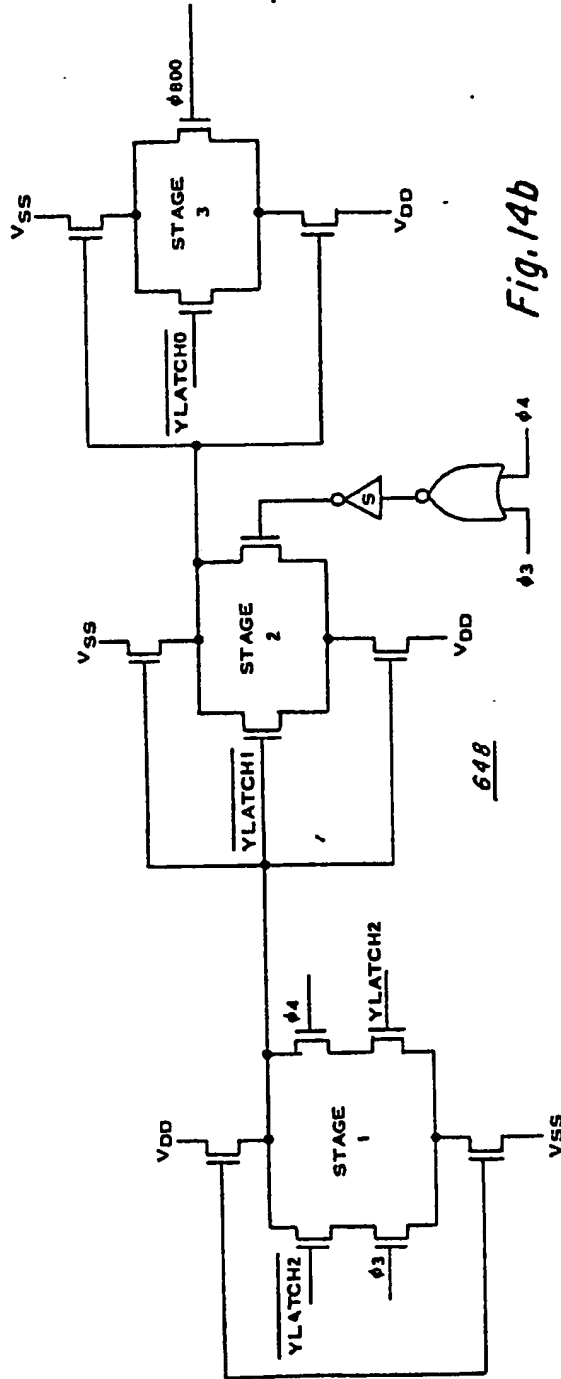
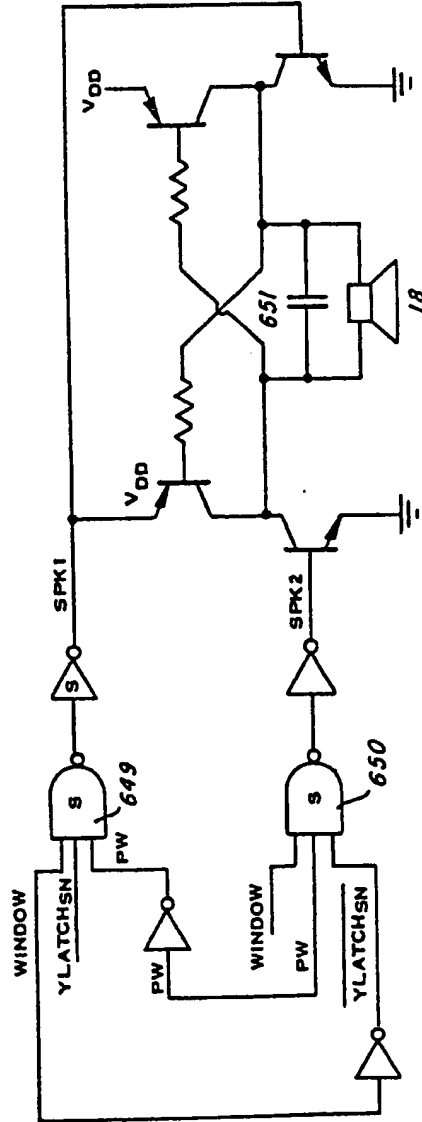


Fig. 14b





12

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Description**BACKGROUND OF THE INVENTION**

5 (1) Field of the Invention

The present invention relates to a voice coding/decoding system having a transmitting part for transmitting a coded signal of an input voice signal and a receiving part for receiving and decoding the coded signal transmitted from the transmission part, and more particularly to a voice coding/decoding system without utilizing
10 a buffer memory.

In general, the transmission part has a coder for adaptive differential PCM (ADPCM), adaptive transform coding (ATC) and so forth, and an entropy coder. The coder provides an encoded word which is obtained by compacting the amount of input information. The coded word is then changed to an entropy-coded word by the entropy coder. The entropy-coded word is transmitted from the transmission part to the receiving part. The
15 receiving part conversely decodes the entropy-coded word to reproduce the voice signal.

Accompanied by the developments of digital lines in recent years, a system for compacting the amount of information to obtain coded signals at a high efficiency has been desired in order to effectively utilize the lines.

Also, to store voice information in a voice storage or voice response system, it is important to decrease the capacity of the storing memory. The system for compacting the amount of information and for coding at a
20 high efficiency will satisfy the above requirements.

(2) Description of the Related Art

As a voice signal coding apparatus, a coding transmission apparatus is conventionally known in which a
25 coder and an entropy coder are combined to code voice signals with high efficiency. The coder carries out compacting and coding of voice signals by means of adaptive differential PCM (ADPCM), adaptive transform coding (ATC) and so forth. The entropy coder carries out removing of statistical redundancy in quantized values.

In the coding transmission apparatus for carrying out coding of voice signals at high efficiency, since the
30 voice signals have nonuniform probability of symbols, the statistical characteristics of the output of the coder are changed so that the code lengths, i.e., bit rates, of the entropy-coded results are not constant, and the bit rate may happen to be larger than the allowable transmission bit rate so that the transmission becomes impossible.

Conventionally, to solve the above problem, the entropy encoded result is stored in a buffer memory and
35 is transmitted from the buffer memory through the transmission line. To this end, a buffer control system has been employed in which the entropy-coded results are controlled by changing the quantization characteristics of a quantizer in the coder. This conventional system is described in "On the Information Rate Control in Entropy-coded Speech Transmission Systems", written by M. Copperi, CSELT Rapportitecnici Vol. X-No. 6-DECEMBER, 1982 PP 435-449.

In the above described conventional art, a buffer memory is used to control the entropy-coded results. In
40 practice, however, an overflow or an underflow of the buffer memory occurs depending on the characteristics of the coder and the entropy coder.

Further, in the control method by means of the buffer memory, the control is carried out in such a way that the input/output characteristics of the quantizer in the coder is changed so that the statistical characteristics of the quantized output codewords are controlled so as to make the entropies small. Namely, the entropies concentrate to certain values. Therefore, the characteristics of the quantizer itself do not become optimum, and the characteristic of the coder is not always good.
45

Further, when there is a transmission error, the error is transmitted in the entropy decoder. Therefore, once a transmission error is generated, the error is superimposed on the next decoded result so that there is a problem in that the one transmission error influences several samples.
50

SUMMARY OF THE INVENTION

In view of the above problems in the conventional art, an object of the present invention is to provide a
55 voice coding/decoding system capable of coding and transmitting input voice signal in an optimum state without passing through a buffer memory and without having a negative influence on the coder.

To attain the above object, there is provided, according to the present invention, a voice coding/decoding system having a transmitting part for transmitting a coded signal of an input voice signal at a bit rate lower

than a predetermined transmission bit rate according to the attached independent claims and a receiving part for receiving and decoding the coded signal transmitted from the transmission part. The transmitting part comprises a plurality of coders for coding the input voice signals. The coders have different numbers of quantizer output levels, different quantization characteristics, or different numbers of quantizer output levels and different quantization characteristics. The transmitting part also comprises a plurality of groups of entropy coders. The inputs of the entropy coders in each of the groups are connected to the output of one of the plurality of coders. The entropy coders in each of the groups have the same number of quantizer output levels as the number of quantizer output levels in one of the plurality of coders connected to the group, and different probability distributions. The transmitting part further comprises an evaluation part, operatively connected to the local decoder outputs of the plurality of coders and the outputs of the plurality of entropy coders, for evaluating the characteristics of the local decoder outputs of the coders and the entropy coders to extract the entropy coders having output bit rates lower than the transmission bit rate and to extract, from the coders connected to the extracted entropy coders, a coder having the best output characteristic, to output a selecting signal indicating the combination of the selected coder and an entropy coder among the extracted entropy coders. The transmitting part still further comprises a selecting part, operatively connected to the outputs of the plurality of entropy coders and to the output of the evaluation part, for selecting, in response to the selecting signal, the codeword passed through the combination of the coder and the entropy coder for transmission.

The receiving part comprises a plurality of decoders for decoding the received codeword, having different numbers of quantizer output levels from each other, different quantization characteristics, or different numbers of quantizer output levels and different quantization characteristics; and a plurality of groups of entropy decoders, the outputs of the entropy decoders in each of the groups being connected to the input of one of the plurality of decoders, the entropy decoders in each of the groups having the same number of quantizer output levels as the number of quantizer output levels in the one of the plurality of coders connected to the group and having different probability distributions; whereby, in accordance with the selecting signal indicating the combination of the selected coder and the selected entropy coder, the transmitted codeword is decoded by the combination of an entropy decoder and a decoder corresponding to the combination of the selected coder and the selected entropy coder.

BRIEF DESCRIPTION OF THE DRAWINGS

The above object and features of the present invention will be more apparent from the following description of the preferred embodiment with reference to the drawings, wherein:

Figure 1 is a diagram showing a conventional voice coding and transmission system;

Fig. 2 is a diagram showing the principal construction of a voice coding/decoding system according to an embodiment of the present invention;

Fig. 3 is a diagram showing in detail the transmitting part of the voice coding/decoding system shown in Fig. 2;

Fig. 4 is a diagram showing in detail the receiving part of the coding/decoding system shown in Fig. 2;

Fig. 5 is a flowchart for explaining the operation of the system shown in Fig. 2; and

Fig. 6 is a diagram showing a transmitting part of a voice coding/decoding system according to another embodiment of the present invention; and

Fig. 7 is a diagram showing a receiving part of a voice coding/decoding system according to another embodiment of the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

For better understanding of the present invention, a conventional voice coding transmission system is first described with reference to Fig. 1. In Fig. 1, 71 represents an ADPCM coder, 72 represents an entropy coder, and 73 represents a buffer memory.

As described before, since the voice signals have nonuniform probability of symbols, the statistical characteristics of the output of the coder are changed so that the code lengths, i.e., bit rates, of the entropy-coded results are not constant, and the bit rate may be larger than the transmission bit rate so that the transmission becomes impossible. To solve this problem, the entropy-coded result is stored in the buffer memory 73 and is transmitted from the buffer memory 73 to the transmission line. To this end, a buffer control system has been employed in which the entropy-coded results are controlled by changing the quantization characteristics of a quantizer in the coder. This conventional system is described in "On the Information Rate Control in Entropy-coded Transmission System", written by M. Copperi, CSELT Rapportitechni Vol.X-No.6-DECEMBER, 1982 PP 435-449.

In the above described conventional art, a buffer memory 73 is used to control the entropy-coded results. In practice, however, an overflow or an underflow of the buffer memory 73 occurs depending on the characteristics of the coder and the entropy coder.

Further, in the control method using part of the buffer memory, the control is carried out in such a way that the input/output characteristics of the quantizer in the coder are changed so that the statistical characteristics of the quantized output codewords are controlled in such a way that the entropy becomes small, namely the entropy becomes a certain small value. Therefore, the characteristics of the quantizer itself do not become optimum, so that the characteristic of the coder is not always good.

Further, when there is a transmission error, the error is transmitted in the entropy decoder. Therefore, once a transmission error is generated, the error is superimposed on the next decoded result so that there is a problem in that the one transmission error influences several samples.

The above-described problems in the conventional art are solved by the present invention.

Embodiments of the present invention will be described in the following.

Fig. 2 is a diagram showing the principal construction of a voice coding/decoding system according to an embodiment of the present invention. In the figure, the system consists of a transmission part 1 and a receiving part 2. The transmission part 1 includes a plurality of coders A1 to An, a plurality of groups GA1 to GAn of entropy coders A11-A1m, ..., An1-Anm, evaluation part 3, and a selecting and multiplexing part 4. Each of the groups GA1 to GAn of the entropy coders corresponds to one of the coders A1 to An. The evaluation part 3 selects outputs of the entropy coders having bit rates below the transmission bit rate, evaluates the qualities of the coders corresponding to the selected entropy coders, selects an optimum combination of a coder and an entropy coder, and generates a selecting signal indicating the combination of the selected coder and the selected entropy coder. The selecting and multiplexing part 4 multiplexes the selected codeword and the selecting signal.

The plurality of coders A1 to An have different numbers of quantizer output levels (bit lengths). Alternatively, the plurality of coders A1 to An may have different quantization characteristics. As another alternative, the plurality of coders A1 to An may have different numbers of quantizer output levels and different quantization characteristics. Each of the coders corresponds to one of the groups GA1 to GAn. In each of the groups GA1 to GAn, a plurality of entropy coders have different probability distributions. The plurality of entropy coders are operated in parallel. The evaluation part 3 selects the outputs of the entropy coders having bit rates lower than the transmission bit rate from all of the outputs of the entropy coders A11 to Anm for each frame of input voice signals, evaluates the qualities of the local decoded signals from all of the coders corresponding to the entropy coders from which the selected outputs are generated, and selects a codeword having the optimum quality. The evaluation part 3 also generates a selecting signal indicating the combination of the coder and the entropy coder from which the codeword is selected. The selecting signal is applied to the selecting and multiplexing part 4. The selecting and multiplexing part 4 multiplexes the selected codeword and the selecting signal to transmit through the transmission line to the receiving part 2.

The receiving part 2 includes a demultiplexing part 5, a switching part 7, a plurality of groups GB1 to GBn of a plurality of entropy decoders B11-B1m, ..., Bn1-Bnm, and a plurality of decoders B1 to Bn each corresponding to one of the plurality of groups B11-B1m, ..., Bn1-Bnm. The demultiplexing part 5 demultiplexes the multiplexed signal received from the transmitting part 1 through the transmission line into the codeword and the selecting signal. The switching part 7 passes, in response to the demultiplexed selecting signal from the demultiplexing part 5, the demultiplexed codeword to the combination of the entropy decoder and the decoder corresponding to the combination of the coder and the entropy coder selected in the transmitting part 1. The thus selected entropy decoder carries out an entropy decoding in accordance with the probability distribution of the entropy decoder, and the selected decoder decodes, in accordance with the number of the quantizer output levels, the quantization characteristics, or the number of the quantizer output levels and the quantization characteristics, the output of the selected entropy decoder to reproduce the voice signal.

Since the voice signal has nonuniform probability of symbols, the statistical characteristics of the codewords output from a coder are different for respective frames. Therefore, the codeword lengths of the entropy coded results are different for respective frames depending on the number of the quantizer output levels, the quantization characteristics, or the number of the quantizer output levels and the quantization characteristics. In view of these facts, according to the present invention, a plurality of coders are provided and each of the coders is made to correspond to one of the groups of a plurality of entropy coders having different probability distributions. And the optimum combination of a coder and an entropy coder is selected to transmit a codeword.

In the transmitting part 1, an input voice signal is input in parallel to the coders A1 to An having different number of quantizer output levels, quantization characteristics, or number of quantizer output levels and quantization characteristics. Then coders A1 to An carry out the coding simultaneously to output codewords and local decoded signals having different numbers of quantizer output levels, different quantization characteristics,

tics, or different numbers of quantizer output levels and different quantization characteristics. The codewords have statistical nonuniformity so that there are redundancies due to the statistical nonuniformity. To remove the redundancies, the plurality of entropy decoders A11 to Anm respectively having the different probability distributions are employed to carry out entropy codings.

5 In the evaluation part 3, the codeword lengths of the entropy-coded results and the qualities of the local decoded signals are evaluated for each frame so that the codewords, having codeword lengths of the entropy coded results each being lower than the transmitting bit rate which is allowed on the transmission line, are selected and, among the selected codewords, a codeword having the highest quality of the characteristics of the local decoded signals is selected. Simultaneously, the selecting signal indicating the combination of the
10 coder and the entropy coder providing the highest quality of characteristics is generated and multiplexed with the selected codeword by the selecting and multiplexing part 4 to be transmitted to the receiving part 2.

In the receiving part 2, based on the selecting signal indicating the selected combination of the coder and the entropy coder, one of the plurality of entropy decoders B11 to Bnm and one of the plurality of decoders B1 to Bn are selected to carry out an entropy decoding and decoding, resulting in the reproduced voice signal.

15 As a result, a voice signal having a high quality characteristics can be reproduced from the receiving part 2 without employing a buffer memory for storing the entropy coded results in order to maintain the transmission bit rate to be constant as was employed in the conventional art. Also, in each coder, since the optimum quantizer can be selected, the characteristics of the output of the coder are not distorted due to deformation of the input-output characteristic of the quantizer. Still further, even when an error occurs in a frame on the transmission
20 line, the error does not influence another frame.

Fig. 3 is a diagram showing in detail the transmitting part in the system shown in Fig. 2 and Fig. 4 is a diagram showing in detail the receiving part in the system shown in Fig. 2.

In Figs. 3 and 4, it is assumed that the transmitting bit rate is 4 bits/sample. As the coders, ADPCM coders having the numbers of quantizer output levels of 4, 5 and 6 bits, respectively, are provided. As the entropy
25 coders, well known Huffman coders (hereinafter referred to simply as H coders) are provided.

In Fig. 3, the 5-bit ADPCM coder 22 corresponds to the 5-bit H coders 24 to 26 having different probability distributions A, B, and C. Similarly, the 6-bit ADPCM coder 23 corresponds to the 6-bit H coders 27 to 29 having different probability distributions A, B and C.

In each of the H coders, a codeword in the entropy coding should be previously prepared based on the
30 statistical characteristics of the quantizer output (symbols). Namely, a low probability codeword is made to correspond to a long codeword and a high probability codeword is made to correspond to a short codeword. The distribution of the predictive error signals in the differential coding such as ADPCM is close to the Laplace distribution (see "The Optimum Quantization of Laplace Distribution Signal" written by Hirohisa Yamaguchi, THE JOURNAL OF THE INSTITUTE OF ELECTRONICS, INFORMATION AND COMMUNICATION ENGINEERS,
35 vol. J67-B No. 2).

Accordingly, in this embodiment, the Laplace distribution is utilized and H coders each having a probability distribution of the entropy coding close to the Laplace distribution are assumed as the actual distribution to be used.

The output of the 4-bit coder 21 is directly connected to the input of the selecting and multiplexing part 4
40 without passing through an H coder. This is to ensure that the codeword can be surely obtained even when all of the bit rates of the codewords from the H coders 24 to 29 exceed the transmission bit rate of 4 bits/sample in the case when the assumed probability distribution of the codeword is greatly different from the actual distribution. Namely, it is always possible to transmit the output of the 4-bit ADPCM coder.

The ADPCM coders 21 to 23 respectively have decoders (not shown in the figure) therein. The local de-
45 coded signals e, f, and g decoded by the decoders are input to the evaluation part 3.

The evaluation part 3 has a signal to noise ratio (S/N) calculation part 31, a selection part 32, a codeword length comparing part 33, and a codeword length calculating part 34. The S/N calculation part 31 calculates, based on the input signal a and the local decoded signals e, f, and g, signal to noise ratios of the local decoded
50 signals from the ADPCM coders 21 to 23. The codeword length calculation part 34 determines the codeword lengths of the outputs of the H coders 24 to 29. The codeword length comparing part 33 compares the codeword lengths with the transmission bit rate to selectively output the codewords having bit rates lower than the transmission bit rates.

The selection part 32 selects, based on the S/N calculated results and the compared results from the co-
55 deward length comparing part 33, a combination of an ADPCM coder and an H coder the output signal of which has a bit rate lower than the transmission bit rate and has the optimum quality. The selection part 32 outputs a selecting signal indicating the combination.

These evaluation and selection are executed in every frame.

In this embodiment, since the number of the quantization bits is changed for each frame of input voice

signal, it is necessary to establish matching between the transmitting part and the receiving part. To this end, the internal coefficients of the number of quantization bits and the quantization characteristic of the ADPCM coder selected in the previous frame are copied into all other ADPCM coders at the beginning of the processing of the next frame to be processed. The frame length is selected in such a way that the characteristic of the ADPCM coder becomes the best when the number of the quantization bits and the quantization characteristic are changed.

In this embodiment, a path without passing through any entropy coder is also provided as mentioned before.

In Fig. 4, the demultiplexing part 5 demultiplexes the multiplexed signal received from the transmitting part through the transmission line into the codeword and the selecting signal. The switching part 7 passes, in response to the demultiplexed selecting signal from the demultiplexing part 5, the demultiplexed codeword to the combination of the entropy decoder and the decoder corresponding to the combination of the coder and the entropy coder selected in the transmitting part 1. The thus selected entropy decoder carries out an entropy decoding in accordance with the probability distribution of the entropy decoder, and the selected decoder decodes, in accordance with the number of the quantizer output levels, the quantization characteristics, or the number of the quantizer output levels and the quantization characteristics, the output of the selected entropy decoder to reproduce the voice signal.

Figure 5 is a flowchart for explaining the operation of the system shown in Figs. 3 and 4. In particular, the operation flow of the evaluation part 3 is shown. In the following, the operation of the system according to the above-described embodiment of the present invention is described in detail.

(1) One frame of voice signal *a* is input into the transmitting part 1 (step S1).

(2) The input voice signal *a* is coded by the plurality of ADPCM coders 21 to 23 having different numbers of quantizer output levels, to output the codewords *b* to *d*. The ADPCM coders 21 to 23 operate in parallel. In addition, the codewords *b* to *d* are decoded by decoders included in the ADPCM coders 21 to 23 to output the local decoded signals *e* to *g* (step S2).

(3) With respect to the codewords *b* to *d*, the codeword *b* is not entropy coded; the codeword *c* is entropy coded by the H coders 24 to 26 having the number of quantizer output levels of 5 bits and having different probability distributions from each other; and the codeword *d* is entropy coded by the H coders 27 to 29 having the number of quantizer output levels of 6 bits and having different probability distributions from each other; whereby the codewords *b* and *h* to *m* are generated. The codewords *b* and *h* to *m* are input into the selecting and multiplexing part 4 and into the evaluation part 3 (step S3).

(4) In the evaluation part 3, the codeword length calculating part 34 calculates the total codeword length of each frame of the codewords *b* and *h* to *m* (step S4).

(5) The codeword length comparing part 33 compares the calculated total codeword length from the codeword length calculating part 34 and the transmission bit rate (4 bits/sample in this embodiment) of the transmission line in this system to determine the lines corresponding to the codewords having bit rates lower than the transmission bit rate of, for example, 4 bit rates/sample (S5). Thus, the codeword length comparing part 33 determines the H decoders outputting the codewords having bit rates lower than the transmission bit rate.

(6) The S/N calculating part 32 calculates characteristics of the local decoded signals *e* to *g* from the ADPCM coders 21 to 23 by comparing these signals with the input signal *a* input into the ADPCM coders 21 to 23. The characteristics in this example are signal to noise ratios (S/N). The larger the value of the characteristic, the better the characteristic is.

The selection part 32 selects one ADPCM coder among the ADPCM coders corresponding to the H coders having the output bit rates lower than the bit rate of the transmission line as determined in step S5. The selected one ADPCM coder is the one which outputs the best characteristic of S/N. The selection part 32 outputs a selection signal *n* to the selecting and multiplexing part 4. The selection signal *n* is used to select the H coder having the bit rate lower than the transmission bit rate from the group of the H coders corresponding to the selected one ADPCM coder (step S6).

(7) The selecting and multiplexing part 4 selects one codeword from among the input codewords in response to the selection signal *n*, and multiplexes one selected codeword and the selection signal *n* (step S7).

(8) The multiplexed signal formed in the step S7 is transmitted (step S8).

(9) In the receiving part 2, the transmitted codeword and the selection signal are demultiplexed by the demultiplexer 5. The demultiplexed selection signal is input as a switching signal into the switching part 7 (step S9).

(10) The switching part 7 passes the demultiplexed codeword to the H decoder specified by the demultiplexed selection signal. The H decoder entropy decodes the codeword. The entropy decoded signal is fur-

ther decoded by the ADPCM decoder connected to the specified H decoder. Thus, the reproduced voice signal is obtained at the output of the H decoder (step S10).

In the above-described embodiment, S/N is employed as the evaluation value of the characteristic of the code. The present invention, however, is not restricted to this, but various alternatives are possible. For example, as other evaluations means, the sum of the absolute values of the error signals, the peak value of the absolute values of the error signals, cepstrum distance, squared summation of the error signals, or a combination thereof can be used. Also, instead of the H coders as the entropy coder, arithmetic code, runlength code Ziv-Jempel code and so forth may also be used for the entropy coder.

Figures 6 and 7 show another embodiment of the present invention. In the figures, Fig. 6 shows a transmitting part and Fig. 7 shows a receiving part. The same reference numerals throughout the figures 2 to 7 represent the same part.

In this embodiment, the transmission bit rate is also assumed to be about 4 bits/sample and ADPCM coders are also used as the coders.

The coders consist of 4-bit ADPCM coders 51 and 52 and 5-bit ADPCM coders 53 and 54. The ADPCM coders 51 and 53 have quantization characteristics of Laplace distributions. The ADPCM coders 52 and 54 have quantization characteristics of Gaussian distributions. The ADPCM coders 51 to 54 are designed in accordance with the Lloyd-Max method ("HIGH-EFFICIENCY CODING OF VOICE" written by Kazuo Nakada, published in 1986 by Morikita Shuppan, pp 22-23) by which the squared summation of the error signals is minimized.

In Fig. 6, 51 is a 4-bit ADPCM coder having a Laplace distribution, 52 is a 4-bit ADPCM coder having a Gaussian distribution, 53 is a 5-bit ADPCM coder having a Laplace distribution, and 54 is a 5-bit ADPCM coder having a Gaussian distribution.

As the entropy coders, Huffman coders (H coders) are also employed. In each of the H coders, a probability codeword in the entropy coding should be previously prepared based on the probability distribution of the quantized output (symbols). The probability codeword in the Huffman coders in this embodiment is formed based on the probability distributions of the quantized results of the quantizer characteristics in the ADPCM coders for which a Laplace distribution and a Gaussian distribution are assumed. 55 is a 5-bit H coder corresponding to the Laplace distribution and connected between the 5-bit ADPCM coder 53 and the selecting and multiplexing part 4, and 56 is a 5-bit H coder corresponding to the Gaussian distribution and connected between the 5-bit ADPCM coder 54 and the selecting and multiplexing part 4.

The ADPCM coders 51 to 54 have local decoders for providing local decoded signals which are input into the evaluation part 3. The codewords from the ADPCM coders 51 and 52, and the codewords from the H coders 55 and 56 are input to the selecting and multiplexing part 4 and the evaluation part 3.

The 4-bit ADPCM coders 51 and 52 are directly connected to the selecting and multiplexing part 4 without passing through an H coder.

The evaluation part 3 generates a selection signal based on the local decoded signals from the coders 51 to 54 and the codewords from the coders 51 and 52 and from the H coders 55 and 56, in the same way as in the previously described embodiment. The selection signal in this embodiment is 2 bits for selecting one of the four signals applied to the selecting and multiplexing part 4.

As is the same as in the first embodiment shown in Fig. 3 and 4, S/N is employed in the evaluation value of the characteristic of the code, however, various alternations are possible. For example, as other evaluation means, the sum of the absolute values of the error signals, the peak value of the absolute values of the error signals, cepstrum distance, squared summation of the error signals, or a combination thereof can be used. Also, instead of the H coders as the entropy coder, arithmetic code, runlength code Ziv-Jempel code and so forth may also be used for the entropy coder.

In this embodiment also, since the number of the quantization bits is changed for each frame of input voice signal, it is necessary to establish matching between the transmitting part and the receiving part. To this end, the internal coefficients of the number of quantization bits and the quantization characteristic of the ADPCM coder selected in the previous frame are copied into all other ADPCM coders at the beginning of the processing of the next frame to be processed. The frame length is selected in such a way that the characteristic of the ADPCM coder becomes the best when the number of the quantization bits and the quantization characteristic are changed.

In this embodiment, two paths without passing through any entropy coder are provided as mentioned before. This is to ensure that the codeword can be surely obtained even when all of the bit rates of the codewords from the H coders 55 and 56 exceed the transmission bit rate of 4 bits/sample in the case when the assumed probability distribution of the codeword is greatly different from the actual distribution. It is always possible to transmit the output of the 4-bit ADPCM coder. In other words, when the assumed probability distribution of the codeword is greatly different from the actual probability distribution, the average codeword length of the

entropy-coded words greatly exceeds the codeword length of a codeword before the entropy codings. In such a case as above, the entropy coding is not employed. This corresponds to the case when entropy coders of uniform characteristics are combined.

5 In Fig. 7, the demultiplexing part 5 demultiplexes the multiplexed signal received from the transmitting part through the transmission line into the code word and the selecting signal. The switching part 7 passes, in response to the demultiplexed selecting signal from the demultiplexing part 5, the demultiplexed codeword to the combination of the dentropy decoder and the decoder corresponding to the combination of the coder and the entropy coder selected in the transmission part.

10 The important difference between Fig. 4 and Fig. 7 is that, in Fig. 7, the H decoders are those of Laplace distribution and Gaussian distribution, and the ADPCM coders are those of Laplace distribution and the Gaussian distribution.

In Fig. 7, 61 is a 5-bit H decoder of Laplace distribution, 62 is a 5-bit H decoder of Gaussian distribution, 63 is a 4-bit ADPCM decoder of Laplace distribution, 64 is a 4-bit ADPCM decoder of Gaussian distribution, 65 is a 5-bit ADPCM decoder of Laplace distribution, and 66 is a 5-bit ADPCM decoder of Gaussian distribution.

15 The selected H decoder carries out an entropy decoding in accordance with its probability distribution. The selected ADPCM coder decodes its input signal in accordance with its quantization characteristic and its number of quantizer output levels to reproduce the input voice signal.

In the receiving part also, paths which do not pass through any entropy decoder are also provided, corresponding to the paths which do not pass through any entropy coder in the transmitting part. This corresponds to the case when the ADPCM decoders 63 and 64 are used.

20 As a still another embodiment of the present invention, adaptive transform coding (ATC) may be employed in the coders.

In the ATC, the input voice signal is passed through a window and then an orthogonal transform such as a discrete cosine transform (DCT), discrete Fourier transform and so forth is carried out. The transformed components are divided into subblocks, and the amount of information to be assigned to the respective subblocks is determined to quantize the input voice signal.

In this quantization process, a plurality of coders having a different number of quantizer output levels and different quantization characteristics are operated in parallel. The quantized results are entropy coded by a plurality of entropy coders having a different number of quantization output levels and a plurality of probability distributions. The quantizers correspond to the entropy coders, respectively. Then, a combination of entropy coders from which codewords having an amount of information below the amount of information allowable for each subblock are output and a coder from which a codeword having the shortest spectrum distance from the quantized signal is selected. The selected codeword and the selection signal indicating which of the combinations is selected are multiplexed to be transmitted.

35 The characteristics of the quantizers, the probability characteristics of the entropy coders and so forth may be designed in the same way as in the ADPCM coders.

According to the present invention, generally, there are four patterns of combinations of the quantizers in the coders and the entropy coders described as follows.

40

45

50

55

5 pattern 1: quantizer:
same level
different characteristics
entropy coder:
same level
different characteristics

10 pattern 2: quantizer:
same characteristics
different levels
15 entropy coder:
same characteristic
different levels

20 pattern 3: quantizer:
same characteristic
different levels
25 entropy coder:
different characteristics
different levels

30 pattern 4: quantizer
different characteristics
35 different levels
entropy coder:
different characteristics
40 different levels

45 When the number of bits of the selection signal is 2 bits, and when the allowable transmission bit rate is 4 bits/sample, the above four patterns can be practically described as follows.

50 pattern 1
combination 1:
quantizer:

55

5 5-bit nonlinear quantization optimized to
 a Gaussian distribution
 entropy coder:
 optimized to the output of the quantizer
 when a signal of the Gaussian distribu-
 10 tion is input to the 5-bit quantizer
 optimized to the Gaussian distribution

15 combination 2:
 quantizer:
 5-bit nonlinear quantization optimized to
 a Laplace distribution
 20 entropy coder:
 optimized to the output of the quantizer
 when a signal of the Laplace distribution
 25 is input to the 5-bit quantizer optimized
 to the Laplace distribution

30 combination 3:
 quantizer:
 5-bit nonlinear quantization optimized to
 a Gaussian distribution
 35 entropy coder:
 optimized to the output of the quantizer
 when a signal of the Laplace distribution
 40 is input to the 5-bit quantizer optimized
 to the Gaussian distribution

45 combination 4:
 quantizer:
 5-bit nonlinear quantization optimized to
 a Laplace distribution
 50 entropy coder:
 optimized to the output of the quantizer
 when a signal of the Gaussian distribu-
 55 tion is input to the 5-bit quantizer
 optimized to the Laplace distribution

pattern 2

5

combination 1:

quantizer:

7-bit linear quantization

10

entropy coder:

optimized to the output of the quantizer

when a signal of a Laplace distribution

is input to the 7-bit linear quantizer

15

.....

combination 2:

quantizer:

6-bit linear quantization

20

entropy coder:

optimized to the output of the quantizer

when a signal of a Laplace distribution

is input to the 6-bit linear quantizer

25

.....

combination 3:

30

quantizer:

5-bit linear quantization

entropy coder:

optimized to the output of the quantizer

when a signal of a Laplace distribution

is input to the 5-bit linear quantizer

35

.....

combination 4:

40

quantizer:

4-bit linear quantization

45

entropy coder:

optimized to the output of the quantizer

when a signal of a Laplace distribution

is input to the 5-bit linear quantizer

50

pattern 3

55

combination 1:

quantizer:

5-bit linear quantization

entropy coder:

optimized to the output of the quantizer
when a signal of a Gaussian distribution
is input to the 5-bit linear quantizer

.....

combination 2:

quantizer:

6-bit linear quantization

entropy coder:

optimized to the output of the quantizer
when a signal of a Laplace distribution
is input to the 6-bit linear quantizer

.....

combination 3:

quantizer:

6-bit linear quantization

entropy coder:

optimized to the output of the quantizer
when a signal of a Gamma distribution is
input to the 6-bit linear quantizer

.....

combination 4:

quantizer:

4-bit linear quantization

entropy coder:

without an entropy coder

pattern 4

combination 1:

quantizer:

5-bit nonlinear quantization optimized to
a Gaussian distribution

entropy coder:

optimized to the output of the quantizer
when a signal of a Gaussian distribution
is input to the 5-bit quantizer optimized

to a Gaussian distribution

.

5 combination 2:

quantizer:

4-bit nonlinear quantization optimized to
a Gaussian distribution

10

entropy coder:

without any entropy coder

.

15 combination 3:

quantizer:

5-bit nonlinear quantization optimized to
a Laplace distribution

20

entropy coder:

optimized to the output of the quantizer
when a signal of a Gaussian distribution
is input to the 5-bit quantizer optimized
to a Laplace distribution

25

.

30 combination 4:

quantizer:

4-bit nonlinear quantization optimized to
a Laplace distribution

35

entropy coder:

without an entropy coder

40

Note that, in the above example, the state of "without any entropy coder" is equivalent to the combination of an entropy coder which is optimized to the output of the quantizer when a signal of uniform distribution is input into the linear quantizer.

45 The pattern 1 corresponds to the first embodiment shown in Figs. 3 and 4, and the pattern 2 corresponds to the second embodiment shown in Figs. 7 and 8.

From the foregoing description it will be apparent that, according to the present invention, by providing, in a transmitting part, a plurality of coders having different numbers of quantizer output levels, different quantization characteristics, or different numbers of quantizer output levels and different quantization characteristics, and a plurality of entropy coders having different probability distributions, and by selecting a suitable combination of a coder and an entropy coder in a transmitting part and corresponding combination of a decoder and an entropy decoder in a receiving part, coding and decoding can be accomplished with the optimal decoded characteristic and with adaptively removing the redundancy of the codewords due to the statistical characteristics without utilizing a buffer memory. Further, even when a transmission error occurs, the error influences only the signals in the frame where the error has occurred so that resistance to transmission errors is improved. Accordingly, by the present invention, a highly reliable voice coding/decoding system can be realized.

55

Reference signs in the claims are intended for better understanding and shall not limit the scope.

Claims

1. A voice coding/decoding system having a transmitting part for transmitting a coded signal of an input voice signal at a bit rate lower than a predetermined transmission bit rate and a receiving part for receiving and decoding the coded signal transmitted from said transmission part, said transmitting part comprising:
- 5 a plurality of coders (A1-A_n) for coding said input voice signal, said coders having predetermined numbers of quantizer output levels and having a predetermined quantization characteristic;
- a plurality of groups of entropy coders (A11-A_{nm}), the inputs of said entropy coders in each of said groups being connected to the output of one of said plurality of coders, said entropy coders having pre-
- 10 determined numbers of quantizer output levels and predetermined probability distributions;
- evaluation means (3), operatively connected to the outputs of said plurality of coders and the outputs of said plurality of entropy coders, for evaluating the characteristics of the outputs of said coders and said entropy coders to extract the entropy coders having output bit rates lower than the transmission bit rate and to extract, from the coders connected to the extracted entropy coders, a coder having the
- 15 best output characteristic, to output a selecting signal indicating the combination of the selected coder and an entropy coder in the extracted entropy coders; and
- selecting means (4), operatively connected to the outputs of said plurality of entropy coders and to the output of said evaluation means, for selecting, in response to said selecting signal, the codeword passed through said combination of the coder and the entropy coder to be transmitted.
- 20
2. A voice coding/decoding system as claimed in claim 1, wherein said predetermined numbers of quantizer output levels of said plurality of coders are the same as each other, said predetermined quantization characteristics of said plurality of coders are different from each other, the numbers of said predetermined quantization output levels of said entropy coders in each of said groups are the same as each other, and the quantization characteristics in each of said groups of entropy coders are different from each other.
- 25
3. A voice coding/decoding system as claimed in claim 1, wherein said predetermined numbers of quantizer output levels of said plurality of coders are different from each other, said predetermined quantization characteristics of said plurality of coders are the same as each other, the numbers of said predetermined quantization output levels of said entropy coders in each of said groups are different from each other, and the quantization characteristics in each of said groups of entropy coders are the same as each other.
- 30
4. A voice coding/decoding system as claimed in claim 1, wherein said predetermined numbers of quantizer output levels of said plurality of coders are different from each other, said predetermined quantization characteristics of said plurality of coders are the same as each other, the numbers of said predetermined quantization output levels of said entropy coders in each of said groups are different from each other, and the quantization characteristics in each of said groups of entropy coders are different from each other.
- 35
5. A voice coding/decoding system as claimed in claim 1, wherein said predetermined numbers of quantizer output levels of said plurality of coders are different from each other, said predetermined quantization characteristics of said plurality of coders are different from each other, the numbers of said predetermined quantization output levels of said entropy coders in each of said groups are different from each other, and the quantization characteristics in each of said groups of entropy coders are different from each other.
- 40
6. A voice coding/decoding system having a transmitting part for transmitting a coded signal of an input voice signal at a bit rate lower than a predetermined transmission bit rate and a receiving part for receiving and decoding the coded signal transmitted from said transmission part, said transmitting part comprising:
- 45 a plurality of coders (53, 54) for coding said input voice signal, said coders having predetermined numbers of quantizer output levels and having a predetermined quantization characteristic;
- a plurality of entropy coders (55, 56), the inputs of said entropy coders being connected to the outputs of said plurality of coders respectively, said entropy coders having predetermined numbers of quantizer output levels and predetermined probability distributions;
- 50 evaluation means (3), operatively connected to the outputs of said plurality of coders and the outputs of said plurality of entropy coders, for evaluating the characteristics of the outputs of said coders and said entropy coders to extract the entropy coders having output bit rates lower than the transmission bit rate and to extract, from the coders connected to the extracted entropy coders, a coder having the
- 55 best output characteristic, to output a selecting signal indicating the combination of the selected coder

- and an entropy coder in the extracted entropy coders; and
 selecting means (4), operatively connected to the outputs of said plurality of entropy coders and to the output of said evaluation means, for selecting, in response to said selecting signal, the codeword passed through said combination of the coder and the entropy coder to be transmitted.
- 5
7. A voice coding/decoding system as claimed in claim 6, further comprising at least one coder directly connected to said selecting means without connecting through any entropy coder.
8. A voice coding/decoding system as claimed in claim 6, wherein said receiving part comprises:
- 10 demultiplexing means (5), operatively connected to the output of said transmitting part through a transmission line, for demultiplexing a received signal from said transmitting part into said codeword and said switching signal;
- switching means (7), operatively connected to said demultiplexing means, having a single input end for receiving said code word and a plurality of output ends, for passing said codeword from said demultiplexing means to one of said plurality of output ends in response to said selecting signal from said demultiplexing means;
- 15 a plurality of entropy decoders (61, 62), the inputs of said entropy decoders being connected to said plurality of output ends of said switching means, said entropy decoders having predetermined numbers of quantizer output levels and predetermined probability distributions corresponding to the corresponding entropy coders; and
- 20 a plurality of decoders (65, 66), the outputs of said entropy coders being connected to the inputs of said plurality of decoders respectively, for decoding the entropy decoded codeword from said entropy decoders, said decoders having predetermined numbers of quantizer output levels and having the predetermined quantization characteristics;
- 25 whereby, in accordance with said selecting signal indicating the best combination of the coder and the entropy coder, by the corresponding combination of one of said entropy decoders and one of said coders, the transmitted codeword is decoded.
9. A voice coding/decoding system as claimed in claim 6 or 8, wherein said predetermined numbers of quantizer output levels of said plurality of coders are the same as each other, said predetermined quantization characteristics of said plurality of coders are different from each other, the numbers of said predetermined quantization output levels of said entropy coders are the same as each other, and the quantization characteristics of said entropy coders are different from each other.
- 30
10. A voice coding/decoding system as claimed in claim 9, wherein said predetermined numbers of quantizer output levels of said plurality of decoders are the same as each other, said predetermined quantization characteristics of said plurality of decoders are different from each other, the numbers of said predetermined quantization output levels of said entropy decoders are the same as each other, and the quantization characteristics of said entropy decoders are different from each other.
- 35
- 40 11. A voice coding/decoding system as claimed in claim 8, further comprising at least one decoder directly connected to said switching means without connecting through any entropy decoder.
12. A voice coding/decoding system as claimed in claim 1, wherein at least one of said coders is directly connected to said selecting means without connecting through said entropy coders.
- 45
13. A voice coding/decoding system as claimed in claim 1 or 6, wherein said selecting means (4) comprises multiplexing means for multiplexing said codeword passed through said combination with said selecting signal.
- 50
14. A voice coding/decoding system as claimed in claim 1 or 6, wherein said plurality of decoders are ADPCM coders.
15. A voice coding/decoding system as claimed in claim 1 or 6, wherein each of said plurality of coders includes a quantizer.
- 55
16. A voice coding/decoding system as claimed in claim 1 or 6, wherein each of said plurality of coders comprises a local decoder for generating a local decoded signal by locally decoding the codeword output from the coder, said local decoded signal being supplied to said evaluation means for extracting a coder having

said best characteristic.

17. A voice coding/decoding system as claimed in claim 6 or 16, wherein the characteristics of said coders are signal to noise ratios in said local decoded signal.
- 5 18. A voice coding/decoding system as claimed in claim 16, wherein the characteristics of said coders are the summation of the absolute values of the error signals in each local decoded signal.
- 10 19. A voice coding/decoding system as claimed in claim 16, wherein the characteristics of said coders are the peak value of the absolute values of the error signals in said local decoded signal.
- 20 20. A voice coding/decoding system as claimed in claim 16, wherein the characteristics of said coders are the cepstrum distances in said local decoded signal.
- 15 21. A voice coding/decoding system as claimed in claim 1 or 6, wherein said entropy coders are Huffman coders.
22. A voice coding/decoding system as claimed in claim 1 or 6, wherein said entropy coders are arithmetic coders.
- 20 23. A voice coding/decoding system as claimed in claim 1 or 6, wherein said entropy coders are runlength coders.
24. A voice coding/decoding system as claimed in claim 1 or 6, wherein said entropy coders are Ziv-lempel coders.
- 25 25. A voice coding/decoding system as claimed in claim 1, wherein said receiving part comprises:
 demultiplexing means (5), operatively connected to the output of said transmitting part through a transmission line, for demultiplexing a received signal from said transmitting part into said codeword and said switching signal;
 30 switching means (7), operatively connected to said demultiplexing means, having a single input end for receiving said codeword from said demultiplexing means and a plurality of output ends, for passing said codeword to one of said plurality of output ends in response to said selecting signal from said demultiplexing means;
 a plurality of groups of entropy decoders (B11-Bnm), the inputs of said entropy decoders in each of said groups being connected to said plurality of output ends of said switching means, said entropy decoders in each of said groups having predetermined numbers of quantizer output levels and predetermined probability distributions corresponding to the corresponding group of entropy coders; and
 35 a plurality of decoders (B1-Bn), the outputs of said entropy decoders in each of said groups being connected to the input of one of said plurality of decoders, for decoding the entropy coded codeword from said entropy decoders, said decoders having predetermined numbers of quantizer output levels and having the predetermined quantization characteristics;
 40 whereby, in accordance with said selecting signal indicating the best combination of the coder and the entropy coder, by the corresponding combination of one of said entropy decoders and one of said coders, the transmitted codeword is decoded.
- 45 26. A voice coding/decoding system as claimed in claim 25, wherein said predetermined numbers of quantizer output levels of said plurality of coders are the same as each other, said predetermined quantization characteristics of said plurality of coders are different from each other, the numbers of said predetermined quantization output levels of said entropy coders in each of said groups are the same as each other, and the quantization characteristics in each of said groups of entropy coders are different from each other.
- 50 27. A voice coding/decoding system as claimed in claim 26, wherein said predetermined numbers of quantizer output levels of said plurality of decoders are the same as each other, said predetermined quantization characteristics of said plurality of decoders are different from each other, the numbers of said predetermined quantization output levels of said entropy decoders in each of said groups are the same as each other, and the quantization characteristics in each of said groups of entropy decoders are different from
 55 each other.
28. A voice coding/decoding system as claimed in claim 25, wherein said predetermined numbers of quantizer

- output levels of said plurality of coders are different from each other, said predetermined quantization characteristics of said plurality of coders are the same as each other, the numbers of said predetermined quantization output levels of said entropy coders in each of said groups are different from each other, and the quantization characteristics in each of said groups of entropy coders are the same as each other.
- 5
29. A voice coding/decoding system as claimed in claim 28, wherein said predetermined numbers of quantizer output levels of said plurality of decoders are different from each other, said predetermined quantization characteristics of said plurality of decoders are the same as each other, the numbers of said predetermined quantization output levels of said entropy decoders in each of said groups are different from each other, and the quantization characteristics in each of said groups of entropy decoders are the same as each other.
- 10
30. A voice coding/decoding system as claimed in claim 25, wherein said predetermined numbers of quantizer output levels of said plurality of coders are different from each other, said predetermined quantization characteristics of said plurality of coders are the same as each other, the numbers of said predetermined quantization output levels of said entropy coders in each of said groups are different from each other, and the quantization characteristics in each of said groups of entropy coders are different from each other.
- 15
31. A voice coding/decoding system as claimed in claim 30, wherein said predetermined numbers of quantizer output levels of said plurality of decoders are different from each other, said predetermined quantization characteristics of said plurality of decoders are the same as each other, the numbers of said predetermined quantization output levels of said entropy decoders in each of said groups are different from each other, and the quantization characteristics in each of said groups of entropy decoders are different from each other.
- 20
32. A voice coding/decoding system as claimed in claim 25, wherein said predetermined numbers of quantizer output levels of said plurality of coders are different from each other, said predetermined quantization characteristics of said plurality of coders are different from each other, the numbers of said predetermined quantization output levels of said entropy coders in each of said groups are different from each other, and the quantization characteristics in each of said groups of entropy coders are different from each other.
- 25
33. A voice coding/decoding system as claimed in claim 32, wherein said predetermined numbers of quantizer output levels of said plurality of decoders are different from each other, said predetermined quantization characteristics of said plurality of decoders are different from each other, the numbers of said predetermined quantization output levels of said entropy decoders in each of said groups are different from each other, and the quantization characteristics in each of said groups of entropy decoders are different from each other.
- 30
34. A voice coding/decoding system as claimed in claim 25, wherein at least one of said decoders is directly connected to said switching means without connecting through said entropy decoders.
- 35
35. A voice coding/decoding system as claimed in claim 25, wherein each of said plurality of decoders includes a quantizer.
- 40
36. A voice coding/decoding system as claimed in claim 8 or 25, wherein said plurality of decoders are ADPCM decoders.
- 45
37. A voice coding/decoding system as claimed in claim 8 or 25, wherein said entropy coders are Huffman decoders.
- 50
38. A voice coding/decoding system as claimed in claim 8 or 25, wherein said entropy decoders are arithmetic decoders.
39. A voice coding/decoding system as claimed in claim 8 or 25, wherein said entropy decoders are runlength decoders.
- 55
40. A voice coding/decoding system as claimed in claim 8 or 25, wherein said entropy decoders are Ziv-lempel decoders.

Patentansprüche

1. Sprachcodier/Decodiersystem mit einem Übertragungsteil zum Übertragen eines codierten Signals eines eingegebenen Sprachsignals mit einer niedrigeren Bitrate als eine vorbestimmte Übertragungsbitrate und einem Empfangsteil zum Empfangen und Decodieren des codierten, von dem Übertragungsteil übertragenen Signals, wobei der Übertragungsteil umfaßt:
 5 eine Vielzahl von Codierern (A1-An) zum Codieren des eingegebenen Sprachsignals, wobei die Codierer vorbestimmte Anzahlen von Quantisiererausgangsniveaus und eine vorbestimmte Quantisierungseigenschaft aufweisen;
 10 eine Vielzahl von Gruppen von Entropiecodierern (A11-Anm), wobei die Eingänge der Entropiecodierer in jeder der Gruppen mit dem Ausgang von einem der Vielzahl von Codierern verbunden sind, die Entropiecodierer vorbestimmte Anzahlen von Quantisiererausgangsniveaus und vorbestimmte Wahrscheinlichkeitsverteilungen aufweisen;
 15 Auswerteeinrichtungen (3), die betriebsmäßig mit den Ausgängen der Vielzahl von Codierern und den Ausgängen der Vielzahl von Entropiecodierern verbunden sind, um die Eigenschaften der Ausgaben der Codierer und der Entropiecodierer auszuwerten, um die Entropiecodierer mit niedrigeren Ausgangsbitraten als die Übertragungsbitrate zu extrahieren, und um von den mit den extrahierten Entropiecodierern verbundenen Codierern einen Codierer mit der besten Ausgabeeigenschaft zu extrahieren, um ein Auswahlsignal auszugeben, welches die Kombination des ausgewählten Codierers und eines Entropiecodierers in den extrahierten Entropiecodierern anzeigt; und
 20 Auswahlrichtungen (4), welche betriebsmäßig mit den Ausgängen der Vielzahl von Entropiecodierern und mit dem Ausgang der Auswerteeinrichtung verbunden sind, um auf das Auswahlsignal hin das durch die Kombination des Codierers und des Entropiecodierers gelaufene, zu übertragene Codewort auszuwählen.
- 25 2. Sprachcodier/Decodiersystem nach Anspruch 1, dadurch gekennzeichnet, daß die vorbestimmten Anzahlen von Quantisiererausgangsniveaus der Vielzahl von Codierern einander gleich sind, die vorbestimmten Quantisierungseigenschaften der Vielzahl von Codierern voneinander verschieden sind, die Anzahlen der vorbestimmten Quantisierungsausgangsniveaus der Entropiecodierer in jeder der Gruppen einander gleich sind, und die Quantisierungseigenschaften in jeder der Gruppen von Entropiecodierern voneinander verschieden sind.
- 30 3. Sprachcodier/Decodiersystem nach Anspruch 1, dadurch gekennzeichnet, daß die vorbestimmten Anzahlen von Quantisiererausgangsniveaus der Vielzahl von Codierern voneinander verschieden sind, die vorbestimmten Quantisierungseigenschaften der Vielzahl von Codierern einander gleich sind, die Anzahlen der vorbestimmten Quantisierungsausgangsniveaus der Entropiecodierer in jeder der Gruppen voneinander verschieden sind, und die Quantisierungseigenschaften in jeder der Gruppen von Entropiecodierern einander gleich sind.
- 35 4. Sprachcodier/Decodiersystem nach Anspruch 1, dadurch gekennzeichnet, daß die vorbestimmten Anzahlen von Quantisiererausgangsniveaus der Vielzahl von Codierern voneinander verschieden sind, die vorbestimmten Quantisierungseigenschaften der Vielzahl von Codierern einander gleich sind, die Anzahlen der vorbestimmten Quantisierungsausgangsniveaus der Entropiecodierer in jeder der Gruppen voneinander verschieden sind, und die Quantisierungseigenschaften in jeder der Gruppen von Entropiecodierern voneinander verschieden sind.
- 40 45 5. Sprachcodier/Decodiersystem nach Anspruch 1, dadurch gekennzeichnet, daß die vorbestimmten Anzahlen von Quantisiererausgangsniveaus der Vielzahl von Codierern voneinander verschieden sind, die vorbestimmten Quantisierungseigenschaften der Vielzahl von Codierern voneinander verschieden sind, die Anzahlen der vorbestimmten Quantisierungsausgangsniveaus der Entropiecodierer in jeder der Gruppen voneinander verschieden sind, und die Quantisierungseigenschaften in jeder der Gruppen von Entropiecodierern voneinander verschieden sind.
- 50 55 6. Sprachcodier/Decodiersystem mit einem Übertragungsteil zum Übertragen eines codierten Signals eines eingegebenen Sprachsignals mit einer niedrigeren Bitrate als eine vorbestimmte Übertragungsbitrate und einem Empfangsteil zum Empfangen und Decodieren des codierten, von dem Übertragungsteil übertragenen Signals, wobei der Übertragungsteil umfaßt:
 eine Vielzahl von Codierern (53, 54) zum Codieren des eingegebenen Sprachsignals, wobei die Codierer

- vorbestimmte Anzahlen von Quantisiererausgangsniveaus und eine vorbestimmte Quantisierungseigenschaft aufweisen;
eine Vielzahl von Entropiecodierern (55, 56), wobei die Eingänge der Entropiecodierer jeweils mit den Ausgängen der Vielzahl von Codierern verbunden sind, und die Entropiecodierer vorbestimmte Anzahlen von Quantisiererausgangsniveaus und vorbestimmte Wahrscheinlichkeitsverteilungen aufweisen;
Auswerteeinrichtungen (3), betriebsmäßig verbunden mit den Ausgängen der Vielzahl von Codierern und den Ausgängen der Vielzahl von Entropiecodierern, um die Eigenschaften der Ausgaben der Codierer und der Entropiecodierer auszuwerten, um die Entropiecodierer mit niedrigeren Ausgangsbitraten als die Übertragungsbitrate zu extrahieren, und um von den mit den extrahierten Entropiecodierern verbundenen Codierern einen Codierer mit der besten Ausgangseigenschaft zu extrahieren, um ein Auswahlsignal auszugeben, welches die Kombination des ausgewählten Codierers und eines Entropiecodierers in den extrahierten Entropiecodierern anzeigt; und
Auswahleinrichtungen (4), betriebsmäßig verbunden mit den Ausgängen der Vielzahl von Entropiecodierern und dem Ausgang der Auswerteeinrichtung, um auf das Auswahlsignal hin das durch die Kombination des Codierers und des Entropiecodierers gelaufene, zu übertragende Codewort auszuwählen.
7. Sprachcodier/Decodiersystem nach Anspruch 6, mit wenigstens einem Codierer, der direkt mit der Auswahleinrichtung verbunden ist, ohne durch irgendeinen Entropiecodierer verbunden zu sein.
8. Sprachcodier/Decodiersystem nach Anspruch 6, dadurch gekennzeichnet, daß der Empfangsteil umfaßt: Demultiplexeinrichtungen (5), welche betriebsmäßig mit dem Ausgang des Übertragungsteils durch eine Übertragungsleitung verbunden sind, um ein von dem Übertragungsteil empfangenes Signal in das Codewort und das Umschaltsignal zu demultiplexen;
Umschaltseinrichtungen (7), welche betriebsmäßig mit den Demultiplexereinrichtungen verbunden sind, mit einem einzelnen Eingangsende zum Empfangen des Codeworts und einer Vielzahl von Ausgangsenden, um das Codewort von der Demultiplexereinrichtung zu einem der Vielzahl von Ausgangsenden auf das Auswahlsignal von der Demultiplexereinrichtung hin zu leiten;
eine Vielzahl von Entropiedecodern (61, 62), wobei die Eingänge der Entropiedecoder mit der Vielzahl von Ausgangsenden der Umschaltseinrichtung verbunden sind, und die Entropiedecoder vorbestimmte Anzahlen von Quantisiererausgangsniveaus und vorbestimmte Wahrscheinlichkeitsverteilungen entsprechend den entsprechenden Entropiecodierern aufweisen; und
eine Vielzahl von Decodern (65, 66), wobei die Ausgänge der Entropiecodierer jeweils mit den Eingängen der Vielzahl von Decodern verbunden sind, um das entropiedecodierte Codewort von den Entropiedecodern zu decodieren, wobei die Decoder vorbestimmte Anzahlen von Quantisiererausgangsniveaus und die vorbestimmten Quantisierungseigenschaften aufweisen;
wodurch in Übereinstimmung mit dem Auswahlsignal, welches die beste Kombination des Codierers und des Entropiecodierers anzeigt, mittels der entsprechenden Kombination von einem der Entropiedecoder und einem der Codierer das übertragene Codewort decodiert wird.
9. Sprachcodier/Decodiersystem nach Anspruch 6 oder 8, dadurch gekennzeichnet, daß die vorbestimmten Anzahlen von Quantisiererausgangsniveaus der Vielzahl von Codierern einander gleich sind, die vorbestimmten Quantisierungseigenschaften der Vielzahl von Codierern voneinander verschieden sind, die Anzahlen der vorbestimmten Quantisierungsausgangsniveaus der Entropiecodierer einander gleich sind, und die Quantisierungseigenschaften der Entropiecodierer voneinander verschieden sind.
10. Sprachcodier/Decodiersystem nach Anspruch 9, dadurch gekennzeichnet, daß die vorbestimmten Anzahlen von Quantisiererausgangsniveaus der Vielzahl von Decodern einander gleich sind, die vorbestimmten Quantisierungseigenschaften der Vielzahl von Decodern voneinander verschieden sind, die Anzahlen der vorbestimmten Quantisierungsausgangsniveaus der Entropiedecoder einander gleich sind, und die Quantisierungseigenschaften der Entropiedecoder voneinander verschieden sind.
11. Sprachcodier/Decodiersystem nach Anspruch 8, gekennzeichnet durch wenigstens einen Decoder, der direkt mit den Umschaltseinrichtungen verbunden ist, ohne durch irgendeinen Entropiedecoder verbunden zu sein.
12. Sprachcodier/Decodiersystem nach Anspruch 1, dadurch gekennzeichnet, daß wenigstens einer der Codierer direkt mit den Auswahleinrichtungen verbunden ist, ohne durch die Entropiecodierer verbunden zu sein.

13. Sprachcodier/Decodiersystem nach Anspruch 1 oder 6, dadurch gekennzeichnet, daß die Auswahleinrichtung (4) Multiplexeinrichtungen zum Multiplexen des durch die Kombination gelaufenen Codeworts mit dem Auswahlsignal umfaßt.
- 5 14. Sprachcodier/Decodiersystem nach Anspruch 1 oder 6, dadurch gekennzeichnet, daß die Vielzahl von Decodern ADPCM-Codierer sind.
15. Sprachcodier/Decodiersystem nach Anspruch 1 oder 6, dadurch gekennzeichnet, daß jeder der Vielzahl von Codierern einen Quantisierer einschließt.
- 10 16. Sprachcodier/Decodiersystem nach Anspruch 1 oder 6, dadurch gekennzeichnet, daß jeder der Vielzahl von Codierern einen lokalen Decoder zum Erzeugen eines lokal decodierten Signals durch lokales Decodieren des von dem Codierer ausgegebenen Codeworts umfaßt, wobei das lokal decodierte Signal an die Auswerteeinrichtung gegeben wird, um einen Codierer mit der besten Eigenschaft zu extrahieren.
- 15 17. Sprachcodier/Decodiersystem nach Anspruch 6 oder 16, dadurch gekennzeichnet, daß die Eigenschaften der Codierer Signal/Rauschverhältnisse in dem lokal decodierten Signal sind.
18. Sprachcodier/Decodiersystem nach Anspruch 16, dadurch gekennzeichnet, daß die Eigenschaften der Codierer die Summierung der Absolutwerte der Fehlersignale in jedem lokaldecodierten Signal sind.
- 20 19. Sprachcodier/Decodiersystem nach Anspruch 16, dadurch gekennzeichnet, daß die Eigenschaften der Codierer der Spitzenwert der Absolutwerte der Fehlersignale in dem lokaldecodierten Signal sind.
20. Sprachcodier/Decodiersystem nach Anspruch 16, dadurch gekennzeichnet, daß die Eigenschaften der Codierer die Capstrumdistanzen in dem lokal decodierten Signal sind.
- 25 21. Sprachcodier/Decodiersystem nach Anspruch 1 oder 6, dadurch gekennzeichnet, daß die Entropiecodierer Huffman-Codierer sind.
- 30 22. Sprachcodier/Decodiersystem nach Anspruch 1 oder 6, dadurch gekennzeichnet, daß die Entropiecodierer arithmetische Codierer sind.
23. Sprachcodier/Decodiersystem nach Anspruch 1 oder 6, dadurch gekennzeichnet, daß die Entropiecodierer Lauflängencodierer sind.
- 35 24. Sprachcodier/Decodiersystem nach Anspruch 1 oder 6, dadurch gekennzeichnet, daß die Entropiecodierer Ziv-Lempel-Codierer sind.
- 40 25. Sprachcodier/Decodiersystem nach Anspruch 1, dadurch gekennzeichnet, daß der Empfangsteil umfaßt: Demultiplexeinrichtungen (5), die betriebsmäßig mit dem Ausgang des Übertragungsteils durch eine Übertragungsleitung verbunden sind, um ein empfangenes Signal von dem Übertragungsteil in ein Codewort und das Umschaltsignal zu demultiplexen; Umschaltseinrichtungen (7), welche betriebsmäßig mit den Demultiplexeinrichtungen verbunden sind, mit einem Einzeleingangsende zum Empfangen des Codeworts von der Demultiplexeinrichtung und einer Vielzahl von Ausgangsenden, um das Codewort zu einem der Vielzahl von Ausgangsenden auf das Auswahlsignal von der Demultiplexeinrichtung hin zu leiten; eine Vielzahl von Gruppen von Entropiedecodern (B1-Bn), wobei die Eingänge der Entropiedecoder in jeder der Gruppen mit der Vielzahl von Ausgangsenden der Umschaltseinrichtungen verbunden sind, und die Entropiedecoder in jeder der Gruppen vorbestimmte Anzahlen von Quantisiererausgangsniveaus und vorbestimmte Wahrscheinlichkeitsverteilungen entsprechend der entsprechenden Gruppe von Entropiecodierern aufweisen; und eine Vielzahl von Decodern (B1-Bn), wobei die Ausgänge der Entropiedecoder in jeder der Gruppen mit dem Eingang von einem der Vielzahl von Decodern verbunden ist, um das entropiecodierte Codewort von den Entropiedecodern zu decodieren, wobei die Decoder vorbestimmte Anzahlen von Quantisiererausgangsniveaus und die vorbestimmten Quantisierungseigenschaften aufweisen; 55 wodurch in Übereinstimmung mit dem Auswahlsignal, welches die beste Kombination des Codierers und des Entropiecodierers anzeigt, mittels der entsprechenden Kombination von einem der Entropiedecoder und einem der Codierer das übertragene Codewort decodiert wird.

26. Sprachcodier/Decodiersystem nach Anspruch 25, dadurch gekennzeichnet, daß die vorbestimmten Anzahlen von Quantisiererausgangsniveaus der Vielzahl von Codierern einander gleich sind, die vorbestimmten Quantisierungseigenschaften der Vielzahl von Codierern voneinander verschieden sind, die Anzahlen der vorbestimmten Quantisierungsausgangsniveaus der Entropiecodierer in jeder der Gruppen einander gleich sind, und die Quantisierungseigenschaften in jeder der Gruppen von Entropiecodierern voneinander verschieden sind.
27. Sprachcodier/Decodiersystem nach Anspruch 26, dadurch gekennzeichnet, daß die vorbestimmten Anzahlen von Quantisiererausgangsniveaus der Vielzahl von Decodern einander gleich sind, die vorbestimmten Quantisierungseigenschaften der Vielzahl von Decodern voneinander verschieden sind, die Anzahlen der vorbestimmten Quantisierungsausgangsniveaus der Entropiedecoder in jeder der Gruppen einander gleich sind, und die Quantisierungseigenschaften in jeder der Gruppen von Entropiedecodern voneinander verschieden sind.
28. Sprachcodier/Decodiersystem nach Anspruch 25, dadurch gekennzeichnet, daß die vorbestimmten Anzahlen von Quantisiererausgangsniveaus der Vielzahl von Codierern voneinander verschieden sind, die vorbestimmten Quantisierungseigenschaften der Vielzahl von Codierern einander gleich sind, die Anzahlen der vorbestimmten Quantisierungsausgangsniveaus der Entropiecodierer in jeder der Gruppen voneinander verschieden sind, und die Quantisierungseigenschaften in jeder der Gruppen von Entropiecodierern einander gleich sind.
29. Sprachcodier/Decodiersystem nach Anspruch 28, dadurch gekennzeichnet, daß die vorbestimmten Anzahlen von Quantisiererausgangsniveaus der Vielzahl von Decodern voneinander verschieden sind, die vorbestimmten Quantisierungseigenschaften der Vielzahl von Decodern einander gleich sind, die Anzahl der vorbestimmten Quantisierungsausgangsniveaus der Entropiecodierer in jeder der Gruppen voneinander verschieden sind, und die Quantisierungseigenschaften in jeder der Gruppen von Entropiedecodern einander gleich sind.
30. Sprachcodier/Decodiersystem nach Anspruch 25, dadurch gekennzeichnet, daß die vorbestimmten Anzahlen von Quantisiererausgangsniveaus der Vielzahl von Codierern voneinander verschieden sind, die vorbestimmten Quantisierungseigenschaften der Vielzahl von Codierern einander gleich sind, die Anzahlen der vorbestimmten Quantisiererausgangsniveaus der Entropiecodierer in jeder der Gruppen voneinander verschieden sind, und die Quantisierungseigenschaften in jeder der Gruppen von Entropiecodierern voneinander verschieden sind.
31. Sprachcodier/Decodiersystem nach Anspruch 30, dadurch gekennzeichnet, daß die vorbestimmten Anzahlen von Quantisiererausgangsniveaus der Vielzahl von Decodern voneinander verschieden sind, die vorbestimmten Quantisierungseigenschaften der Vielzahl von Decodern einander gleich sind, die Anzahlen der vorbestimmten Quantisiererausgangsniveaus der Entropiedecoder in jeder der Gruppen voneinander verschieden sind, und die Quantisierungseigenschaften in jeder der Gruppen von Entropiedecodern voneinander verschieden sind.
32. Sprachcodier/Decodiersystem nach Anspruch 25, dadurch gekennzeichnet, daß die vorbestimmten Anzahlen von Quantisiererausgangsniveaus der Vielzahl von Codierern voneinander verschieden sind, die vorbestimmten Quantisierungseigenschaften der Vielzahl von Codierern voneinander verschieden sind, die Anzahlen der vorbestimmten Quantisiererausgangsniveaus der Entropiecodierer in jeder der Gruppen voneinander verschieden sind, und die Quantisierungseigenschaften in jeder der Gruppen von Entropiecodierern voneinander verschieden sind.
33. Sprachcodier/Decodiersystem nach Anspruch 32, dadurch gekennzeichnet, daß die vorbestimmten Anzahlen von Quantisiererausgangsniveaus der Vielzahl von Decodern voneinander verschieden sind, wobei die vorbestimmten Quantisierungseigenschaften der Vielzahl von Decodern voneinander verschieden sind, die Anzahlen der vorbestimmten Quantisiererausgangsniveaus der Entropiedecoder in jeder der Gruppen voneinander verschieden sind, und die Quantisierungseigenschaften in jeder der Gruppen von Entropiedecodern voneinander verschieden sind.
34. Sprachcodier/Decodiersystem nach Anspruch 25, dadurch gekennzeichnet, daß wenigstens einer der Decoder direkt mit den Umschalteneinrichtungen verbunden ist, ohne durch die Entropiedecoder verbunden zu sein.

35. Sprachcodier/Decodiersystem nach Anspruch 25, dadurch gekennzeichnet, daß die Vielzahl von Decodern einen Quantisierer einschließt.
- 5 36. Sprachcodier/Decodiersystem nach Anspruch 8 oder 25, dadurch gekennzeichnet, daß die Vielzahl von Decodern ADPCM-Decoder sind.
37. Sprachcodier/Decodiersystem nach Anspruch 8 oder 25, dadurch gekennzeichnet, daß die Entropiecodierer Huffman-Decoder sind.
- 10 38. Sprachcodier/Decodiersystem nach Anspruch 8 oder 25, dadurch gekennzeichnet, daß die Entropiedecoder arithmetische Decoder sind.
39. Sprachcodier/Decodiersystem nach Anspruch 8 oder 25, dadurch gekennzeichnet, daß die Entropiedecoder Lauflängendecoder sind.
- 15 40. Sprachcodier/Decodiersystem nach Anspruch 8 oder 25, dadurch gekennzeichnet, daß die Entropiedecoder Ziv-Lempel-Decoder sind.

Revendications

- 20 1. Système de codage/décodage de la parole ayant une partie émettrice pour émettre un signal codé d'un signal vocal d'entrée à un débit binaire inférieur à un débit binaire de transmission prédéterminé, et une partie réceptrice pour recevoir et décoder le signal codé transmis à partir de ladite partie émettrice, ladite partie émettrice comprenant:
- 25 - une pluralité de codeurs (A1-An) pour coder ledit signal d'entrée, lesdits codeurs ayant des nombres prédéterminés de niveaux de sortie de quantificateur et ayant une caractéristique de quantification prédéterminée;
- une pluralité de groupes de codeurs à entropie (A11-Anm), les entrées desdits codeurs à entropie dans chacun desdits groupes étant connectés à la sortie d'un codeur de ladite pluralité de codeurs, lesdits codeurs à entropie ayant des nombres prédéterminés de niveaux de sortie de quantificateur et des répartition de probabilité prédéterminées;
- 30 - des moyens d'évaluation (3), connectés fonctionnellement aux sorties de ladite pluralité de codeurs et aux sorties de ladite pluralité de codeurs à entropie, pour évaluer les caractéristiques des signaux de sortie desdits codeurs et desdits codeurs à entropie pour extraire les codeurs à entropie ayant des débits binaires de sortie inférieurs au débit binaire de transmission et pour extraire, parmi les codeurs connectés aux codeurs à entropie extraits, un codeur ayant la meilleure caractéristique de
- 35 sortie, pour fournir un signal de sélection indiquant la combinaison du codeur sélectionné et d'un codeur à entropie parmi les codeurs à entropie; et
- des moyens de sélection (4) connectés fonctionnellement aux sorties de ladite pluralité de codeurs à entropie et à la sortie desdits moyens d'évaluation pour sélectionner, en réponse audit signal de
- 40 sélection, le mot de code ayant passé par ladite combinaison du codeur et du codeur à entropie pour être transmis.
2. Système de codage/décodage de la parole selon la revendication 1, dans lequel lesdits nombres prédéterminés de niveaux de sortie de quantificateur de ladite pluralité de codeurs sont les mêmes les uns que les autres, lesdites caractéristiques de quantification prédéterminées de ladite pluralité de codeurs sont différentes les unes des autres, les nombres desdits niveaux de sortie de quantification prédéterminés desdits codeurs à entropie dans chacun desdits groupes sont les mêmes les uns que les autres, et les caractéristiques de quantification dans chacun desdits groupes de codeurs à entropie sont différentes les unes des autres.
- 50 3. Système de codage/décodage de la parole selon la revendication 1, dans lequel lesdits nombres prédéterminés de niveaux de sortie de quantificateur de ladite pluralité de codeurs sont différents les uns des autres, lesdites caractéristiques de quantification prédéterminées de ladite pluralité de codeurs sont les mêmes les unes que les autres, les nombres desdits niveaux de sortie de quantification prédéterminés desdits codeurs à entropie dans chacun desdits groupes sont différents les uns des autres, et les caractéristiques de quantification dans chacun desdits groupes de codeurs à entropie sont les mêmes les unes que les autres.
- 55

4. Système de codage/décodage de la parole selon la revendication 1, dans lequel lesdits nombres prédéterminés de niveaux de sortie de quantificateurs de ladite pluralité de codeurs sont différents les uns des autres, lesdites caractéristiques de quantification prédéterminées de ladite pluralité de codeurs sont les mêmes les unes que les autres, les nombres desdits niveaux de sortie de quantification prédéterminés desdits codeurs à entropie dans chacun desdits groupes sont différents les uns des autres, et les caractéristiques de quantification dans chacun desdits groupes de codeurs à entropie sont différentes les unes des autres.
5. Système de codage/décodage de la parole selon la revendication 1, dans lequel lesdits nombres prédéterminés de niveaux de sortie de quantificateur de ladite pluralité de codeurs sont différents les uns des autres, lesdites caractéristiques de quantification prédéterminées de ladite pluralité de codeurs sont différentes les unes des autres, les nombres desdits niveaux de sortie de quantification prédéterminés desdits codeurs à entropie dans chacun desdits groupes sont différents les uns des autres, et les caractéristiques de quantification dans chacun desdits groupes de codeurs à entropie sont différentes les unes des autres.
6. Système de codage/décodage de la parole ayant une partie émettrice pour émettre un signal codé d'un signal vocal d'entrée à un débit binaire inférieur à un débit binaire prédéterminé de transmission, et une partie réceptrice pour recevoir et décoder le signal codé transmis à partir de la partie émettrice, ladite partie émettrice comprenant:
- une pluralité de codeurs (53, 54) pour coder ledit signal vocal d'entrée, lesdits codeurs ayant des nombres prédéterminés de niveaux de sortie de quantificateur et ayant une caractéristique de quantification prédéterminée;
 - une pluralité de codeurs à entropie (55, 56), les entrées desdits codeurs à entropie étant connectées aux sorties de ladite pluralité de codeurs, respectivement, lesdits codeurs à entropie ayant des nombres prédéterminés de niveaux de sortie de quantificateur et des répartitions de probabilité prédéterminées;
 - des moyens d'évaluation (3), connectés fonctionnellement aux sorties de ladite pluralité de codeurs et aux sorties de ladite pluralité de codeurs à entropie, pour évaluer les caractéristiques des signaux de sortie desdits codeurs et desdits codeurs à entropie pour extraire les codeurs à entropie ayant des débits binaires de sortie inférieurs au débit binaire de transmission et pour extraire, parmi les codeurs connectés aux codeurs à entropie extraits, un codeur ayant la meilleure caractéristique de sortie pour fournir un signal de sélection indiquant la combinaison du codeur sélectionné et d'un codeur à entropie parmi les codeurs à entropie extraits; et
 - des moyens de sélection (4) connectés fonctionnellement aux sorties de ladite pluralité de codeurs à entropie et à la sortie desdits moyens d'évaluation pour sélectionner, en réponse audit signal de sélection, le mot de code ayant passé par ladite combinaison du codeur et du codeur à entropie pour être transmis.
7. Système de codage/décodage de la parole selon la revendication 6, comprenant en outre au moins un codeur connecté directement auxdits moyens de sélection, sans être connecté par l'intermédiaire d'un codeur à entropie.
8. Système de codage/décodage de la parole selon la revendication 6, dans lequel ladite partie réceptrice comprend:
- des moyens de démultiplexage (5) connectés fonctionnellement à la sortie de ladite partie émettrice par l'intermédiaire d'une ligne de transmission pour démultiplexer un signal reçu de ladite partie émettrice en ledit mot de code et ledit signal de commutation;
 - des moyens de commutation (7) connectés fonctionnellement auxdits moyens de démultiplexage, ayant une extrémité d'entrée unique pour recevoir ledit mot de code, et une pluralité d'extrémités de sortie pour transmettre ledit mot de code issu desdits moyens de démultiplexage à une extrémité de ladite pluralité d'extrémités de sortie en réponse audit signal de sélection issu desdits moyens de démultiplexage;
 - une pluralité de décodeurs à entropie (61, 62), les entrées desdits décodeurs à entropie étant connectées à ladite pluralité d'extrémités de sortie desdits moyens de commutation, lesdits décodeurs à entropie ayant des nombres prédéterminés de niveaux de sortie de quantificateur et des répartitions de probabilité prédéterminées correspondant aux codeurs à entropie correspondants; et

- une pluralité de décodeurs (65, 66), les sorties desdits décodeurs à entropie étant connectées aux entrées de ladite pluralité de décodeurs, respectivement, pour décoder le mot de code décodé avec entropie issu desdits décodeurs à entropie, lesdits décodeurs ayant des nombres prédéterminés de niveaux de sortie de quantificateur et ayant les caractéristiques de quantifications prédéterminées; ce par quoi, selon ledit signal de sélection indiquant la meilleure combinaison du codeur et du codeur à entropie, par la combinaison correspondante d'un desdits codeurs à entropie et d'un desdits codeurs, le mot de code transmis est décodé.
9. Système de codage/décodage de la parole selon la revendication 6 ou 8, dans lequel lesdits nombres prédéterminés de niveaux de sortie de quantificateur de ladite pluralité de codeurs sont les mêmes les uns que les autres, lesdites caractéristiques de quantification prédéterminées de ladite pluralité de codeurs sont différentes les unes des autres, les nombres desdits niveaux de sortie de quantification desdits codeurs à entropie sont les mêmes les uns que les autres, et les caractéristiques de quantification desdits codeurs à entropie sont différentes les unes des autres.
 10. Système de codage/décodage de la parole selon la revendication 9, dans lequel lesdits nombres prédéterminés de niveaux de sortie de quantificateur de ladite pluralité de décodeurs sont les mêmes les uns que les autres, lesdites caractéristiques de quantification prédéterminées de ladite pluralité de décodeurs sont différentes les unes des autres, les nombres desdits niveaux de sortie de quantification prédéterminés desdits décodeurs à entropie sont les mêmes les uns que les autres, et les caractéristiques de quantification desdits décodeurs à entropie sont différentes les unes des autres.
 11. Système de codage/décodage de la parole selon la revendication 8, comprenant en outre au moins un décodeur connecté directement auxdits moyens de commutation, sans être connecté par l'intermédiaire d'un décodeur à entropie quelconque.
 12. Système de codage/décodage de la parole selon la revendication 1, dans lequel au moins un desdits codeurs est connecté directement auxdits moyens de sélection, sans être connecté par l'intermédiaire desdits codeurs à entropie.
 13. Système de codage/décodage de la parole selon la revendication 1 ou 6, dans lequel lesdits moyens de sélection (4) comprennent des moyens de multiplexage pour multiplexer ledit mot de code ayant passé par ladite combinaison avec ledit signal de sélection.
 14. Système de codage/décodage de la parole selon la revendication 1 ou 6, dans lequel ladite pluralité de décodeurs sont des décodeurs à modulation différentielle adaptative par impulsions codées (ADPCM).
 15. Système de codage/décodage de la parole selon la revendication 1 ou 6, dans lequel chaque codeur de ladite pluralité de codeurs comporte un quantificateur.
 16. Système de codage/décodage de la parole selon la revendication 1 ou 6, dans lequel chaque codeur de ladite pluralité de codeurs comprend un décodeur local pour produire un signal décodé local en décodant localement le mot de code issu du codeur, ledit signal décodé local étant fourni auxdits moyens d'évaluation pour extraire un codeur ayant ladite meilleure caractéristique.
 17. Système de codage/décodage de la parole selon la revendication 6 ou 16, dans lequel les caractéristiques desdits codeurs sont des rapports signal/bruit dans ledit signal décodé local.
 18. Système de codage/décodage de la parole selon la revendication 16, dans lequel les caractéristiques desdits codeurs sont la somme des valeurs absolues des signaux d'erreur dans chaque signal décodé local.
 19. Système de codage/décodage de la parole selon la revendication 16, dans lequel les caractéristiques desdits codeurs sont la valeur de pic des valeurs absolues des signaux d'erreur dans ledit signal décodé local.
 20. Système de codage/décodage de la parole selon la revendication 16, dans lequel les caractéristiques desdits codeurs sont les distances du cepstre dans ledit signal décodé local.
 21. Système de codage/décodage de la parole selon la revendication 1 ou 6, dans lequel lesdits codeurs à entropie sont des codeurs de Huffman.

22. Système de codage/décodage de la parole selon la revendication 1 ou 6, dans lequel lesdits codeurs à entropie sont des codeurs arithmétiques.
- 5 23. Système de codage/décodage de la parole selon la revendication 1 ou 6, dans lequel lesdits codeurs à entropie sont des codeurs "runlength".
24. Système de codage/décodage de la parole selon la revendication 1 ou 6, dans lequel lesdits codeurs à entropie sont des codeurs Ziv-lempel.
- 10 25. Système de codage/décodage de la parole selon la revendication 1, dans lequel ladite partie réceptrice comprend:
- des moyens de démultiplexage (5), connectés fonctionnellement à la sortie de ladite partie émettrice par l'intermédiaire d'une ligne de transmission, pour démultiplexer un signal reçu issu de ladite partie émettrice en un mot de code et ledit signal de commutation;
 - 15 - des moyens de commutation (7) connectés fonctionnellement auxdits moyens de démultiplexage, ayant une extrémité d'entrée unique pour recevoir ledit mot de code issu desdits moyens de démultiplexage et une pluralité d'extrémités de sortie pour transmettre ledit mot de code à une extrémité de ladite pluralité d'extrémités de sortie en réponse audit signal de sélection issu desdits moyens de démultiplexage;
 - 20 - une pluralité de groupes de décodeurs à entropie (B11-Bnm), les entrées desdits décodeurs à entropie dans chacun desdits groupes étant connectées à ladite pluralité d'extrémités de sortie desdits moyens de commutation, lesdits décodeurs à entropie dans chacun desdits groupes ayant des nombres prédéterminés de niveaux de sortie de quantificateur et des répartitions de probabilité prédéterminées correspondant aux groupes correspondants de codeurs à entropie; et
 - 25 - une pluralité de décodeurs (B1-Bn), les sorties desdits décodeurs à entropie dans chacun desdits groupes étant connectées à l'entrée d'un décodeur de ladite pluralité de décodeurs, pour décoder le mot de code codé avec entropie issu desdits décodeurs à entropie, lesdits décodeurs ayant des nombres prédéterminés de niveaux de sortie de quantificateur, et ayant les caractéristiques de quantification prédéterminées;
- 30 ce par quoi, selon ledit signal de sélection indiquant la meilleure combinaison du codeur et du codeur à entropie, par la combinaison correspondante d'un desdits décodeurs à entropie et d'un desdits décodeurs, le mot de code transmis est décodé.
- 35 26. Système de codage/décodage de la parole selon la revendication 25, dans lequel lesdits nombres prédéterminés de niveaux de sortie de quantificateur de ladite pluralité de codeurs sont les mêmes les uns que les autres, lesdites caractéristiques de quantification prédéterminées de ladite pluralité de codeurs sont différentes les unes des autres, les nombres desdits niveaux de sortie de quantification prédéterminés desdits codeurs à entropie dans chacun desdits groupes sont les mêmes les uns que les autres, et les caractéristiques de quantification dans chacun desdits groupes de codeurs à entropie sont différentes les unes des autres.
- 40 27. Système de codage/décodage de la parole selon la revendication 26, dans lequel lesdits nombres prédéterminés de niveaux de quantificateur de ladite pluralité de décodeurs sont les mêmes les uns que les autres, lesdites caractéristiques de quantification prédéterminées de ladite pluralité de décodeurs sont différentes les unes des autres, les nombres desdits niveaux de sortie de quantification prédéterminés desdits codeurs à entropie dans chacun desdits groupes sont les mêmes les uns que les autres, et les caractéristiques de quantification dans chacun desdits groupes de décodeurs à entropie sont différentes les unes des autres.
- 45 28. Système de codage/décodage de la parole selon la revendication 25, dans lequel lesdits nombres prédéterminés de niveaux de sortie de quantificateur de ladite pluralité de codeurs sont différents les uns des autres, lesdites caractéristiques de quantification prédéterminées de ladite pluralité de codeurs sont les mêmes les unes que les autres, les nombres desdits niveaux de sortie de quantification prédéterminés desdits codeurs à entropie dans chacun desdits groupes sont différents les uns des autres, et les caractéristiques de quantification dans chacun desdits groupes de codeurs à entropie sont les mêmes les unes que les autres.
- 50 29. Système de codage/décodage de la parole selon la revendication 28, dans lequel lesdits nombres prédéterminés de niveaux de sortie de quantificateur de ladite pluralité de décodeurs sont différents les uns
- 55

- des autres, lesdites caractéristiques de quantification prédéterminées de ladite pluralité de décodeurs sont les mêmes les unes que les autres, les nombres desdits niveaux de sortie de quantification prédéterminés desdits décodeurs à entropie dans chacun desdits groupes sont différents les uns des autres, et les caractéristiques de quantification dans chacun desdits groupes de décodeurs à entropie sont les mêmes les unes que les autres.
- 5
30. Système de codage/décodage de la parole selon la revendication 25, dans lequel lesdits nombres prédéterminés de niveaux de sortie de quantificateur de ladite pluralité de codeurs sont différents les uns des autres, lesdites caractéristiques de quantification prédéterminées de ladite pluralité de codeurs sont les mêmes les unes que les autres, les nombres desdits niveaux de sortie de quantification prédéterminés desdits codeurs à entropie dans chacun desdits groupes sont différents les uns des autres, et les caractéristiques de quantification dans chacun desdits groupes de codeurs à entropie sont différentes les unes des autres.
- 10
31. Système de codage/décodage de la parole selon la revendication 30, dans lequel lesdits nombres prédéterminés de niveaux de sortie de quantificateur de ladite pluralité de décodeurs sont différents les uns des autres, lesdites caractéristiques de quantification de ladite pluralité de décodeurs sont les mêmes les unes que les autres, les nombres desdits niveaux de sortie de quantification prédéterminés desdits codeurs à entropie dans chacun desdits groupes sont différents les uns des autres, et les caractéristiques de quantification dans chacun desdits groupes de décodeurs à entropie sont différentes les unes des autres.
- 15
- 20
32. Système de codage/décodage de la parole selon la revendication 25, dans lequel lesdits nombres prédéterminés de niveaux de sortie de quantificateur de ladite pluralité de codeurs sont différents les uns des autres, lesdites caractéristiques de quantification prédéterminées de ladite pluralité de codeurs sont différentes les unes des autres, les nombres desdits niveaux de sortie de quantification prédéterminés desdits codeurs à entropie dans chacun desdits groupes sont différents les uns des autres, et les caractéristiques de quantification dans chacun desdits groupes de codeurs à entropie sont différentes les unes des autres.
- 25
33. Système de codage/décodage de la parole selon la revendication 32, dans lequel lesdits nombres prédéterminés de niveaux de sortie de quantificateur de ladite pluralité de décodeurs sont différents les uns des autres, lesdites caractéristiques de quantification prédéterminées de ladite pluralité de décodeurs sont différentes les unes des autres, les nombres desdits niveaux de sortie de quantification prédéterminés desdits décodeurs à entropie dans chacun desdits groupes sont différents les uns des autres, et les caractéristiques de quantification dans chacun desdits groupes de décodeurs à entropie sont différentes les unes des autres.
- 30
- 35
34. Système de codage/décodage de la parole selon la revendication 25, dans lequel au moins un desdits décodeurs est connecté directement auxdits moyens de commutation, sans être connecté par l'intermédiaire desdits décodeurs à entropie.
- 40
35. Système de codage/décodage de la parole selon la revendication 25, dans lequel chaque décodeur de ladite pluralité de décodeurs comporte un quantificateur.
36. Système de codage/décodage de la parole selon la revendication 8 ou 25, dans lequel les décodeurs de ladite pluralité de décodeurs sont des décodeurs à modulation différentielle adaptative par impulsions codées (ADPCM).
- 45
37. Système de codage/décodage de la parole selon la revendication 8 ou 25, dans lequel lesdits décodeurs à entropie sont des décodeurs de Huffman.
- 50
38. Système de codage/décodage de la parole selon la revendication 8 ou 25, dans lequel lesdits décodeurs à entropie sont des décodeurs arithmétiques.
39. Système de codage/décodage de la parole selon la revendication 8 ou 25, dans lequel lesdits décodeurs à entropie sont des décodeurs "runlength".
- 55
40. Système de codage/décodage de la parole selon la revendication 8 ou 25, dans lequel lesdits décodeurs à entropie sont des décodeurs de Ziv-Lempel.

Fig. 1

PRIOR ART

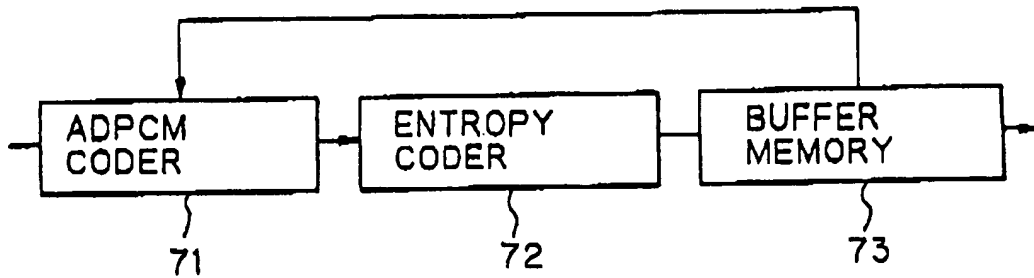


Fig. 2

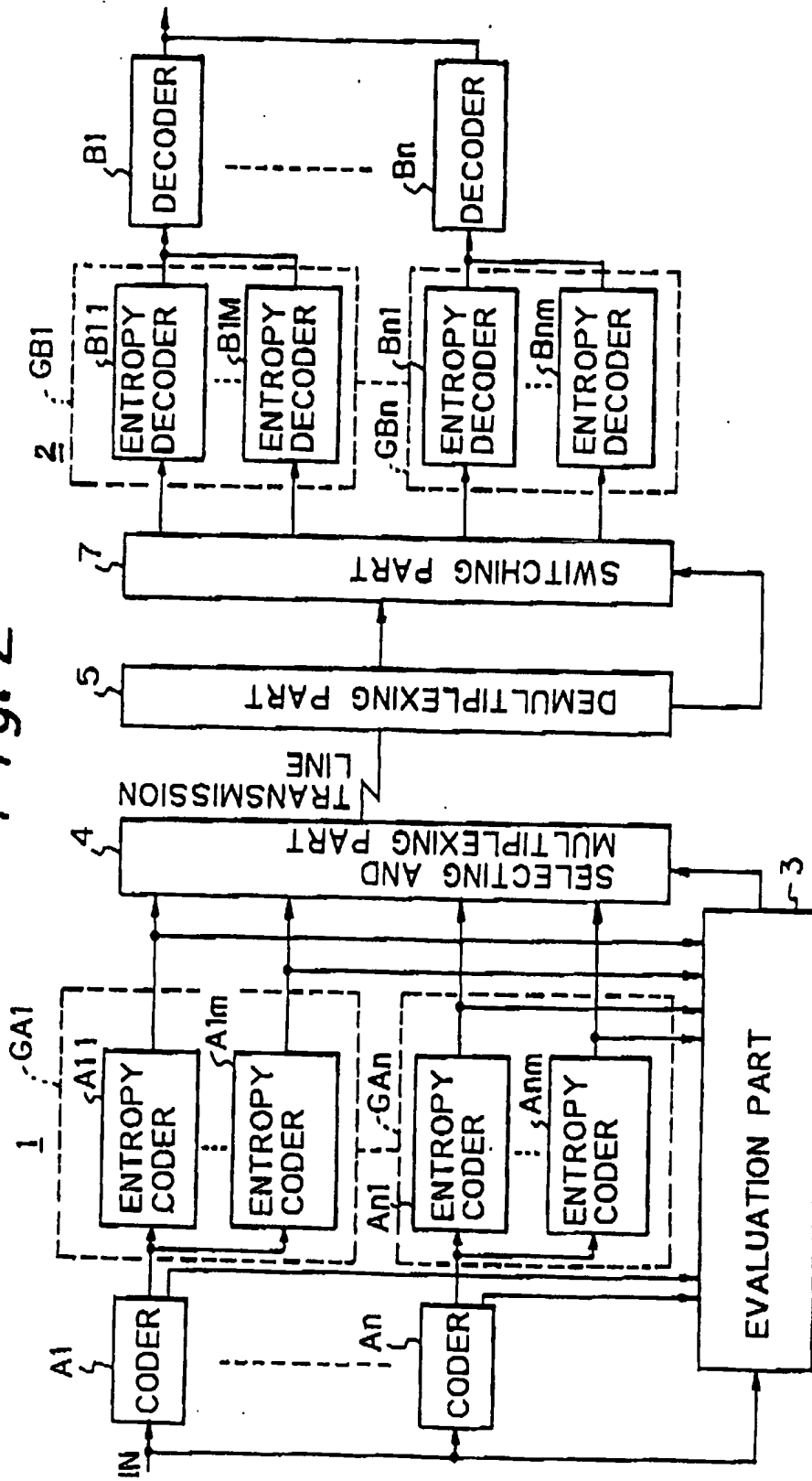


Fig. 3

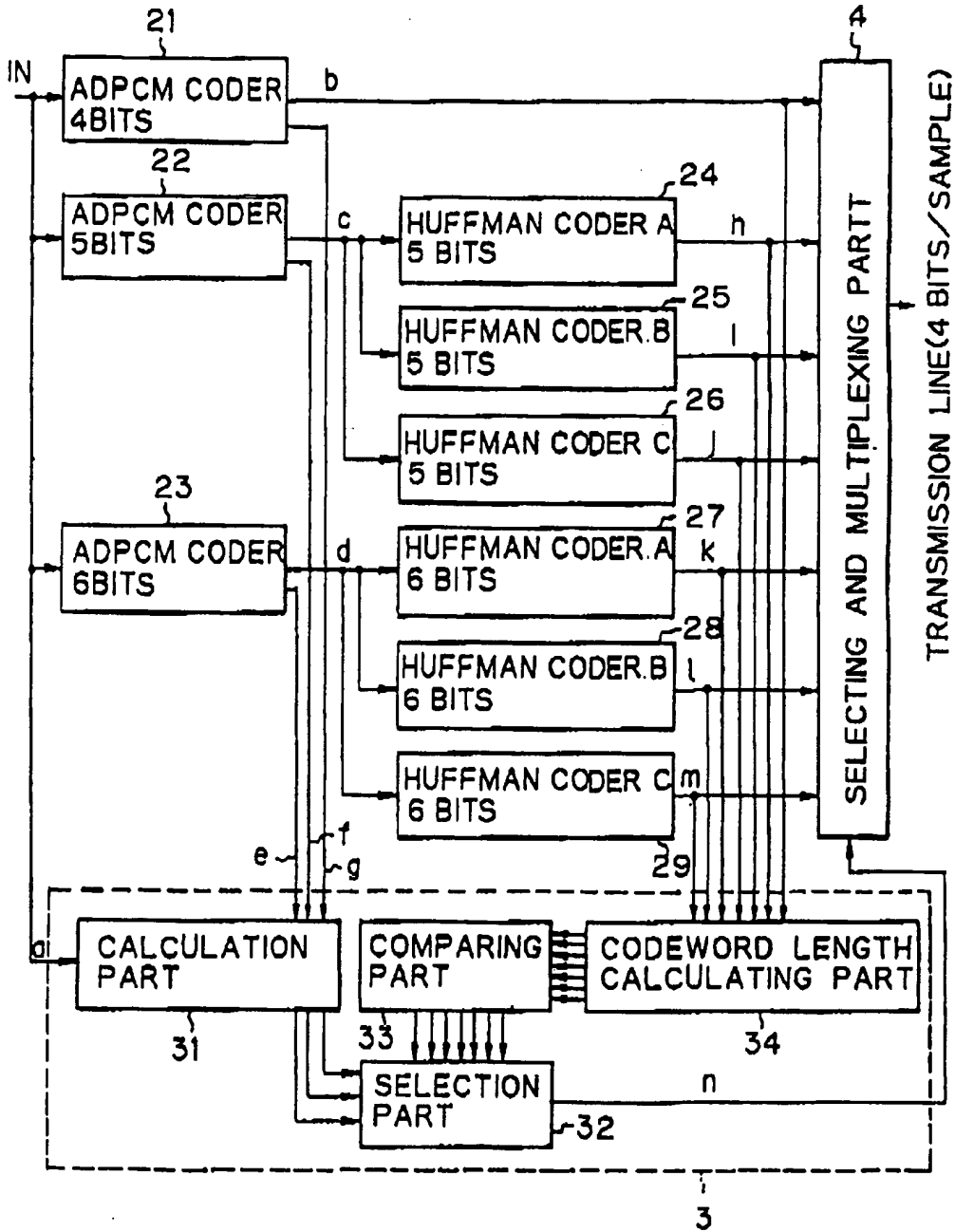


Fig. 4

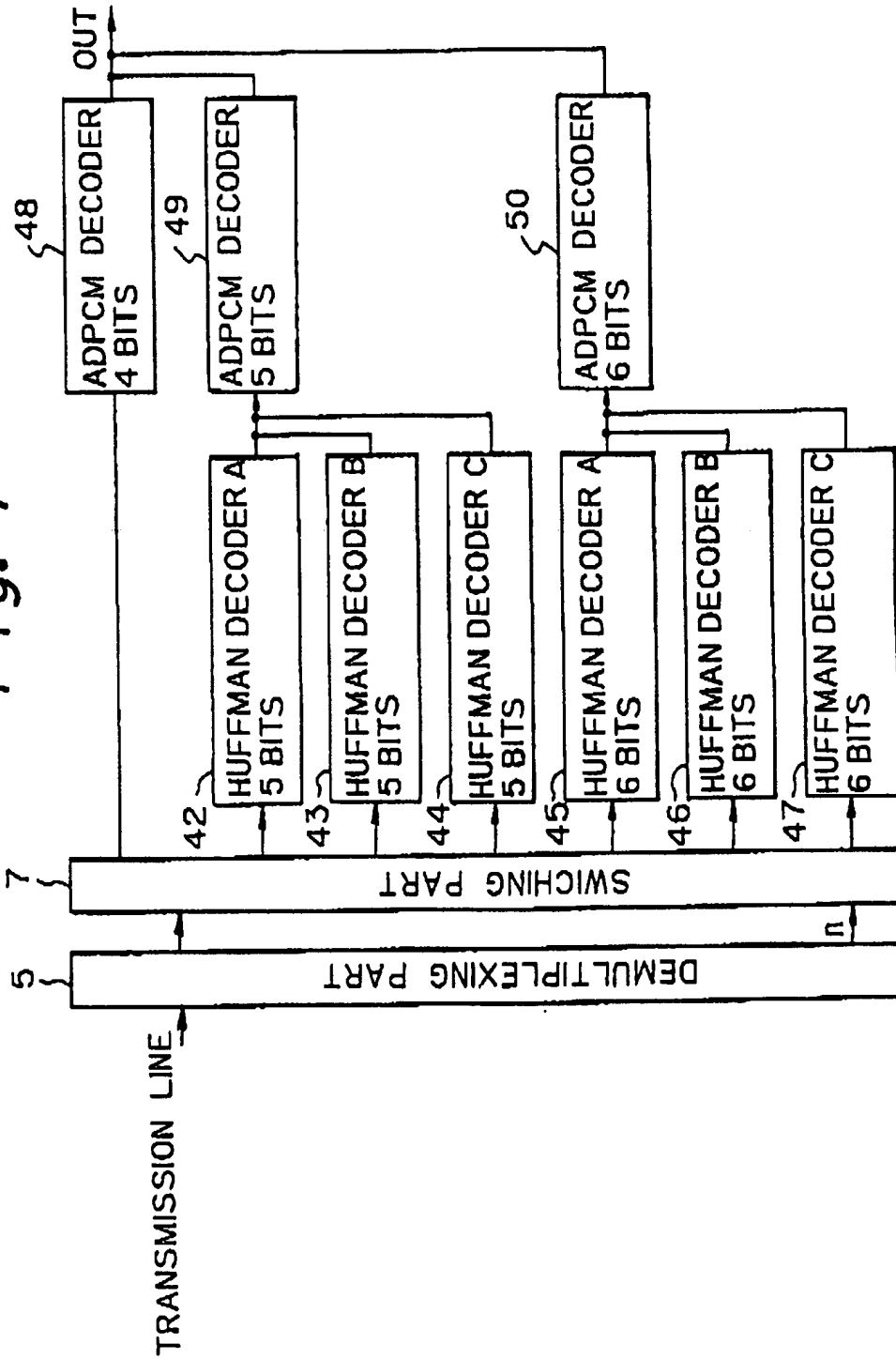


Fig. 5

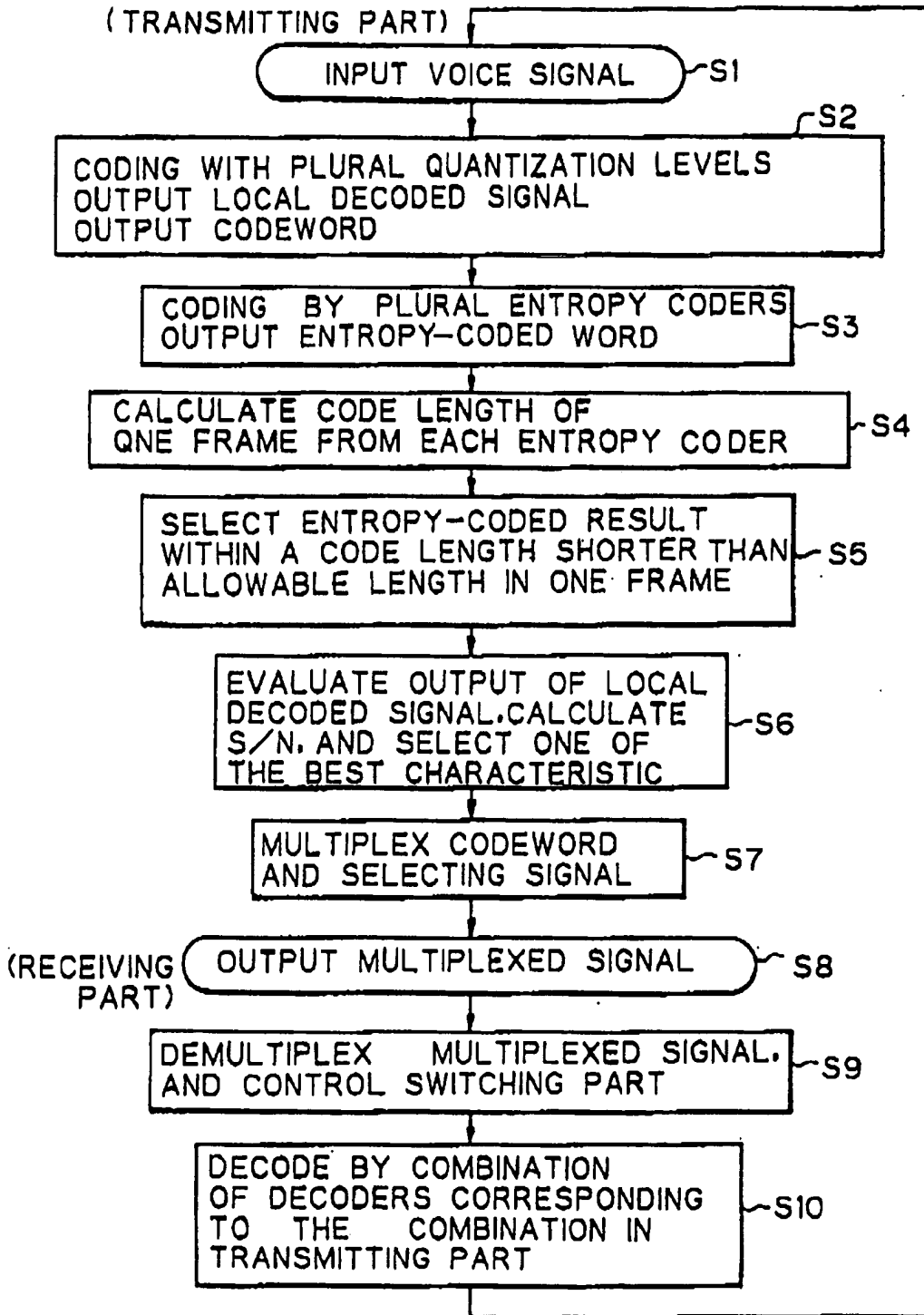


Fig. 6

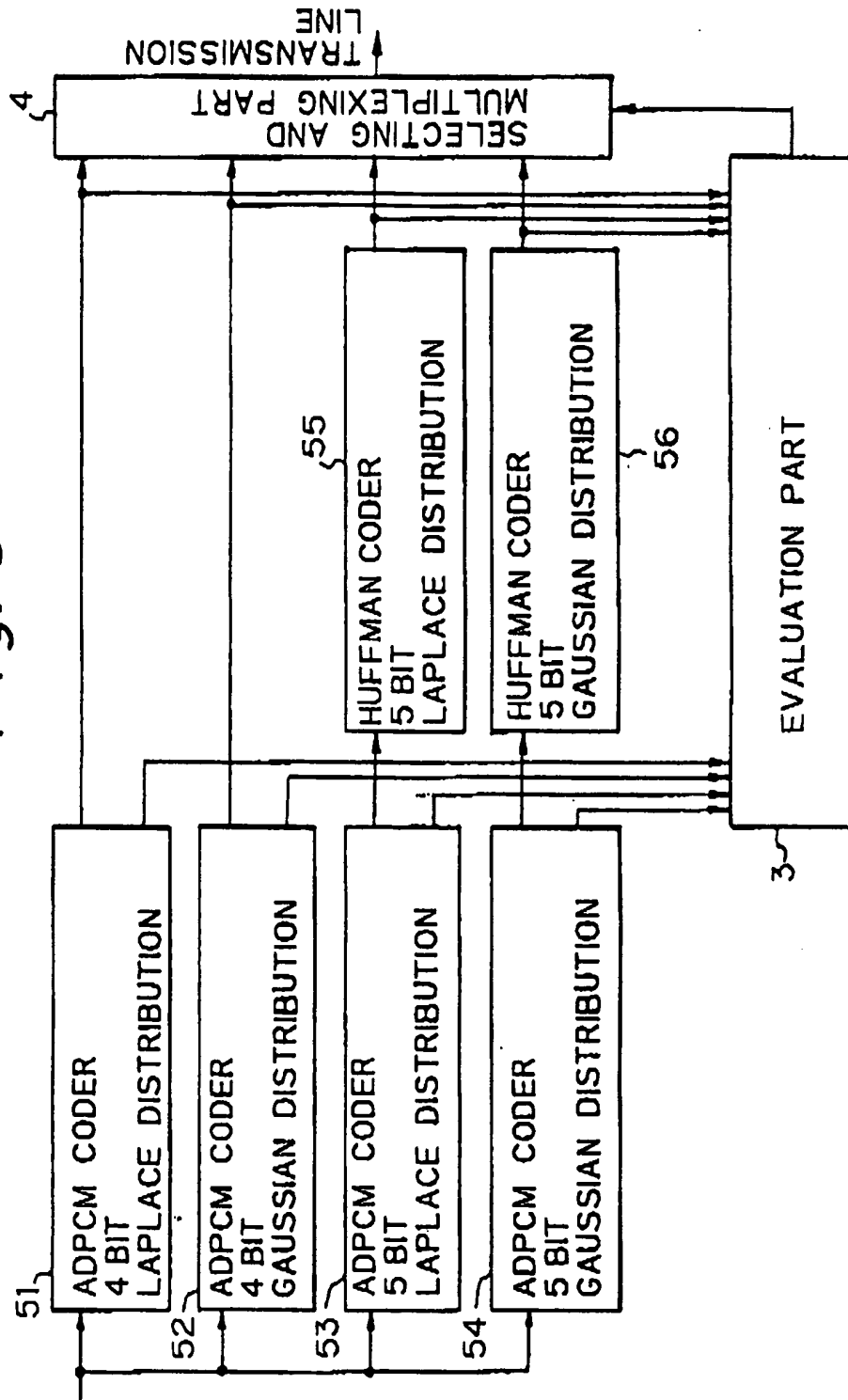
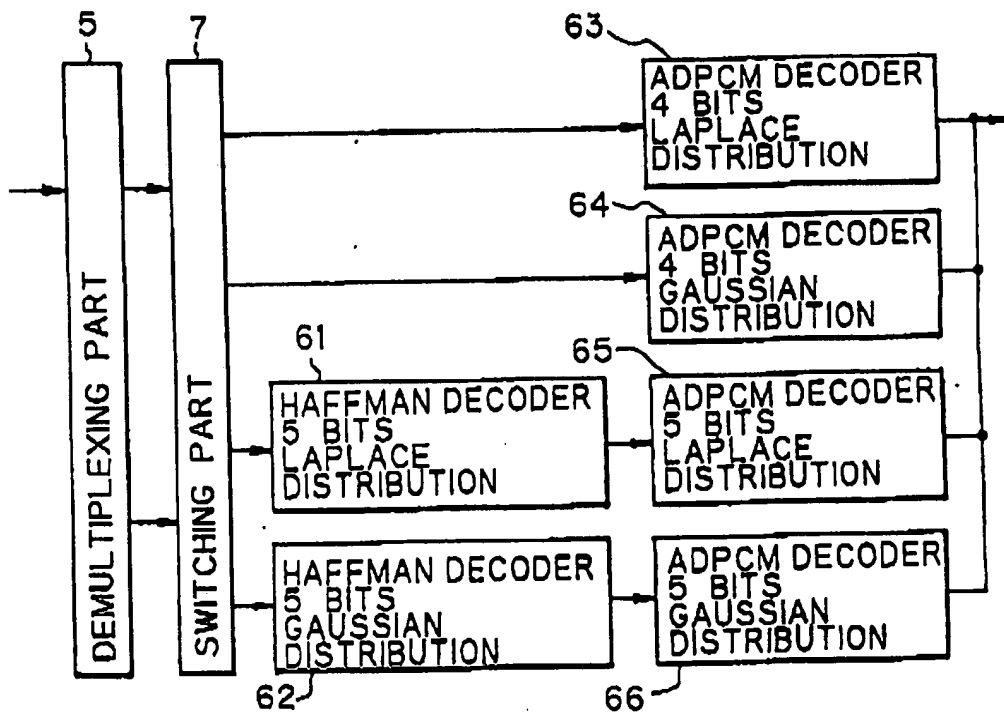


Fig. 7



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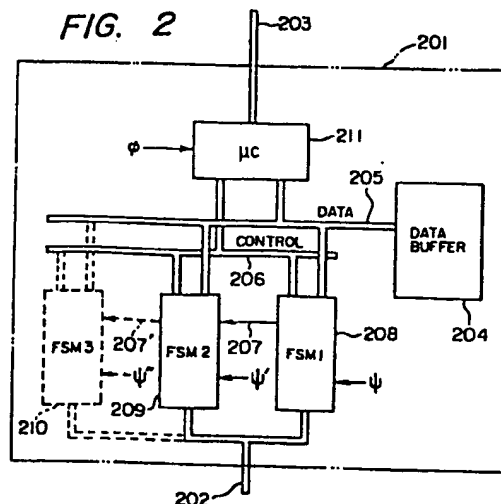
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64 CONTROL INTEGRATED CIRCUIT.

57 A control integrated circuit of the invention is based upon a hierarchical processor structure. A microprogram controller (211) is employed for a high-order processor to give sophisticated functions. A plurality of finite-state transition machines (208, 209) are employed for a low-order processor to increase the speed of operation. The control function for an external input/output device is divided and is executed by a plurality of finite-state transition machines (208, 209), the performance thereof being controlled by the microprogram controller (211). According to the present invention, a new control function is processed by adding a finite-state transition machine (210). Namely, the invention provides the general structure of an integrated circuit for controlling various input/output devices.



SPECIFICATION

TITLE OF THE INVENTION:

INTEGRATED CIRCUIT CONTROLLER

[Technical Field]

This invention relates to an integrated circuit controller, and more particularly to an integrated circuit controller which contributes to shorten the time of developing large scale integrated circuits (hereinafter referred to simply as "LSI" for brevity) with a view to realizing various peripheral I/O device controllers.

[Description of the Prior Art]

It is known in the art that an LSI can be designed efficiently in a short time period by the use of the so-called regular logic circuits such as read-only memory (hereinafter referred to simply as "ROM") and a programmable logic array (hereinafter referred to simply as "PLA"). Especially, it is a universal expedient to store a microprogram in ROM thereby to control the circuits in LSI.

Although not related to LSI, Japanese Patent Publication No. 59-4736 discloses a disk drive

controller using the microprogram control, in which the branch control of a microprogram is improved to reduce the program size and to secure compatibility to drives of different types. In this case, however, the microprogram does not execute all of the disk control facility, relying on other logic circuits for control of counters and the like.

Accordingly, the above-mentioned device can cope with connection of disk drives of different types by alteration of the microprogram but it cannot be applied to serial I/O controls other than disk drives, for example, to the communication protocol without entailing a considerable amount of corrections in the logic circuits.

In order to obtain a versatile structure which can be applied to a diversity of peripheral I/O controllers with less alterations, it becomes necessary to incorporate the regular logics in a large extent. In spite of easiness of making alterations in design, the regular logics have a large structure due to existence of redundant circuits and therefore are slow in operation speed. Besides, notwithstanding the higher versatility, the microprogram control which requires more than several steps for performing a predetermined

operation lacks ability of real time control.

[Summary of the Invention]

It is an object of the present invention to provide a general purpose integrated circuit which incorporates regular logics in a large extent to facilitate alterations in design but which can be applied to designing of various external I/O controllers of high performance quality.

The integrated circuit of the invention employs a processor hierarchy in LSI to preclude degradations of performance quality which would result from adoption of regular logics in a large extent. Namely, the integrated circuit of the invention employs a microprogram controller as a high-level processor and a finite state machine (hereinafter referred to simply as "state machine") as low-level processors to increase the operation speed. Besides, alterations in design can be made by reprogramming of the controller and state machines, and a connection structure which permits addition of low-level processors if necessary is employed.

BRIEF DESCRIPTION OF THE DRAWINGS

In the accompanying drawings:

Fig. 1 is a pictorial diagram of a state machine;

Fig. 2 is a pictorial diagram of an LSI controller according to the present invention;

Fig. 3 is a pictorial diagram showing the operation sequence of the LSI of Fig. 2;

Fig. 4 is a pictorial diagram of the internal structure of the state machine; and

Fig. 5 is a layout of the LSI controller according to the invention.

DESCRIPTION OF THE PREFERRED EMBODIMENT

Hereafter, the invention is described more particularly by way of a preferred embodiment.

In the finite state machine shown in Fig. 1, the control signals flow through a couple of registers 102a and 102b and a combinational logic circuit 101 between the two registers 102a and 102b. The input 103 and a feed-back signal 105 of the output of the register 102b are fed to the register 102a. The register 102a which is driven by clock $\psi 1$ retains these inputs and sends them to the combinational logic circuit 101. The register 102b which is driven by clock $\psi 2$ stores the output of the combinational logic circuit 101 upon receipt of the clock signal $\psi 2$, producing output partly as control signal output 104 and partly as a "state" or

a feed-back signal 105 to the register 102a.

Normally, the clock signals ψ_1 and ψ_2 are non-overlapped two phase clock signals which are obtained from a clock generator 106 on the basis of primary clock signal. Therefore, at one cycle time after application of the input 103 to the register 102a, the state in the register 102b changes and the control output 104 is produced. In a case where the clock signals ψ are identical with the clock signals which control the external I/O device, the state machine can be synchronized with the signals from the external I/O device (led to input 103), with a delay of one cycle time in response, so that it is suitable for real time control of an external I/O device. Further, alterations in control functions can be facilitated to a considerable degree by using PLA (programmable logic array) for the combinational logic circuit 101.

However, if a single state machine is applied to the entire external I/O device controller LSI, the numbers of input lines 103 and output lines 104 will have to be increased to a considerable extent in most cases, resulting in a combinational logic circuit 101 of a large size which is incapable of high-speed operation.

Therefore, for controlling an external I/O

device, the present invention employs a number of state machines to realize high speed operation.

More particularly, according to the present invention, PLA is used for the state machines to facilitate alterations in design, and the control functions are separately allotted to and executed by a plural number of state machines. In addition, according to the invention, operation management of a plural number of state machines is performed by a microprogram controller of a higher level from the standpoint of connection structure. The microprogram controller of the present invention has a microprogram stored in ROM (read-only memory) thereby to carry out necessary data processing in addition to the operation management of the state machines for enhancing the controller function.

Referring now to Fig. 2, there is illustrated a general structure of the integrated circuit controller according to the invention. The integrated circuit controller 201 (hereinafter referred to simply as "controller LSI") for external I/O device (not shown) is connected to the latter through a signal line 202 and to a computer system or a host machine (not shown) through a signal line 203. The controller LSI controls the

external I/O device according to a command from the host machine, and transfers data between the host machine and external I/O device.

According to the present invention, the structure of Fig. 2 is commonly applied in designing various types of controller LSI for the purpose of shortening the designing time. To this end, the basic universal structure is used in the designing processes of LSIs, e.g., in the processes of logic design, testing and layout design and the like.

The common structure of the invention allots the external I/O device control functions to a plural number of state machines 208 and 209 (FSM1 and FSM2). For addition of a control function, another state machine 210 (FSM3 in the example shown in Fig. 2) is added. In general, the state machine responds to an externally applied input in a period of one cycle of the driving clock, so that it is suitable for high-speed I/O control. If the driving clock of the state machine is in concordance with the driving clock of external I/O device, it becomes possible to provide high-speed control as the response of the state machine can be synchronized with the latter. In a case where the external I/O device is a disk drive or a communication

network, the external device is driven by different clocks in transmission and reception. Therefore, the state machine FSM1 for the receive control is operated on a receive clock ψ , and the state machine FSM2 for transmission control is operated on a transmission clock ψ' .

In a case where there is a large difference in data transfer rate between a host system and an external I/O device in transferring data therebetween or in a case where a host system takes time for preparation of data transfer, a data buffer 204 is provided in the controller LSI. Known random access memory or first-in first-out register is useful for the data buffer circuit.

In order to secure a structure which permits easy addition of a state machine for each control function of the external I/O device, the connection port is normalized in the present invention, while providing a microprogram controller (μC) 211 which has a function of allocating the start sequences of the state machines. Namely, the present invention employs an on-chip processor hierarchy having $\mu C211$ as a high-level processor and FSM 208 to 210 as low-level processors.

The connection port includes a data path and a

control path. The data path employs a known bus structure 205, while the control path includes three kinds of signals, i.e., FMS start signal to be sent from μ C through the signal line 206, FSM busy signal to be sent to μ C from a state machine on the signal line 206, and start signal 207 from one state machine to another state machine. Looking from the side of the microprogram controller μ C211, a start signal and a busy signal are addressed in a pair to each of the state machines 208 to 210.

The allocating function of μ C211 is now explained with reference to Fig. 3. The microprogram controller μ C is constituted by a processor including a known microprogram, a decoder for deciphering the microprogram and an execution circuit, issuing a command 301 to FSM1 through signal lines 205 and 206. Upon receipt of the command, FSM1 immediately starts execution and sets a signal FSM1BUSY which is generated in FSM1. After confirming by the microprogram function that FSM1BUSY = 1 and FSM2BUSY = 0, a signal which is generated in FSM2 (209), μ C issues a command 302 to FSM2 in a similar manner. Whereupon, FSM2 sets FSM2BUSY but does not start execution until it receives a start signal 207 from FSM1. The data from the external I/O

device has a time-series-like structure as indicated at 303, and on initiation of execution FSM1 finds an ID field 304 which identifies a data field. After detection of the ID field, FSM1 makes a judgment as to whether or not the ID field read from the external I/O device is in conformity with an ID information which has been given beforehand by the host system. If the result of judgment is affirmative, FSM1 terminates execution, clears FSM1BUSY, and starts FSM2.

FSM2 transmits the contents of data buffer 204 to the external I/O device in a time period corresponding to the DATA field 305 and in synchronism with the operation of the external I/O device.

In the time-series-wise control of the external I/O device, the control in a certain specific time region is handled by one state machine as described hereinbefore, facilitating the operation management of the state machines by μ C. It is easy to arrange the structure in such a manner as to allocate the state machine starting sequences by μ C, actually starting a state machine by an external I/O device or by another state machine. Further, depending upon circumstances, the state machines can be started directly by μ C. Accordingly, it becomes possible to eliminate mutual

interferences of the respective state machines, and facilitates the parallel design of state machines because they may operate independently. It also becomes easy to add a state machine or machines each for an intended function.

More particularly, state machines can be added by the following method. Namely, connection of a state machine is completed simply through a connecting port containing the two signals on the bus lines 205 and 206, and the signal line 207. On the other hand, the microprogram controller μC allocates the state machine starting sequences by issuing a command (e.g., 301) which starts a state machine in non-real time fashion relative to the external I/O device and a real time start command (e.g., 302). In Fig. 3, after issuing the command 302, μC is sensing FSM2BUSY. Accordingly, the above-described structure can control the added state machines simply by supplementing an allocating microprogram.

Since the state machines are driven by the clock signals which are supplied to the external I/O device, they are suitable for synchronized control. However, since the clock ψ of the external I/O device varies depending upon application, it is preferred that

the driving clock ψ of μC is independent of the clock Ψ . Therefore, control functions which do not require strict synchronism with Ψ or which involve executions of high level are realized by the use of μC . Examples of such functions include head positioning, data error correction, string search in input data and editing of input data in disk drive control functions.

As a storage means for the microprogram of the above-described μC , it is conceivable to use random access memory. However, in case of an integrated circuit which is intended for mass production, it is more convenient to store the microprogram in read-only memory (ROM) for eliminating the trouble of program loading and reducing the chip area. The integrated circuit can be remodeled for control of a different type of external I/O device by changing the microprogram in the ROM.

Reference is now had to Fig. 4 for explanation of the internal structure of the state machines. The command from μC is stored in register (REG) 401 through the data bus 205. At this time, a command issue signal is led to interface (IF) 413 through the signal line 206 to serve as a strobe signal for the register 401 and as a set signal for an R-S flip-flop 402. When the

contents of register 401 are same as the command 301, a programmable logic array (PLA) 403 with AND face 41 and OR face 42 transits its state upon receipt of the output of the flip-flop 402. On the other hand, when the contents of the register 401 are same as the command 302, the transit of state takes place when the output of the flip-flop 402 is ANDed with a start signal 207 of another state machine, which is ψ -synchronized by a synchronizing circuit 404, or with a start signal 405 from an external I/O device. The state is retained by master/slave registers (master register 410 and slave register 411). The output of OR plain 42 of PLA partly serves as a start signal 412 for other state machine and partly as an external I/O device control signal 406, and part of output signal 413 is applied to a control circuit 408 in the state machine. This control circuit 408 controls an executing unit 409. The executing unit 409 serves to transfer data between the external I/O device and μ C, or between the external I/O device and a data buffer memory. In a case where the external I/O device is a serial I/O device, for example, the contents of the executing unit 409 include serial/parallel conversion, parallel/serial conversion, detection/generation of specific pattern in input

string, detection/generation of address in data block such as a sector or packet, decode/encode of error detection code, and modulation/demodulation.

The above-mentioned state machine functions are allotted to a couple of state machines, and full duplex communication is feasible by assigning to the executing unit of one state machine the functions of serial/parallel conversion, detection of specific pattern, detection of address, decode of error detection code and demodulation and to the executing unit of the other state machine to functions of parallel/serial conversion, generation of specific pattern, generation of address, encode of error detection code and modulation. In this instance, the former state machine is driven by receive clock of the external I/O device, while the latter state machine is driven by transmit clock.

Shown in Fig. 5 is a layout pattern of the controller LSI according to the invention, which has the data buffer 501 located at one end of the chip since its capacity has to be changed depending upon the data transfer rate of the external I/O device or the like. On the other hand, the state machines 502 and 503 to be added according to the control functions are located at

the other end of the chip. The size of ROM 504 which stores the microprogram of μC is increased or reduced depending upon the intended control functions, so that the shape of the FSM which confronts the ROM is changed according to the shape of the ROM to eliminate the wasteful spaces which would otherwise result from changes in the ROM size. The executing circuit 505 of μC is used commonly for all of the controller LSIs without alterations. On the other hand, alterations in part of the state machine functions are realized by changing logics of PLA. It will be appreciated therefrom that manpower reduction is also possible even in the stage of layout design.

As stated hereinbefore, the individual state machines operate independently of each other. Therefore, the function test of a certain state machine by μC using the microprogram control is feasible irrespective of operations of other state machines, and, when a state machine is added, it suffices to add to μC a test program of the added state machine alone. With regard to the contents of test, it is suitable to employ the known scan path method.

It will be appreciated from the foregoing description that the controller LSI according to the

invention has a hierarchical structure including a microprogram controller and state machines, which permits to design controller LSIs for various external I/O devices in a short time period since additional state machines may be provided for additional external I/O control functions. The LSI structure of the invention can be effectively applied to LSI designs such as logic designs, layout designs and testing designs.

WHAT IS CLAIMED FOR PATENT IS:

1. An integrated circuit controller to be connected to an external I/O device, comprising:

a plural number of state machines driven by a clock signal driving said external I/O device as a clock source of the state machine;

a microprogram controller; and

a plural number of connecting ports connecting said state machines with said microprogram controller;

said controller having the functions of (1) reading a signal A indicating whether or not a state machine is busy and (2) issuing a start command to said state machine in response to said signal A to allocate the start sequences of said state machines;

said state machines having part or all of separate functions of (1) transiting the state thereof in response to a start signal B, (2) sending said controller said signal A indicating whether or not busy, and (3) transferring data to and from said controller in synchronism with said external I/O control device; and

said connecting ports consisting of a couple of control signal lines for said signals A and B and a data line for data transfer between said state machines and said controller.

2. The integrated circuit controller of claim 1, wherein the state transit functions of said state machines are realized by a programmable logic array, and the microprogram of said controller is stored in read-only memory.

3. The integrated circuit controller of claim 1, wherein said controller has at least one of functions of starting said state machines by issuing said signal B, controlling said external I/O device in such a manner as to permit off-line data transfer to and from said external I/O device, receiving data from said external I/O device through said state machines and sending same to a computer system after correction or other processing, and receiving data from a computer system and sending same to said external I/O device through said state machines after correction or other processing.

4. The integrated circuit controller of claim 1, wherein said start signal B for starting a state machine is dispatched from said controller, external I/O device or another state machine.

5. The integrated circuit controller of claim 1, wherein said external I/O device is a serial I/O device, a first state machine is driven by receive clock

of said serial I/O device, and a second state machine is driven by transmission clock of said serial I/O device, said first state machine having part or all of the functions of receiving and demodulating serial data from said serial I/O device, converting serial data into parallel form, detecting a specific pattern at the head of said serial data and the numbers allotted to succeeding data blocks and decoding error detection codes, and said second state machine having part or all of the functions of encoding error detection codes, generating a specific pattern at the head of serial data and numbers of succeeding data blocks, converting parallel data into serial form and modulating serial data for output to said serial I/O device.

6. The integrated circuit controller of claim 1, wherein a data buffer for temporarily storing data to be transferred between said controller and said state machines is located at one end on one face of an LSI chip, and said state machines are located at the other end, thereby facilitating increases or reductions in the buffer memory capacity as well as addition and deletion of a state machine or machines.

7. The integrated circuit controller of claim 1, wherein said controller has a function of testing

0185098

logic circuits in said state machines, adding or increasing testing microprograms according to the number of increased or deleted state machines.

FIG. 1

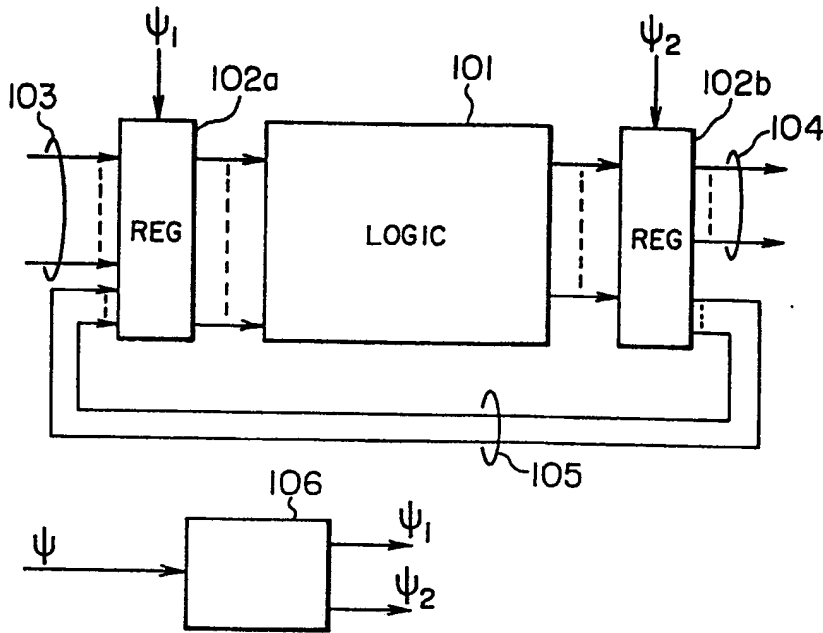


FIG. 5

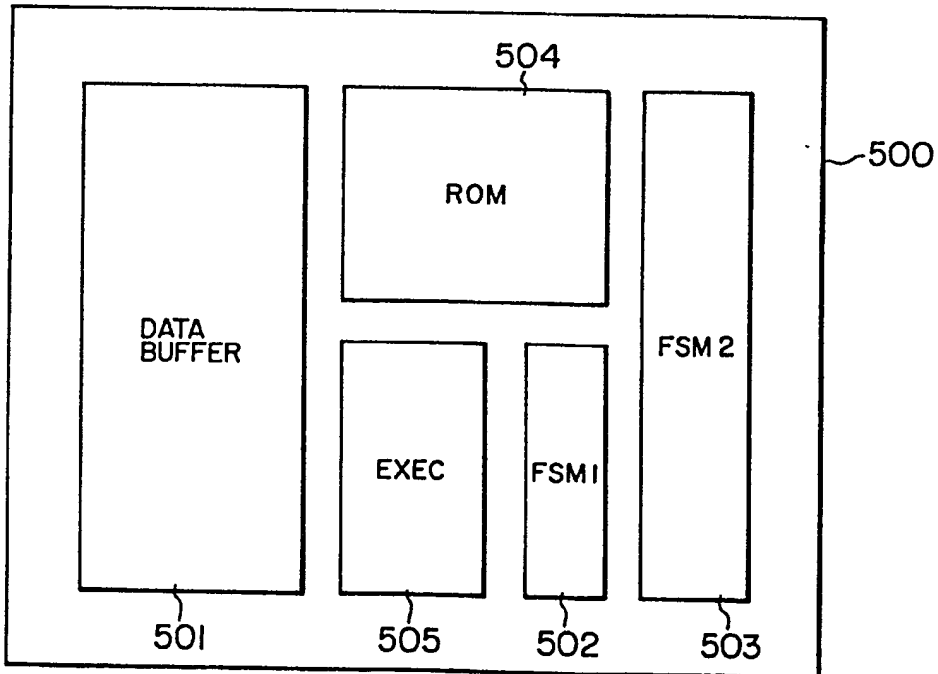


FIG. 2

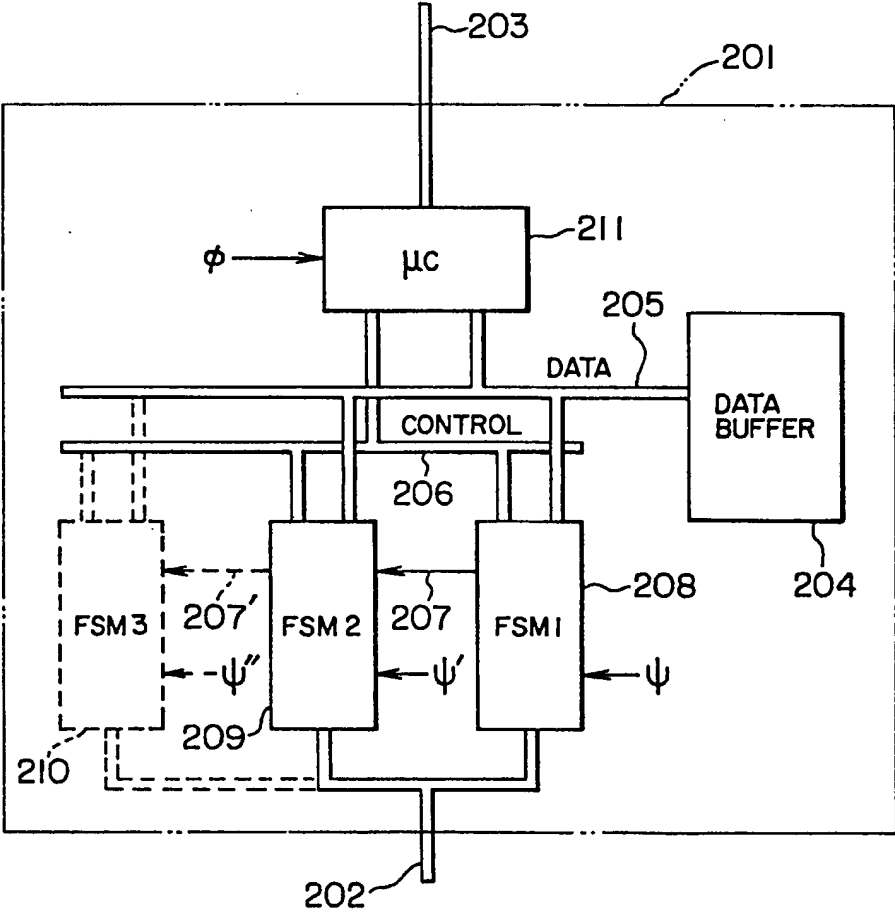


FIG. 3

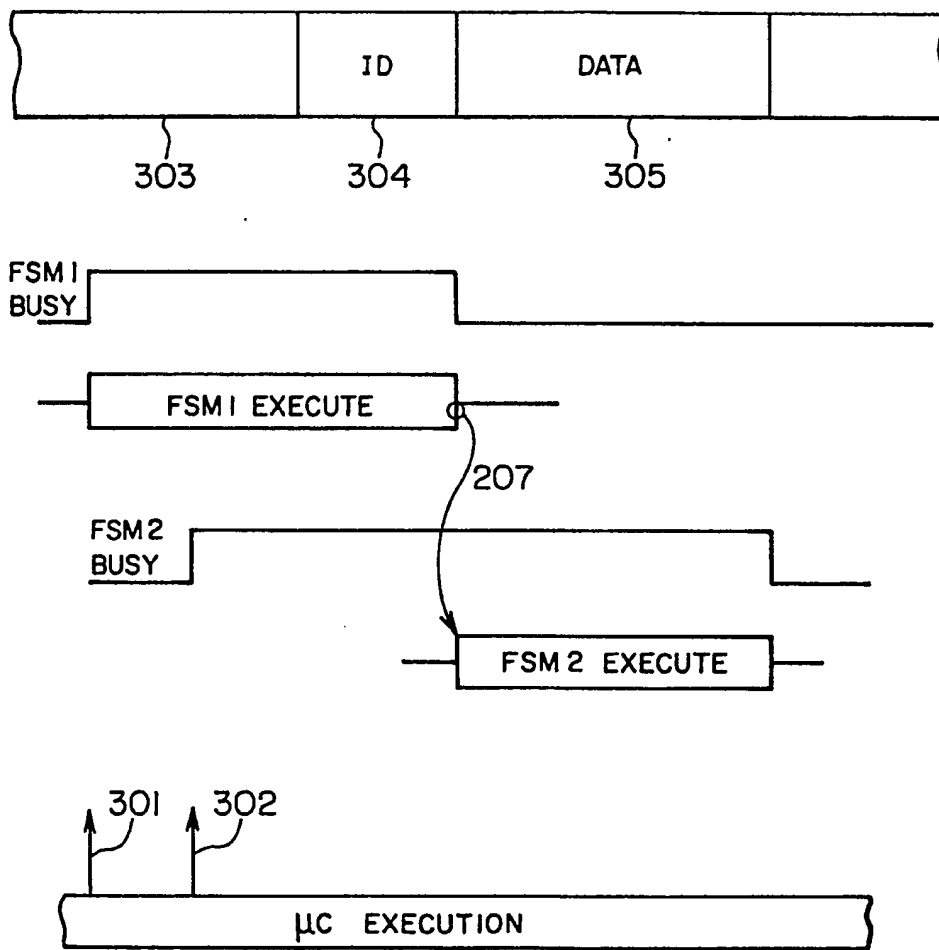
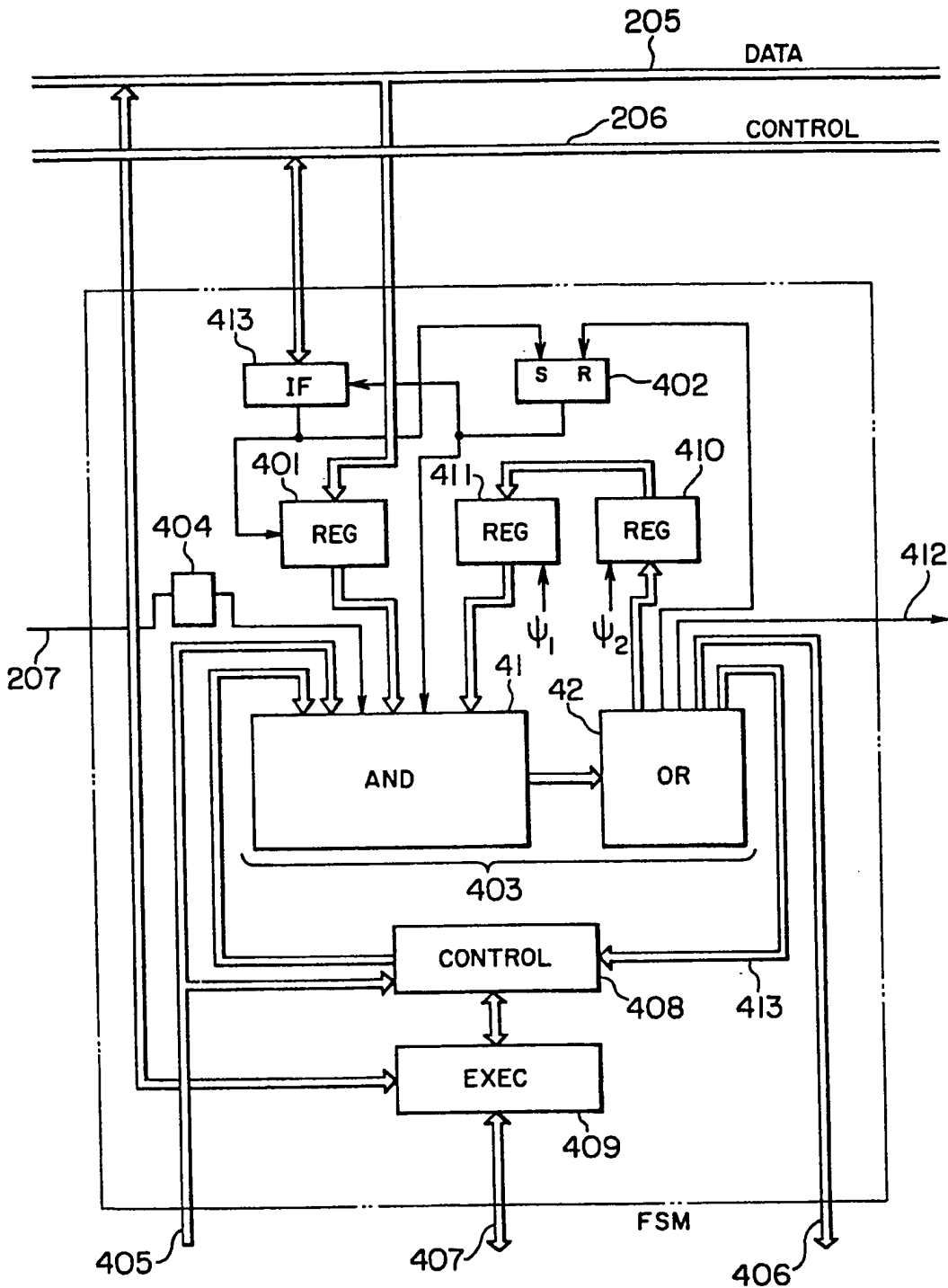


FIG. 4



INTERNATIONAL SEARCH REPORT

International Application No.

0185098
PCT/JP85/00298

I. CLASSIFICATION OF SUBJECT MATTER (If several classification symbols apply, indicate all) ¹				
According to International Patent Classification (IPC) or to both National Classification and IPC				
Int. Cl ⁴ G06F13/12				
II. FIELDS SEARCHED				
Minimum Documentation Searched ⁴				
Classification System	Classification Symbols			
IPC	G06F13/12, G06F9/22			
Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched ⁴				
Jitsuyo Shinan Koho		1956 - 1984		
Kokai Jitsuyo Shinan Koho		1971 - 1984		
III. DOCUMENTS CONSIDERED TO BE RELEVANT ¹⁴				
Category ¹⁵	Citation of Document, ¹⁶ with indication, where appropriate, of the relevant passages ¹⁷	Relevant to Claim No. ¹⁸		
A	JP, A, 51-40043 (Nippon Telegraph & Telephone Public Corporation) 3 April 1976 (03. 04. 76) (Family : none)	1 - 7		
A	JP, A, 51-98930 (Burroughs Corp.) 31 August 1976 (31. 08. 76) & DE, A1, 2505842 & FR, A1, 2262828 & CA, A1, 1017461	1 - 7		
<p>¹⁴ Special categories of cited documents: ¹⁵</p> <table style="width: 100%; border: none;"> <tr> <td style="width: 50%; border: none;"> <p>"A" document defining the general state of the art which is not considered to be of particular relevance</p> <p>"E" earlier document but published on or after the international filing date</p> <p>"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)</p> <p>"O" document referring to an oral disclosure, use, exhibition or other means</p> <p>"P" document published prior to the international filing date but later than the priority date claimed</p> </td> <td style="width: 50%; border: none;"> <p>"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention</p> <p>"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step</p> <p>"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art</p> <p>"Z" document member of the same patent family</p> </td> </tr> </table>			<p>"A" document defining the general state of the art which is not considered to be of particular relevance</p> <p>"E" earlier document but published on or after the international filing date</p> <p>"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)</p> <p>"O" document referring to an oral disclosure, use, exhibition or other means</p> <p>"P" document published prior to the international filing date but later than the priority date claimed</p>	<p>"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention</p> <p>"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step</p> <p>"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art</p> <p>"Z" document member of the same patent family</p>
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IV. CERTIFICATION				
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July 31, 1985 (31. 07. 85)	August 12, 1985 (12. 08. 85)			
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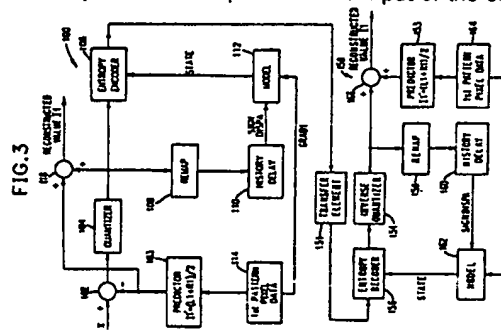
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Compression and decompression of column-interlaced, row-interlaced graylevel digital images.

In an image in which some pixels in some rows of an image have values associated therewith, apparatus and method of processing, for subsequent entropy coding or decoding, graylevel data for the remaining pixels in the image. A compressor (300) includes a graylevel model (302) and an entropy encoder (304). One input of the encoder (304) corresponds to the quantized value and its second input represents the state which points to a specific probability in a table of probabilities used to define decision context. The compressed data is communicated via a transfer element (306) to a decompressor (101) including an entropy decoder (312) which operates in an invers fashion to entropy encoder (304). A graylevel model (314) provides a state input to the decoder (312) pointing the decoder to the same probability entry in the probability table as is pointed too in the encoder (304) during the compression. From the compressed data and the state input the entropy decoder (312) provides an output to the graylevel model element (314) which corresponds to the graylevel model (302) and is thereby able to generate an output that corresponds to the input of the compressor (300).

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COMPRESSION AND DECOMPRESSION OF COLUMN-INTERLACED, ROW-INTERLACED GRAYLEVEL DIGITAL IMAGES

The present invention relates to the compression of gray-level data images.

In many applications, an image is to be communicated rapidly or is to be contained in limited storage. Typically, the image is partitioned into numerous picture elements to facilitate the processing of image data. A picture element is typically referred to as a "pixel" or "pel". Generally, the image is defined as m lines of n pixels/line. Collectively, the lines of pixels represent the image. Each pixel may be white or black, or may have a graylevel (or grayscale) value associated therewith. The binary or multilevel data is normally provided in digital form, which facilitates communication and storage thereof.

One way of representing the information contained in an image is to scan the pixels line-by-line and provide the value for each pixel. For example, suppose the upper left pixel is identified as $X_{1,1}$ where the first subscript corresponds to the line number and the second subscript corresponds to the pixel in the line. The second pixel in the first line is then $X_{1,2}$. If there are 480 lines and 512 pixels/line, an image for a given instant can be represented by information gathered by scanning the 480×512 pixels.

In a graylevel image, each pixel has a graylevel value assigned thereto, ranging between a black value (e.g., 0) and a white value (e.g., 255). That is, given 8 bits, the graylevel of a pixel can have any of 256 values. Proceeding line-by-line, an image can be represented by the successively recorded values of pixels $X_{1,1}, X_{1,2}, \dots, X_{480,512}$.

Typically in the past, a top-to-bottom scan of the image has been referred to as a "field" and a plurality of fields have been interlaced to form a "frame". For example, one field may comprise the odd-numbered lines which are scanned first and a second field may comprise the even-numbered lines which are scanned thereafter. The two fields together form a single "frame".

The above straightforward approach results in a large number of bits required for each image to be recorded. The large number of bits can make the storing and/or rapid conveying of data impractical where storage space is limited or rapid data transfer is required. It is thus desirable to reduce, or compress, the number of bits required to represent the graylevel data.

To address the problem of reducing the number of required bits, a number of data compression techniques have been taught.

One technique of data compression is referred to as "entropy coding". In entropy coding, the number of bits used in representing events is intended to be inversely related to event probability. More probable events are represented by code-words characterized by a relatively short length (of bits) whereas less probable events are represented by relatively longer lengths.

To perform entropy coding, an entropy coder typically receives two inputs. The first input is a decision and the second input is a state input which provides a context for the decision input. For example, a binary decision input may represent a heads or tails event for a coin toss; or an ON or OFF condition for a switch; or a 1 or 0 value of a bit in a string. The state input --usually based on history, theory, or estimate--provides some contextual index for the decision input. For example, in an image in which a pixel may be either black or white, different neighborhoods of the image may have different likelihoods of a pixel therein being white. That is, each neighborhood has a respective estimated black-white probability ratio associated therewith. Hence, to provide meaning to the decision input, a state input is furnished to reflect the neighborhood corresponding to the decision input. Based on the state input, the entropy coder transforms the decision input into a code-word of appropriate length.

The state input to the entropy coder is the result of modelling, i.e. defining the contexts in which code-words are assigned to decisions. A well-known example of modelling involves Markov states. The compression of the entropy encoder depends on the quality of the modelling --that is, how well the state input to the entropy coder represents the actual decision context, e.g. the decisional probability given the context neighborhood.

The correct assignment of code-word lengths is dictated by information theory concepts and is based on the estimated probability of occurrence of the possible decision outcomes. The better the probability estimate, the more efficient the code-word length assignment, and the better the compression.

One example of an entropy coder is described in detail in co-pending patent applications:

"ARITHMETIC CODING DATA COMPRESSION/DE-COMPRESSION BY SELECTIVELY EMPLOYED, DIVERSE ARITHMETIC CODING ENCODERS AND DECODERS", invented by J. L. Mitchell and W. B. Pennebaker, U.S.S.N. 06/907,700; "PROBABILITY ESTIMATION BASED ON DECISION HISTORY", invented by J. L. Mitchell and W. B. Pennebaker, U.S.S.N. 06/907,695; and "ARITHMETIC CODING

ENCODER AND DECODER SYSTEM" (Q-coder), invented by G. G. Langdon, Jr., J. L. Mitchell, W. B. Pennebaker and J. J. Rissanen, U.S.S.N. 08/907,714.

The invention disclosed in the above-cited co-pending patent applications were invented by the present inventors and co-workers thereof at, and are all assigned to, the IBM Corporation; said applications being incorporated herein by reference for their teachings involving entropy coding, or more specifically arithmetic coding and adaptive probability estimation.

Other entropy coders include Huffman coding coders and Elias coding coders. Numerous publications describe such coding approaches.

Another technique used in data compression is referred to as "Differential Pulse Code Modulation" (DPCM), which is a form of "predictive coding". According to basic DPCM teachings, a predicted value based on one or more neighboring pixel values is determined for a "subject" pixel --i.e., a pixel whose informational content is currently being coded. The difference between the value for the subject pixel and the predicted value is then used as a basis for subsequent coding. Where there is high correlation between nearby pixels, using the difference value rather than the actual graylevel value can result in significant compression. Typically, a factor-of-two compression can be achieved by using predictive coding techniques to obtain reasonably good quality pictures.

A patent application filed by the present inventors and also assigned to IBM Corporation, USSN 946542, filed December 22, 1986, relates to an "Adaptive Graylevel Image Compression System" in which the DPCM prediction error is quantized and entropy encoded. The apparatus and method set forth therein may be used in coding values for all pixels in an image. Alternatively, however, the method may be applied to coding just pixels where alternate rows and alternate columns intersect. Such pixels may represent a first pattern which is interlaced with another pattern to form the complete image. A pixel X in the first pattern has a pixel A to the left thereof (in said first pattern); a pixel B to the upper left diagonal (in said first pattern); a pixel C adjacent and above (in said first pattern); and pixel D to the upper right diagonal (in said first pattern). From data derived from pixels A,B,C, and D, data for pixel X is determined. By processing successive pixels in a line, one-line-after-another in the first pattern, all pixels in the first pattern are coded.

In U.S. Pat. No. 4488174, an approach is proposed in which one field of alternate lines of an image (frame) is encoded from data derived during the prior encoding of pixels in the other field. That is, the algorithm encodes pixels in the "missing" rows.

The encoding of pixels in the missing rows and missing columns --which result from processing pixels in the first pattern discussed hereinabove--is not disclosed by any known prior or contemporaneous technology.

The present invention involves apparatus and method for coding and decoding data relating to the pixels not contained in the first pattern (as described hereinabove).

Moreover, the present invention extends to the coding and decoding of pixels not contained in a first pattern of previously coded pixels, wherein the first pattern includes, generally, some pixels in some rows. For example, rather than alternate pixels in alternate rows, the first pattern may include every fourth pixel in every eighth row.

That is, in an image in which some pixels in some rows --e.g., pixels at the intersections of alternate rows and alternate columns--have previously defined graylevel values associated therewith, the present invention provides apparatus and method for efficiently encoding the values of the remaining (uncoded) pixels. More particularly, the invention features a two-stage algorithm: the first stage being used to encode quantized prediction errors for pixels in rows which include previously encoded first pattern pixel values; and the second stage being used to encode prediction error values in rows having no first pattern pixels therein.

In accordance with the invention, data compression is achieved --at least in part--by employing an entropy encoder. A quantized prediction error for each pixel represents the decision input to the entropy encoder. The state input, which defines a context for the quantized value, is generated according to a model. The first stage and the second stage each include respective models for generating state inputs for the pixels processed thereby.

For each pixel to be encoded thereby, the first stage generates a state input based on (a) a horizontal gradient (magnitude) value GRAD1 and (b) a sign value derived from the quantized value of a previously encoded pixel in a row processed earlier in the first stage. For each pixel encoded thereby, the second stage generates a state input based on (a) a vertical gradient (magnitude) value GRAD2 and (b) a sign value derived from preferably the quantized value of the left adjacent pixel. The second stage uses (re-constructed) graylevel values generated during the first stage as well as pixels from the first pattern.

For a preferred embodiment in which the first pattern of pixels form a quarter resolution image by including alternate pixels in alternate rows, first pattern pixels have graylevel values corresponding

therewith. The graylevel values may be the original values or may be the result of a re-construction process. The first stage of the present algorithm generates --by simple linear interpolation--prediction error values for the "missing" pixels in the half resolution rows. The prediction error, or difference, values are quantized and compressed using entropy coding techniques. By adding the quantized difference value for each "missing" pixel with the predicted value thereof, the first stage produces a re-constructed graylevel value for each "missing" pixel in a row containing first pattern pixels. After re-constructing "missing" pixel values, the image has full resolution in alternate rows and has half-resolution in the vertical direction (every other row is "missing"). In the second stage, data for the missing rows is generated and compressed using entropy coding techniques. The prediction and compression stages used in bringing the original half-resolution image into a full resolution image are symmetrical in the horizontal and vertical directions.

Where pixels at the intersections of alternate rows and alternate columns of an image have been previously coded, the present invention provides apparatus and algorithm for coding and decoding graylevel-related data for the remaining pixels in the image.

Similarly, where other arrangements of pixels form the first pattern, the coding and generating of re-constructed values for the remaining pixels is provided.

In particular, the present invention features a unique apparatus and method of coding and re-constructing values for previously uncoded (missing) pixels which are in rows that contain previously coded pixels in a first pattern, wherein the coding involves generating state inputs for entropy coding. Also, the present invention features a unique apparatus and method of coding values in rows that contain no previously coded first pattern, wherein the coding involves generating state inputs for entropy coding.

As suggested hereinabove, the present invention achieves the object of supplying decision input and state (i.e., decision context) input to an entropy encoder (and decoder) to enable data compression (and decompression).

The invention is also directed to data compression and decompression which features entropy encoding and decoding wherein the encoder and decoder each receive state inputs determined according to the two-stage algorithm previously described. In this regard, the algorithm for decompressing compressed data is essentially the same as the algorithm for compressing data, except that the compressor employs a quantizer before entropy encoding and the decompressor employs a corresponding inverse quantizer after entropy decoding.

Accordingly, for a graylevel image formed of (i) a first matrix pattern which includes all pixels at the intersections of alternating rows and alternating columns of pixels in the image and (ii) a second matrix pattern which includes the remaining pixels, wherein each pixel in the first pattern has a value which has been previously coded, a preferred compressor for image data in the second pattern comprises: (a) means for entropy encoding a digital decision input based on a state input which defines a context for the digital decision input; (b) first means for predicting a value $I1'$ for a previously uncoded pixel $i1$ in a row containing first pattern pixels, wherein $I1' = (L1 + R1)/2$ where $L1$ and $R1$ are values for previously coded pixels which are, respectively, to the left and right of pixel $i1$; (c) first subtractor means for computing a difference value between the input value $X1$ for pixel $i1$ and the predicted value $I1'$ for pixel $i1$; (d) first means for quantizing the difference value, the quantized value corresponding to a decision input to said entropy encoder means; (e) first means for generating a sign history value for pixel $i1$ as the arithmetic sign of the quantized difference value previously determined for the pixel vertically above and one pixel away from pixel $i1$; (f) first means for generating a horizontal gradient value for pixel $i1$ based on the difference between values of a pixel to the left and a pixel to the right of pixel $i1$; (g) first means for combining the horizontal gradient value and the sign history value to provide a state input to said entropy encoding means for pixel $i1$; and (h) second means for predicting a value $I2'$ for a previously uncoded pixel $i2$ in a row containing no first pattern pixels, wherein $I2' = (A2 + B2)/2$ where $A2$ and $B2$ are previously coded pixels which are, respectively, vertically above and below pixel $i2$; (j) second subtractor means for computing a difference value between the input value $X2$ of pixel $i2$ and the predicted value $I2'$ of pixel $i2$; (k) second means for quantizing the difference value, the quantized value corresponding to a decision input to said entropy encoder means; (l) second means for generating a sign history value for pixel $i2$ as arithmetic sign of the quantized difference value previously determined for the pixel coded immediately before and in the row containing pixel $i2$; (m) second means for generating a vertical gradient value for pixel $i2$ based on the difference between values of a pixel vertically above and below pixel $i2$; and (n) second means for combining the vertical gradient value and the sign history value to provide a state input to said entropy encoding means for pixel $i2$. A preferred corresponding decompressor includes: (a) entropy decoder means for generating output decisions which correspond to the digital decision inputs to the encoding means; and (b) decoder model means for generating state inputs as successive decisions are decoded by said entropy decoding means; said entropy decoder means generating output decisions in response to the inputting

thereto of (i) compressed data generated by the entropy encoding means and (ii) state inputs from the decoder model means.

The present invention also features a two-dimensional sampling pattern of an image.

The invention achieves the above objects while maintaining high compression rate with good image
5 quality.

One way of carrying out the invention is described below with reference to the drawings.

FIG.1 is a diagram showing, for a preferred embodiment, (i) pixels in a first pattern which have been previously coded; (ii) a pixel i_1 being processed in the first stage of the algorithm of the present invention; and (iii) pixels that are to be processed in the second stage of the algorithm of the present invention.

FIG.2 is a diagram showing pixels involved in coding a pixel i_2 during the second stage of the algorithm for the preferred embodiment.

FIG.3 is a block diagram of elements employed in implementing the first stage of the algorithm for the preferred embodiment, which involves compressing the data of pixels located in rows that include previously coded and re-constructed first pattern pixel values. Also included in this figure is a corresponding decompressor which decompresses entropy encoded compressed data.

FIG.4 is a block diagram of elements employed in implementing the second stage of the algorithm for the preferred embodiment, which involves compressing the data of pixels located in rows that do not include first pattern pixels. Also included in this figure is a corresponding decompressor which decompresses entropy encoded compressed data.

FIG.5 is an illustration showing a tree structure used in converting a multivalued graylevel into a binary stream which can be encoded by a binary arithmetic coding encoder.

FIG.6 is a block diagram which generally illustrates graylevel modelling and entropy coding operating in combination.

FIG.7 is a flowchart illustrating the encoding, or data compressing, portion of the invention.

FIG.21 is a flowchart illustrating the decoding, or data decompressing, portion of the preferred embodiment.

FIGS.8 through 20 and 22 through 26 are flowcharts illustrating processes embodied within the encoder or decoder portions of the preferred embodiment.

Referring to FIG.1, a plurality of pixels in an image are shown. Typically, an image includes a frame of
30 480 lines with 512 pixels/line with each pixel having an 8-bit graylevel value. The present invention is directed to reducing the number of bits required to represent the graylevel values of the pixels in the image.

In FIG.1, a number of pixels are shown with a hatched representation. These pixels (with hatched representation) are located at intersections of alternate rows and alternate columns of pixels. Together these pixels form a first pattern of pixels which portray the image with half-resolution both vertically and
35 horizontally. Each pixel in the first pattern has been previously encoded and a re-constructed value therefor has been determined.

The present invention is directed to coding the remaining pixels (which do not have hatched representation). Pixel i_1 is a sample subject pixel which is to be processed in the first stage of the algorithm of the present invention. The pixel to the left of pixel i_1 --which has a value L_1 --and the pixel to the right of pixel i_1
40 --which has a value R_1 --are first pattern pixels and have been previously coded, and a re-constructed value for each has been previously determined.

The previous processing of the pixels in the first pattern may have been performed according to the teachings of the aforementioned co-pending patent application or according to teachings set forth in an article entitled: "Conditional Variable Length Coding for Graylevel Pictures," by Gharavi, AT&T Bell Labs
45 Technical Journal, 63, pp.249-260, 1984.

Still referring to FIG.1, a pixel A_1 is shown vertically above pixel i_1 one pixel away. The row immediately above and immediately below the pixel i_1 include pixels (marked with a "2") which are to be processed during the second stage of the algorithm.

In FIG.2, a pixel i_2 is shown as a sample pixel which is processed during the second stage of the present algorithm. Pixel i_2 is in a row of pixels, none of which have hatched representation. To the left of pixel i_2 is pixel with value L_2 ; directly above is a pixel with value A_2 ; and directly below is a pixel with value B_2 . Pixels with respective values A_2 and B_2 are processed during the first stage of the algorithm (prior to the second stage). It is observed that pixel of value L_2 has been processed in the second stage just before processing of pixel i_2 commences. (The pixels involved in the earlier processing of pixel with value L_2 may
50 be envisioned by sliding each of the four pixels i_2 , L_2 , A_2 , and B_2 one pixel position to the left -- A_2 and B_2 in such case representing pixels processed in the first pattern.) It is noted that the same variable, e.g. L_1 , L_2 , R_1 , A_1 , and B_2 may represent the pixel or the value of the pixel. The meaning of the variable will be clear from context.

Referring now to FIG.3, a specific data compression system 100 for implementing the first stage is shown. The graylevel value X for pixel i1 enters a subtractor 102 together with a predicted value I1' = (L1 + R1)/2 from predictor element 103. The difference value (X-I1') enters a quantizer 104. The quantizer 104 assigns the difference value to one of a plurality of predefined quantization levels. A preferred quantization table is set forth below in Table 1.

TABLE 1

QUANTIZATION TABLE

Prediction difference	Binary stream	Quantized value	
from	to	QDIF	
		EX	
-256	-105	hex ff	-112
-104	-89	hex fe	-96
-88	-73	hex fc	-80
-72	-57	hex f8	-64
-56	-41	hex f0	-48
-40	-25	hex e0	-32
-24	-13	hex c0	-18
-12	12	hex 00	0
13	24	hex 40	18
25	40	hex 60	32
41	56	hex 70	48
57	72	hex 78	64
73	88	hex 7c	80
89	104	hex 7e	96
105	255	hex 7f	112

The column under "binary stream" is described hereinbelow. EX represents the quantized value of input pixel difference.

The quantization value (or level) serves as an input to an entropy encoder 106. The entropy encoder 106 may include the Q-Coder described in the afore-mentioned co-pending patent application or may include any of various known arithmetic coders (e.g. Huffmann coders or Elias coders) or other coders which, given a state input and a decision input, provide an output having a length based on the probability of the decision outcome.

The output of the quantizer 104 also enters a remap element 108. The remap element 108 evaluates whether the quantized output has a "sign" of zero, -, or +. A history of remapped sign values is contained in a delay 110. The remapped value for pixel A1 --zero, negative, or positive--is assigned a corresponding SIGNDISPA value of hex 000, hex 040, or hex 080. The value of SIGNDISPA enters a model element 112.

A second input also enters the model element 112. In particular, from data corresponding to pixels in the first pattern (of hatched pixels), a gradient value for pixel i1 is determined. The gradient is defined as:
 $Gradient = I1' - L1 = (R1 - L1) / 2$

The gradient value is re-mapped to one of four values, GRAD1(x), according to the following table, where $x = \text{abs}(I1'-L1)$:

Table 2

	Input x	GRAD (x)
5		
10	0 to 12	hex 00
	13 to 24	hex 10
	25 to 40	hex 20
15	41 to 128	hex 30

The above definition of GRAD1(x) has been chosen so that 16 bytes (hex 10) will separate the beginning of the statistics for different contexts or states. This separation allows for storage of the statistics of four binary decisions in the Q-coder described in the co-pending application; these decisions correspond to the four topmost decisions in the binary tree described hereinbelow.

It is noted that the predicted value I1' is used in the gradient calculation. The I1' value, which is derived from data stored in the first pattern image data store 114, thus serves a dual purpose and reduces computation requirements. It is also noted that, because the resulting gradient is half the value of (R1-L1), the GRAD1(x) look-up-table is halved in size.

The value GRAD1(x) and SIGNDISPA are concatenated by the model element 112 to form a state input for the entropy encoder 106. Taken together, the four GRAD1(x) possible values and the three possible SIGNDISPA values provide 12 possible state inputs to the entropy encoder 106. The model 112 may thus be viewed as a 12-state Markov-type model which uses the magnitude of the gradient computed from the left and right neighboring pixels, together with arithmetic sign history information, to define decisional context (i.e., the state input) for entropy coding.

Still referring to FIG.3, it is noted that a re-constructed value for pixel i1 is computed by combining the predictor value I1' and the quantized value in summing element 116. The sum is clipped as appropriate to maintain a value within the range of values between 0 and 255. The re-constructed values (which approximate the original graylevel values) are used in second stage computations.

In FIG. 3, a first stage decompressor 150 is also illustrated. The compressed output from first stage compressor 100 enters the first stage decompressor 150 via a transfer element 151. The transfer element 151 includes a communication medium and may include a storage medium. The first stage decompressor 150 includes an inverse quantizer 154 and entropy decoder 156.

The entropy decoder 156 decodes a QDIF value (in Table 1) given the compressed data and state inputs thereto. The inverse quantizer 154 converts QDIF to a corresponding EX value (also in Table 1). The other elements of the decompressor 150 are functionally the same as their counterparts in the compressor 100. Elements 103, and 108 through 116 correspond respectively to elements 153 and 158 through 166.

It will be noted that the re-constructed value may differ from the input value, due to error which may be introduced due to the quantization step. When the input graylevel varies from the re-constructed value, the compression is referred to as "lossy". The amount of loss is determined by the quantization table. When each difference value is mapped to itself in the quantization table, there is zero lossiness. On the other hand, the more difference values allocated to each quantization level, the greater the degree of lossiness. The present invention is applicable to zero loss and lossy compression.

Referring to FIG.4, a data compression system 200 implementing the second stage of the algorithm is illustrated. The graylevel value for pixel i2 (see FIG.2) is shown entering a subtractor 202. A predicted value I2' produced by a predictor 203 according to the expression $I2' = (A2 + B2)/2$ is subtracted from the value X, the difference (i.e., the prediction error) serving as input to a quantizer 204. The values combined in the predictor 203 are entered from storage 205. Storage 205 contains re-constructed values for pixels previously processed, e.g. A2, B2, and L2. Re-constructed values for the second stage are generated by combining the quantizer output with the predictor output in a summer 207. The output of the summer 207 is a re-constructed value I2 for pixel i2.

The quantizer 204 operates like quantizer 104 and may include the same quantization values as in

Table 1.

As in FIG.3, the compression system 200 of FIG.4 provides the quantized values to an entropy encoder 206. A state input to the entropy encoder 206 is furnished by a model element 208. A first input to the model element is GRAD2(x) which is defined as a "vertical" gradient relative to pixel i2. In the present embodiment, the gradient is $(I2'-A2)$. As discussed with reference to the gradient value in FIG.3, the gradient value in system 200 is re-mapped to a fewer number of values GRAD2(x) based on Table 2. GRAD2(x) provides a one out of four possible input values to the model element 208.

The other input to the model element 208 is determined by means of a re-map element 210 and a 1-pixel delay element 212. The re-map element 210 preserves the sign value of the quantized value output from the quantizer 204. Either a zero, -, or + value is assigned. The 1 pixel delay serves to store the re-mapped value for the previously processed pixel in the row, i.e. pixel L2. The three sign values are defined as hex 000, hex 040, and hex 080, respectively. The appropriate hex value is supplied to the model element 208 as SIGNDISPL. The state input may be the concatenation of GRAD2(x) and SIGNDISPL.

In practice, however, the sign value (i.e. SIGNDISPA or SIGNDISPL depending on stage) and GRAD value (i.e., GRAD1 or GRAD2 depending on stage) are added. For each stage, the sign values and GRAD values thereof are defined so that the adding of a given sign value and a given GRAD value provides a unique sum, the unique sum representing an address to corresponding state input statistics.

Also in FIG. 4, a second stage decompressor 250 is illustrated. The compressed output from second stage compressor 200 enters the second stage decompressor 250 via a transfer element 251. The transfer element 251 includes a communication medium and may include a storage medium. The second stage decompressor 250 includes an inverse quantizer 254 and entropy decoder 256.

The entropy decoder 256 decodes a QDIF value (in Table 1) given the compressed data and state inputs thereto. The inverse quantizer 254 converts QDIF to a corresponding EX value (also in Table 1). The other elements of the decompressor 250 are functionally the same as their counterparts in the compressor 200. Elements 203, 205, and 207 through 212 correspond respectively to elements 253, 255 and 257 through 262.

Referring again to Table 1, the binary stream QDIF is now discussed in more detail. It is observed that the prediction difference is quantized into one of 15 possible levels allowed by the quantization table.

The entropy encoder (106/206) must then assign different code words to each one of these quantization levels, such that the code words are uniquely decodable. If the entropy encoder is a binary arithmetic coder as described in the aforementioned Q-Coder patent application, multilevel data must be converted into binary data to enable the entropy encoder (106/206) to process it.

The binary decision tree shown in FIG.5 is used to achieve this conversion. The binary sequence that represents a given quantization level is determined by following the tree from the root down to the corresponding leaf. If the left branch is followed, a "zero" is encoded; otherwise a "one" is encoded.

Each state normally has associated with it a separate tree. This means that probability distributions associated with trees corresponding to different states are estimated separately. Furthermore, within each tree (or state), each binary decision should be estimated separately from other binary decisions. These requirements could translate into separate storage allocations for the statistics of each one of the nodes in each tree. However, in the present implementation, some decisions have been consolidated and are represented by "common statistics" under a single statistic or storage cell, regardless of the state. This last feature reduces the storage requirements to four binary decisions per tree with a minimal impact, if any, on compression. The common statistics are shown in FIG.5.

The tree of FIG.5 is not required when the entropy encoder 106/206 is capable of processing multilevel decision inputs.

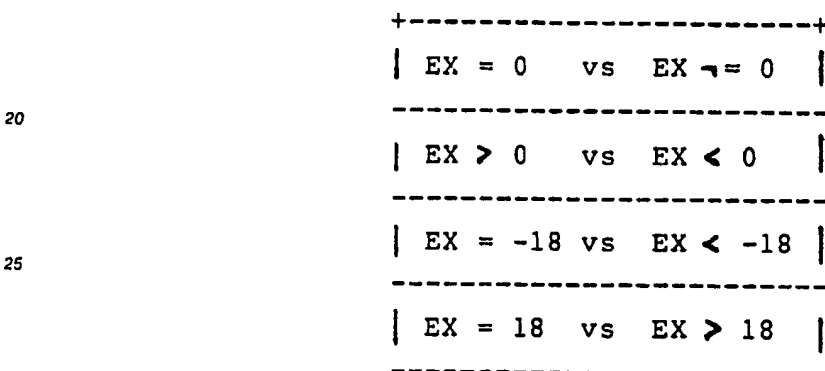
Table 1 shows a hexadecimal code for the binary decision stream, which can be used for efficiently traversing the decision tree. In the present embodiment, the value of QDIF is loaded into a byte-size register which is then tested to encode the decision 0 versus not 0. If the result is not zero, the most significant bit of the binary stream is tested for the occurrence of a positive sign (0) or a negative sign (1). Shifting this register to the left by two bits leaves the binary representation of the remaining decisions of the tree. By sequentially examining the most significant bit (the sign of the register contents) and shifting the register to the left by one, the tree is traversed. A leaf is reached whenever a zero (a nonnegative sign in the register) is encountered.

Referring to FIG.6, the data compression and decompression aspects of the invention are shown. Specifically, the compressor 300 is shown to include a graylevel model 302 and an entropy encoder 304. The compressor 300 includes the elements of FIGS. 3 and 4. The YN line to the encoder 304 corresponds to the quantized value (in binary form) which enters the entropy encoder 106/206 (of FIG.3 and FIG.4). SP is the state input which, in the present embodiment, points to a specific probability in a table of probabilities

used by the entropy encoder 106/206 to define decision context. The compressed data from the compressor 300 is communicated (with or without intermediate storage) via a transfer element 306 to decompressor 310. The decompressor 310 includes an entropy decoder 312 which operates in inverse fashion to entropy encoder 304. A graylevel model 314 provides a state input to the decoder 312, pointing the decoder to the same probability entry in the probability table as is pointed to in the encoder 304 during encoding. From the compressed data and the state input, the entropy decoder 312 provides a binary output YN to a graylevel model element 314. The graylevel model element 314 corresponds to the model 302, and is thereby able to generate output DATAOUT that corresponds to the DATAIN which enters the compressor 300.

The above-described system has been implemented in both the IBM S370 and the IBM PC-AT. The statistics area used in coding the quantized prediction difference consists of 12 contiguous cells, each corresponding to a given state or context. Each cell has 16 bytes of storage assigned to the statistics of four binary decisions; they correspond to the four topmost nodes in the decision tree of FIG.5. The following diagram, in which each box represents a 4-byte unit, illustrates this structure:

15



30

Other binary decisions in this tree are computed using a single 4-byte statistic area common to all states (STATBITSLEFT). In the following text and charts, the 4-byte statistics unit that is to be used by the entropy encoding unit (e.g., the Q-coder) is always pointed by the pointer SP.

To aid in the discussion of the flowcharts according to figures 7 to 26, a list of definitions is set forth below.

CODEYN Binary decision encoder

YN YN=0 means 0 was decoded. YN=1 means a 1 was decoded.

40

SP Pointer used for the statistics of the current binary decision.

STAT1 Statistics storage area for the first stage processes (GSE1A and GSD1A).

STAT2 Statistics storage area for the second stage processes (GSE2A and GSD2A).

STATBITSLEFT Storage for common statistic binary decisions.

HP Pointer used for the original pixel data. All other history and re-constructed lines are at a fixed displacement from this pointer (i.e., I1, R1, L1, A2, B2, L2, SIGNDISPA, etc.)

BUFF1 Input buffer contains a line of original pixels

LSIZE1 Size of input first stage line

55

LSIZE2 Size of input second stage line

TEM Temporary register used in intermediate ALU operations

TPOINTER Temporary pointer used to access look-up-tables

DLUT Look-up-table used in the encoder's evaluation of QDIF (see Table 1)

5

GLUT Look-up-table used in the evaluation of GRAD --GRAD1 or GRAD2

QLUT Look-up-table used in the evaluation of EX (see Table 1)

10 MASK Temporary variable used in the decoder's evaluation of QDIF.

X Input pixel value for either stage

I' Interpolated predicted value of the input pixel

15

I Re-constructed value for the input pixel

Bold lettering in the flowcharts indicates that a more detailed flow chart can be found elsewhere. Identical processes for encoder and decoder are often given in bold lettering and explained in a separate figure (even when it is just a simple calculation) to emphasize the commonality. All multiplications (*) and divisions (/) are by powers of two; they are implemented with the appropriate shifts to the left or right (SLL or SRL). Flowcharts for similar functions (with implementation variations) are shown in sequence.

FIG.7 shows the basic structure of the compression (encoding) portion of the present graylevel compression/decompression system. The encoder process is labelled as EMAIN. After any required setup and initialization operations, the first line to be encoded is read by READLINE; assuming that this line is not null, the odd pixels (i.e., pixels of the first pattern) are encoded and re-constructed by some known technique. The even pixels are then encoded and re-constructed by GSE1A (FIG.8), which corresponds to the first stage of the pixel processing.

After storing the re-constructed first line as a history line, the main recursion of the encoding system is entered. In this recursion, there is always an attempt to read two successive lines. If successful, the second line is encoded and re-constructed by using the known technique on the odd pixels and GSE1A on the even pixels. The newly re-constructed line, together with the history line can now be used to encode (and re-construct) the intermediate line by using GSE2A (FIG.9), which corresponds to the second stage of pixel processing. The re-constructed second line now becomes the history line for the next pass in the recursion.

FIG.7 also illustrates one of several possible ways of handling a dangling second field line when the recursion is finished. After replicating the history line into the re-constructed first stage line, the dangling line is simply encoded by using GSE2A.

In FIG.7, CODELINE and LASTLINE represent binary decisions that are encoded to indicate whether more lines are present (LSIZE1 or LSIZE2 not zero). In the present preferred system, these decisions are encoded by using the entropy coder (e.g., Q-coder), as if they were part of the binary stream generated by GSE1A or GSE2A. Fixed probabilities are assigned to these decisions.

FIG.8 shows a flow chart of the encoder used in the first stage of processing the pixels not in the first matrix pattern. After the initialization process takes place in SETUPGS1A (FIG.10), the main recursion of the algorithm follows. Since in the first stage, only the even pixels are encoded, the HP data pointer is always updated by two inside the loop. INTERPOLATE1 (FIG.12) calculates the predicted value I' for the input pixel value X, by averaging L1 and R1. CALCQDIF (FIG.14) then obtains QDIF by a simple look-up-table operation on the difference between X1 and I1' (see Table 1). STATMODEL1 (FIG.15) sets the SP statistics pointer to the correct address by first evaluating the gradient through another look-up-table operation, and then adding the value of GRAD to the address of the STAT1 statistics storage area. Further, the value of SIGNDISPA, which was stored as part of the history buffer of the previous first stage line, is also tagged on to SP.

The binary decision stream represented by QDIF can now be encoded. If QDIF is zero, no further correction is needed, as the value of I1' is also the value of the re-constructed pixel I1; thus a zero is encoded by CODEYN, and SIGNDISPA is reset to zero for the next first stage line. Note that SIGNDISPA is at a fixed offset from pointer HP and thus forms part of the history data used to encode successive first stage lines.

If QDIF is not zero, a test is made as to whether encoding of the input line is completed. This test is needed in the QDIF = 0 path only, as the initialization of SETUPGS1A forces this condition when the right

edge of the input line is exceeded. In this manner, substantial computational efficiency over a system that performs this test for every pixel is achieved, as the statistics of the process will favor the QDIF=0 condition. Assuming that the right edge has not yet been reached, a one is encoded by CODEYN to indicate QDIF=0.

5 RECONSTRUCT (FIG.17) is now used to modify the interpolated pixel value to a "corrected" reconstructed value. The correction is obtained through another look-up-table operation using the value of QDIF as an index into the table (QLUT). The QLUT table provides the EX value in TABLE 1 corresponding to the QDIF value which is also shown in TABLE 1. A computationally efficient test is also made to insure that the corrected value does not overflow or underflow the byte-size pixels. The corrected pixel is
10 calculated in the TEM register which should be at least two bytes wide. Using the two-complement representation of negative numbers common to most computers, the test determines whether the contents of TEM are negative or greater than 255 by a single logical comparison against 255. This is illustrated in FIG.17.

After updating the statistics pointer SP, encoding of the binary decision for the sign and then the binary stream for the magnitude is performed. These operations are performed in CODESIGN1 (FIG.18) and CODEMAGNITUDE (FIG.20) respectively. The recursion now proceeds with the next even pixel in the input line.

CODESIGN1 encodes the decision zero (positive QDIF) or one (negative QDIF) by a simple comparison and an invocation to CODEYN. It also resets the value of SIGNDISPA to be used in the next first stage line, updates the statistic pointer for the first magnitude binary decision, and finally shifts the msb in QDIF (the
20 sign bit) out of the decision stream.

CODEMAGNITUDE (FIG.20) encodes the binary decision stream that indicates the correct quantized magnitude. The encoding process is achieved by successive invocations to CODEYN after testing the msb in QDIF. This bit is shifted out of QDIF before every test and the loop is terminated when a zero msb in
25 QDIF is present. The succession of bits is in effect a representation of the binary stream needed to reach a leaf in FIG.5. CODEMAGNITUDE also resets the statistics pointer SP after the first decision is coded, to point to the area of common statistics.

FIG.9 illustrates a procedure that can be used to encode a missing line in the second stage of the second field matrix (GSE2A). By virtue of the symmetry of GSE1A and GSE2A, both processes are very
30 similar; in fact, they share many of the same blocks. Minor differences do occur as explained in the main body of this disclosure. These differences require a different interpolation algorithm (INTERPOLATE2 in FIG.13) and a symmetrical statistical modeler (STATMODEL2 in FIG.16).

Although all functions are essentially symmetric and equivalent, computational efficiency demands some slight variations of detail. For example SIGNDISPL does not need to be stored as line history data and is better computed in STATMODEL2 rather than in CODESIGN1 as in GSE1A. This variation forces a
35 different version for the second stage encoding of the sign (CODESIGN2 in FIG.19). Functionally however, all of the abovementioned modules having implementation differences are equivalent or symmetrical.

Finally, the decoders for the first and second stage algorithms are illustrated in FIGS.21 through 26. The processes involved are essentially the reverse of those in the encoders and should be self-explanatory.
40 FIG.21 illustrates a decoding system, DMAIN, that reverses the operations of EMAIN. GSD1A and GSD2A decode the first stage and second stage compressed data and, therefore, reverse the action of GSE1A and GSE2A. Similarly, DE CODELINE and DECODELAST decode the data generated by CODELINE and LASTLINE. It should also be noted that many of the same blocks used in the encoders appear in the flow charts for the corresponding decoders.

45 While the invention has been described with reference to preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made without departing from the scope of the invention. For example, the same entropy encoder may be used as encoder 106 and encoder 206 or, alternatively, separate encoders may be used. In addition, any of various entropy encoders --e.g. Huffman coders--may be used with varying accuracy and outputs. Moreover, more
50 intricate computations may be performed in generating, for example, gradient values. That is, instead of two values to determine gradient four values may be used. And, instead of one pixel being used in determining the SIGNDISPA or SIGNDISPL, several pixels may be used. Such variations, although within the contemplation of the invention, are not preferred.

As remarked hereinabove, the first pattern may differ from the alternate pixel of alternate row pattern
55 described in the preferred embodiment. For example, referring to FIG.1, it is noted that first pattern pixels in the third and fifth row are aligned with first pattern pixels in the first row. The invention contemplates that the first pattern pixels of the third row may be offset to the right one position, providing a staggered pattern in which first pattern (hatched) pixels in the odd rows of the first pattern are vertically aligned and first

pattern pixels in the even rows of the first pattern are vertically aligned and in which first pattern pixels in odd rows are not aligned with first pattern pixels in the even rows.

The processing would be similar to that described in the preferred embodiment described hereinabove, it being noted however that the sign value, used in the entropy model for coding pixel $i1$, would be determined from a pixel which was coded using the first stage in a previous row.

Further, the first pattern may include, by way of example, every fourth pixel in every fourth line. That is, in row 1, pixels $X_{1,1}$, $X_{1,5}$, $X_{1,9}$, ..., $X_{1,509}$ are previously coded and are in the first pattern; in the fifth row, pixels $X_{5,1}$, $X_{5,5}$, $X_{5,9}$, ..., $X_{5,509}$ are previously coded and are in the first pattern; and so on. The remaining pixels are not part of the first pattern. Encoding with this first pattern is demonstrated with reference to pixel $X_{5,3}$ as a first input pixel. Based on the values of $X_{5,1}$ and $X_{5,5}$, a GRAD1 value is determined. From pixel $X_{1,3}$ determined earlier in the first stage, a state input for the subject pixel is generated. With $X_{5,3}$ coded, pixels $X_{5,2}$ may then be processed --the GRAD1 value being based on $X_{5,1}$ and $X_{5,3}$. The entire row may be coded and re-constructed values for each pixel may be computed by successive steps of interpolation. Similarly, after first pattern rows are coded, the coding of interleaved rows containing no first patterns pixels may be performed. That is, given that all pixels in rows 1,5,9, ..., 477 have been coded, second stage may be applied to code the remaining pixels. The operation of the second stage is demonstrated with reference to pixel $X_{3,5}$, assuming that $X_{3,4}$ was previously coded in the second stage. In processing pixel $X_{3,5}$, pixel A2 would be pixel $X_{1,5}$; pixel B2 would be pixel $X_{5,5}$; and the sign would be based on pixel $X_{3,4}$ (which would correspond to pixel L2 as described in the preferred embodiment). Each pixel in row 3 may be processed in sequence. Once row 3 is processed by the second stage, rows 2 and 4 may then be processed based on the pixels coded in rows 1 and 3. From the two alternative first patterns set forth above, it is noted that the algorithm of the present invention is generally applicable where a first stage codes pixels in rows containing first pattern (previously coded) pixels and a second stage codes pixels in all rows which do not contain first pattern pixels.

Alternatively, once pixels in rows 1 and 5 have all been coded, pixels in missing rows 2, 3, and 4 can be coded. This permits the first stage and second stage to be interleaved, which requires less buffering.

It is further noted that reference to a pixel "above", "below", "to the left", or "to the right" is not limited to immediately adjacent pixels. For example, a pixel "above" pixel $i2$ may be vertically above pixel $i2$ with zero, one or more pixels therebetween.

Furthermore, the described embodiment discloses the scanning of lines top-to-bottom, each line being scanned from left-to-right. The invention contemplates other scan patterns, for example, scanning lines from bottom-to-top or scanning pixels in a line from right-to-left. The present invention may be applied to such alternative scanning patterns in substantially the same way to achieve substantially the same results.

In this regard, it is observed that pixel-position notation is for convenience of identification and is not intended as a limitation. For example, in the described embodiment having top-to-bottom, left-to-right scan, the GRAD1 value is determined from a pixel "above" the subject pixel. In an alternative embodiment that features the scanning of lines from "bottom-to-top", the GRAD1 value would depend on a pixel "below" the subject pixel. In the latter case, the pixel "below" is treated the same as the pixel "above" in the former scanning scheme. The two embodiments may be viewed as equivalents or the latter may be viewed as a top-to-bottom scan with the image re-oriented. Similarly, pixels may be scanned in either direction vertically or either direction horizontally depending on whether the rows are disposed vertically or horizontally.

Such varying scan patterns and pixel-position references are viewed as equivalents.

It is finally observed that "graylevel" has been illustrated in this application in the context of monochrome data (i.e., luminance). However, "graylevel" coding herein is intended to include the coding of color components as well. One embodiment relating to color would be to apply the graylevel compression/decompression apparatus or method to each of the chrominance components separately.

Claims

1. For a graylevel image formed of (i) a first matrix pattern which includes some pixels in at least some rows in the image and (ii) a second matrix pattern which includes the remaining pixels, wherein each pixel in the first pattern has a predetermined value associated therewith, apparatus for generating a state input for subsequent entropy coding of difference values of second pattern pixels, wherein the difference value of a second pattern pixel is based on the difference between a graylevel value and a predicted value of said second pattern pixel, the apparatus comprising:

first stage means (112) for generating a gradient state value for a subject uncoded pixel in a row containing

at least two first pattern pixels, the gradient value being determined based on known values of at least one pixel on each side of the subject uncoded pixel; and

5 first stage means (108, 110) for determining a sign state value for the subject uncoded pixel, based on the arithmetic sign of a difference value corresponding to at least one pixel previously coded;

the state input of the subject uncoded pixel being derived from the gradient state value and the sign state value thereof.

10 2. Apparatus as in Claim 1 further comprising:

first stage means (103, 104, 114, 116) for re-constructing a graylevel value for an uncoded pixel in a row containing first pattern pixels.

3. Apparatus as in Claim 2 wherein said first stage re-constructing means includes:

15 means (103, 114) for interpolating the values of pixels in a row containing first pattern pixels, the interpolated value for each pixel in a row containing first pattern pixels being based on known values of at least two pixels between which the uncoded pixel is positioned, wherein the known values are either (i) values corresponding to first pattern pixels or (ii) previously re-constructed values; and means (116) for adding the interpolated value and difference value.

20 4. For a graylevel image formed of (i) a first matrix pattern which includes rows of previously coded pixels, each having a graylevel value associated therewith and (ii) a second matrix pattern which includes pixels in the remaining rows, apparatus for generating a state input for subsequent entropy coding of difference values of second pattern pixels, wherein the difference value of a second pattern pixel is based on the difference between a graylevel value and a predicted value of said second pattern pixel, the
25 apparatus comprising:

second stage means (208) for generating a gradient state value for a subject uncoded pixel in a second pattern row, the gradient value being determined based on known values of at least one pixel above and one pixel below the subject uncoded pixel;

30 second stage means (210) for determining a sign state value for the subject uncoded pixel, based on the arithmetic sign of the difference value corresponding to at least one pixel previously coded;

35 the state input of the subject uncoded pixel being derived from the gradient state value and the sign state value thereof.

5. Apparatus as in Claim 4 further comprising:

second stage means (203, 204, 205, 207) for re-constructing a graylevel value for an uncoded pixel in a row containing only second pattern pixels.

40 6. Apparatus as in Claim 5 wherein said second stage re-constructing means includes:

45 means (203, 205) for interpolating the values of pixels in a row containing only second pattern pixels, the interpolated value for each pixel in a row containing only second pattern pixels being based on known values of at least one pixel above and one pixel below the uncoded pixel, wherein the known values are either (i) values corresponding to first pattern pixels or (ii) previously re-constructed values; and means (207) for adding the interpolated value and the difference value.

50 7. For a graylevel image formed of (i) a first matrix pattern which includes all pixels at the intersections of alternating rows and alternating columns of pixels in the image and (ii) a second matrix pattern which includes the remaining pixels, wherein each pixel in the first pattern has a value associated therewith, apparatus for generating, for each pixel in the second pattern, a state input for subsequent entropy coding, the apparatus comprising:

55 first stage means (100) for generating a state input value and a re-constructed value for one uncoded pixel after another along a row containing first pattern pixels; and

second stage means (200) for generating a state input value for one uncoded pixel after another along a row containing no first pattern pixels;

wherein said first stage means generates a respective state input and a respective re-constructed value for a pixel along a row containing first pattern pixels based selectively on (i) the arithmetic sign of at least one corresponding pixel previously generated by said first stage means and (ii) values corresponding to pixels in the first pattern; and

5 wherein second stage means generates a respective state input and a respective re-constructed value for a pixel along a row containing no first pattern pixels based selectively on (i) values corresponding to pixels in the first pattern; (ii) re-constructed values corresponding to pixels previously generated by said first stage means; and (iii) the arithmetic sign of at least one corresponding pixel previously generated by said second
10 stage means.

8. Apparatus as in Claim 7 wherein said first stage means comprises:

means (108, 110) for selecting, for a pixel i_1 in a row containing first pattern pixels, one sign history value from a plurality of predefined arithmetic sign values, the selected sign history being based on the arithmetic
15 sign of a value for at least one previous ly coded pixel which is positioned in a previous row of pixels;

means (114) for computing a horizontal gradient value for i_1 based on the difference in value between pixels on either side of and along the row of pixel i_1 ; and

20 model means (112) for combining the selected sign history value and the horizontal gradient value to form the state input for pixel i_1 .

9. Apparatus as in Claim 8 wherein said second stage means comprises:

means (210, 212) for selecting, for a pixel i_2 in a row containing no first pattern pixels, one sign history
25 value from a plurality of predefined arithmetic sign values, the selected sign history being based on the arithmetic sign of a difference value for at least one previously coded pixel which is positioned in the row containing i_2 ;

means (205) for computing a vertical gradient value for i_2 based on the difference in value between pixels
30 vertically above and vertically below pixel i_2 ; and

model means (208) for combining the selected sign history value and the vertical gradient value to form the state input for pixel i_2 .

10. Apparatus as in Claim 9 wherein said means for selecting the i_1 sign history value includes:

35 means for selecting a value corresponding to a zero, -, or + arithmetic sign of the difference value for the pixel vertically above pixel i_1 and at least one pixel away from pixel i_1 .

11. Apparatus as in Claim 10 wherein said means for selecting the i_2 sign history value includes:

40 means for selecting a value corresponding to a zero, -, or + arithmetic sign of the difference value for the pixel coded immediately before and in the row of pixel i_2 .

12. For a graylevel image formed of (i) a first matrix pattern which includes all pixels at the intersections of alternating rows and alternating columns of pixels in the image and (ii) a second matrix pattern which
45 includes the remaining pixels, wherein each pixel in the first pattern has a value which has been previously coded,

apparatus for compressing and decompressing data in the second pattern comprising:

means for compressing image data including:

50 means (106) for entropy encoding a digital decision input based on a state input which defines a context for the digital decision input;

first means (103) for predicting a value I_1' for a previously uncoded pixel i_1 in a row containing first
55 pattern pixels, wherein $I_1' = (L_1 + R_1)/2$ where L_1 and R_1 are values for previously coded pixels which are, respectively, to the left and right of pixel i_1 ;

first subtractor means (102) for computing a difference value between the input value X_1 for pixel i_1 and the predicted value I_1' for pixel i_1 ;

first means for quantizing (104) the difference value, the quantized value corresponding to a decision input to said entropy encoder means;

5 first means (108, 110) for generating a sign history value for pixel i_1 as the arithmetic sign of the quantized difference value previously determined for the pixel vertically above and one pixel away from pixel i_1 ;

10 first means (114) for generating a horizontal gradient value for pixel i_1 as the difference between reconstructed values of a pixel to the left and a pixel to the right of pixel i_1 ;

first means (112) for combining the horizontal gradient value and the sign history value to provide a state input to said entropy encoding means for pixel i_1 ; and

15 means (150, 250) for decompressing the entropy encoded compressed data.
13. Apparatus as in Claim 12 further comprising:

20 second means (203) for predicting a value I_2' for a previously uncoded pixel i_2 in a row containing no first pattern pixels, wherein $I_2' = (A_2 + B_2)/2$ where A_2 and B_2 are previously coded pixels which are, respectively, vertically above and below pixel i_2 ;

second subtractor means (202) for computing a difference value between the input value X_2 of pixel i_2 and the predicted value I_2' of pixel i_2 ;

25 second means (204) for quantizing the difference value, the quantized value corresponding to a decision input to said entropy encoder means;

30 second means (210, 212) for generating a sign history value for pixel i_2 as arithmetic sign of the quantized difference value previously determined for the pixel coded immediately before and in the row containing pixel i_2 ;

second means (205) for generating a vertical gradient value for pixel i_2 as the difference between reconstructed values of a pixel vertically above and below pixel i_2 ;

35 second means (208) for combining the vertical gradient value and the sign history value to provide a state input to said entropy encoding means for pixel i_2 .

14. Apparatus as in Claim 13 wherein said first quantizer means and said second quantizer means comprise storage means containing a single quantization table.

40 15. Apparatus as in Claim 13 wherein said first means for generating a horizontal gradient includes first mapping means for selecting one of four possible values for the horizontal gradient; and

wherein said second means for generating a vertical gradient includes second mapping means (108) for selecting one of four possible values for the vertical gradient; and

45 wherein each sign history value corresponds to a zero, -, or + arithmetic sign;

each state input thereby being one of twelve possible states.

16. Apparatus as in Claim 13 wherein said decompressing means includes:

50 entropy decoder means (156, 256) for generating output decisions which correspond to the digital decision inputs to the encoding means; and

decoder model means (162, 258) for generating state inputs as successive decisions are decoded by said entropy decoding means;

55 said entropy decoder means generating output decisions in response to the inputting thereto of (i) compressed data generated by the entropy encoding means and (ii) state inputs from the decoder model means.

17. In an image in which each of a first pattern of pixels at the intersections of alternating rows and alternating columns have been previously coded and have re-constructed values associated therewith, a method of processing, for subsequent entropy coding, graylevel data for uncoded pixels, the method comprising the steps of:

- 5 (a) selecting a pixel $i1$ positioned between two first pattern pixels having respective values of $L1$ and $R1$;
- (b) predicting a value $I1'$ as $(L1 + R1)/2$;
- (c) subtracting the predicted value $I1'$ from the input value $X1$ of pixel $i1$;
- (d) quantizing the $(X1-I1')$ difference with a quantizer;
- 10 (e) from the sign of at least one quantized difference for at least one corresponding pixel in a previously coded row, determining a sign value $SIGNDISPA$ for $i1$;
- (f) computing a gradient value as $G1 = I1' - L1$;
- (g) entering as inputs to an entropy coder (1) the quantized difference for pixel $i1$ and (2) a state input based on $SIGNDISPA$ and $G1$;
- 15 (h) repeating steps (a) through (g) for one uncoded pixel after another in a row containing first pattern pixels.

18. The method of Claim 17 comprising the further steps of:

- (j) selecting a pixel $i2$ in a row containing no first pattern pixels, wherein a pixel with a value $A2$ is positioned vertically above and a pixel with a value $B2$ is positioned vertically below pixel $i2$;
- 20 (k) predicting a value $I2'$ as $(A2 + B2)/2$;
- (l) subtracting the predicted value $I2'$ from the input value for $X2$;
- (m) quantizing the difference $(X2-I2')$ with a quantizer;
- (n) from the previously quantized difference for the left adjacent pixel of $i2$, determining a sign value $SIGNDISPL$ for pixel $i2$;
- 25 (p) computing a gradient value as $G2 = I2' - A2$;
- (q) entering as inputs to an entropy coder (1) the quantized difference for pixel $i2$ and (2) a state input based on $SIGNDISPL$ and $G2$; and
- (r) repeating steps (j) through (q) for one uncoded pixel after another in a row containing no first pattern pixels.

- 30 19. For a graylevel image formed of (i) a first matrix pattern which includes some pixels in at least some rows in the image and (ii) a second matrix pattern which includes the remaining pixels, wherein each pixel in the first pattern has a predetermined value associated therewith and wherein first stage pixels are second pattern pixels in rows containing first pattern pixels and second stage pixels are second patterns pixels in rows containing no first pattern pixels; a method of decompressing entropy encoded compressed difference value inputs, the method comprising the steps of:
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generating a horizontal gradient state value for a subject undecoded first stage pixel in a row containing at least two first pattern pixels, the horizontal gradient value being determined based on known values of at least one pixel on each side of the subject undecoded pixel; and

- 40 determining a sign state value for the subject undecoded first stage pixel, based on the arithmetic sign of the difference value corresponding to at least one pixel previously decoded;

45 the state input of the subject undecoded first stage pixel being derived from the gradient state value and the sign state value thereof.

20. The method of Claim 19 comprising the further steps of:

- entropy decoding a compressed difference value input for an undecoded first stage pixel based on the state input derived therefor, re-constructing a graylevel value for said undecoded first stage pixel in a row containing first pattern pixels, including the steps of:
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interpolating the values of said undecoded first stage pixels, the interpolated value being based on known values of at least two pixels between which the undecoded first stage pixel is positioned, wherein the known values are either (i) values corresponding to first pattern pixels or (ii) previously re-constructed first stage values;

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adding the interpolated value and the entropy decoded difference value of said first stage pixel; and

for each pixel in a row of undecoded second stage pixels positioned between two rows in which every pixel has a graylevel value associated therewith:

5 generating a vertical gradient state value for a subject undecoded second stage pixel in a second pattern row, the vertical gradient value being determined based on known values of at least one pixel above and one pixel below the subject undecoded pixel;

10 determining a sign state value for the subject undecoded second stage pixel, based on the arithmetic sign of the difference value corresponding to at least one pixel previously decoded;

15 the state input of the subject undecoded second stage pixel being derived from the gradient state value and the sign state value thereof; and

20 entropy decoding a compressed difference value input for an undecoded second stage pixel based on the state input derived therefor.

21. The method of Claim 20 comprising the further step of:

re-constructing a graylevel value for said undecoded second stage pixel, including the steps of:

25 interpolating the value of said undecoded second stage pixel, the interpolated value being based on known values of at least one pixel above and one pixel below said undecoded pixel wherein the known values are either (i) values corresponding to first pattern pixels or (ii) previously re-constructed values; and adding the interpolated value and the entropy decoded difference value of said second stage pixel.

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FIG. 1

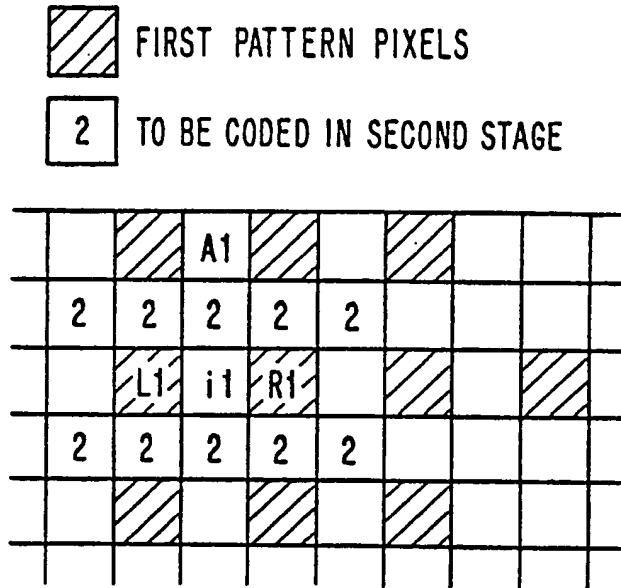


FIG. 2

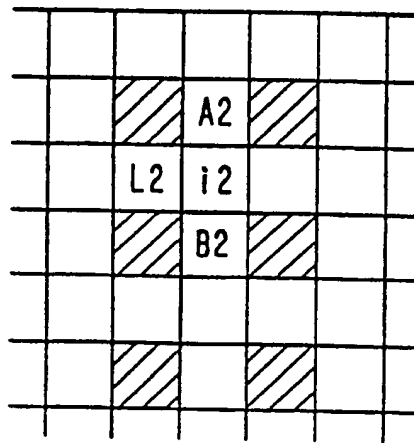


FIG. 3

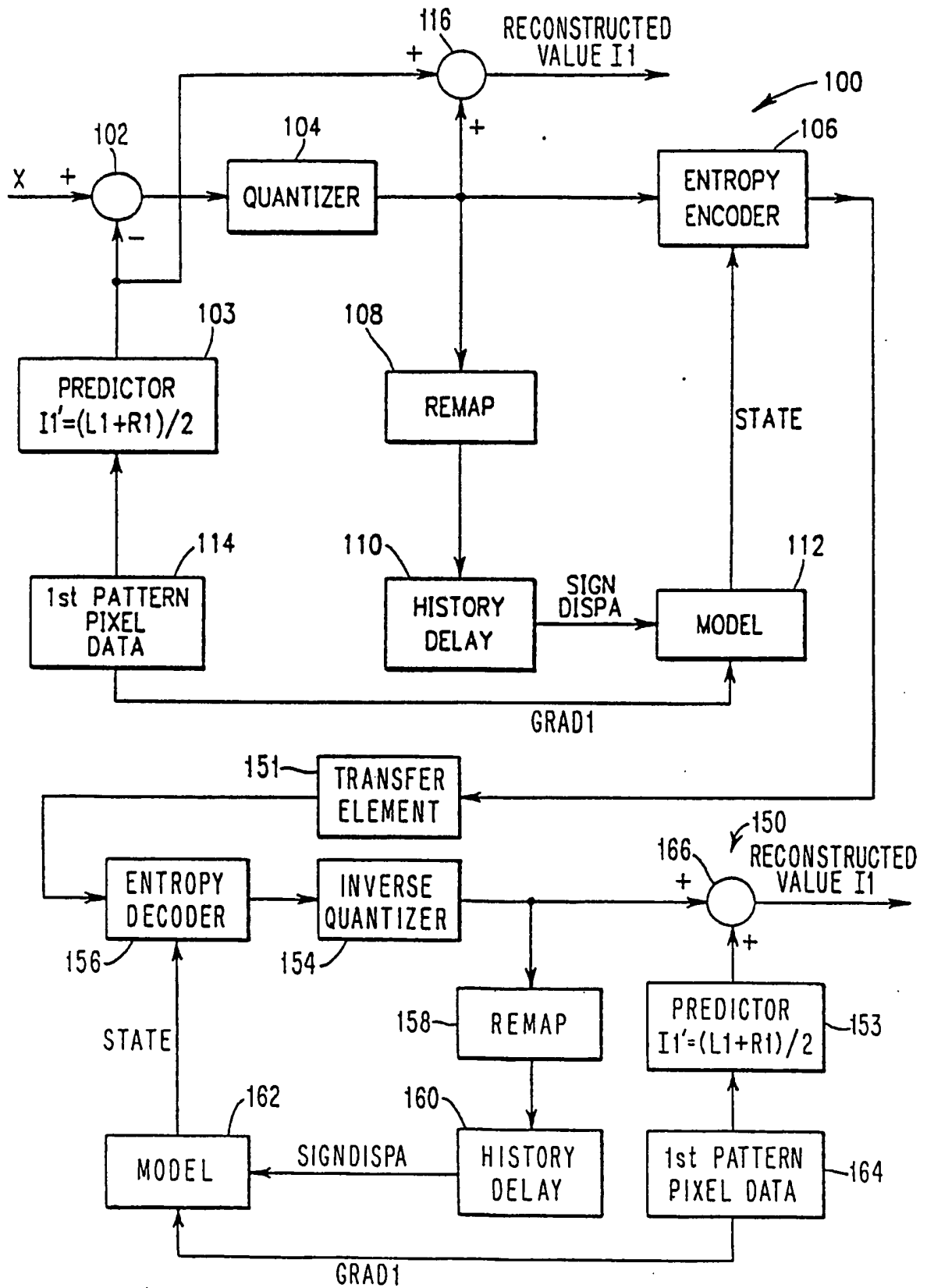


FIG. 4

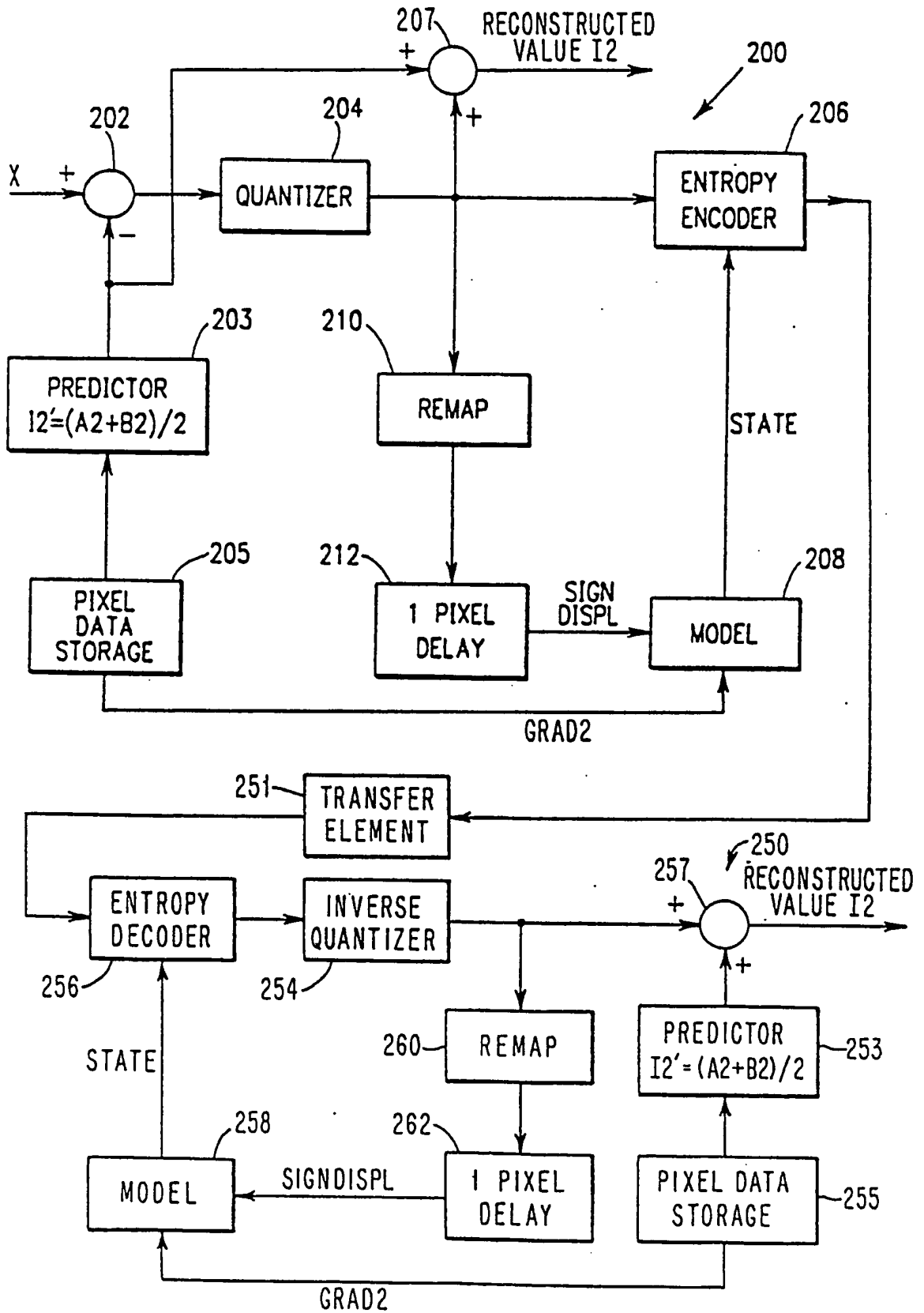


FIG. 5

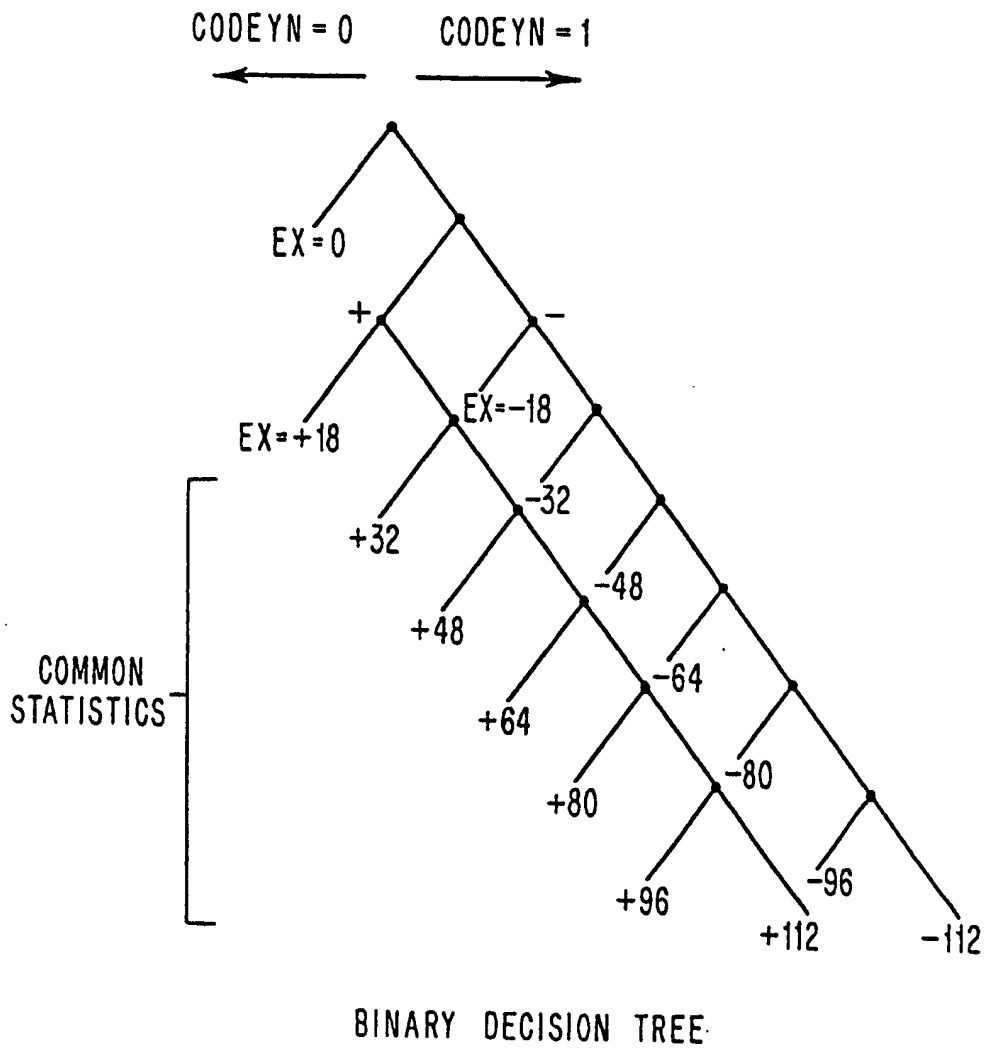


FIG. 6

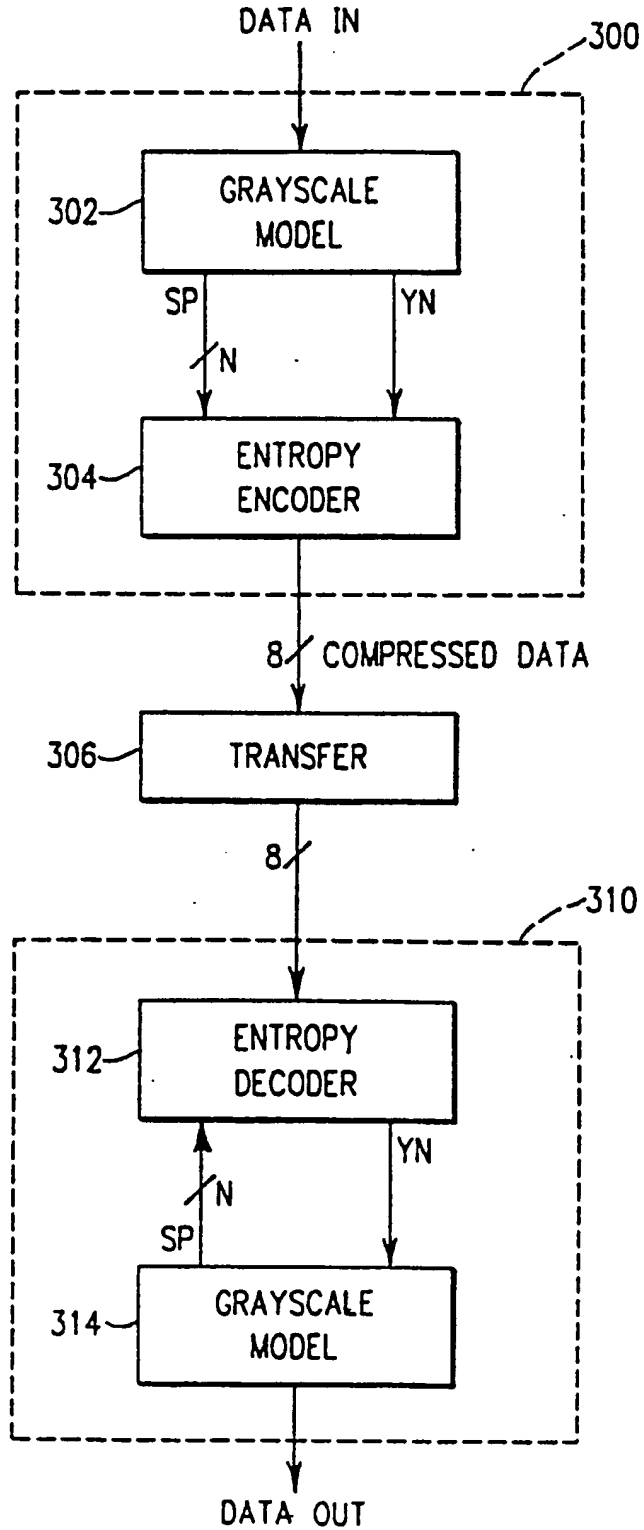


FIG.7

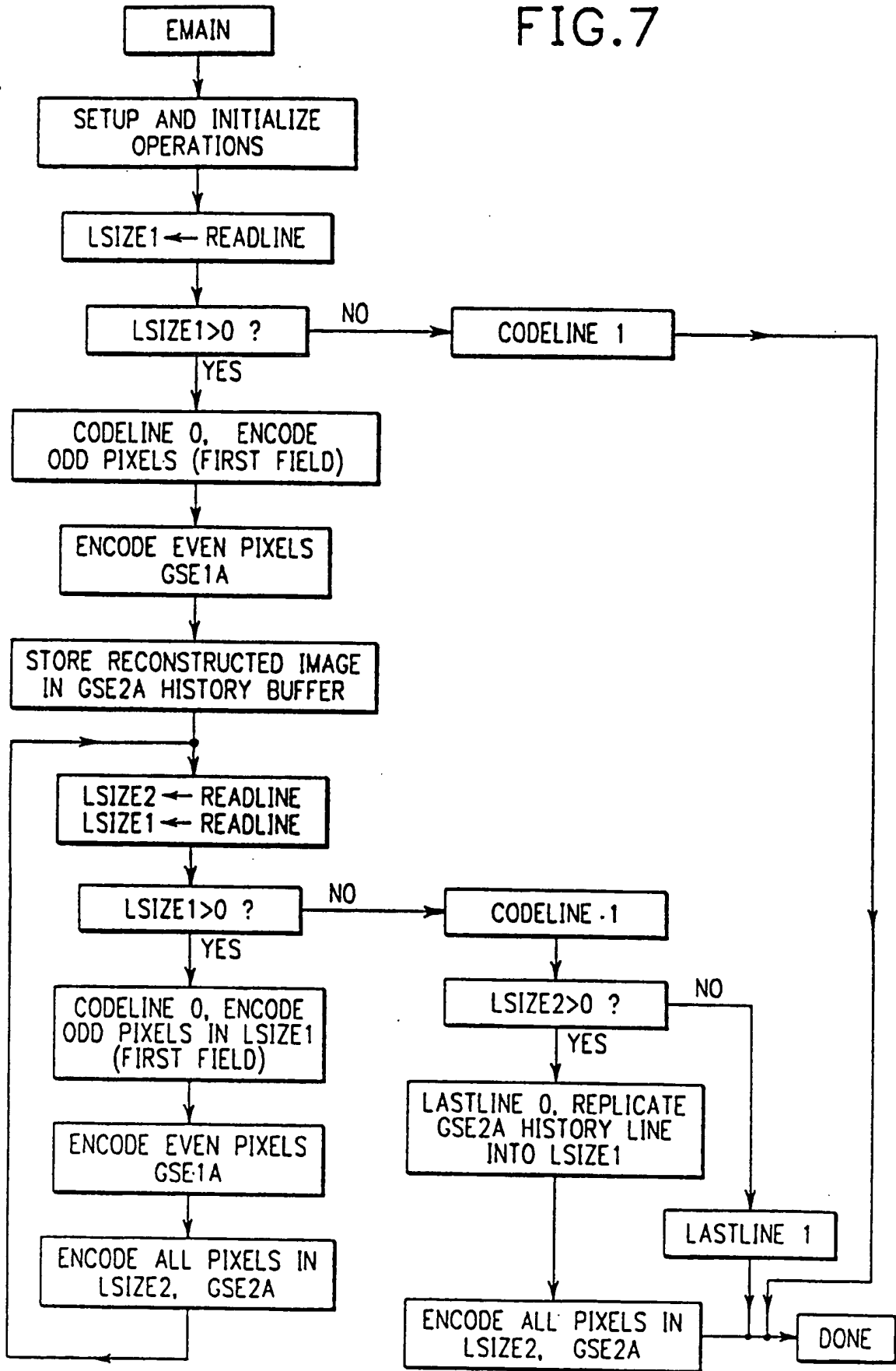


FIG.8

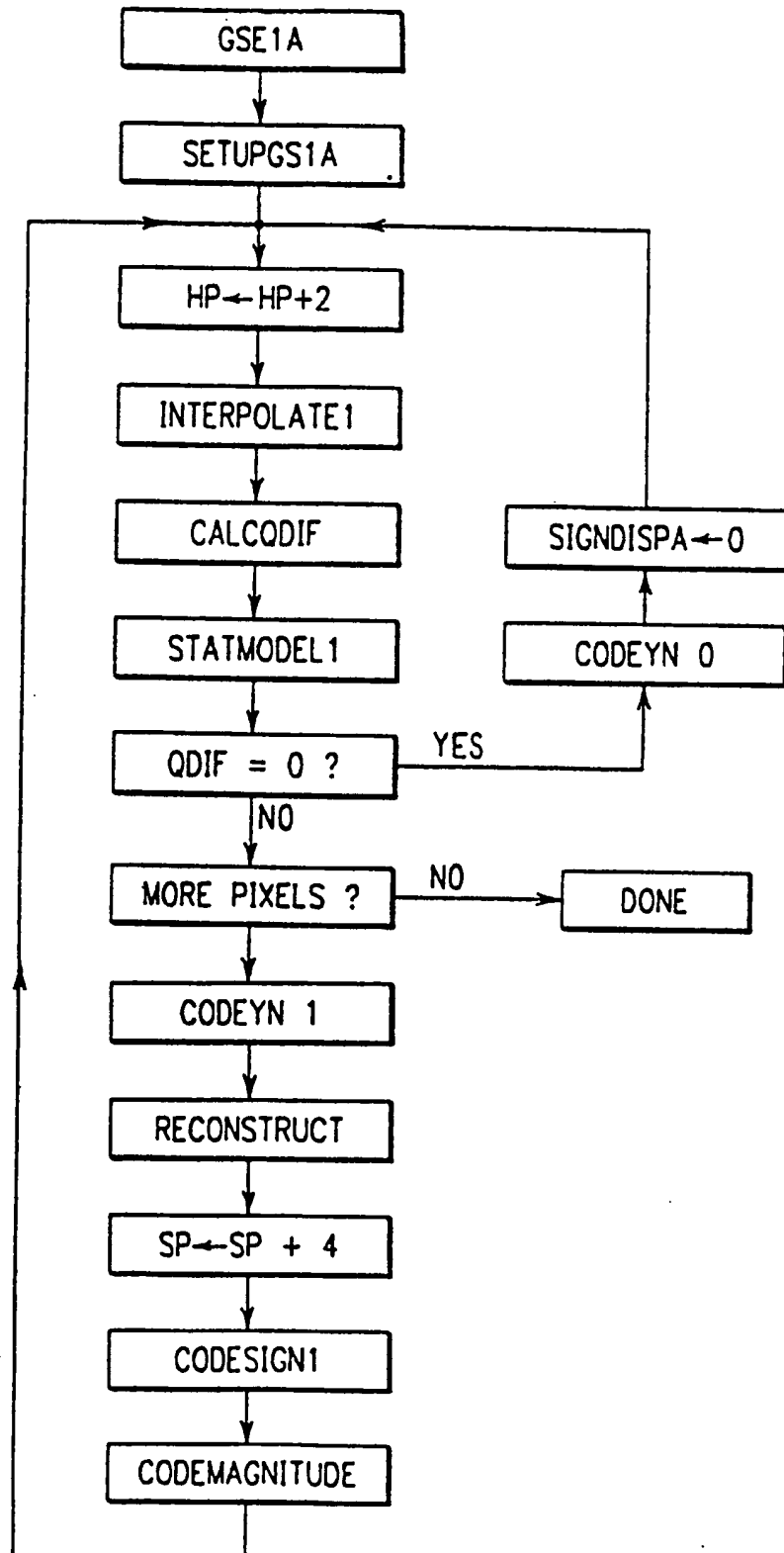


FIG.9

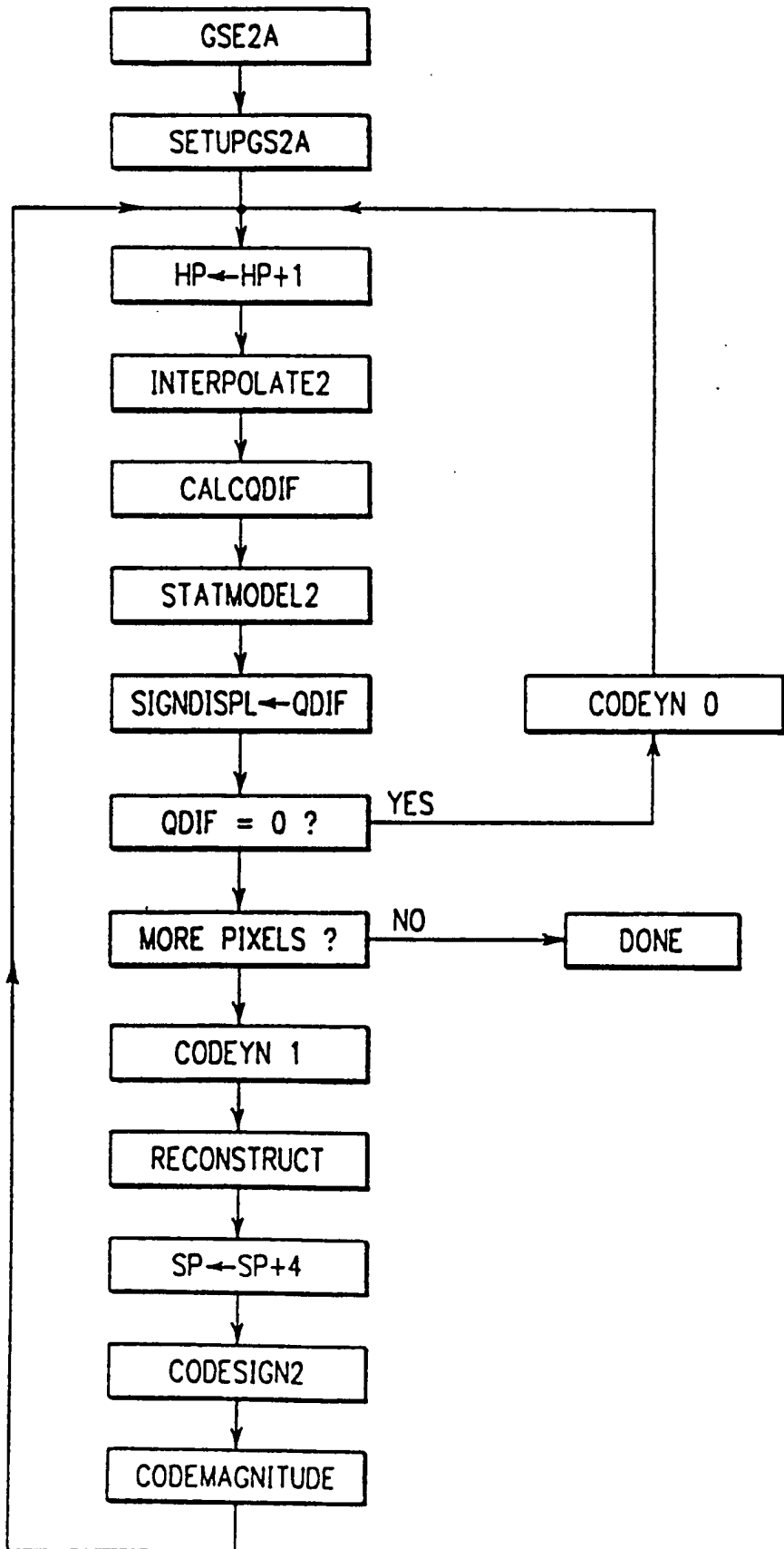


FIG.10

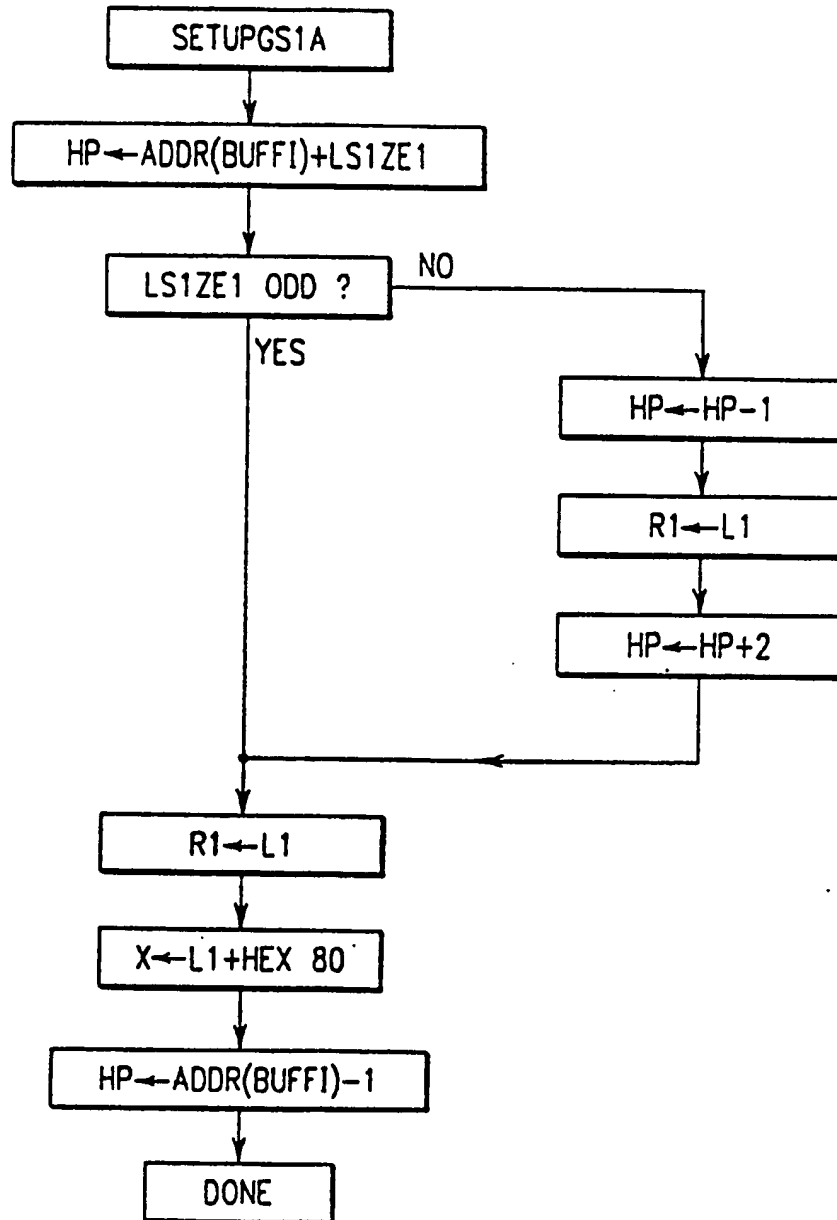


FIG.11

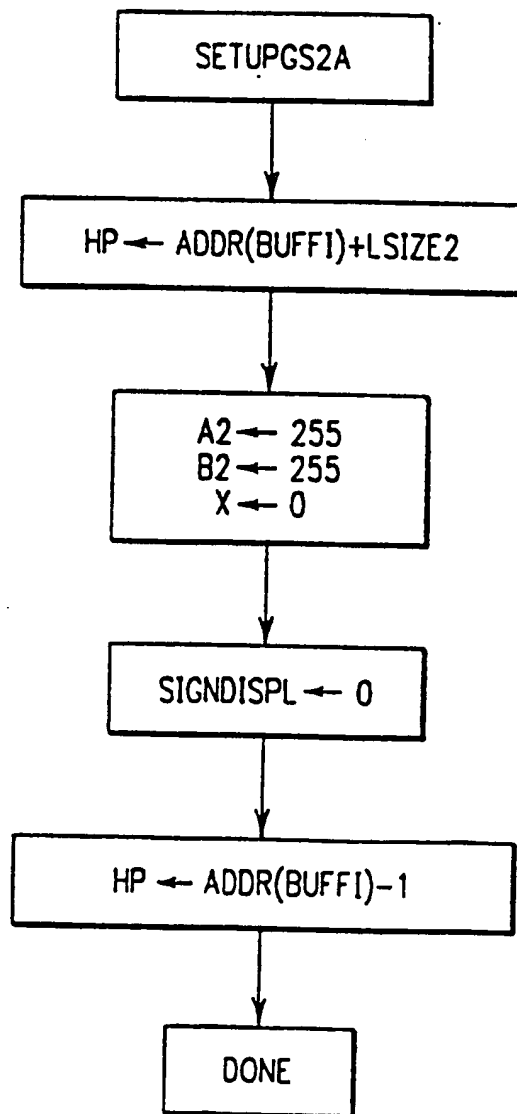


FIG.12

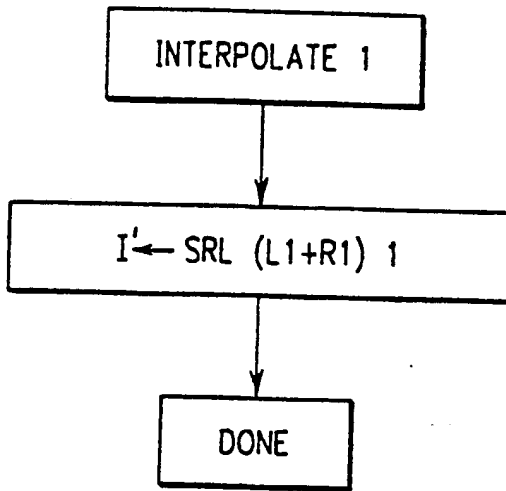


FIG.13

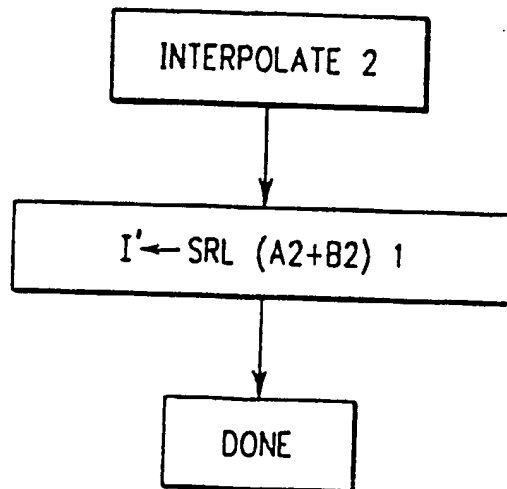


FIG.14

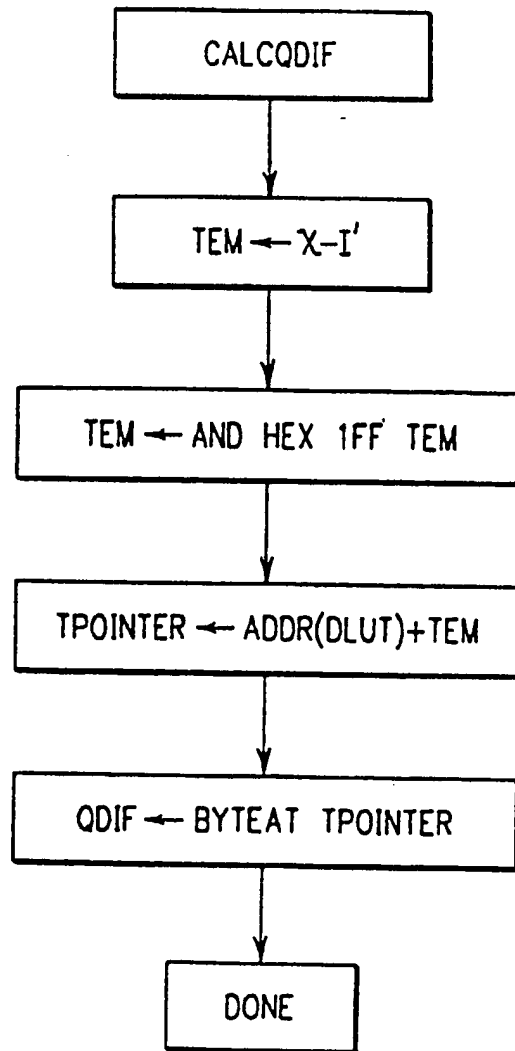


FIG.15

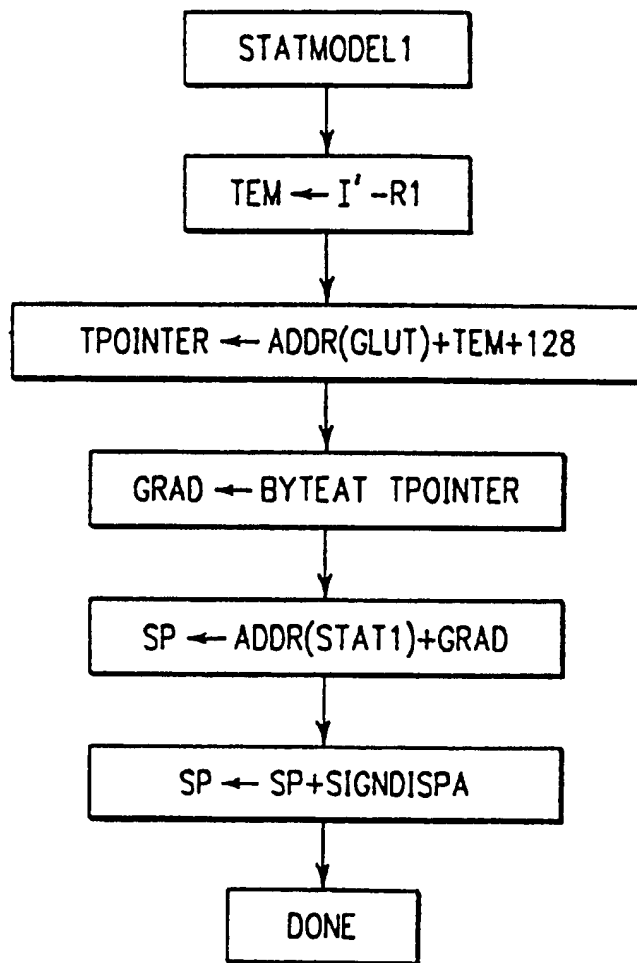


FIG.16

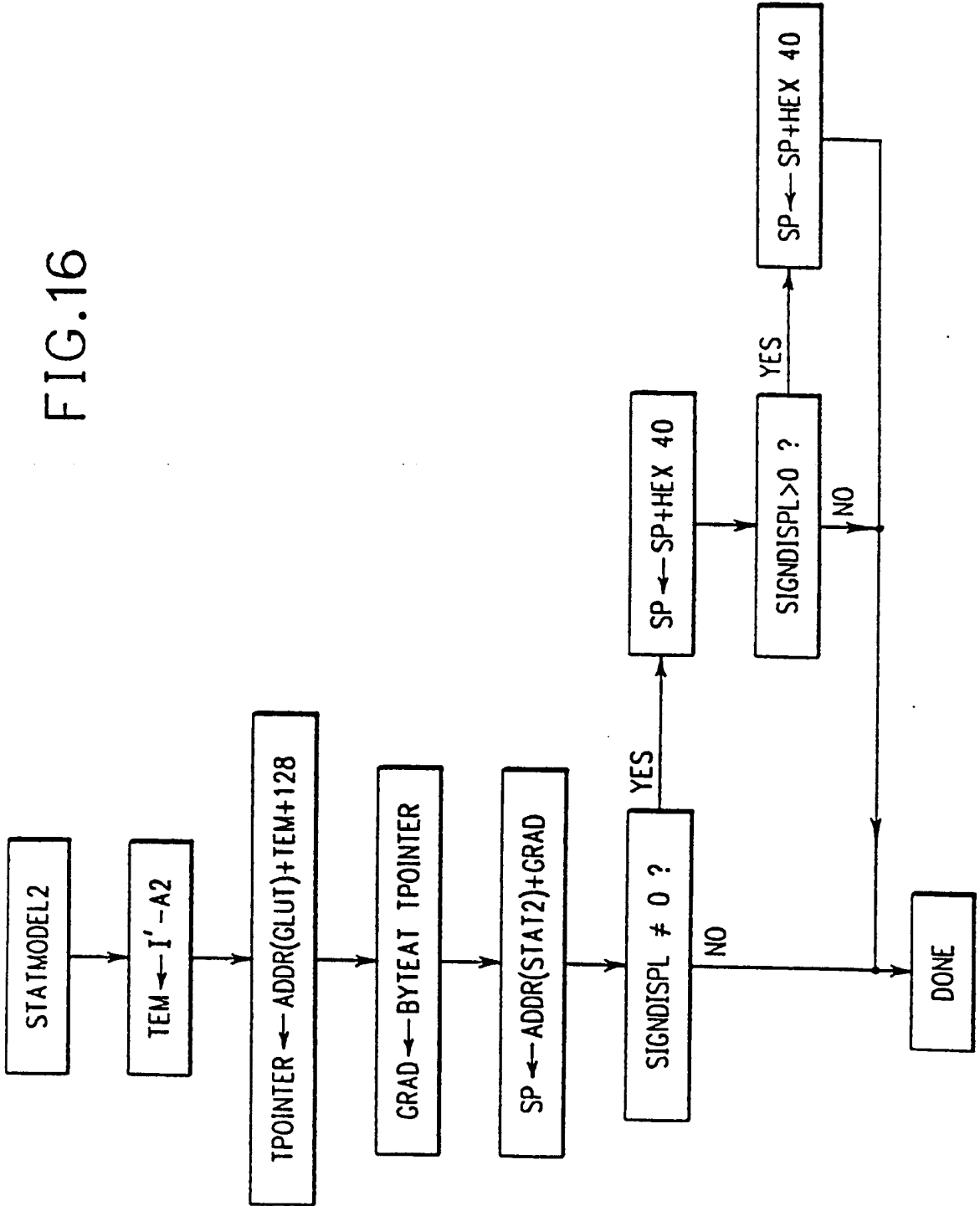


FIG.17

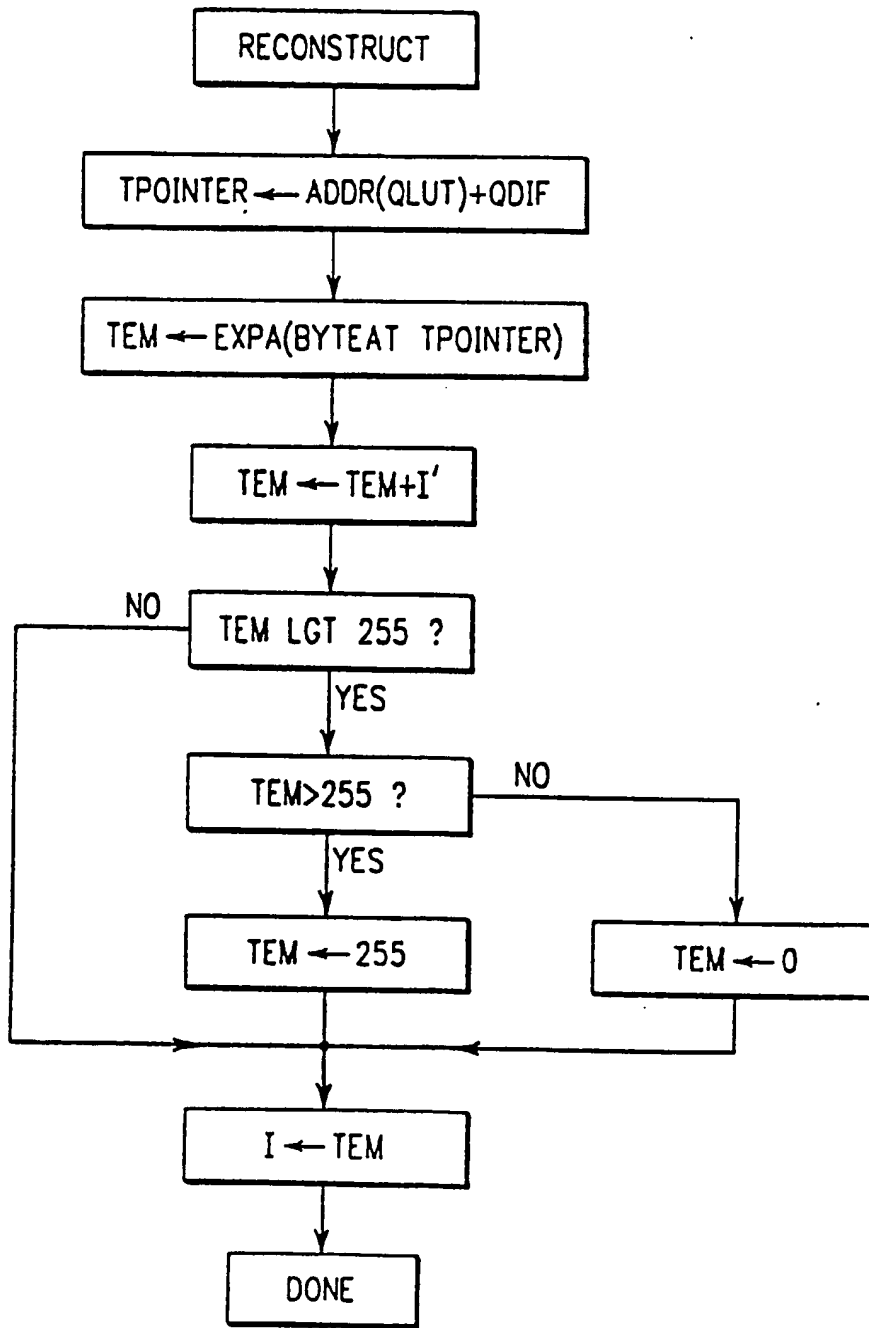


FIG.18

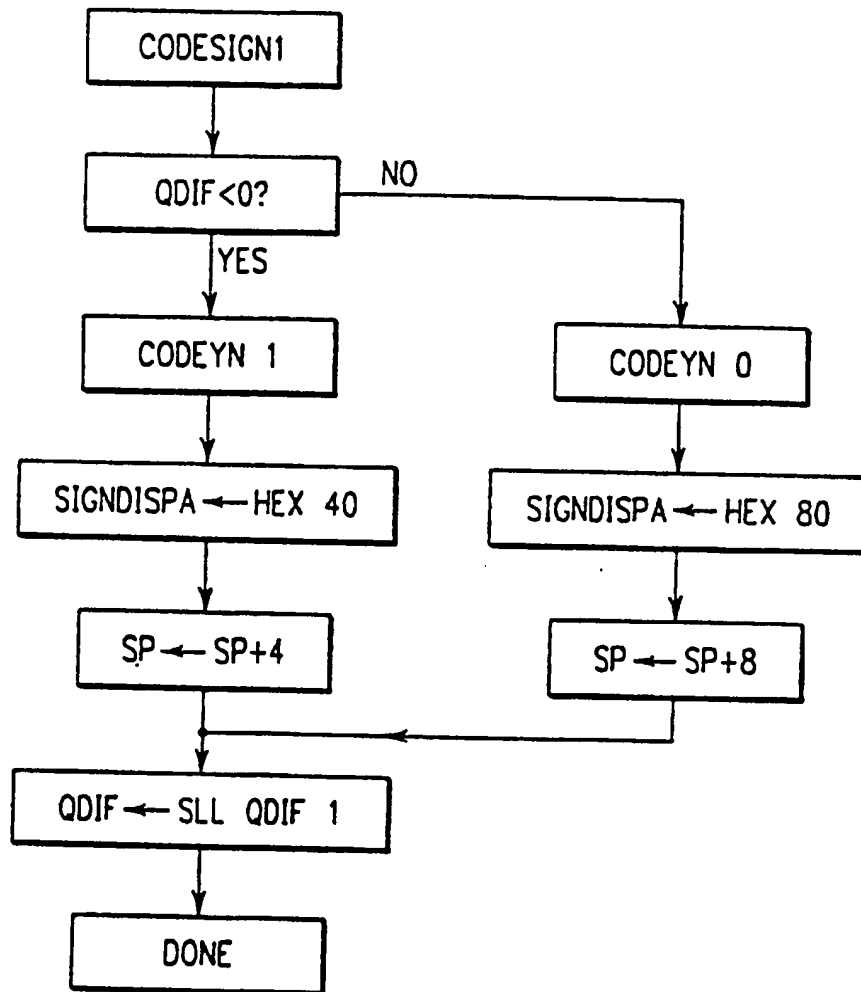


FIG.19

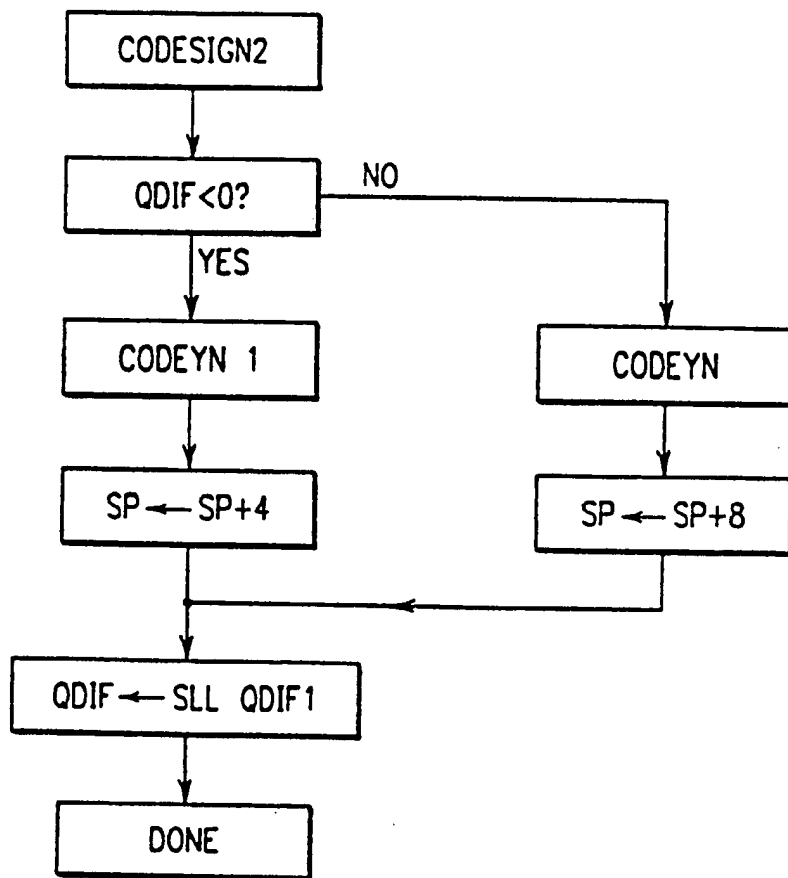


FIG.20

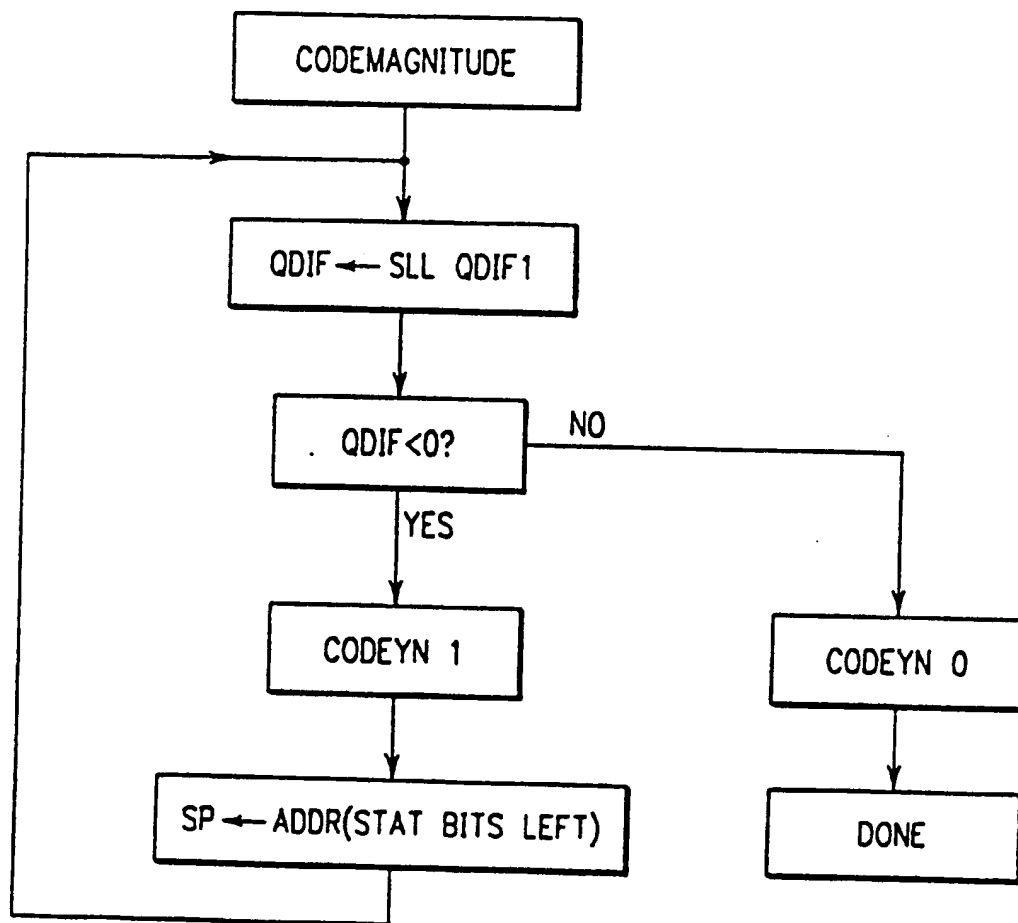


FIG.21

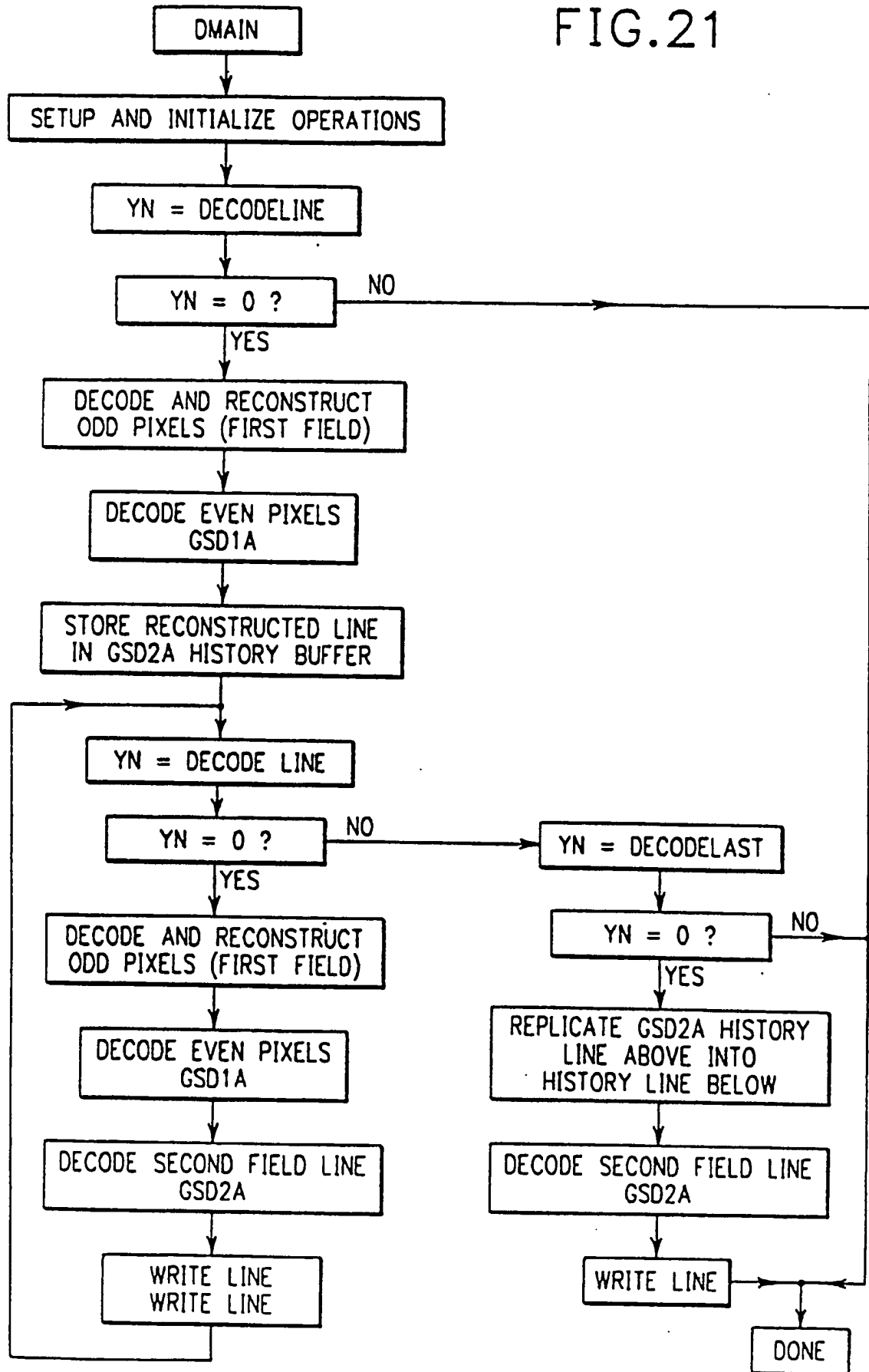


FIG.22

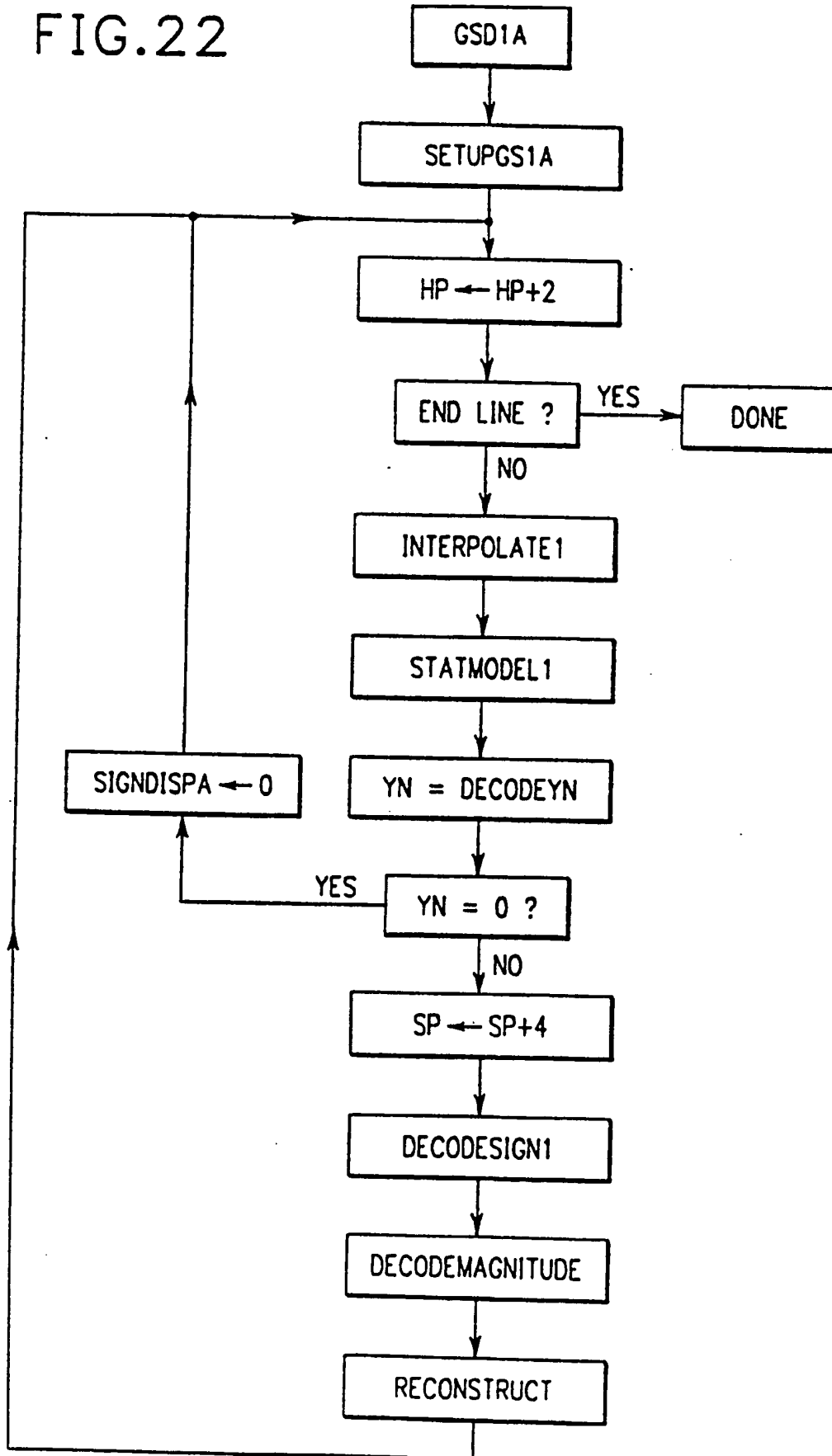


FIG.23

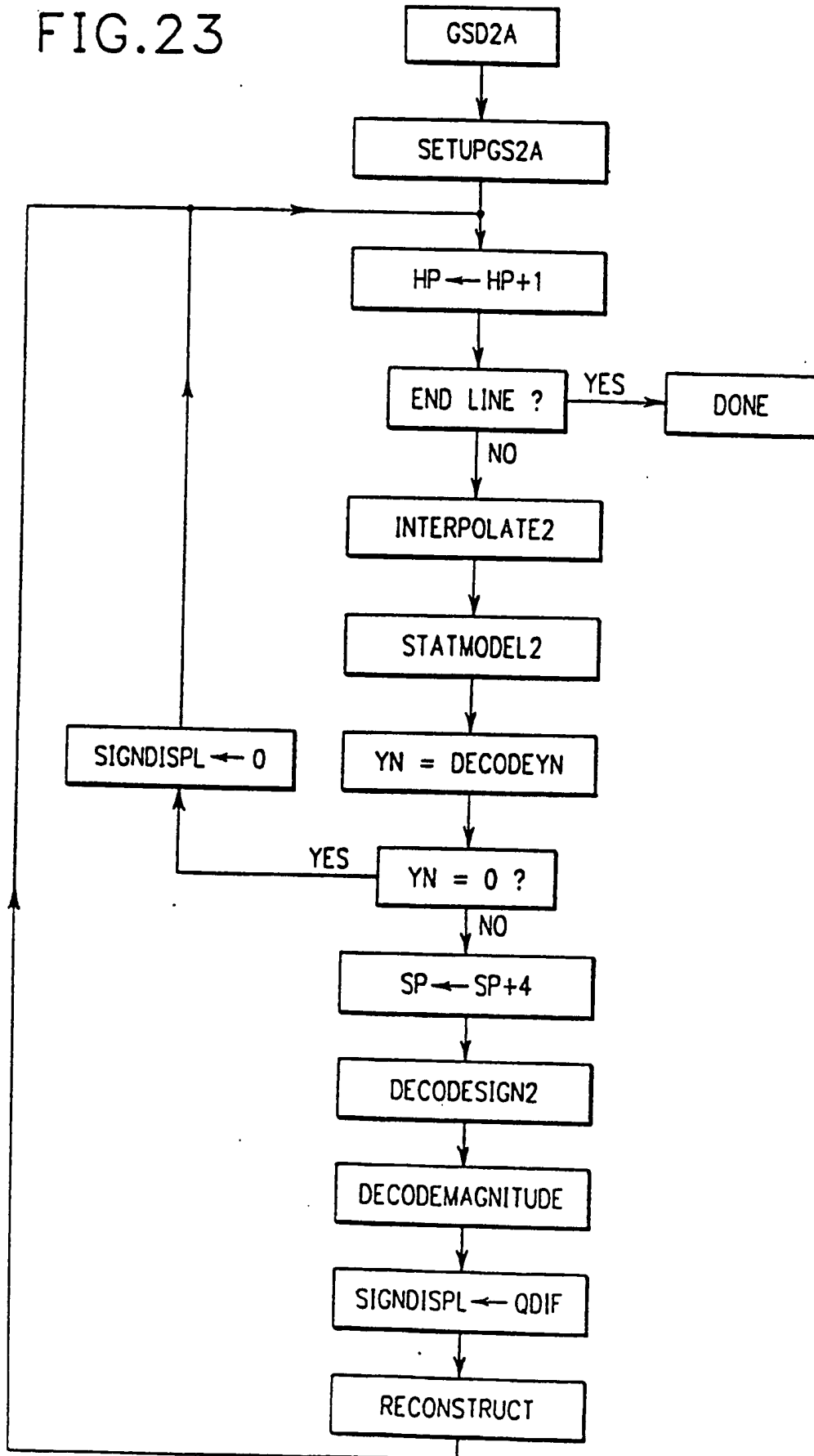


FIG.24

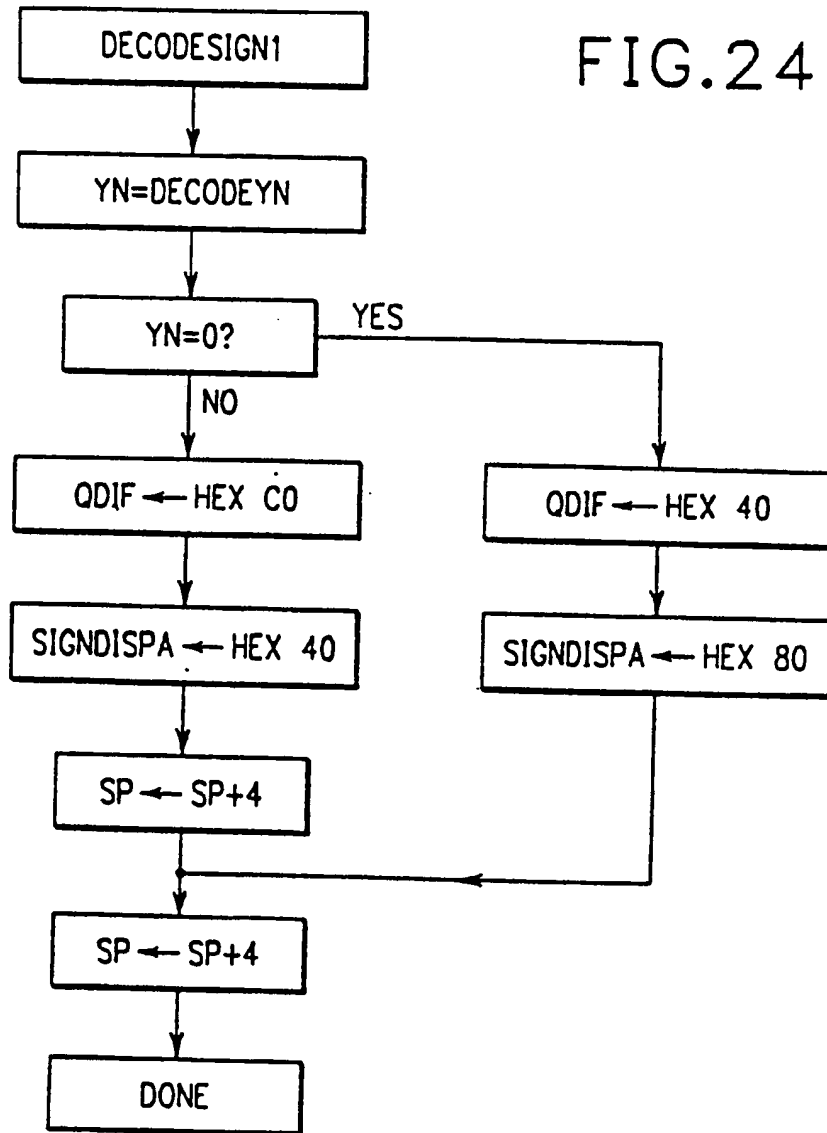


FIG.25

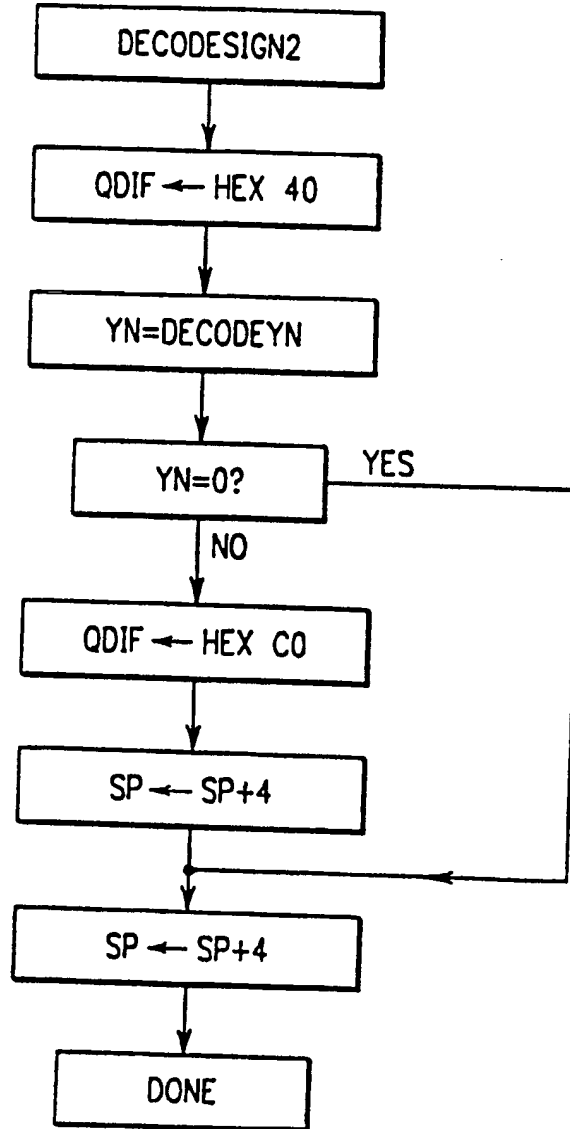
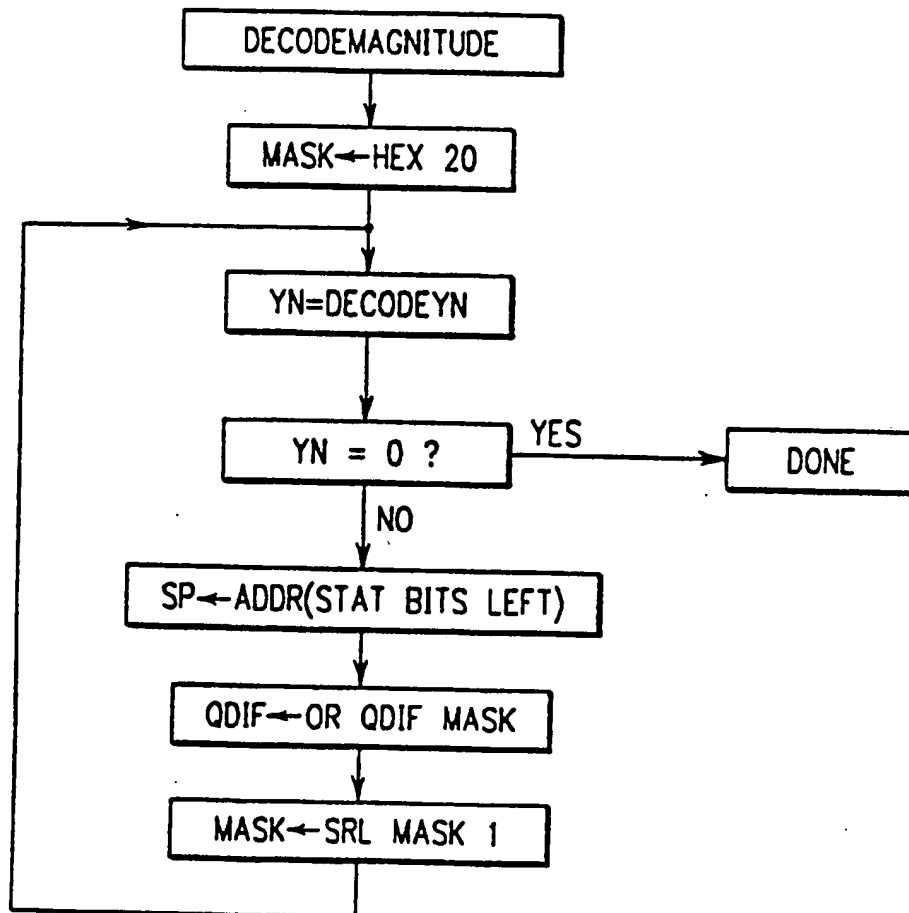


FIG.26



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12

EUROPEAN PATENT APPLICATION

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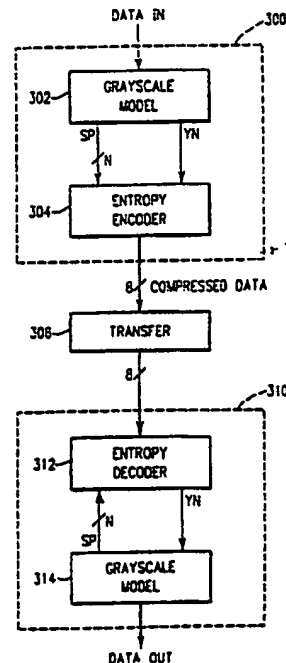
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54 Compression and decompression of column-interlaced, row-interlaced graylevel digital images.

57 In an image in which some pixels in some rows of an image have values associated therewith, apparatus and method of processing, for subsequent entropy coding or decoding, graylevel data for the remaining pixels in the image. A compressor (300) includes a graylevel model (302) and an entropy encoder (304). One input of the encoder (304) corresponds to the quantized value and its second input represents the state which points to a specific probability in a table of probabilities used to define decision context. The compressed data is communicated via a transfer element (306) to a decompressor (101) including an entropy decoder (312) which operates in an inverse fashion to entropy encoder (304). A graylevel model (314) provides a state input to the decoder (312) pointing the decoder to the same probability entry in the probability table as is pointed too in the encoder (304) during the compression. From the compressed data and the state input the entropy decoder (312) provides an output to the graylevel model element (314) which corresponds to the graylevel model (302) and is thereby able to generate an output that corresponds to the input of the compressor (300).

EP 0 283 798 A3

FIG.6





DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.4)
D, A	US-A-4488174 (MITCHELL ET AL.) * abstract * * column 3, line 50 - column 6, line 24; figures 2, 3 *	1-21	H04N7/137 H03M7/40
A	IBM JOURNAL OF RESEARCH AND DEVELOPMENT. vol. 28, no. 2, March 1984, NEW YORK US pages 135 - 149; Langdon G.: "AN INTRODUCTION TO ARITHMETIC CODING" * page 135, column 1, line 10 - page 136, column 2, line 29 *	1, 4, 7-13, 17, 19-21	
			TECHNICAL FIELDS SEARCHED (Int. Cl.4)
			H04N H03M
The present search report has been drawn up for all claims			
Place of search BERLIN		Date of completion of the search 10 OCTOBER 1990	Examiner MATERNE, A
CATEGORY OF CITED DOCUMENTS X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons & : member of the same patent family, corresponding document			

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(12) **EUROPEAN PATENT SPECIFICATION**

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(51) Int Cl.7: **H03M 7/30, G11B 20/10, G11B 20/00**
(21) Application number: **93307149.0**
(22) Date of filing: **10.09.1993**

(54) **Data compression/decompression and storage of compressed and uncompressed data on a single data storage volume**
Datenkompression/-dekompression und Speicherung von komprimierten und nicht komprimierten Daten in einem einzigen Datenspeichervolumen
Compression/décompression de données et stockage de données comprimées et non-comprimées sur un seul volume de stockage de données

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(56) References cited:
EP-A- 0 490 239 **WO-A-91/19255**
US-A- 4 506 303
• **IBM TECHNICAL DISCLOSURE BULLETIN, vol. 22, no. 9, February 1980 NEW YORK, US, pages 4191-4193, ANONYMOUS 'Data Compaction Storage System. February 1980.'**
• **IBM TECHNICAL DISCLOSURE BULLETIN, vol. 24, no. 7A, December 1981 NEW YORK, US, pages 3202-3203, ANONYMOUS 'Compacting Indexed Data. December 1981.'**
• **IBM TECHNICAL DISCLOSURE BULLETIN, vol. 33, no. 9, 1 February 1991 pages 158-164, XP 000109445 'COMPRESSED SEQUENTIAL DATA ON A FIXED BLOCK DEVICE'**
• **IBM TECHNICAL DISCLOSURE BULLETIN, vol. 33, no. 9, February 1991 NEW YORK, US, pages 158-164, ANONYMOUS 'Compressed Sequential Data On a Fixed Block Device.'**

EP 0 587 437 B1

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Description

FIELD OF THE INVENTION

5 **[0001]** This invention relates to data storage systems that are capable of storing both compressed and uncompressed data on one data storage volume and to data processing systems utilizing such data storage systems. This invention also relates to data storage systems that minimize wasted data storage space on a data storage volume while storing compressed data.

10 BACKGROUND OF THE INVENTION

[0002] Many data storage media, such as data storage optical disks, have a so-called fixed block architecture (FBA) format. Such format is characterized in an optical disk by so-called hard sectoring the disk's single spiral track into a plurality of sectors. Everyone of the sectors have identical data storage capacity, i.e. 512 bytes, 1024 bytes, 4096
15 bytes, etc. Because of the FBA disks and the variability of data lengths of compressed data with respect to the source uncompressed data, in-line data compression has not been employed with FBA formatted disks. It is desired to efficiently store and enable simple random address accessing of a variable amount of compressed data resulting from compressing data which has been formatted into addressable blocks. Such compressed data can then be recorded on a FBA formatted disk. If the sector data does not compress to fewer bytes, then the data are stored without data
20 compression on the data storage disk.

[0003] It is also desired when a plurality of addressable data blocks is segmented into a plurality of groups of such data blocks, to maintain host processor addressability of the compressed data blocks within each compressed group of data blocks. It is also desired when compressing data for storage on a FBA storage medium to maintain a maximal addressability of all unused data storing sectors even though the number of sectors required to store the compressed
25 data blocks is unknown. A further desire is to provide for random addressing of the compressed data blocks recorded in an FBA formatted storage medium.

[0004] The data pattern randomness of most input data streams and the variability in the resulting length of the compressed data output after the application of the various compression algorithms, does not allow for the prediction of the amount of storage space required to contain the compressed data. This situation requires a link between the
30 transmission of the data stream to be compressed and recorded and the results of the compression process to assist the host processor in its storage management process.

[0005] The function of updating a data file in this environment can not use any usual data updating process (read, update, write back) because the data pattern as a result of the update may not compress to the same degree as the original data block and therefore updated compressed data most probably will not fit in the original storage space
35 required to store the original data.

[0006] In a fixed block architecture (FBA) environment, data are recorded on a data storage medium in fixed sized units of storage called sectors where each recording track on the medium contains a fixed number of such sectors. The addressing convention for optical disk devices consists of a track address on the medium and a sector number of the particular track. On optical media storage devices, each of the sectors consists of two major parts; an Identification
40 field (ID) used by the device controller to locate a particular sector by a physical address and a data field for storing data. The informational content of the ID's on hard sectored optical disks are indelibly recorded, as by a stamping/molding process, on the medium at the time of manufacture. Other data storage formats also are usable to practice the present invention, such as the known count-key-data (CKD) and extended count-key-data (ECKD) formats used on many magnetic disk media.

[0007] An FBA device attached to a host via the known Small Computer Standard Interface (SCSI) must provide the capability to resolve a Logical Block Address (LBA) used by SCSI architected direct-access data storage devices to address fixed sized units of storage to a unique physical address (track and sector) on the medium. The SCSI attached
45 FBA device provides to the host a contiguous address space of N (N is a positive integer) storage locations which can be accessed for reading or writing in any sequence. Each LBA directory structure (addresses ranging from 0 to N) is the addressing mechanism used to store and retrieve data blocks in the SCSI-FBA environment (some FBA devices also provide the capability to address the storage space using the physical address).

[0008] As can be seen from the preceding paragraphs, the principal problem facing a designer of a storage system using data compression techniques in the SCSI-FBA environment is to provide a mechanism by which fixed size units of data, herein termed data blocks, in an input data stream can be recorded in a variable amount of storage medium
50 space and still maintain addressability to the unoccupied storage space and provide for addressability to the recorded data blocks.

[0009] Since many optical disks today are of the removable type, it is further desired to enable each removable data storage medium to be self-describing as to compressed and uncompressed data held thereon.

DISCUSSION OF THE PRIOR ART

5 [0010] The Vosacek US patent 4,499,539 shows first allocating a number of data storage segments of a cache or buffer for storing a maximum number of data bytes that are storable in an addressable track of a direct access storage device (DASD) connected to the cache or buffer. The DASD is a magnetic disk storage device. The protocol is to stage or transfer one track of DASD data to the cache or buffer in one input-output operation (one access to the DASD). Upon completion of the actual data transfer, the cache or buffer is examined. If less than all of the first allocated segments contain data, then the empty allocated segments are deallocated. Pointers are recorded in a first one of the allocated segments for pointing to additional allocated segments that store data from the same DASD track. In this manner the DASD track is emulated in the cache or buffer.

10 [0011] US Patent No 5097261 (application No USSN 07/441,126) shows a data compaction system for a magnetic tape peripheral data storage system. Tapes do not have any addressable data storage areas. The entire tape is formatted each time it is recorded. This formatting feature in magnetic tapes enables storing variably sized records as variably sized blocks of data. The storage of uncompressed and compressed data is by addressable blocks of such data. The application does show including a plurality of records in one block of data recorded on the tape. Co-pending commonly-assigned US patent No 5 200 864 (application USSN 07/372,744, filed 6/28/89, (Attorney docket TU989003)) shows a magnetic tape data storage system that automatically stores a plurality of small records in each block of recorded data. Each of the records remain individually addressable. A purpose of combining a plurality of records in one block is to reduce the number of inter-block gaps for increasing the storage capacity of the magnetic tape.

15 [0012] Data compression and decompression algorithms and systems are well known. US patent 5109226 shows an in line (real time) data compression/decompression system for use in high speed data channels. This system uses an algorithm shown in the Langdon, Jr. et al US patent 4,467,317. Batch processed (software) data compression and decompression is also well known. PKWARE, Inc., 7032 Ardara Avenue, Glendale WI 53209 USA provides the software programs PKZIP for batch compression, PKUNZIP for batch decompression among other compression-decompression software. Another data compression-decompression algorithm has been used for both batch (software processing) and in-line (hardware-integrated semiconductor chips) processing. The known Lempel Ziv-1 data compression/decompression algorithm is used for both in-line (real time) and batch data compression and decompression. It is preferred to use the latter algorithm. Shah and Johnson in the article DATA COMPRESSOR DECOMPRESSOR IC in the "1990 IEEE International Symposium on Circuits and Systems, New Orleans LA USA (pp 41-43) on May 1-3, 1990 describe an integrated circuit using the known Lempel-Ziv algorithm mentioned above. In practicing the present invention, it is preferred that a compression-decompression algorithm that facilitates both batch and in line operations be used. Of course, only batch or only in line data compression-decompression may be used to successfully practice the present invention.

20 [0013] Images or "non-coded" data have been compressed and decompressed for saving data storage space. Reitsma US patent 4,622,585 shows one video compression scheme.

25 [0014] WO91/19255 discloses storing compressed data to disk, using a logical block size smaller than the physically formatted block size. A user sets an estimated compression ratio which determines a fixed logical block size from the size of physical disk sectors, and compressed data is stored in the logical block. When a block of compressed data is too large to fit within a single logical block, an overflow condition occurs and the overflow data is stored in other physical blocks. A table stores information linking the blocks that contain data from a compressed data block.

30 [0015] EP-A-0490239 discloses a random access storage device, formatted to provide multiple predefined partitions with different block sizes. The data to be stored is in blocks of fixed size, and these blocks are compressed if the compressed size fits in the block size of a small partition in the storage device. If a data block is not compressible to the small block size, it is stored uncompressed in another of the partitions. The memory device contains a table storing the locations of the blocks in the partitions.

35 [0016] US 4,506,303 discloses an optical data recording system and method for receiving an input data stream to be recorded, dividing the input data stream into sections, compressing each section into a period shorter than the original section, providing data gaps between each compressed data section, and recombining the compressed data including data gaps into a gapped output stream, and recording the gapped output data. This enables accurate data retention when using butted or staggered CCD arrays.

SUMMARY OF THE INVENTION

40 [0017] The present invention provides flexible data compression-decompression controls that enable randomly accessing compressed data through relatively simple accessing mechanisms.

45 [0018] According to a first aspect, the present invention provides apparatus for storing data in compressed form in a data storage device having a plurality of addressable like-sized data storage areas, each for recording a predetermined number of data bytes, the data storage device being connected to means for receiving data to be recorded, said

received data being arranged in a plurality of addressable data blocks, characterised in that the apparatus comprises, in combination: selection means in the means for receiving data for selecting one or more data transfer units of data blocks to be recorded, each said transfer unit of data blocks having a given number of data bytes and including one or more of said addressable data blocks; allocation means connected to the selection means for responding to the number of data bytes in each said transfer unit of data blocks to determine, based on said number of data bytes, a required first number of addressable data storage areas for storing said transfer unit of data blocks, and to indicate that said transfer unit requires said first number of addressable data storage areas to record said transfer unit; compression means connected to the selection means for compressing said transfer unit of data blocks to be recorded as a group of compressed data blocks; data access means in the device connected to said compression means for recording said group of compressed data blocks in a second number of said addressable data storage areas as one continuum of compressed data, said second number being equal to or less than said first number; and directory means indicating which ones of said addressable data storage areas said continuum of data is recorded in, and indicating that said continuum of data contains said selected transfer unit of data blocks in a compressed form.

[0019] In a second aspect of the present invention there is provided a method of compressing and recording onto a data storage medium data of a file which is arranged in a plurality of addressable data blocks, the method comprising the steps of: selecting a plurality of said data blocks of said file to be compressed and recorded; segmenting the selected plurality of addressable data blocks into one or more data transfer units, each data transfer unit of data blocks having a given number of data bytes and including one or more of said addressable data blocks; allocating a first number of addressable data storage areas of the storage medium for recording each of said one or more data transfer units as respective separate groups of compressed data blocks, said first number being determined based on the number of data bytes in each of said one or more data transfer units; compressing each of said one or more data transfer units and recording them as respective separate groups of compressed data blocks in a second number of addressable data storage areas of the storage medium, said second number being equal to or less than said first number; creating and maintaining a file directory indicating the address and size of each of said recorded groups for enabling random access to recorded data within said file of data blocks.

[0020] Preferably, the file directory provides information for addressing each of the compressed data blocks within a group. It is further preferred that the directory is maintained in a host processor and is also stored on the data storage medium containing the group of compressed data blocks.

[0021] In a preferred embodiment of the present invention, a data file having a plurality of addressable data blocks is segmented into a plurality of groups of such data blocks. Each group of data blocks is separately compressed and decompressed as one unit of data. Each such group is separately transmitted between a host processor and a data storage unit, communications link, etc as one data transfer unit (DTU). The size of the DTU, in terms of the number of data blocks to be included, is determined empirically based upon the data storage capacity of (number of data bytes storable in) sectors into which a data storage volume is divided, the number of bytes in each of the data blocks of the data file, and other system parameters. The data storage of each group in compressed form in a data storage device is described by the data storage system to the host processor, preferably by a command linked to the host processor command effecting the data storage in compressed form. The host processor establishes a directory describing the storage of each and every group of the data file. If the data file is transferred to another system or host processor in the compressed form, the compressed data file directory accompanies the compressed groups. Retrieving compressed data from a data storage device is by retrieving the group of data blocks having the data block(s) desired to be read. Each compressed group of data blocks is transferrable between host processors and data storage units without decompression. The DTU or group-receiving data storage medium may be formatted in the well known fixed-block architecture (FBA) format, the well known count-key-data (CKD) format, the well known extended count-key-data (ECKD) format or any other format.

[0022] Embodiments of the present invention will now be described in more detail, with reference to the accompanying drawings in which:

Fig. 1 is a flow chart illustrating data storing operations according to an embodiment of the present invention;

Fig. 2 is a simplified block diagram of a data processing system in which the data storing operations according to Fig. 1 may be advantageously employed;

Fig. 3 is a diagrammatic representation of a Logical Block Address (LBA) directory for identifying recorded compressed groups of data blocks of a data file;

Fig. 4 is a block diagram showing details of an optical data storage system attached to a host processor such as is shown in Fig. 2;

Fig. 5 is a block diagram of a peripheral controller usable in data processing systems such as are shown in Fig's 2 and 4;

Fig. 6 diagrammatically illustrates storing a compressed group of data blocks according to the steps of Fig. 1;

Fig. 7 diagrammatically illustrates host processor commands using a SCSI connection to a data storage system such as is shown in Fig. 2 or Fig. 4;

Fig. 8A diagrammatically illustrates a file directory of a plurality of compressed groups of data blocks of a file according to an embodiment of the present invention;

Fig. 8B diagrammatically illustrates the format of a disk sector according to an embodiment of the present invention;

Fig's 9-13 are flow charts showing details of the operation shown in Fig. 1;

Fig. 14 is a logic diagram illustrating an application of the present invention to a multi-unit data processing system that has a plurality of data storage devices and host processors interconnected by a data link or local area network; and

Fig. 15 is a flow chart showing machine operations that update a compressed data file according to an embodiment of the present invention.

DETAILED DESCRIPTION

[0023] Referring now more particularly to the appended drawings, like numerals indicate like parts and structural features in the various figures. A data file having a plurality of data blocks is divided into one or more transfer units of data blocks. Before data storage, each transfer unit of data blocks is subjected to its own data compression cycle to create a group of compressed data blocks. The size of the data transfer unit, in bytes, is selected to be facile for addressing and retrieving individual recorded groups of compressed data blocks while providing good channel utilization and compression efficiency. Also the data transfer unit size is selected in part based upon data storage efficiency, i.e. the storage of the data, after compression, should fill several allocated addressable data storage areas. Each of the allocated sectors in each group is filled to capacity except the last sector of a group that may be partially filled. It is desired to reduce the number of partially filled data storage sectors for more efficiently filling the FBA data storage disk with data. This desire is balanced with enabling efficient random access to the compressed data blocks stored on the FBA data storage disk.

[0024] Each stored or recorded group of compressed data blocks is accessed from disk 30 as a single data unit irrespective of the number of disk 30 sectors in which the group is recorded. Since each group of compressed data blocks is compressed in a separate data compression operation, all of the data in each such group must be decompressed starting with the beginning, i.e. first compressed bytes, in each group. Therefore, in randomly accessing a compressed desired data block in a given group, all of the compressed data blocks of each stored group are read from disk 30 as a single disk record. The single disk record is decompressed up to the desired or addressed compressed data block. The desired compressed data block is then decompressed for processing. Limiting the size of the groups of compressed data blocks provides for quicker access to any desired compressed data block. This desire is balanced with a desire to maximize utilization of the disk 30 data storage space. An example of managing these two parameters for creating a facile size group of compressed data blocks (that varies with each application) is described later.

[0025] In an alternate arrangement, each data block is separately compressed. A plurality of such separately compressed data blocks are combined into a single disk record. The byte position within the single disk record for each of the separately compressed data blocks is recorded in the single disk record. Such byte position or offset enables addressing each of the compressed data blocks within a group.

[0026] To facilitate access to the groups of compressed data blocks, the host processor program maintains a directory that identifies the addressable data storage areas containing the group as well as the data blocks in the respective groups. This directory identification preferably takes the form of a file directory that is maintained in host processor 11. Such directory is also stored on the volume or data storage disk containing the group(s) of compressed data blocks. Preferably, the directory is transmitted to the disk device as a part of each transfer of a compressed file having plural groups of compressed data blocks. This arrangement establishes on the FBA disk a directory that effects addressability of the compressed data blocks within the respective groups.

[0027] Fig. 1 illustrates recording a data file by grouping a plurality of data blocks of the file into a smaller number of groups of compressed data blocks. Step 10 is executed in a host processor 11 (Fig. 2). A data file, or part of a data

file, is identified for compressed data storage. The data file consists of a plurality of data blocks. The term data block includes data records (coded data), sub-file structures, individual images, graphs and the like, drawings and other forms of graphics, combined graphics (non-coded data) and text(coded data), and the like. As later detailed, the data file is divided into facile sized groups of data blocks for transfer as a data transfer unit DTU to a storage unit or over a communication link and for maintaining a random access capability to the recorded groups of compressed data blocks. The size of each DTU and resultant recorded group is dependent on diverse variables, as will become apparent. Completion of one execution of step 10 results in one such group of data blocks being selected for compression and storage.

[0028] Step 13 is executed by host processor 11 (Fig. 2). The number of uncompressed data bytes in the DTU of data blocks (the product of the number of data blocks times the number of bytes in each data block) is divided by the data storage capacity of one addressable data storage area (sector of an FBA formatted disk) and rounded to a next higher integer if the product includes a fraction. This number represents a maximum number of addressable data storage areas required to store the data; either uncompressed or if a compression does not compress the data into fewer bytes for storage. At this juncture, it is not known how many addressable data storage areas are required to store the group of data blocks after compression. To ensure that the group of data blocks is storable on the data storage medium (optical disk 30 is used in the illustrative embodiment), a number of the addressable data storage areas sufficient to store the entire group of compressed data blocks is initially determined for storing the group of data blocks in an uncompressed form.

[0029] Step 15 is executed by both the host processor 11 and data storage system 12. The selected DTU of data blocks is transmitted by the host processor to the data storage system. The data compression of the selected DTU of data blocks is compressed before storage on the data storage medium 30 (Fig. 4). There are several methodologies that may be employed herein. The Fig. 1 indicated methodology requires the data storage system to allocate the maximum number of addressable data storage areas. Then the data transfer occurs requiring the data storage system to compress the selected DTU of data blocks just before the data are recorded on the data storage medium 30 (Fig. 4). Upon completion of the compression and data storage or recording as one continuum of data, data storage system 12 determines the number of addressable data storage areas actually used to store the compressed group of data blocks. The unused but allocated addressable data storage areas are then deallocated. In the event that certain data blocks compress to a greater number of bytes than the original or uncompressed data, then, as will become apparent, the data compression step is not used. Control data are recorded on the FBA disk that indicates which data are compressed and which data are not compressed. Such control data are used in retrieving data from the data storage (FBA) disk, as will become apparent. As later detailed in this specification, at step 16 data storage system 12 sends the storage locations of the just-recorded group of compressed data blocks to the host processor 11 for inclusion in a directory of the data file to which the recorded group of data blocks is a member.

[0030] A second methodology has the data compression-decompression performed in host processor 11. As such, host processor 11 includes the data compression mechanism, either software or hardware, and sends the compressed selected group of data blocks to data storage system 12 for storage. In this instance, if batch compression is used, host processor determines the number of addressable data storage areas required for storing the compressed group of data blocks. Host processor 11 then sends the required number of addressable data storage areas to data storage system 12 for allocation just before the compressed data are transmitted to the data storage system.

[0031] In a third methodology, the uncompressed group of data blocks are transmitted twice by host processor 11 to data storage system 12. A first transmission enables data storage system 12 to accurately measure the number of addressable data storage areas that will be required to store the compressed data. In the first transmission the data are compressed but not recorded. The number of compressed data bytes are counted to determine the data storage extent (number of sectors or addressable areas) for the compressed data. The data storage system 12 then allocates the indicated number of contiguous sectors for receiving and storing the compressed data. A second transmission of the same data to the data storage system 12 results in the compression and storage of the compressed data in a data storage medium.

[0032] In each of the above described methodologies, if the number of bytes in the compressed file is greater than the number of uncompressed data bytes, then the data are recorded in the uncompressed form. Further, when updating a group of compressed data blocks, the number of compressed data bytes may exceed the capacity of the currently allocated sectors. As described later with respect to Fig. 15, a change in allocation of sectors for storing the updating DTU may be required.

[0033] Also, in each of the above described methodologies, the data blocks to be compressed and stored from each DTU are preferably compressed and stored as one group. That is, all data blocks in each DTU are compressed during one data compression cycle to produce one group of compressed data blocks. An alternate data compression approach is to individually compress each of the data blocks in each DTU. Then the group of compressed data blocks consists of a plurality of individually compressed data blocks. In the alternative data compression, a header in each group can identify the byte offset within each group of the individually compressed data blocks. Such individually compressed

data blocks may also be identified on the data recording disk by illegal recording code characters, such characters are well known for diverse data recording codes.

5 **[0034]** Host processor 11 in step 19 logically associates all recorded groups of compressed data blocks via a later described file directory. When employing the above described first methodology, upon storing the compressed data, data storage system 12 reports to host processor 11 the actual number of sectors used to store the compressed data and further address and identifying data therefore, as will be described.

10 **[0035]** At step 20, host processor 11 determines whether all of the data to be compressed and recorded have been recorded. The details regarding the recorded group of compressed data blocks (see step 19) have been entered into the later described file directory (Fig. 8A). If all of the above described machine operations have been completed, then the operation is "done", enabling exiting to other machine operations beyond the present description. Otherwise, steps 10-19 are repeated as above described until all of the data have been compressed and recorded. It is to be noted that other machine operations may be performed by host processor 11 in a multi-tasking or interrupt driven data processing environment while steps 10-19 are in the process of execution as is known in the data processing art.

15 **[0036]** Fig. 2 shows a data processing system in simplified form. Host processor 11 attaches a data storage system 12. Data storage system 12 includes a peripheral control 20 that connects host processor 11 to data storage device 21. Device 21, in one embodiment of this invention, is a magneto-optical data storage device that operates with removable magneto-optical data storage media or a single medium (disk). As later used in this specification, the term programmed machine includes host processor 11, peripheral controller 20 and programmed portions of data storage device 21. The compression-decompression mechanisms are preferably in the programmed machine. For in-line compression-decompression, it is preferred that the compression-decompression occurs in the peripheral controller 20. As later described with respect to Fig. 14, the location of the compression-decompression mechanism can be anywhere in the programmed machine. For batch compression-decompression it is preferred to place the compression-decompression in host processor 11.

20 **[0037]** Fig. 3 illustrates a logical block address (LBA) structure 23 used in magneto-optical disk data storage systems for addressing sectors of an optical disk. LBA 23 is a logical to real address translation mechanism that enables full advantage of practicing the present invention. This sector addressing is based upon the logical addressing found in many present day optical disk data storage devices. The attaching host processor 11 addresses data on disk 30 (Fig. 4) using a logical block address included in LBA 23. LBA 23 determines which of the addressable physical data storage addressable areas, such as sectors, are addressed by the respective LBA address. In an alternate addressing arrangement, host processor 11 requests access to a named file. This alternate addressing arrangement includes host processor 11 identifying byte location within the file to begin a data operation and a number of bytes (byte length) to be subjected to the data operation, i.e. read from the disk, for example.

25 **[0038]** LBA 23 is managed by either one of two algorithms. A first one has been used for optical disks. In this algorithm, the number of entries in LBA 23 is constant for each disk and is based upon the number of addressable entities in the disk designated for storing data. Spare addressable data storage areas or sectors are not included in the LBA 23 logical address sequence, as is known. Known secondary pointers enable addressing spare sectors via LBA 23.

30 **[0039]** A second algorithm for addressing using LBA 23 is used in magnetic flexible diskettes. In this second algorithm, the address range of LBA 23 varies with the number of demarked or unusable sectors. LBA 23 identifies for addressing only the tracks and sectors that are designated for storing data. In the event one of the sectors identifiable by the illustrated address translation becomes unusable, then the unusable or defective sector is skipped and replaced by another sector. Such substitution is well known.

35 **[0040]** All of the addressable tracks and sectors on disk 30 are addressed via LBA 23. Such addressing is a table look up matching the host processor 11 supplied logical address to a physical disk track and sector storing the data identified by the supplied logical address. Each LBA logical address has one entry 14 in LBA 23.

40 **[0041]** Numerals 17 and 18 indicate groups of compressed data blocks recorded on disk 30 using the present invention. Numeral 17 indicates the first group of compressed data blocks of one file. Numeral 18 indicates subsequently recorded groups of compressed data blocks from the same file. The enumeration of the data blocks in the recorded groups 17-18 is maintained in its original sequence as generated by host processor 11. As will become apparent, the compressed data blocks in the respective groups are identified in a file directory shown in Fig. 8A.

45 **[0042]** A magneto-optic data storage drive or device 21 is illustrated in Fig. 4 as it is connected to host processor 11 via peripheral controller 20. As usual, peripheral controller 20 is packaged with the optical disk drive. A magneto-optic record disk 30 is removeably mounted for rotation on spindle 31 by motor 32. A usual disk cartridge receiver (not shown) is in operative relation to spindle 31 for inserting and ejecting magneto optical or other optical disks 30 into and from drive 21. Optical portion 33 of drive 21 is mounted on frame 35. A headarm carriage 34 moves radially of disk 30 for carrying an objective lens 45 from track to track. A frame 35 of recorder suitably mounts carriage 34 for reciprocating radial motions. The radial motions of carriage 34 enable access to any one of a plurality of concentric tracks or circumventions of a spiral track for recording and recovering data on and from the disk. Linear actuator 36 suitably mounted on frame 35, radially moves carriage 34 for enabling track accessing. The recorder is suitably attached

to one or more host processors 11, such host processors may be control units, personal computers, large system computers, communication systems, image signal processors, and the like. Attaching circuits 38 provide the logical and electrical connections between the optical recorder and peripheral controller 20.

[0043] Device microprocessor 40 controls device 21 including the attachment circuits connected to peripheral controller 20. Control data, status data, commands and the like are exchanged between attaching circuits 38 and device microprocessor 40 via bidirectional bus 43. Included in micro-processor 40 is a program or microcode-storing, read-only memory (ROM) 41 and a data and control signal storing random-access memory (RAM) 42.

[0044] The optics of the recorder(drive or device) 21 include an objective or focusing lens 45 mounted for focusing and radial tracking motions on headarm 33 by fine actuator 46. This actuator includes mechanisms for moving lens 45 toward and away from disk 30 for focusing and for radial movements parallel to carriage 34 motions; for example, for changing tracks within a range of 100 tracks so that carriage 34 need not be actuated each time a track adjacent to a track currently being accessed is to be accessed. Numeral 47 denotes a two-way light path between lens 45 and disk 30.

[0045] In magneto-optic recording, magnetic bias field generating coil 48. In a constructed embodiment electromagnet provides a weak magnetic steering or bias field for directing the remnant magnetization direction of a small spot on disk 30 illuminated by laser light from lens 45. The laser light spot heats the illuminated spot on the record disk to a temperature above the Curie point of the magneto-optic layer (not shown, but can be an alloy of rare earth and transitional metals as taught by Chaudhari et al., USP 3,949,387). This heating enables magnet coil 48 generated bias field to direct the remnant magnetization to a desired direction of magnetization as the spot cools below the Curie point temperature. Magnet coil 48 is shown as supplying a bias field oriented in the "write" direction, i.e., binary ones recorded on disk 30 normally are "north pole remnant magnetization". To erase disk 30, magnet coil 48 supplies a field so the south pole is adjacent disk 30. Magnet coil 48 control 49 is electrically coupled to magnet coil 48 over line 50 to control the write and erase directions of the coil 48 generated magnetic field. Microprocessor 40 supplies control signals over line 51 to control 49 for effecting reversal of the bias field magnetic polarity.

[0046] It is necessary to control the radial position of the beam following path 47 such that a track or circumvolution is faithfully followed and that a desired track or circumvolution is quickly and precisely accessed. To this end, focus and tracking circuits 54 control both the coarse- actuator 36 and fine actuator 46. The positioning of carriage 34 by actuator 36 is precisely controlled by control signals supplied by circuits 54 over line 55 to actuator 36. Additionally, the fine actuator 46 control by circuits 54 is exercised through control signals travelling to fine actuator 46 over lines 57 and 58, respectively for effecting respective focus and track following and seeking actions. Sensor 56 senses the relative position of fine actuator 46 to headarm carriage 33 to create a relative position error (RPE) signal. Line 57 consists of two signal conductors, one conductor for carrying a focus error signal to circuits 54 and a second conductor for carrying a focus control signal from circuits 54 to the focus mechanisms in fine actuator 46.

[0047] The focus and tracking position sensing is achieved by analyzing laser light reflected from disk 30 over path 47, thence through lens 45, through one-half mirror 60 and to be reflected by half-mirror 61 to a so-called "quad detector" 62. Quad detector 62 has four photoelements which respectively supply signals on four lines collectively denominated by numeral 63 to focus and tracking circuits 54. Aligning one axis of the detector 62 with a track center line, track following operations are enabled. Focusing operations are achieved by comparing the light intensities detected by the four photoelements in the quad detector 62. Focus and tracking circuits 54 analyze the signals on lines 63 to control both focus and tracking.

[0048] Recording or writing data onto disk 30 is next described. It is assumed that magnet 48 is rotated to the desired position for recording data. Microprocessor 40 supplies a control signal over line 65 to laser control 66 for indicating that a recording operation is to ensue. This means that laser 67 is energized by control 66 to emit a high-intensity laser light beam for recording; in contrast, for reading, the laser 67 emitted laser light beam is a reduced intensity for not heating the laser illuminated spot on disk 30 above the Curie point. Control 66 supplies its control signal over line 68 to laser 67 and receives a feedback signal over line 69 indicating the laser 67 emitted light intensity. Control 68 adjusts the light intensity to the desired value. Laser 67, a semiconductor laser, such as a gallium-arsenide diode laser, can be modulated by data signals so the emitted light beam represents the data to be recorded by intensity modulation. In this regard, data circuits 75 (later described) supply data indicating signals over line 78 to laser 67 for effecting such modulation. This modulated light beam passes through polarizer 70 (linearly polarizing the beam), thence through collimating lens 71 toward half mirror 60 for being reflected toward disk 30 through lens 45. Data circuits 75 are prepared for recording by the micro-processor 40 supplying suitable control signals over line 76. Microprocessor 40 in preparing circuits 75 is responding to commands for recording received from a host processor 11 via attaching circuits 38. Once data circuits 75 are prepared, data is transferred directly between peripheral controller 20 and data circuits 75 through attaching circuits 38. Data circuits 75, also ancillary circuits (not shown), relating to disk 30 format signals, error detection and correction and the like. Circuits 75, during a read or recovery action, strip the ancillary signals from the readback signals before supply corrected data signals over bus 77 to peripheral controller 20 via attaching circuits 38.

[0049] Reading or recovering data from disk 30 for transmission to host processor 11 requires optical and electrical processing of the laser light beam from the disk 30. That portion of the reflected light (which has its linear polarization

from polarizer 70 rotated by disk 30 recording using the Kerr effect) travels along the two-way light path 47, through lens 45 and half-mirrors 60 and 61 to the data detection portion 79 of the headarm 33 optics. Half-mirror or beam splitter 80 divides the reflected beam into two equal intensity beams both having the same reflected rotated linear polarization. The half-mirror 80 reflected light travels through a first polarizer 81 which is set to pass only that reflected light which was rotated when the remnant magnetization on disk 30 spot being accessed has a "north" or binary one indication. This passed light impinges on photocell 82 for supplying a suitable indicating signal to differential amplifier 85. When the reflected light was rotated by a "south" or erased pole direction remnant magnetization, then polarizer 81 passes no or very little light resulting in no active signal being supplied by photocell 82. The opposite operation occurs by polarizer 83 which passes only "south" rotated laser light beam to photocell 84. Photocell 84 supplies its signal indicating its received laser light to the second input of differential amplifier 85. The amplifier 85 supplies the resulting difference signal (data representing) to data circuits 75 for detection. This detection, in the illustrated embodiment, does not include digital demodulation (decoding the read back signals from a 1-7 d-k code to data in a host processor format). The detected signals include not only data that is recorded but also all of the so-called ancillary signals as well. The term "data" as used herein is intended to include any and all information-bearing signals, preferably of the digital or discrete value type.

[0050] The rotational position and rotational speed of spindle 31 is sensed by a suitable tachometer or emitter sensor 90. Sensor 90, preferably of the optical-sensing type that senses dark and light spots on a tachometer wheel (not shown) of spindle 31, supplies the "tach" signals (digital signals) to RPS circuit 91 which detects the rotational position of spindle 31 and supplies rotational information-bearing signals to microprocessor 40. Microprocessor 40 employs such rotational signals for controlling access to data storing segments on disk 30 as is widely practiced in the magnetic data storing disks. Additionally, the sensor 90 signals also travel to spindle speed control circuits 93 for controlling motor 32 to rotate spindle 31 at a constant rotational speed. Control 93 may include a crystal-controlled oscillator for controlling motor 32 speed, as is well known. Microprocessor 40 supplies control signals over line 94 to control 93 in the usual manner.

[0051] Peripheral controller 20 is shown in Fig. 5 This controller includes the compression-decompression mechanism for in-line or real time data compression-decompression. A connection between host processor 11 and peripheral controller 20 is effected by a SCSI module 100 that implements the known small computer system interface. An IO data buffer 103(dynamically allocated into input data buffers and output data buffers using known techniques) temporarily stores data received from or to be transmitted to the host processor 11. An Optical Disk Controller (ODC) 104 manages the reading and writing of the data to the disk 30 (Fig.4). Error Correction Control (ECC) module 106 detects and corrects errors in data being read and generates ECC error detection and correction redundancy characters to be written to the medium with the data. Run Length Limited (RLL) (mod-demod) encoding and decoding is performed in data circuits 75 (Fig. 4). Such mod-demod encodes and decodes recorded data patterns, such as used in the known 1-7 d-k code. Microprocessor 107 (plus control store 108 and dynamic store 109) controls the various elements of the controller 20. A Compression/Decompression (CD) module 101, such as an integrated circuit referred to by Shah et al, supra, implements the compression algorithms. CD module 101 includes automatic circuit timing and control, as is known, to control data flow through peripheral controller 20 under supervision of microprocessor 107. This compression-decompression is in real time (in-line) with the data transfer. Busses 102, 110 and 111 interconnect the modules, as shown. Controller 20 is preferably packaged with a device 21 on a common frame.

[0052] Fig. 6 illustrates compression of several data blocks into one group of compressed data blocks recorded in a number of data storing sectors 118 of track 117 of disk 30. A group 115 of a plurality of data blocks 116 is selected for recording as described with respect to Fig. 1. Group 115 of compressed data blocks is transmitted to controller 20 by host processor 11. CD 101 in controller 20 compresses group 115 sufficiently to be recorded as a group of compressed data blocks in sectors 118 plus about one-half of sector 119. The remaining half of last sector 119 is filled with padding bytes, as is known. Numeral 122 indicates a sector that was allocated previously. Numeral 123 indicates a next sector(s) that were initially allocated according to the above-described first methodology. The linked response of controller 20 to the write-compress command indicates to host processor 11 that sector(s) 123 are to be deallocated as such sectors did not receive any of the data from group 115. Host processor 11 responds to controller 20 to deallocate sectors 123.

[0053] The above description assumes that host processor 11 is performing data space management. This arrangement is usual. It is to be pointed out that in a multi-host arrangement of sharing device 21 that one of the hosts may be designated to perform space management. Also, in some systems the peripheral controller performs data storage space management.

[0054] Fig. 7 illustrates in abbreviated form three commands for use in a known SCSI interface. WRITE command 130 includes the operation code field 131 that indicates the command is a WRITE command. LBA address field 132 indicates the first LBA address that data being transmitted in accordance with the instant WRITE command is to begin (the lowest LBA address of possibly several LBA addresses required to be used in storing data into a plurality of disk 30 sectors). Field 133 indicates the number of units of data that are to be transferred from host processor 11 to device

21 for storage on disk 30. One unit is that data storable in one sector of the disk 30. FBA disks may have different data storing capacity sectors, such as 512, 1024 (1 kb), 2048, or 4096 bytes of data. Field 134 indicates whether or not the data to be transmitted is to be compressed. Field 135 indicates that this WRITE command is linked to read buffer command 140. This command linkage requires peripheral controller 20 to report to host processor 11 the details of the data storage, i.e. number of sectors actually used, the data that enables host processor 11 to build an entry for the later described Fig. 8A illustrated file directory, and identifies the sectors to be deallocated. It is noted that LBA 23 is updated in host processor 11 with a copy thereof recorded in a sector of disk 30. Also, a copy of the Fig. 8A illustrated file directory is recorded on disk 30, preferably in an uncompressed form at a first LBA 23 logical address that immediately precedes the first LBA address for storing compressed data.

[0055] Read buffer SCSI command 140 includes operation code field 141 that indicates the command is a READ BUFFER command. Controller 20 responds to receipt of a READ BUFFER command to transfer data from an output register(s) of IO buffer 103. Controller 20 stores the information relating to storing a group of compressed data blocks in such output buffer 103 register(s) in preparation to respond to the READ BUFFER command linked to the WRITE command 130. Field 142 indicates to controller 20 the number of sectors used to store the compressed data blocks. That is, host processor 11 knows the number of disk sectors required for storing the compressed data blocks, hence the new entry for the Fig. 8A illustrated file directory.

[0056] READ DATA command 145 has operation code field 146 having an indication that the command is a READ DATA command. The first LBA address to be used for transferring data from disk 30 to host processor 11 is indicated in field 147. Field 148 indicates the number (n) of data blocks requested or commanded to be transferred from the FBA disk to the host processor 11. Field 149 indicates to controller 20 the number (N) of disk sectors that are to be read. Field 150 indicates that decompress is either on or off. Link on bit 151 is usually reset to be inactive. For reading one group of compressed data blocks, controller 20 reads the indicated number (N) of sectors, decompresses the data blocks, then transfers the decompressed data blocks to host processor 11. Controller 20 counts the number of data blocks transferred such that when the indicated number n of field 148 is reached, the data transfer is terminated. The data block counting is also used as an integrity check.

[0057] The Fig. 8A illustrated file directory can indicate different levels of detail, the selected level is application dependent. Every file that has data blocks recorded in groups of compressed data blocks has a separate portion of the directory respectively indicated by numerals 161, 162 and 163 for three different data files. Each row 160 of each directory represents one entry. A first entry in each directory include in column 164 the filename of the file and the LBA address at which the directory is recorded on disk 30. Column 165 in the first or top most entry indicates the number of data blocks in each data transfer unit. The term data transfer unit (DTU) indicates that a given number of data blocks are to be transferred between disk 30 and host processor 11 during each data transfer. The remaining entries 160 are respectively for the transmitted and recorded groups of compressed data blocks. Again, column 164 in the respective entries indicates the first LBA address used to store the group. Column 165 indicates the number of data blocks recorded and the number of sectors used to store the respective groups of compressed data blocks on disk 30. Once all of the data blocks are compressed in a single data compress operation, the group of compressed data blocks are a continuum of data with no external indication of the data block boundaries. The decompression mechanism and associated controls identify the data block boundaries after decompression, as is known.

[0058] In addition to the information contained in the Fig. 8A illustrated file directory, additional details of each group may be provided. In such an alternate implementation of the file directory, controller 20 returns, in addition, for each group of compressed data blocks (i.e. for each respective entry of the Fig. 8A illustrated file directory) a map of the relation of data blocks and data storing sectors (uses the LBA logical address, not the actual physical location on disk 30) for each of the groups. This additional information is used by the host to manage the recorded data and unused disk 30 sectors indicated in LBA 23.

[0059] All entries contain the above indicated mapping of data blocks to LBA addresses for each and every group (Gp.) of compressed data blocks in the current file. That is, each data block is indicated as being recorded in one or more sectors, depending on the compression and size of the data blocks. Several compressed data blocks may be recorded in one sector. In this instance, the LBA addresses are the same for starting and ending, i.e. LBA₁₀ to LBA₁₀ for example could occur for several data blocks.

[0060] A format of the Fig. 8A illustrated directory using the additional addressing information is set forth below.

First entry	Filename	Number of data blocks in a data transfer unit
Second entry	Gp. 1 LBA	Number of data blocks and sectors in this group
	data block n	LBA N at byte B
	data block n+1	LBA N at byte B ²
	data block n+2	LBA N ₂ at byte B ³

(Map of all data blocks in group (Gp.) 1 continues, term "byte" indicates byte displacement of the respective compressed data block as recorded in a sector.)

Third entry	Gp. 2 LBA	Number of data blocks and sectors
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(Map of data blocks to LBA addresses is set forth above)

[0061] The super scripts merely indicate 1st (no super script), second, etc byte positions of the respective blocks n, n+1, n+2 etc.

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[0062] The above described directory structures enable the data contents of a single group of compressed data blocks to be updated without the necessity of reading and then rewriting the entire file. An update of a group of compressed data block only requires the reading of one group of compressed data blocks. The update group of compressed data blocks may require more sectors for storage than that use to store the previous generation group of compressed data blocks. That is additional sectors have to be allocated. Since it is desired that each group of compressed data blocks are recorded in contiguous sectors (except of unaddressable intervening defective sectors), a new allocation may be required. All of this activity is explained later with respect to Fig. 15. Host processor 11 uses this information to determine the next available set of contiguous LBA addresses that have sufficient number of addresses (sectors) for storing the updated group of compressed data blocks.

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[0063] For WORM (write once, read many) optical disks, the host processor may issue a MEDIUM SCAN command to locate the next available LBA addressed sector for storing the updated group of compressed data blocks. Host processor 11 saves this information in an expanded directory entry for use when the data are to be retrieved or read.

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[0064] As later described with respect to Fig. 10, another control parameter is a minimum or maximum number of sectors to be used in the CKD and ECKD examples for practicing the present invention. The number N of sectors required to store the uncompressed data is compared with a MIN (minimum value) and a MAX (maximum value). If the number of required sectors is between the MIN and MAX values, then a DTU is made using the number N. MIN ensures a reasonable usage of disk storage space while MAX ensures a reasonable access to compressed data blocks. If N is greater than MAX, then N is made equal to MAX. If N is less than MIN, then N is made equal to MIN. The number of data bytes in a DTU is $N \cdot SB$ (SB is number of bytes storable in one sector) for FBA devices and $N \cdot DB$ (DB is number of data bytes desired for storing one data block) for CKD and ECKD devices. The number of bytes in a DTU is stored in the first or top entry 160 (Fig. 8A) of each file directory. As one variation, field 166 in each of the entries 160 contains a compress DTU indicating bit C. If C is unity, then the data represented by the respective entry 160 are recorded in a compressed form. If bit C is zero or nil, then the data are recorded on disk 30 without data compression. The compressed bit C may also be recorded in each and every sector storing data in accordance with the present invention.

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[0065] Fig. 8B diagrammatically illustrates format of a disk sector of an FBA disk. Sector 170 is in track 169 of disk 30. Intersector gap 171 separates sector 170 from an immediately preceding sector (not shown). Sector ID 172 is an embossed area that contains the track and sector address of sector 170. Intrasector gap 173 separates the hard sector or embossed mark 172 from the magneto-optically recorded portion that constitutes the remainder of sector 170. Data synchronization signals DATA SYNC 174 are magneto-optically recorded with the data stored in portion 175 of sector 170. Control area 176 stores magneto-optically recorded control signals, as may be desired. A compress bit C 177 (considered a part of the control signals in area 176) if set to unity indicates that the data in portion 175 are compress. If C 177 is set to zero or nil, then the data stored in portion 175 are not compressed. Sector 170 ends with the error detection and correction redundancy in ECC 178 portion. ECC 178 stored signals are generated and stored in a known manner that is not pertinent to an understanding of the present invention. Intersector gap 179 separates sector 170 from a next succeeding sector 180. It is preferred that compress bit 177 be used while practicing the present invention.

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[0066] Fig. 9 is a flow chart showing a sequence of machine operations for storing a file in a plurality of groups of compressed data blocks wherein each group is separately transmitted from a host processor to a data storage system as a DTU having a number of uncompressed bytes as set forth above. At step 185 the data to be recorded is analyzed for determining the number of DTU's to be generated. The actual size in bytes/data blocks of a DTU may be different from file to file. In step 186, the DTU size is modified to accommodate the number of data blocks to be initially recorded for equalizing the sizes of a plurality of DTU's to be used. For example, if the number of data blocks to be compressed and recorded is less than two desired DTU's and one half of the number of data blocks results in a number of data bytes greater than MIN, then two DTU's each having one-half of the data blocks are created. This same principle is applied to transferring data blocks having any number of DTU's except for updating a recorded group of compressed data blocks, as will become apparent. If the DTU sizes cannot be equalized, then a last DTU may have a number of bytes less than the MIN (minimum) number of bytes. Upon updating the recorded group of compressed data blocks resulting from a small last DTU, a DTU is generated that adds a number of data blocks to make the size of the DTU, hence group of compressed data blocks, larger to meet the DTU size requirements set forth with respect to Fig's 9

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and 11. Fig. 15 relating to updating a recorded group of compressed data blocks illustrates machine steps for storing an updated DTU that is too large for the current allocated data storage space for a recorded group of compressed data blocks resulting from compressing and storing the updated DTU.

5 [0067] Following "GET DTU" step 186 (Fig. 9), a DTU of data blocks is built for data transfer. Step 189 transfers the DTU to data storage system 12. Data storage system 12 compresses and stores the transferred DTU as described earlier. At step 190, host processor 11 ascertains whether another DTU is to be transferred. If not (DONE = 1), then host processor 11 exits for performing other work not related to practicing the present invention. Otherwise, steps 188 and 189 are repeated until all DTU's have been transmitted to data storage unit 12.

10 [0068] Fig. 10 is a flow chart showing selecting a MIN and a MAX value respectively for image (non-coded or graphics) data and text (coded) data. The compressibility of data is a measure for selecting MIN and MAX. In this regard, each file of image or text data may compress substantially different from data from other files as well as changing from data block to data block in either type of data, image or text. Once a first group of data blocks have been compressed and recorded as a group of compressed data blocks, the compression ratio may be recorded in the Fig. 8A illustrated file directory as a reference for subsequent compression and storage of data blocks. The Fig. 10 illustration assumes that the image data has been compressed 75% (compressed image data blocks are 25% of original size) and text data blocks have been compressed about 50%. These measured values may be changed for calculation purposes for adding a margin of error accommodation into the calculations.

15 [0069] Step 195 determines whether the data in the file is text or image. If image, step 196 calculates the MIN value as $4 \cdot SB$ (bytes in a sector), i.e. at least four sectors are to be used for storing a group of compressed data blocks. The number four is selected in an arbitrary manner. Sector size affects the minimum number of sectors to be used. Step 197 calculates MAX as being $64 \cdot SB$. In a FBA disk having 1024 byte sectors, then the maximum DTU size is 64 KB (Kilobytes). Again, system considerations may change these values. Such considerations are beyond the present description. From step 195, for text data (IMAGE DATA = NO), step 200 calculates MIN as $2 \cdot SB$ while step 201 calculates MAX as $32 \cdot SB$. The number of uncompressed bytes for image data in MIN and MAX is equal to the number of uncompressed bytes for text data. The different compression ratios change MIN and MAX values inversely to the expected compression ratio. Upon completing either calculation, host processor 11 stores the MIN and MAX values in the first entry 160 (Fig. 8A) of the appropriate file directory and then exits the calculation.

20 [0070] The MIN and MAX values may also be predetermined and included as parameter data defining a class of data as set forth in Gelb et al US patent number 5,018,060 titled "ALLOCATING DATA STORAGE SPACE OF PERIPHERAL DATA STORAGE DEVICES USING IMPLIED ALLOCATION BASED ON USER PARAMETERS". Gelb et al teach that data set parameters implicitly control peripheral data storage operations. Such implicit control based on data base or file parameter data may be applied to practicing the present invention.

25 [0071] Fig. 11 shows execution of a WRITE command by data storage system 12 wherein the data blocks received in on DTU are compressed then recorded as a group of compressed data blocks. Step 210 receives a WRITE command 130. Step 211 sets the link commanded in field 135 for reporting the actual number of sectors used to store the resultant group of compressed data blocks and a compression ratio CR achieved. Step 212 sets a compress mode in data storage system 12 for activating CD 101 to compress the data blocks being received into one continuum of compressed data. Step 213 receives, compresses and stores the DTU data blocks. Step 216 compares the number of sectors actually used to store the compressed data with the number of sectors initially allocated. Step 217 compares the byte count of the original data blocks in the received DTU with the byte count of the compressed data blocks. In most instances, the byte count of the compressed data blocks will be less than the byte count of the original DTU data blocks. In this instance, at step 218, data storage system 12 indicates to host processor 11 that the data storage operation has been completed. The identification of any unused sectors plus other information describing the just-completed data recording operation is to be transferred from data storage system 12 to host processor 11. This transfer is effected by host processor 11 responding to the indication of a completed recording operation by issuing a READ BUFFER command 140 to data storage system 12 to send the number of unused allocated sectors and all other compression information to host processor 11. Host processor 12 in step 219 responds to the indication of unused allocated sectors to deallocate such sectors for use in storing other data. Note that if the compress bit 134 is off, then no compression occurs.

30 [0072] If at step 217, it is determined that the data compression resulted more data bytes in the compressed data blocks than were in the original data blocks, then the data blocks will be recorded without data compression. This growth in size of the compressed data blocks may occur when the original data blocks have certain data patterns. In any event, at step 220, data storage system 12 sends a channel command retry (CCR) or its equivalent to host processor 11. CCR indicates that the DTU has to be retransmitted by host processor 11 to data storage system 12. That is, the increased in size of the DTU after compression is considered an error condition. The CCR indicates that a recording error has occurred. Host processor 11 responds to the CCR at step 221 by resending the DTU to data storage system 11. At step 222, data storage system 12 stores the DTU without data compression. The above-described operations are exited from either step 219 or 222.

[0073] Fig. 12 is a flow chart showing system operations for reading data. Host processor 11 in step 225 prepares to read data, i.e. identifies the data blocks to be read. Host processor 11 then in step 226 searches for a file directory (Fig. 8A). Such file directory may be read from disk 30. If there is no file directory relating to compression, then the data are not compressed. Also, if the field 166 of the Fig. 8 illustrated directory for the identified group is zero, then that group is not compressed. Further, if data to be read are compressed and it is desired to decompress in a unit other the storing data storage system 12, step 226 directs host processor operations to read all identified data without decompression via path 227. From path 227, a usual data recording operation not involving data compression is performed (not shown). Host processor 11 builds issues one READ command 145 for each of the recorded groups of compressed data blocks to be read. Depending on the desired read operation, field 150 or READ command will be set to indicate either decompress or no decompress OFF. Host processor 11 before sending the READ command 145 to data storage system 12 examines field 150 at step 226. If host processor 11 at step 226 finds that the data to be read are compressed and decompression is desired, then step 230 sets field 150 to compress ON. All of the groups of compressed data blocks having data blocks to be read are identified in step 231 via examination of the appropriate file directory 161-163. Host processor 11 in step 232 then builds one or more READ commands 145 for reading the step 231 identified groups of compressed data blocks with decompression. The term build used above indicates that the appropriate control data are inserted into a READ command for commanding data storage system 12 to perform a desired read. Such command includes the number of LBA addressed sectors to be read as well as the logical address in LBA of a first one of the sectors. One READ command is sent by host processor 11 to data storage system 12 in step 232, there can be a number of READ commands sent for fetching a plurality of groups of record blocks. Data storage system 12 receives the READ command. At step 233, data storage system checks the sector compress bit of- the first sector storing the requested group to be read. If bit C 177 (Fig. 8B) is unity, then the data are compressed. Data storage system 12 then in step 234 reads the requested group including decompressing the data. It is to be noted, that if the READ command field 150 indicates decompression is OFF, then no decompression occurs even if bit C 177 is set to unity. On the other hand, if bit C 177 equals zero (data in the sector are not compressed), the at step 235 data storage system 12 reads and sends the read data without decompression to host processor 11. The Fig. 2 illustrated system exits the read operation for one group from either step 234 or 235.

[0074] Fig. 13 illustrates operation of data storage system responding to a READ command 145. Step 236 receives the READ command. Step 237 checks the compress field 150. If the compress field indicates that decompress is ON, then C bit 177 of the sector being accessed is checked to ensure that the data to be read is in fact recorded and stored in a compressed form. Step 238 executes the READ command by decompressing the data being read if field 150 indicates compression and C bit 177 is ON. If the field 150 indicates decompression if OFF, the data stored in the addressed sectors are transferred without decompression whether compressed or not. That is, in all cases, data storage system 12 transfers the data without decompression if field 150 indicates compress is OFF. This control enables transferring data in either compressed or decompressed form.

[0075] Fig. 14 illustrates one application of the invention in a system having linked host processors. Both batch and in line data compression/decompression are employed. Compression-decompression software modules 251 and 273 provide batch data compression and decompression while integrated circuit chips (hardware compress decompress) 253 and 272 provide in line (real time) data compression-decompression. Two data processing systems 240 and 241 are linked by data link 263. Link 263 may be a local area network (LAN), a data communication circuit or transfer of a removable data cartridge manually or via a library, mail etc between the two data processing systems. Host processor 250 in system 240 has a software compress-decompress facility 251, a transfer link facility 252 that involves no compression or decompression and an in-line hardware compress-decompress facility 253. Facilities 251-253 may be physically located in data processing system 240 in host processor 250 or as a part of a channel connection that includes logic switch 254 (programmed or hardware) connecting host processor 250 to facilities 251-253. Dashed line 255 indicates that switch 254 is programmably controlled by host processor 250. A given data processing system may have only 1) batch compress facility 251 and link facility 252, 2) in-line facility 253 and link facility 252, 3) all facilities 251-253 or 4) either facility 251 or 253 may be located either in data storage system 262 or data link 263.

[0076] The input-output (IO) connections from facilities 251-253 are effected by logic switch 260 that is programmably controlled by host processor 250 as indicated by dashed line 261. Switch 260 directs IO data flow between facilities 251-253 and a data storage system 262 or data line 263.

[0077] Data processing system 241 is shown as being identical to data processing system 240. Data processing system 241 includes host processor 270 that may have a different computational arrangement and capability from host processor 250, logic switch 271, facilities 272-274, data storage system 275 and switch 277 that selectively connects data processing system 241 to data link 263 to other systems and data processing system 240.

[0078] Fig. 15 illustrates updating a recorded group of compressed data blocks. Host processor 11 in step 280 has updated data blocks and desires to update a file recorded in data storage system 12 as a plurality of groups of compressed data blocks. Step 281 compares the data length (number of uncompressed data bytes) of the updating DTU with the number of bytes in sectors currently recorded as one group to be updated. Host processor 11 also examines

the number of padding bytes in a last sector storing compressed data for estimating whether or not the updated data blocks are storable in the currently allocated sectors for the group(s) to be updated.

[0079] At step 282 host processor 11 determines whether or not the updating DTU can be stored in currently allocated sectors or if more or different sectors should be allocated. That is, if the updating DTU has more data bytes than the currently recorded group, then additional sectors are allocated at step 288 (host processor 11 does the allocation). Such new sectors are preferably contiguous sectors that may not include any sectors containing the recorded group of data blocks to be updated. Following allocation step 288, the updating DTU is recorded at step 289. Then, host processor 11 at step 290 deallocates the sectors containing the group of data blocks to be updated. The Fig. 2 illustrated system then exits the updating operation from step 290.

[0080] If, at step 282, the number of data bytes in the updating DTU is substantially equal to the number of bytes (uncompressed) of the recorded DTU, then the updating occurs at step 283 using the sectors currently storing the group to be updated. The Fig. 2 illustrated system then performs step 290 before exiting the updating operation. If the updating DTU has fewer bytes than the recorded group, then the updating DTU is recorded in sectors selected from the sectors containing the group to be updated. The sectors not used to record the updating DTU are deallocated at step 290.

[0081] It may be decided that, independently of any data growth patterns, to always store the updated data blocks in a newly allocated set of sectors and to deallocate or free the sectors storing the current group(s) of compressed data blocks to be updated. In this situation, steps 288-290 are performed. For example, if there is a desire to save the original group(s) of compressed data blocks, such original recording may be retained. Host processor 11 then updates the appropriate file directory 160-162 and exits the storage operation.

[0082] In the updating operation shown in Fig. 15, whenever the compressed data has more bytes than the original uncompressed data, the data are recorded in an uncompressed form. the steps shown in Fig. 11 are added to the Fig. 15 illustrated sequence.

Claims

1. Apparatus for storing data in compressed form in a data storage device having a plurality of addressable like-sized data storage areas, each for recording a predetermined number of data bytes, the data storage device being connected to means for receiving data to be recorded, said received data being arranged in a plurality of addressable data blocks, **characterised in that** the apparatus comprises, in combination:

selection means in the means for receiving data for selecting one or more data transfer units of data blocks to be recorded, each said transfer unit of data blocks having a given number of data bytes and including one or more of said addressable data blocks;

allocation means connected to the selection means for responding to the number of data bytes in each said transfer unit of data blocks to determine, based on said number of data bytes, a required first number of addressable data storage areas for storing said transfer unit of data blocks, and to indicate that said transfer unit requires said first number of addressable data storage areas to record said transfer unit;

compression means connected to the selection means for compressing said transfer unit of data blocks to be recorded as a group of compressed data blocks;

data access means in the device connected to said compression means for recording said group of compressed data blocks in a second number of said addressable data storage areas as one continuum of compressed data, said second number being equal to or less than said first number; and

directory means indicating which ones of said addressable data storage areas said continuum of data is recorded in, and indicating that said continuum of data contains said selected transfer unit of data blocks in a compressed form.

2. Apparatus according to claim 1 including update means connected to said selection means and to said allocation means for updating a recorded group of compressed data blocks with updated data blocks, including receiving updated ones of said data blocks and selecting a data transfer unit of data blocks to include said updated data blocks; said update means being connected to said allocation means for allocating a number of said addressable data storage areas for receiving and recording said updated compressed data blocks and for deallocating ones of said allocated addressable data storage areas in which are stored the original group of compressed data blocks

to be updated.

5 3. Apparatus according to claim 1 or claim 2, wherein the selection means is connected to the data storage device for selecting said given number of data bytes to form a transfer unit in dependence on the number of data bytes which are recordable in each of said data storage areas.

10 4. Apparatus according to any one of claims 1 to 3, including range means indicating a range of number of bytes to be used for transferring data blocks between said means for receiving data and said data storage device, wherein said selection means is connected to said range means for receiving said range indication and responding to the received range indication for selecting a predetermined number of said data blocks to be a data transfer unit and to be in one of said groups of data blocks such that each said group of data blocks has a number of data bytes equivalent to a plurality of uncompressed data blocks.

15 5. Apparatus according to any one of claims 1 to 4 wherein the apparatus includes:

CKD means for supplying a plurality of CKD data blocks;

a CKD formatted disk within the data storage device for receiving and recording CKD data;

20 said selection means being connected to said CKD means for receiving and selecting a predetermined number of said CKD data blocks as a data transfer unit of said CKD data blocks;

said data access means having CKD recording means for recording said transfer unit of CKD data as compressed by said compression means as a single record on said CKD formatted disk; and

25 repeat means connected to said selection means and to said CKD means for repeatedly actuating the CKD means to supply a transfer unit of CKD data blocks for compression and recording in respective single CKD records.

30 6. Apparatus according to any one of claims 1 to 4, including:

a host processor connected to a peripheral controller, said data storage device being connected to said peripheral controller;

35 an FBA sectored disk in said data storage device having a plurality of addressable sectors for receiving and recording data blocks;

said selection means having means for selecting said data blocks for said data transfer unit to be recorded in a predetermined number of sectors on said FBA sectored disk; and

40 repeat means connected to said selection means for repeatedly actuating the selection means for selecting a plurality of said transfer units of data blocks from one file of such data blocks for compression and recording of said transfer units of data blocks such that said file of data blocks is recorded in compressed form on said FBA sectored disk in a plurality of said continua of data wherein each said continua consists of one said group of compressed data blocks.

45 7. Apparatus according to any one of the preceding claims, including data recording management means connected to said directory means and to said data access means for actuating the directory means to establish a plurality of said file directories, one file directory for each file of data recorded in compressed form; said recording management means actuating said directory means to record in each of said file directories a number of said data blocks to be included in each of said data transfer units of data and including recording a maximum number of bytes to be included in any one of said data transfer units.

50 8. A method of compressing and recording onto a data storage medium data of a file which is arranged in a plurality of addressable data blocks, **characterised in that** the method comprises the steps of:

55 selecting (10) a plurality of said data blocks of said file to be compressed and recorded;

segmenting the selected plurality of addressable data blocks into one or more data transfer units, each data transfer unit of data blocks having a given number of data bytes and including one or more of said addressable data blocks;

5 allocating (13) a first number of addressable data storage areas of the storage medium for recording each of said one or more data transfer units as respective separate groups of compressed data blocks, said first number being determined based on the number of data bytes in each of said one or more data transfer units;

10 compressing (15) each of said one or more data transfer units and recording them as respective separate groups of compressed data blocks in a second number of addressable data storage areas of the storage medium as one continuum of compressed data for each group, said second number being equal to or less than said first number;

15 creating and maintaining (16) a file directory indicating the address and size of each of said recorded groups for enabling random access to recorded data within said file of data blocks.

9. A method according to claim 8 including the step, after recording said one group of compressed data blocks, of deallocating (219) allocated addressable data storage areas, if any, into which said one group of compressed data blocks was not recorded.

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10. A method according to claim 8 or claim 9, including:

supplying CKD formatted data blocks of one CKD formatted file and selecting said CKD data blocks to be compressed and recorded;

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compressing one or more data transfer units of said CKD data blocks into one or more groups, respectively, of compressed CKD data blocks; and

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recording the one or more groups of compressed CKD data blocks as one record on a CKD formatted record member.

11. A method according to claim 8 or claim 9, including:

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selecting an FBA formatted record medium to be said record medium, said FBA formatted record medium having a plurality of addressable data-storing sectors, each data-storing sector being capable of recording a given number of data bytes; and

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selecting said data transfer unit to have a first predetermined number of said data blocks having a number of uncompressed data bytes equal to a data storage capacity, in data bytes, of a second predetermined number of said data-storing sectors.

12. A method according to any one of claims 8 to 11, including:

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setting a range of number of bytes to be included in each of said data transfer units; and

selecting a number of said data blocks such that a number of data bytes in the selected number of data blocks is within the set range.

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Patentansprüche

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1. Eine Vorrichtung zum Speichern von Daten in komprimierter Form in einem Datenspeichergerät mit einer Vielzahl von adressierbaren, gleich großen Datenspeicherbereichen, wobei jeder für die Aufzeichnung einer vordefinierten Anzahl an Datenbytes vorgesehen ist, wobei das Datenspeichergerät mit einem Mittel zum Empfang der aufzuzeichnenden Daten verbunden ist, wobei die genannten empfangenen Daten in einer Vielzahl an adressierbaren Datenblöcken angeordnet sind, **dadurch gekennzeichnet, dass** die Vorrichtung in Kombination folgendes umfasst:

Ein Mittel zur Auswahl im Mittel zum Empfang der Daten, um eine oder mehrere Datenübertragungseinheiten der aufzuzeichnenden Datenblöcke auszuwählen, wobei jede Datenübertragungseinheit über eine gegebene Anzahl an Datenbytes verfügt und einen oder mehrere der genannten adressierbaren Datenblöcke enthält;

5 Ein Mittel zur Zuordnung, verbunden mit dem Mittel zur Auswahl, um für die Anzahl an Datenbytes in jeder genannten Übertragungseinheit mit Datenblöcken, basierend auf der genannten Anzahl an Datenbytes, eine erforderliche erste Anzahl an adressierbaren Datenspeicherbereichen festzulegen, zum Speichern der genannten Datenübertragungseinheit mit Datenblöcken, und um anzuzeigen, dass die genannte Datenübertragungseinheit die genannte erste Anzahl an adressierbaren Datenspeicherbereichen benötigt, um die genannte Datenübertragungseinheit aufzuzeichnen;

10 Ein Mittel zur Kompression, verbunden mit dem Mittel zur Auswahl, zur Kompression der genannten Übertragungseinheit mit Datenblöcken, die als eine Gruppe mit komprimierten Datenblöcken aufzuzeichnen sind;

15 Ein Mittel zum Datenzugriff in dem Gerät, das mit dem Mittel zur Kompression verbunden ist, um die genannte Gruppe mit komprimierten Datenblöcken in einer zweiten Anzahl der genannten adressierbaren Datenspeicherbereiche als zusammenhängende Einheit an komprimierten Daten aufzuzeichnen, wobei die genannte zweite Anzahl gleich oder kleiner als die genannte erste Anzahl ist; und

20 Ein Verzeichnismittel zur Anzeige, in welchem der genannten adressierbaren Datenspeicherbereiche die genannte zusammenhängende Dateneinheit aufgezeichnet wurde sowie zur Anzeige, dass die zusammenhängende Dateneinheit die genannte ausgewählte Übertragungseinheit mit Datenblöcken in komprimierter Form enthält.

25 2. Eine Vorrichtung nach Anspruch 1, einschließlich einem Aktualisierungsmittel, verbunden mit dem genannten Auswahlmittel und dem genannten Zuordnungsmittel, zum Aktualisieren einer aufgezeichneten Gruppe mit komprimierten Datenblöcken mit aktualisierten Datenblöcken, einschließlich dem Empfang der aktualisierten genannten Datenblöcke sowie der Auswahl einer Datenübertragungseinheit mit Datenblöcken zur Einbeziehung der genannten aktualisierten Datenblöcke, wobei das genannte Aktualisierungsmittel mit dem genannten Zuordnungsmittel verbunden ist, um eine Anzahl der genannten adressierbaren Datenspeicherbereiche zum Empfang und Aufzeichnen der genannten aktualisierten komprimierten Datenblöcke zuzuordnen und die Zuordnung derjenigen der zugeordneten adressierbaren Datenspeicherbereiche rückgängig zu machen, in denen die ursprüngliche Gruppe mit komprimierten, zu aktualisierenden Datenblöcken enthalten ist.

35 3. Eine Vorrichtung nach Anspruch 1 oder nach Anspruch 2, wobei das Mittel zur Auswahl mit dem Datenspeichergerät verbunden ist, um die genannte gegebene Anzahl an Datenbytes auszuwählen, um eine Übertragungseinheit zu bilden, abhängig von der Anzahl an Datenbytes, die in jedem Datenspeicherbereich aufgezeichnet werden kann.

40 4. Eine Vorrichtung nach jedem der Ansprüche 1 bis 3, einschließlich einem Mittel zur Angabe des Bereichs für die Anzahl an Datenbytes, zur Verwendung für die Übertragung von Datenblöcken zwischen dem genannten Mittel zum Empfang von Daten und dem genannten Datenspeichergerät, wobei das genannte Mittel zur Auswahl mit dem genannten Mittel zur Angabe des Datenbytebereichs verbunden ist, um die genannte Bereichsangabe zu empfangen und um auf die empfangene Bereichsangabe zur Auswahl einer vordefinierten Anzahl an genannten Datenblöcken zu reagieren, die eine Datenübertragungseinheit bilden und sich in einer der genannten Gruppen mit Datenblöcken befinden, so dass jede der genannten Gruppen mit Datenblöcken über eine Anzahl an Datenbytes verfügt, die mit der Vielzahl an nicht komprimierten Datenblöcken übereinstimmt.

5. Eine Vorrichtung nach jedem der Ansprüche 1 bis 4, wobei die Vorrichtung folgendes umfasst:

50 Ein CKD Mittel zum Bereitstellen einer Vielzahl an CKD Datenblöcken;

Ein CKD-formatierter Datenträger innerhalb des Datenspeichergeräts zum Empfang und Aufzeichnen von CKD Daten;

55 Wobei das genannte Auswahlmittel mit dem genannten CKD Mittel verbunden ist, um eine vordefinierte Anzahl der genannten CKD Datenblöcke als eine Datenübertragungseinheit der genannten Datenblöcke zu empfangen und auszuwählen;

Wobei das genannte Datenzugriffsmittel über ein CKD Aufzeichnungsmittel verfügt, um die genannte Übertragungseinheit mit CKD Daten aufzuzeichnen, die durch das genannte Kompressionsmittel als einzelner Datensatz auf dem genannten CKD-formatierten Datenträger komprimiert ist; und

5 Ein Mittel zur Wiederholung, verbunden mit dem genannten Auswahlmittel und mit dem genannten CKD Mittel, um auf das CKD Mittel wiederholt zuzugreifen und so eine Übertragungseinheit mit CKD Datenblöcken zur Kompression und Aufzeichnung in entsprechenden einzelnen Datensätzen bereitzustellen.

6. Eine Vorrichtung nach jedem der Ansprüche 1 bis 4, einschließlich:

10 Einem Hostprozessor, verbunden mit einem peripheren Controller, wobei das genannte Datenspeichergerät mit dem peripheren Controller verbunden ist;

15 Einem in FBA-Sektoren unterteilten Datenträger mit einer Vielzahl an adressierbaren Sektoren zum Empfang und zum Aufzeichnen von Datenblöcken;

20 Wobei das genannte Auswahlmittel über ein Mittel zum Auswählen der genannten Datenblöcke für die genannte Datenübertragungseinheit verfügt, die in vordefinierter Anzahl an Sektoren auf dem genannten in FBA-Sektoren unterteilten Datenträger aufzuzeichnen ist; und

25 Einem Mittel zur Wiederholung, verbunden mit dem genannten Mittel zum wiederholten Zugriff auf das Auswahlmittel zur Auswahl einer Vielzahl der genannten Übertragungseinheiten mit Datenblöcken von einer Datei dieser Datenblöcke zur Kompression und zur Aufzeichnung der genannten Übertragungseinheiten mit Datenblöcken, so dass die genannte Datei mit Datenblöcken in komprimierter Form auf dem in FBA-Sektoren unterteilten Datenträger in einer Vielzahl an zusammenhängenden Dateneinheiten aufgezeichnet wird, wobei jede zusammenhängende Dateneinheit aus einer der genannten Gruppen mit komprimierten Datenblöcken besteht.

30 7. Eine Vorrichtung nach einem der vorangegangenen Ansprüche, einschließlich einem Mittel zur Verwaltung der Datenaufzeichnung, verbunden mit dem genannten Verzeichnismittel sowie mit dem genannten Datenzugriffsmittel für den Zugriff auf das Verzeichnismittel zum Erstellen einer Vielzahl der genannten Dateiverzeichnisse, wobei ein Dateiverzeichnis für jede Datei mit Daten in komprimierter Form bereitgestellt wird; wobei das genannte Mittel zum Verwalten der Aufzeichnung auf das genannte Verzeichnismittel zugreift, um in jedem der genannten Dateiverzeichnisse eine Anzahl der genannten Datenblöcke aufzuzeichnen, die in jede der Datenübertragungseinheiten eingefügt werden sollen sowie einschließlich dem Aufzeichnen einer maximalen Anzahl an Bytes für jede der Datenübertragungseinheiten.

35 8. Eine Methode zur Kompression und Aufzeichnung von Daten einer Datei auf einem Datenspeichermedium, die in einer Vielzahl von adressierbaren Datenblöcken angeordnet ist, **dadurch gekennzeichnet, dass** die Methode die folgenden Schritte umfasst:

40 Auswahl (10) einer Vielzahl der genannten Datenblöcke der genannten Datei zur Kompression und Aufzeichnung;

45 Segmentieren der ausgewählten Vielzahl an adressierbaren Datenblöcken in eine oder mehrere Datenübertragungseinheiten, wobei jede Datenübertragungseinheit über eine gegebene Anzahl an Datenbytes verfügt und einen oder mehrere der genannten Datenblöcke umfasst;

50 Zuordnen (13) einer ersten Anzahl an adressierbaren Datenspeicherbereichen des Speichermediums zur Aufzeichnung jeder der genannten Datenübertragungseinheiten als entsprechende separate Gruppe mit komprimierten Datenblöcken, wobei die genannte erste Anzahl basierend auf der Anzahl an Datenbytes in jeder der Datenübertragungseinheiten bestimmt wird;

55 Komprimieren (15) jeder der genannten Datenübertragungseinheiten und deren Aufzeichnung als entsprechende separate Gruppe mit komprimierten Datenblöcken in einer zweiten Anzahl an adressierbaren Datenspeicherbereichen des Speichermediums als zusammenhängende, komprimierte Daten für jede Gruppe, wobei die zweite Anzahl gleich oder kleiner als die erste Anzahl ist;

Erstellen und Verwalten (16) eines Dateiverzeichnisses, das die Adresse und die Größe jeder der genannten aufgezeichneten Gruppen angibt, um einen Direktzugriff auf aufgezeichnete Daten innerhalb der genannten Datei mit Datenblöcken zu ermöglichen.

5 9. Eine Methode nach Anspruch 8 einschließlich des Schritts, nach dem Aufzeichnen der genannten einen Gruppe mit komprimierten Datenblöcken, zum Rückgängig machen der Zuordnung (219) der zugeordneten adressierbaren Datenspeicherbereiche, falls vorhanden, in denen die genannte Gruppe mit komprimierten Datenblöcken nicht aufgezeichnet wurde.

10 10. Eine Methode nach Anspruch 8 oder Anspruch 9, einschließlich:

Bereitstellen von CKD-formatierten Datenblöcken einer CKD-formatierten Datei und Auswählen der genannten CKD- Datenblöcke zur Kompression und zur Aufzeichnung;

15 Komprimieren von einer oder mehreren Datenübertragungseinheiten der genannten CKD-Datenblöcke in eine oder mehrere Gruppen mit komprimierten CKD- Datenblöcken; und

Aufzeichnen der Gruppen mit komprimierten CKD- Datenblöcken als ein Datensatz auf einem CKD- formatierten Datenträger.

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11. Eine Methode nach Anspruch 8 oder 9, einschließlich:

25 Auswählen eines FBA-formatierten Aufzeichnungsmediums, wobei das genannte FBA-formatierte Aufzeichnungsmedium über eine Vielzahl an adressierbaren, Daten speichernden Sektoren verfügt, wobei jeder der Daten speichernden Sektoren in der Lage ist, eine gegebene Anzahl an Datenbytes aufzuzeichnen; und

30 Auswählen der genannten Datenübertragungseinheit, um eine erste vordefinierte Anzahl der genannten Datenblöcke zu haben, die über eine Anzahl nicht komprimierter Datenbytes verfügen, die gleich einer Datenspeicherkapazität, in Datenbytes, einer zweiten vordefinierten Anzahl der genannten Daten speichernden Sektoren ist.

12. Eine Methode nach jedem der Ansprüche 8 bis 11, einschließlich:

35 Setzen eines Anzahlbereichs an Bytes, die in jede Datenübertragungseinheit eingefügt werden können; und

Auswählen einer Anzahl der genannten Datenblöcke, so dass sich eine Anzahl an Datenbytes innerhalb der ausgewählten Anzahl an Datenblöcken innerhalb des festgelegten Bereichs bewegt.

40 Revendications

1. Dispositif destiné à mémoriser des données sous une forme compressée dans un dispositif de mémorisation de données comportant une pluralité de zones de mémorisation de données de tailles identiques adressables, chacune étant destinée à enregistrer un nombre prédéterminé d'octets de données, le dispositif de mémorisation de données étant relié à un moyen destiné à recevoir des données devant être enregistrées, lesdites données reçues étant agencées dans une pluralité de blocs de données adressables, **caractérisé en ce que** le dispositif comprend, en combinaison :

50 un moyen de sélection dans le moyen destiné à recevoir des données afin de sélectionner une ou plusieurs unités de transfert de données des blocs de données à enregistrer, chaque dite unité de transfert de blocs de données comportant un nombre donné d'octets de données et comprenant un ou plusieurs desdits blocs de données adressables,

55 un moyen d'allocation relié au moyen de sélection afin de répondre au nombre des octets de données dans chaque dite unité de transfert de blocs de données pour déterminer sur la base dudit nombre d'octets de données, un premier nombre requis de zones de mémorisation de données adressables destinées à mémoriser ladite unité de transfert de blocs de données, et pour indiquer que ladite unité de transfert demande ledit premier nombre de zones de mémorisation de données adressables pour enregistrer ladite unité de transfert,

un moyen de compression relié au moyen de sélection en vue de compresser ladite unité de transfert de blocs de données à enregistrer sous forme d'un groupe de blocs de données compressées,

5 un moyen d'accès aux données dans le dispositif relié audit moyen de compression afin d'enregistrer ledit groupe de blocs de données compressées dans un second nombre desdites zones de mémorisation de données adressables sous forme d'une suite continue de données compressées, ledit second nombre étant inférieur ou égal audit premier nombre, et

10 un moyen de répertoire indiquant dans lesquels desdites zones de mémorisation de données adressables, ladite suite continue de données est enregistrée, et indiquer que ladite suite continue de données contient ladite unité de transfert sélectionnée des blocs de données sous une forme compressée.

2. Dispositif selon la revendication 1, comprenant un moyen de mise à jour relié audit moyen de sélection et audit moyen d'allocation afin de mettre à jour un groupe enregistré de blocs de données compressées avec des blocs de données mis à jour, comprenant la réception des blocs mis à jour parmi lesdits blocs de données et la sélection d'une unité de transfert de données des blocs de données pour inclure lesdits blocs de données mis à jour, ledit moyen de mise à jour étant relié audit moyen d'allocation afin d'allouer un certain nombre desdites zones de mémorisation de données adressables en vue de recevoir et d'enregistrer lesdits blocs de données compressées mis à jour et en vue de désallouer celles desdites zones de mémorisation de données adressables allouées dans lesquelles est mémorisé le groupe d'origine des blocs de données compressées devant être mis à jour.

3. Dispositif selon la revendication 1 ou la revendication 2, dans lequel le moyen de sélection est relié au dispositif de mémorisation de données afin de sélectionner ledit nombre donné d'octets de données pour élaborer une unité de transfert suivant le nombre des octets de données qui sont enregistrables dans chacune desdites zones de mémorisation de données.

4. Dispositif selon l'une quelconque des revendications 1 à 3, comprenant un moyen de plage indiquant une plage d'un nombre d'octets à utiliser pour transférer des blocs de données entre lesdits moyens en vue de recevoir des données et ledit moyen de mémorisation de données, dans lequel ledit moyen de sélection est relié audit moyen de plage afin de recevoir ladite indication de plage et répondant à l'indication de plage reçue pour sélectionner un nombre prédéterminé desdits blocs de données devant constituer une unité de transfert de données et devant figurer dans l'un desdits groupes de blocs de données de sorte que chaque dit groupe de blocs de données comporte un nombre d'octets de données équivalent à une pluralité de blocs de données non compressées.

5. Dispositif selon l'une quelconque des revendications 1 à 4 dans lequel le dispositif comprend :

un moyen de format CKD destiné à fournir une pluralité de blocs de données au format CKD,

40 un disque formaté au format CKD à l'intérieur du dispositif de mémorisation de données afin de recevoir et d'enregistrer des données au format CKD,

45 ledit moyen de sélection étant relié audit moyen de format CKD pour recevoir et sélectionner un nombre prédéterminé desdits blocs de données au format CKD sous forme d'une unité de transfert de données desdits blocs de données au format CKD,

ledit moyen d'accès aux données comportant un moyen d'enregistrement au format CKD destiné à enregistrer ladite unité de transfert des données au format CKD telles qu'elles sont compressées par ledit moyen de compression sous forme d'un enregistrement unique sur ledit disque formaté au format CKD, et

50 un moyen de répétition relié audit moyen de sélection et audit moyen de format CKD destiné à actionner de façon répétitive le moyen de format CKD afin de fournir une unité de transfert des blocs de données au format CKD en vue d'une compression et d'un enregistrement dans des enregistrements au format CKD uniques respectifs.

6. Dispositif selon l'une quelconque des revendications 1 à 4 comprenant :

un processeur hôte relié à un contrôleur de périphérique, ledit dispositif de mémorisation de données étant relié audit contrôleur de périphérique,

un disque à secteurs à architecture FBA dans ledit dispositif de mémorisation de données comportant une pluralité de secteurs adressables pour recevoir et enregistrer des blocs de données,

5 ledit moyen de sélection comportant un moyen destiné à sélectionner lesdits blocs de données pour ladite unité de transfert de données devant être enregistrée dans un nombre prédéterminé de secteurs sur ledit disque à secteurs à architecture FBA, et

10 un moyen de répétition relié audit moyen de sélection afin d'actionner de façon répétitive le moyen de sélection en vue de sélectionner une pluralité desdites unités de transfert de blocs de données à partir d'un fichier de tels blocs de données en vue d'une compression et d'un enregistrement desdites unités de transfert des blocs de données de sorte que ledit fichier de blocs de données soit enregistré sous forme compressée sur ledit disque à secteurs à architecture FBA dans une pluralité de ladite suite continue de données dans lequel chacune dites suites continues est constituée d'un bloc dudit groupe de blocs de données compressées.

15 7. Dispositif selon l'une quelconque des revendications précédentes, comprenant un moyen de gestion d'enregistrement de données relié audit moyen de répertoire et audit moyen d'accès aux données afin d'actionner le moyen de répertoire pour établir une pluralité desdits répertoires de fichiers, un répertoire de fichiers pour chaque fichier des données enregistrées sous forme compressée, ledit moyen de gestion d'enregistrement actionnant ledit moyen de répertoire pour enregistrer dans chacun desdits répertoires de fichiers un certain nombre desdits blocs de données devant être inclus dans chacune desdites unités de transfert des données et comprenant l'enregistrement d'un nombre maximum d'octets devant être inclus dans l'une quelconque desdites unités de transfert de données.

20 8. Procédé de compression et d'enregistrement sur un support de mémorisation de données, des données d'un fichier qui sont disposées dans une pluralité de blocs de données adressables, **caractérisé en ce que** le procédé comprend les étapes consistant à :

sélectionner (10) une pluralité desdits blocs de données dudit fichier devant être compressées et enregistrées,

30 segmenter la pluralité sélectionnée des blocs de données adressables en une ou plusieurs unités de transfert de données, chaque unité de transfert de données des blocs de données comportant un nombre donné d'octets de données et comprenant un ou plusieurs desdits blocs de données adressables,

35 allouer (13) un premier nombre de zones de mémorisation de données adressables du support de mémorisation afin d'enregistrer chacune desdites une ou plusieurs unités de transfert de données sous forme de groupes séparés respectifs de blocs de données compressées, ledit premier nombre étant déterminé sur la base du nombre des octets de données dans chacune desdites une ou plusieurs unités de transfert de données,

40 compresser (15) chacune desdites une ou plusieurs unités de transfert de données et les enregistrer sous forme de groupes séparés respectifs de blocs de données compressées dans un second nombre de zones de mémorisation de données adressables du support de mémorisation, sous forme d'une suite continue de données compressées pour chaque groupe, ledit second nombre étant inférieur ou égal audit premier nombre,

45 créer et entretenir (16) un répertoire de fichiers indiquant l'adresse et la taille de chacun desdits groupes enregistrés afin de permettre un accès aléatoire aux données enregistrées à l'intérieur dudit fichier de blocs de données.

50 9. Procédé selon la revendication 8, comprenant l'étape, après l'enregistrement dudit un groupe de blocs de données compressées, consistant à désallouer (219) des zones de mémorisation de données adressables allouées, s'il en existe, dans lesquels ledit un groupe de blocs de données compressées n'a pas été enregistré.

10. Procédé selon la revendication 8 ou la revendication 9, comprenant :

55 la fourniture de blocs de données formatés au format CKD d'un fichier formaté au format CKD et la sélection desdits blocs de données au format CKD devant être compressées et enregistrées, et

la compression d'une ou plusieurs unité de transfert de données desdits blocs de données au format CKD en un ou plusieurs groupes, respectivement, de blocs de données au format CKD compressées, et

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l'enregistrement des un ou plusieurs groupes de blocs de données au format CKD compressées sous forme d'un enregistrement sur un élément d'enregistrement formaté au format CKD.

11. Procédé selon la revendication 8 ou la revendication 9, comprenant :

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la sélection d'un support d'enregistrement formaté à architecture FBA devant constituer ledit support d'enregistrement, ledit support d'enregistrement formaté à architecture FBA comportant une pluralité de secteurs de mémorisation de données adressables, chaque secteur de mémorisation de données étant capable d'enregistrer un nombre donné d'octets de données, et

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la sélection de ladite unité de transfert pour qu'elle présente un premier nombre prédéterminé desdits blocs de données comportant un nombre d'octets de données non compressées égal à une capacité de mémorisation de données, en octets de données, d'un second nombre prédéterminé desdits secteurs de mémorisation de données.

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12. Procédé selon l'une quelconque des revendications 8 à 11, comprenant :

l'établissement d'une plage du nombre des octets devant être inclus dans chacune desdites unités de transfert de données, et

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la sélection d'un nombre desdits blocs de données tel qu'un nombre d'octets de données dans le nombre sélectionné des blocs de données soit à l'intérieur de la plage établie.

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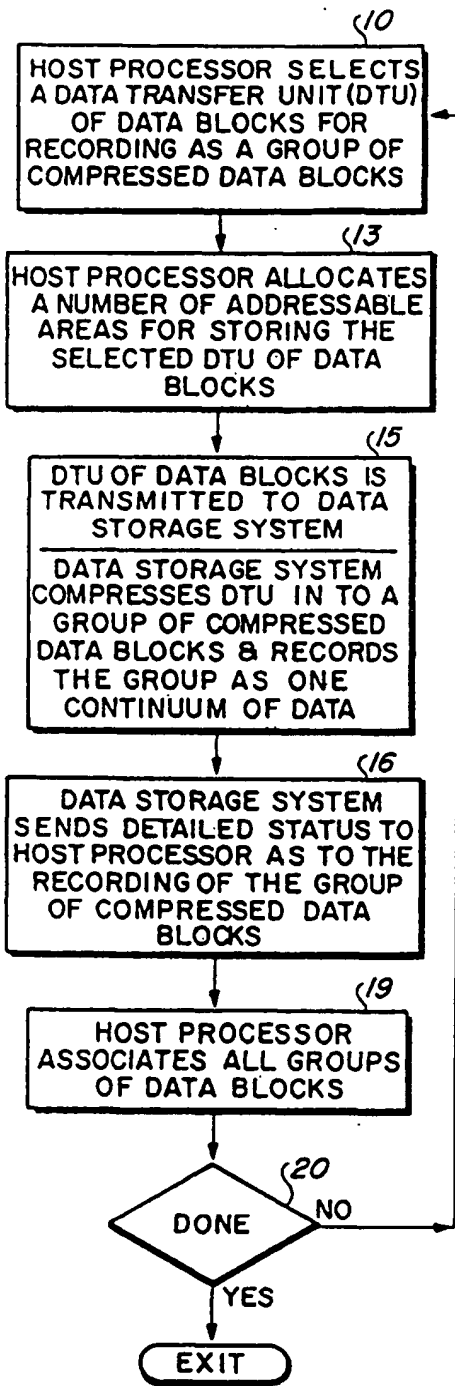


FIG. 1

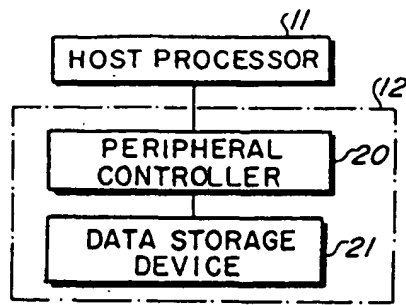


FIG. 2

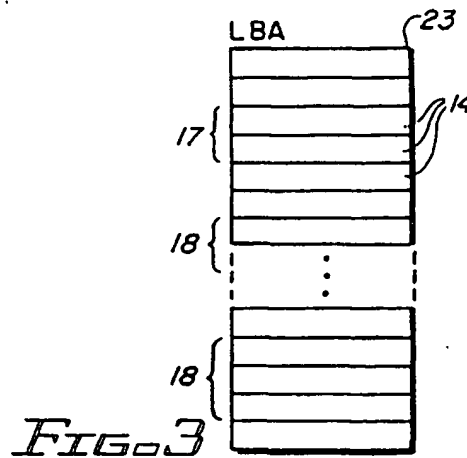


FIG. 3

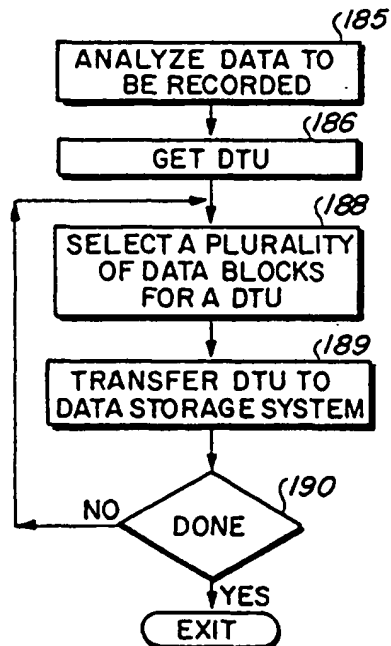


FIG. 9

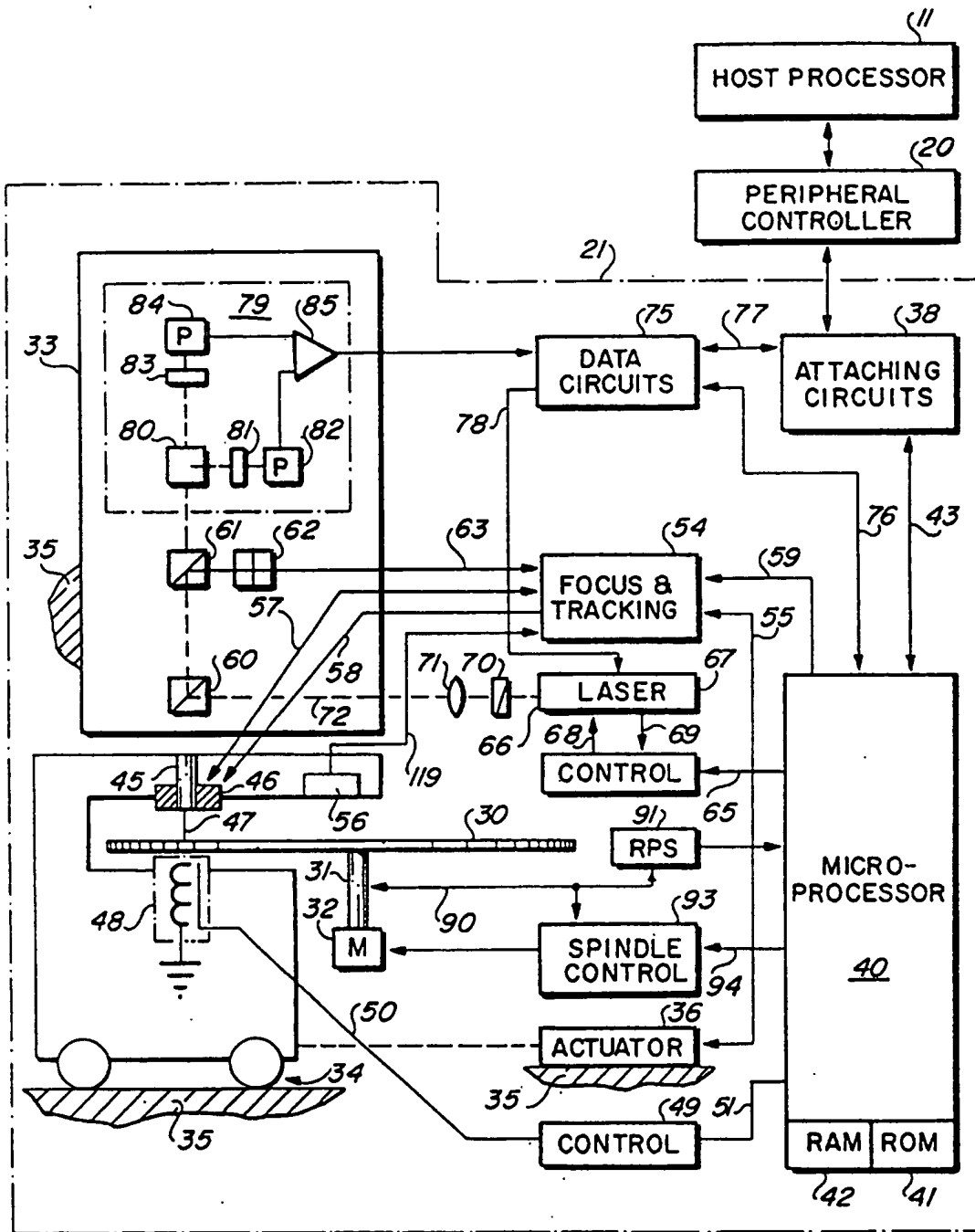
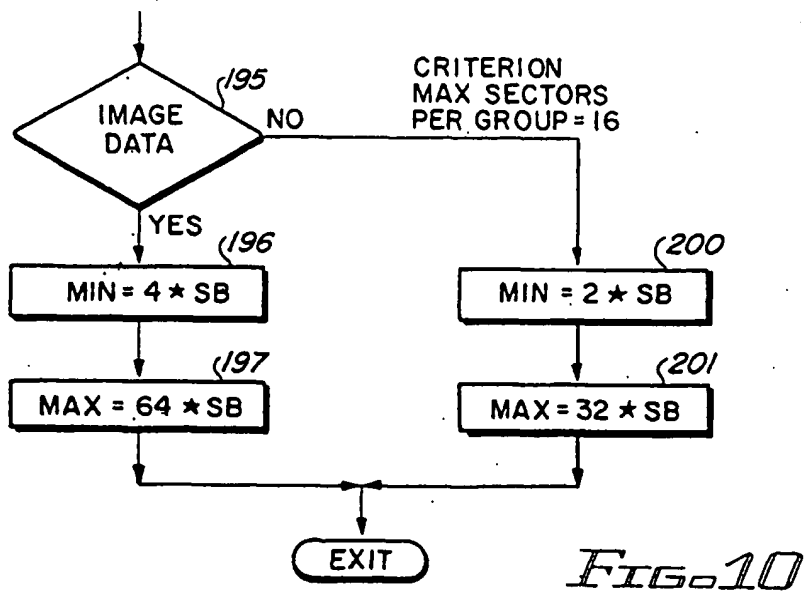
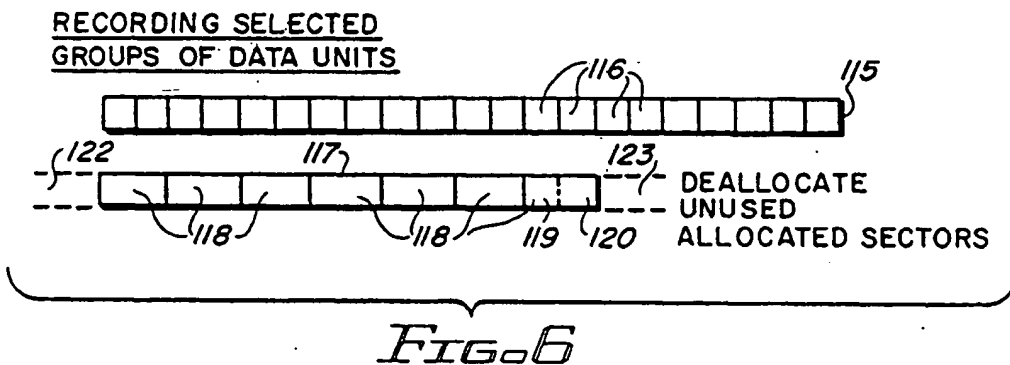
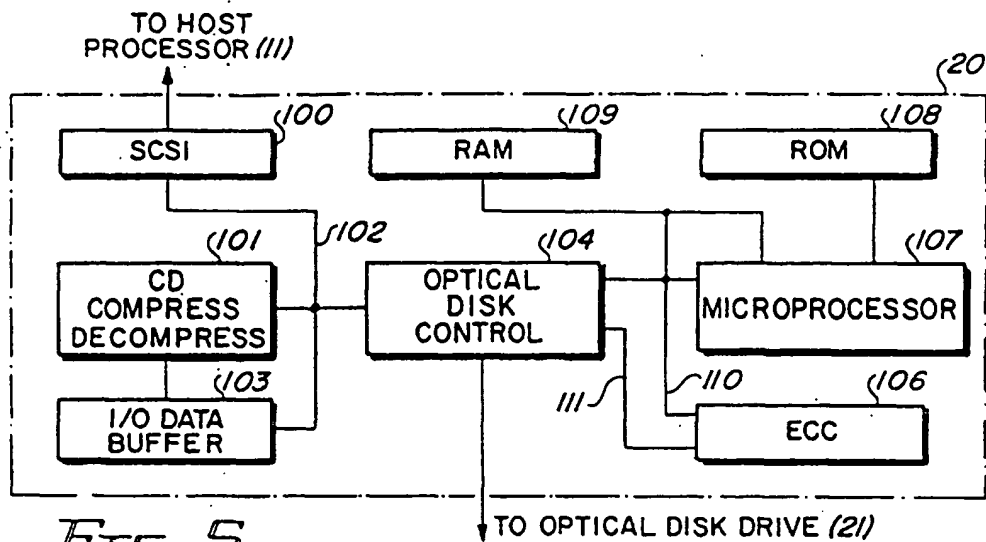


FIG. 4



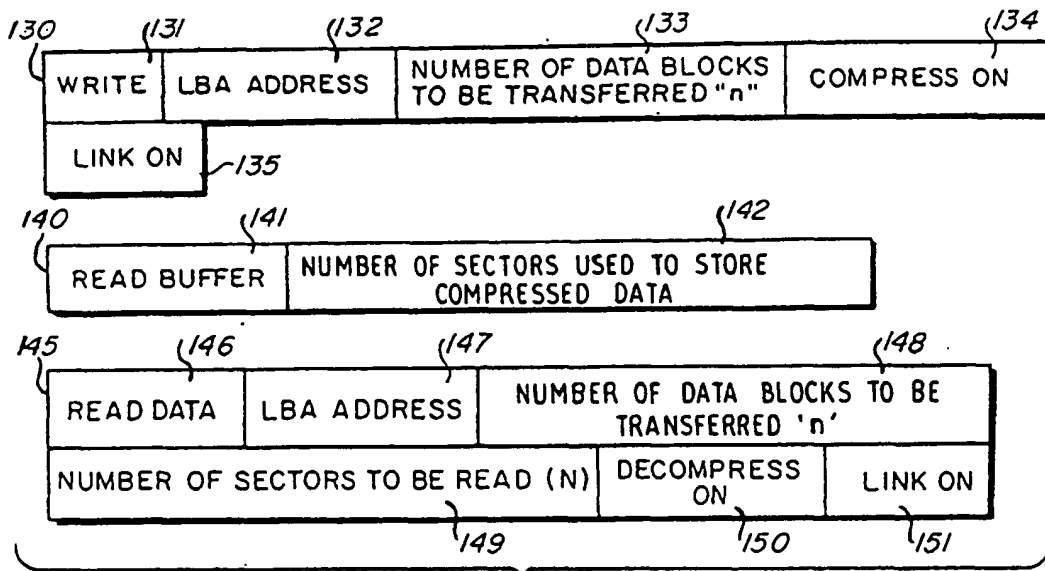


FIG. 7

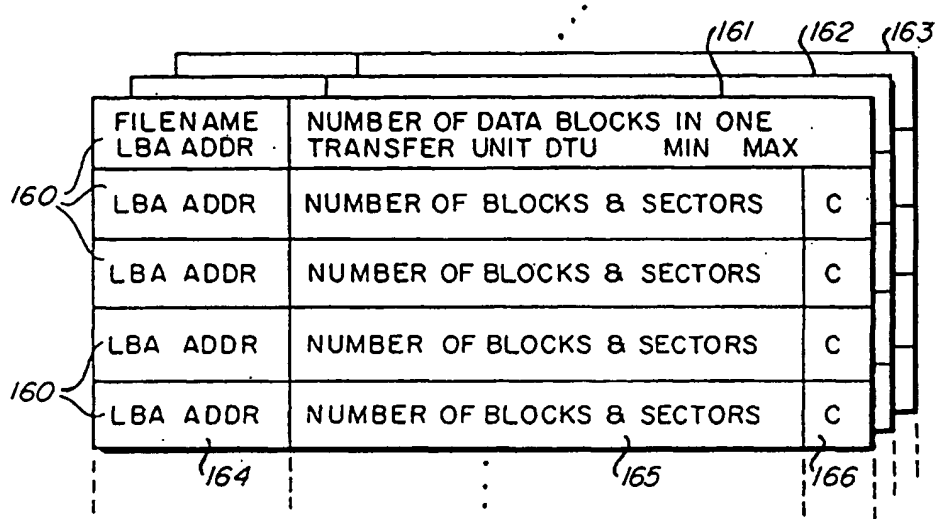


FIG. 8A

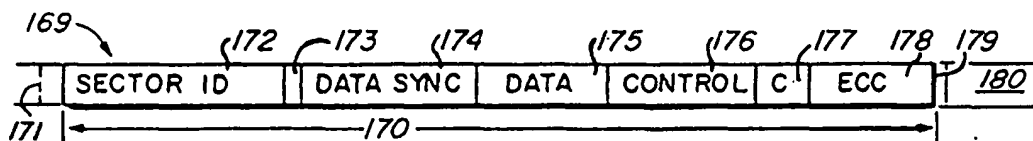
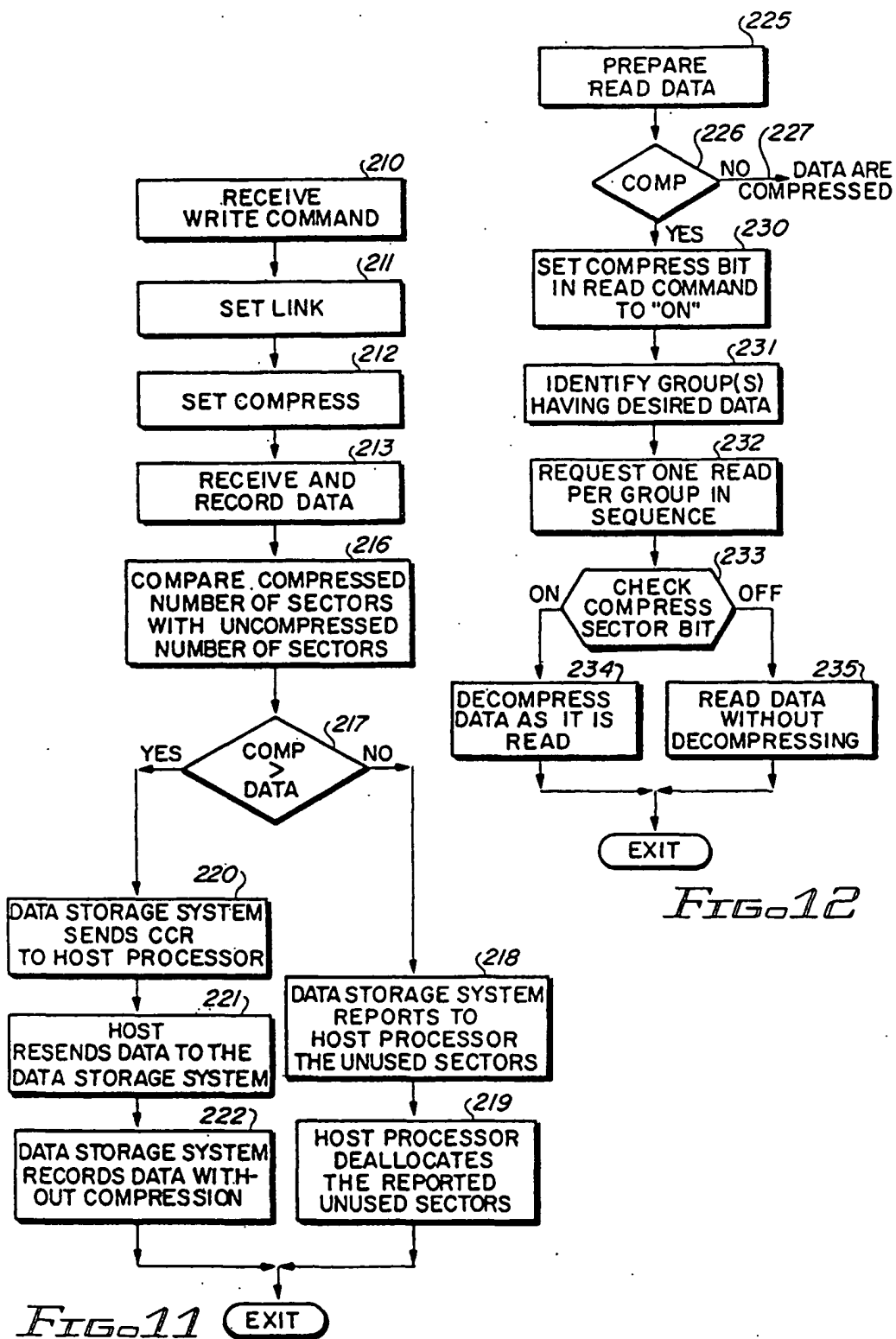


FIG. 8B



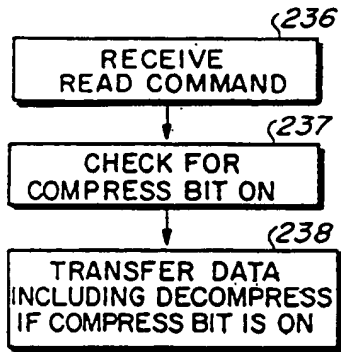


FIG. 13

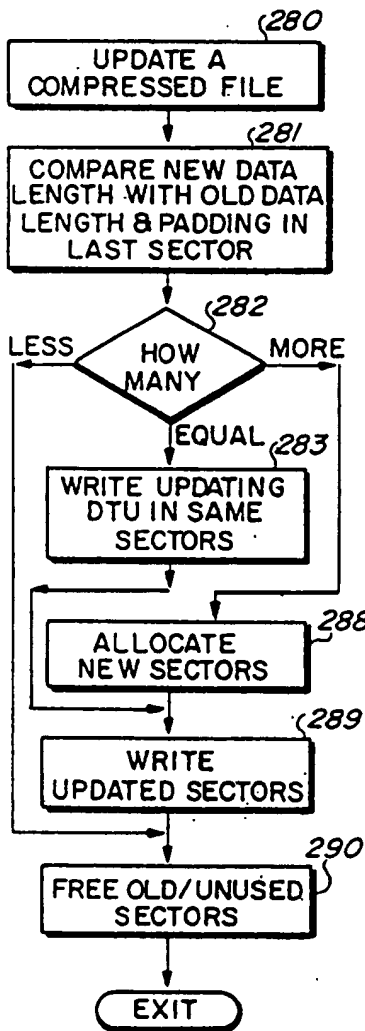


FIG. 15

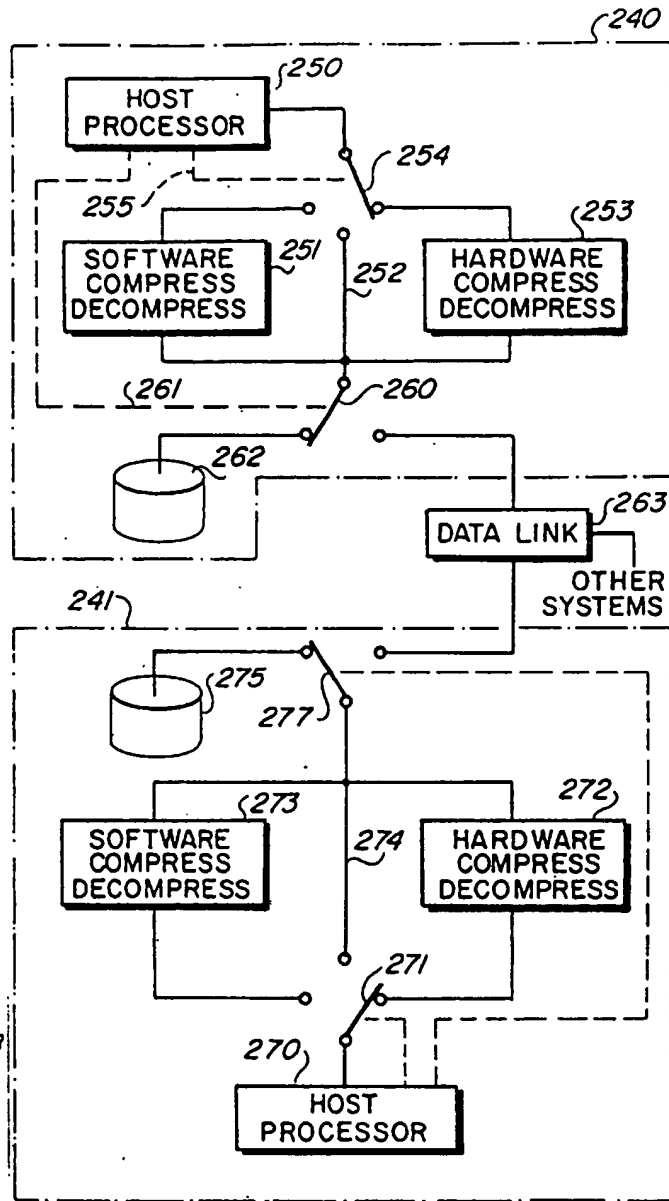


FIG. 14

(19)



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(54) **Image encoding apparatus optimizing the amount of generated code**

Bildcodierungsgerät mit Optimierung der erzeugten Codemenge

Appareil pour codage d'images optimisant la quantité du code généré

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• IEEE Transactions On Communications Vol.
COM-32, No. 3, March 1984, pp. 280-287, "An
Interframe Coding System for Video
Teleconferencing Signal Transmission at a 1.5
Mbit/s Rate".

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Description

The present invention relates to an image processing apparatus, and, more particularly to an image processing apparatus for compressing a digital image and transmitting compressed data to a transmission path or a storage medium.

Fig. 7 illustrates a conventional image encoding apparatus in which image data received at a terminal 101 is analog-to-digital (hereinafter abbreviated to "A/D") converted in an A/D converter 102 before it is formed into a variable-length compressed code in an encoding unit 103. Then the variable-length compressed code is temporarily stored in a transmission buffer memory 104 before it is transmitted to a transmission path 106. At this time, a control coefficient (parameter) for use to control the quantity of data of the variable-length compressed code generated in the encoding unit 103 is generated depending upon the degree of the data occupancy of a buffer memory 104 and the transmission rate of the transmission path 106 so as to be fed back to the encoding unit 103 via a filter 105. As a result compressed data representing an image can, in an averaged manner, be transmitted at a rate of the transmission path 106. Data received via the transmission path 106 is temporarily stored in a receiving buffer memory 107 so as to, together with the supplied control coefficient, be transmitted to a decoding unit 108. As a result, variable-length compressed encoded data is expanded and decoded before it is digital-to-analog converted in a D/A converter 109 so that an image is transmitted to a terminal 110.

A variety of systems for compressing a colour image to be performed in the encoding unit 103 shown in Fig. 7 have been disclosed. Among others a so-called Adaptive Discrete Cosine Transform (ADCT) system has been suggested as a preferable colour image encoding system.

Fig. 8 is a schematic structural view which illustrates an image encoding apparatus structured to act according to the above-described ADCT system. The above-described apparatus is arranged to receive an image represented by 8-bit data, that is, data converted into 256 gradations/colour by the A/D converter 102 shown in Fig. 7, the input image being composed of three or four colours, that is, RGB, YUV, YPbPr, L*a*b* or YMCK or the like. The input image is, by a DCT unit 201, immediately subjected to a two-dimensional discrete cosine transformation (hereinafter abbreviated by "DCT") in units of sub-blocks each of which is composed of 8 x 8 pixels. Then, the obtained conversion coefficients are linearly quantized in a linear quantizing unit 202. Each conversion coefficient has a different quantizing step size which is made to be a value obtained by, multiplying by K an element of an 8 x 8 quantization matrix the 8 x 8 quantization matrix being employed while taking into consideration for each conversion coefficient the difference of the visual sensitivity for sensing the quantization noise, where K is called a "control coefficient". The value of K is used to control the image quality and the quantity of compressed and generated data. Table 1 shows an example of a quantization matrix stored in a quantization matrix storage unit 203. That is, since the number of quantization steps is reduced when K is enlarged, the image quality deteriorates and the data quantity decreases.

16	11	10	16	24	40	51	61
12	12	14	19	26	58	60	55
14	13	16	24	40	57	69	56
14	17	22	29	51	87	80	62
18	22	37	56	68	109	103	77
24	35	55	64	81	104	113	92
49	64	78	87	103	121	120	101
72	92	95	98	112	100	103	99

After the quantization has been completed, a DC conversion component (hereinafter called a "DC component") is, in a one-dimensional prediction unit 204, subjected to a one-dimensional forecasting between adjacent sub-blocks. As a result, the forecasted error is Huffman-encoded in a Huffman encoding unit 205.

Then, the quantization output denoting the forecast error is divided into groups so that the identification number of a group which includes the forecasted error is Huffman-encoded before the value of the quantization output in the group is expressed by a fixed length code.

The AC conversion component (hereinafter called "AC component") is encoded using a zigzag scanning unit 206 in such a manner that the above-described quantization output is diagonally zigzag scanned in a direction from low spatial frequency to high spatial frequency as shown in Fig. 9.

That is, significant conversion coefficients, i.e. coefficients of non-zero value, are identified by an identification number according to horizontal and vertical spatial frequency. Also, the number of insignificant conversion coefficients, i.e. coefficients of zero value, scanned between each respective significant conversion coefficient and the next following scanned significant conversion coefficient is extracted. Each respective identification number and the corresponding extracted number of insignificant coefficients are paired and are Huffman encoded by the Huffman encoding unit 207.

The respective values of the quantization output, ie the significant conversion coefficients, are each expressed by a fixed length code.

Since the number of significant conversion coefficients is dependent on spatial frequency distribution, and will thus vary from one image frame to the next, the length of code generated for each image frame also will vary. It is thus difficult to match the capacity of the buffer memory 107, shown in Fig.7, to the amount of encoded data generated. If the capacity is too small, overflow will occur and the reproduced image will be degraded. If a large size memory is chosen to avoid such overflow, then there are penalties in extra hardware size and cost.

The above problem of avoiding overflow has been addressed by Mukana et al., IEEE Transactions on Communications, Vol. Com -32, No. 3 March 1984, pages 280-287. The apparatus described therein is of the type defined in the preamble of claim 1 appended. In the case of transmitting or recording still image data, if the quantization is not controlled adaptively it is neither possible to predict the time required for transmission nor possible to predict the storage capacity required for recording.

A variety of code length control technologies have been disclosed in European Patent Application EP-A-0447247 published 18 September 1991, and European Patent Application EP-A-0469835, European Patent Application EP-A-0469852, both published 5 February 1992.

EP-A-0 469 835 discloses iteratively controlling the quantization characteristic to keep the amount of code below a desired value. Moreover, plural encoders are arranged in parallel, using respectively different encoding control parameters. The output from the encoder whose amount of code is an optimum approximation of the desired amount is selected.

The present invention, as defined in the appended claims, is intended as a solution to the problems discussed above.

In the accompanying drawings

Fig. 1 is a structure block diagram which illustrates a first embodiment of the present invention;

Fig. 2 illustrates an image to be transmitted in a structure according to the first embodiment of the present invention;

Fig. 3 illustrates a calculating method according to the first embodiment of the present invention;

Fig. 4 is a structure view which illustrates a second embodiment of the present invention;

Fig. 5 illustrates a calculating method according to the second embodiment of the present invention;

Fig. 6 illustrates a calculation flow according to the second embodiment of the present invention;

Fig. 7 is a structural block diagram according to a conventional example;

Fig. 8 illustrates an ordinary variable-length encoding system;

Fig. 9, in detail, illustrates the ordinary variable-length encoding system;

Fig. 10 illustrates a relationship between control coefficients and information quantities, according to a third embodiment of the invention;

Fig. 11 illustrates another relationship between control coefficients and information quantities, according to the third embodiment;

Fig. 12 illustrates a further-detailed calculating method according to a fourth embodiment of the present invention;

Fig. 13 illustrates a calculating flow according to the fourth embodiment of the present invention;

Fig. 14 illustrates a further-detailed calculating method according to a fifth embodiment of the present invention;

Fig. 15 illustrates a calculating flow according to the fifth embodiment of the present invention;

Fig. 16 is a block diagram which illustrates a sixth embodiment of the image encoding apparatus according to the present invention;

Fig. 17 is a block diagram which illustrates the schematic structure of a conventional encoding system which employs a DCT conversion;

Fig. 18 illustrates a quantization process shown in Fig. 17;

Fig. 19 illustrates a quantization process shown in Fig. 17;

Fig. 20 illustrates a sixth embodiment of the present invention;

Fig. 21 further illustrates the sixth embodiment of the present invention; and

Fig. 22 further illustrates the sixth embodiment shown in Fig. 16.

First Embodiment

A first embodiment of the present invention will be described now with reference to the drawings. Fig. 1 is a structural block diagram which illustrates an image processing apparatus according to the present invention. An image received from a video camera or a host computer or an image scanner or the like is A/D converted by an A/D converter 2 before it is variable-length encoded by an encoding unit (1) given reference numeral 3 by the above-described so-called ADCT system. At this time the control coefficient K has a constant value Q_1 for the current one frame of the image. As a result, the compressed information quantity B_1 is measured and the measured quantity B_1 is transmitted to a calculating

unit 5.

Simultaneously, the image data is also variable-length encoded by an encoding unit (2) given reference numeral 4 by the so-called ADCT system. At this time control coefficient K has a different constant value Q_2 , for the current one frame of the image. The resulting, compressed information quantity B_2 is measured and also transmitted to the calculating unit 5. Reference numeral 6 represents an image data delay unit for delaying the image, which has been A/D-converted, by about one image frame.

Reference numeral 7 represents an encoding unit (0) for compressing and encoding the delayed image data under control of an optimum control coefficient $K=Q_0$ which is calculated by a linear approximation from Q_1 , Q_2 , the measured amounts B_1 and B_2 in the calculating unit 5, and from the predetermined desired quantity value B_0 of compressed and encoded data which value is already stored in a memory such as a ROM, a RAM and the like so as to be transmitted to the calculating unit 5.

Reference numeral 9 represents a transmission path comprising a transmission medium such as ground waves or an optical space or the like exemplified by an optical fibre, a satellite or microwaves in the case of instantaneous transmission. In case of accumulated transmission, it is a storage medium such as a tape type medium exemplified by a digital VTR or a DAT or the like, a disc-like medium such as a floppy disk or an optical disk or the like or a solid medium such as a semiconductor memory.

The transmission rate is determined depending upon the quantity of information of the original image, the compression rate and a required transmission time such that it is varied from several tens of kbits/second to several tens of Mbits/second.

On the other hand, data received through the transmission path 9 is temporarily stored in a receiving buffer memory 10 so that compressed encoded data read from the receiving buffer memory 10 is extended and decoded in the decoding unit 11 with the optimum control coefficient Q_0 which has been received simultaneously with the above-described data item. Then, it is digital-to-analog converted a D/A converting unit so that an image is transmitted to a terminal 13.

Referring to Figs. 2 and 3, the present invention will now be described in detail. Fig. 2 illustrates an example of an image to be transmitted, one frame of the image being an A/D converted image composed of 1280 pixels, each of which is constituted by 8 bits, in the horizontal direction and 1088 pixels in the longitudinal direction. The data capacity of one image is made of $1,280 \times 1,088 \times 8 = 11,141,120$ bits. If the image is transmitted as a moving image at a speed of 30 frames/second a high speed transmission path capable of realizing $11,141,120 \times 30 = 334,233,600$ bits/second must be used.

On the other hand, the transmission path is usually arranged to act at a predetermined transmission rate. Therefore, an information quantity which exceeds the predetermined transmission rate will cause a data overload to occur and thereby the transmission cannot be made. Assuming that a transmission path, the transmission rate of which is 36.0000 Mbits/second, is used and as well assuming that the redundancy degree for information such as a sink code, an ID code and a parity is 5%, the transmission rate at which image information can be transmitted is 34.2000 Mbits/second and thereby the compressed information quantity for one image (one frame) is 1.1400 Mbits/frame. Therefore, the image of frame must be compressed to a degree which is 10.23% or less. Furthermore, dummy data amounting to the residual quantity: $1,140,000 - (11,141,120 \times 0.1023) = 263.424$ bits/frame, that is, $263.424 \times 30 = 7,902.72$ bits/second must be inserted.

Assuming that the control coefficient is a certain value and thereby the compressed information quantity of a certain image is 10%, the capacity of image information is $334,233,600 \times 0.1 = 33,423,360$ bits/seconds and thereby dummy data of $34,200,000 - (334,233,600 \times 0.1) = 776,640$ bits/second must be inserted.

Assuming that the control coefficient has a certain value and thereby the compressed information quantity of a certain image is 11%, the capacity of image information is $334,233,600 \times 0.11 = 36,765,696$ bits/seconds, resulting in a negative amount of dummy data of $34,200,000 - (344,233,600 \times 0.1) = -2,565,696$ bits/second, which corresponds to exceeding the transmission rate of the transmission path, causing a data overload to occur.

Therefore, it is necessary to constitute a structure in such a manner that the target compression rate set to 10.23% and an optimum control coefficient Q_0 is given to the encoding unit (0) given reference numeral 7 shown in Fig. 1 in order to obtain an approximate value which does not exceed the target compression rate of 10.23%.

Fig. 3 illustrates a process of determining optimum control coefficient Q_0 , wherein a case in which the information quantity is compressed and encoded to about 1/10 by the so-called ADCT system is illustrated.

The encoding system is arranged to be similar to that shown in Fig. 8 such that 8 horizontal pixels x 8 longitudinal pixels are collected into a DCT sub-block and the DCT conversion is performed in units of the DCT sub-blocks before the conversion coefficient is linearly quantized. Each conversion coefficient has a different quantizing step size which is made to be a value obtained by multiplying an 8 x 8 quantization matrix element shown in Table 1 by K, the 8 x 8 quantization matrix being employed while taking into consideration for each conversion coefficient the difference of the visual sensitivity for sensing the quantization noise. The value of K is used to control the image quality and the quantity of generated data so that the above-described desired compression ratio of about 1/10 is realized. After the quantization has been completed, a DC conversion component is, as a subtraction value from zero, subjected to a one-dimensional

forecasting between adjacent sub-blocks. Then, the forecast error is Huffman-encoded. Then, the quantization output denoting the forecast error is divided into groups so that the identification number of a group which includes the forecasted error is Huffman-encoded before the value of the quantization output in the group is expressed by a fixed length code. An AC conversion component excluding the DC component is encoded in such a manner that the above-described quantization output is zigzag scanned from the low frequency component to the high frequency component. That is, the significant coefficients are classified into groups depending upon their values, and the identification number of the group and the number of the insignificant coefficients held between each significant coefficient and a following significant coefficient positioned in front of it in the direction of the scan, are paired with the significant coefficient and then Huffman encoded. At this time, two control coefficients Q_1 and Q_2 are selected and relationships $Q_1 < Q_0$ and $Q_0 < Q_2$ are established.

Fig. 3 illustrates the relationship between control coefficient K for an ordinary image frame and the compressed information quantity Y . The above-described relationship between Y and K is expressed by function g , that is, $Y = g(K)$, where function g is considered such that it extremely approximates a log curve expressed by:

$$Y = g(K) = p \log K + q$$

(where p and q are constants) (1)

Then, encoding using control coefficient Q_1 is performed in the encoding unit (1) given reference numeral 3 shown in Fig. 1 so that compressed information quantity B_1 is obtained.

Furthermore, encoding using control coefficient Q_2 is performed in the encoding unit (2) given reference numeral 4 shown in Fig. 1 so that compressed information quantity B_2 is obtained.

In the calculating unit 5 shown in Fig. 1, a straight $Y = aK + b$ (wherein a and b are constants) which connects two points (Q_1, B_1) and (Q_2, B_2) is calculated.

$$Y = \frac{B_1 - B_2}{Q_1 - Q_2} \cdot K + \frac{Q_2 \cdot B_1}{Q_2 - Q_1} - \frac{Q_1 \cdot B_2}{Q_2 - Q_1}$$
(2)

Transformation is performed so that the following equation is obtained:

$$K = \frac{(Q_2 - Q_1) \cdot Y - Q_2 \cdot B_1 + Q_1 \cdot B_2}{B_2 - B_1}$$
(3)

Then, by setting B_0 shown in Fig. 3 to the compressed information quantity corresponding to the desired compression ratio (10.23%), the optimum control coefficient Q_0 can be obtained by substituting B_0 into Y in Equation (2).

$$Q_0 = \frac{(Q_2 - Q_1) B_0 - Q_2 \cdot B_1 + Q_1 \cdot B_2}{B_2 - B_1}$$
(4)

Actually, since the compressed information quantity generated with optimum control coefficient $K = Q_0$ has a value given by $Y = g(K)$, the actual quantity is B_0' . Since equation (1) is a downward-convex log curve, the straight line, which connects two points on the downward-convex curve, necessarily is positioned on or above this curve as shown in Fig. 3. This means that: $B_0 > B_0'$ so that the desired compression ratio is not exceeded in any case. Therefore, data overload is avoided.

Q_1 , Q_2 and B_0 of Equation (4) are known constant values. Therefore it is necessary to be capable of obtaining B_1 and B_2 by a trial of encoding. Therefore, the encoding units (1) and (2) respectively given reference numerals 3 and 4 shown in Fig. 1 are only required to generate the compressed information quantities.

Although the calculating unit 5 shown in Fig. 1 calculates the above-described Equation (4), the calculation may be performed by using a CPU or a look-up table which uses a ROM or a RAM or the like.

Although the above-described embodiment is arranged in such a manner that the relationship between the control coefficients and the compressed information quantities are expressed by a log curve, the actual relationship is sometimes different from this such that it can sometimes be approximated by a quadratic curve or a cubic curve depending upon the way of the quantization and the type of encoding employed in the encoding unit. However, any of the cases are commonly characterized in that each curve is a downward-convex curve (the tangent is always present below the

curve). Therefore, the above-described method of determining the control coefficient can be effectively employed because of the above-described characteristics.

Second Embodiment

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Fig. 4 is a structural block diagram which illustrates a second embodiment of the image encoding apparatus according to the present invention. An image received through a terminal 20 is A/D converted by an A/D converter 21 before it is variable-length encoded by an encoding unit (1) given reference numeral 22 by the above-described so-called ADCT system. At this time, control coefficient K is, as Q_1 which is a constant value, used to compress one frame of the image. As a result, a compressed information quantity B_1 is obtained so as to be transmitted to a comparison and calculating unit 26. Simultaneously, the image is also variable-length encoded by an encoding unit (2) given reference numeral 23 by the so-called ADCT system. At this time, control coefficient K is, as Q_2 , which is a constant value, used to compress the one frame of the image. As a result, a compressed information quantity B_2 is obtained so as to be transmitted to the comparison and calculating unit 26. The same image is similarly variable-length encoded by an encoding unit (3) given reference numeral 24 by the so-called ADCT system. At this time, control coefficient K is, as Q_3 , which is a constant value, used to compress the one frame of the image. As a result, a compressed information quantity B_3 is obtained so as to be transmitted to the comparison and calculating unit 26. Furthermore, the same image is similarly variable-length encoded by an encoding unit (4) given reference numeral 25 by the so-called ADCT system. At this time, control coefficient K is, as Q_4 , which is a constant value, used to compress the one frame of the image. As a result, a compressed information quantity B_4 is obtained so as to be transmitted to the comparison and calculating unit 26.

Reference numeral 27 represents an image data delay unit for delaying the image, which has been A/D-converted, by about one image frame. Reference numeral 28 represents an encoding unit (0) for compressing and encoding the image data in dependence upon the optimum control coefficient $K = Q_0$ calculated by the comparison and calculating unit 26 so as to cause compressed and encoded data to be stored in a transmission buffer memory 29.

Reference numeral 30 represents a transmission path. Data received through the transmission path 30 is temporarily stored in a receiving buffer memory 31. Compressed and encoded data read from the receiving buffer memory 31 is, in the encoding and decoding unit 32, extended and decoded with optimum control coefficient Q_0 which has been received simultaneously. Then, it is digital-to-analog converted in the D/A converter 33 so that an image is transmitted from a terminal 34.

Then, the second embodiment of the present invention will now be described with reference to Figs. 5 and 6.

Then, a description will be made with reference to a case in which an image to be transmitted is, as shown in Fig. 2, similar to that according to the above-described first embodiment and one image frame is compressed to 10.23% or less, respectively.

That is, it is necessary to constitute a structure in such a manner that the target compression rate is set to 10.23% and an optimum control coefficient Q_0 is given to the encoding unit (0) given reference numeral 28 shown in Fig. 4 in order to obtain an approximate value which does not exceed the target compression rate 10.23%.

Fig. 5 illustrates a process of determining the optimum control coefficient Q_0 .

The encoding system is arranged to employ the so-called ADCT system shown in Fig. 8 similarly to the first embodiment.

Then, an assumption is made that four control coefficients $Q_1, Q_2, Q_3,$ and Q_4 are selected which hold relationships $Q_1 < Q_0$ and $Q_0 < Q_4$.

Fig. 5 illustrates the relationship between control coefficient K for an ordinary one image frame and the compressed information quantity Y thereof. The above-described relationship between Y and K is expressed by function g, that is, $Y = g(K)$.

In this state, $Y = g(K)$ closely approximates a log curve.

Then, encoding using control coefficient Q_1 is performed in the encoding unit (1) given reference numeral 22 shown in Fig. 4 so that compressed information quantity B_1 is obtained. Encoding using control coefficient Q_2 is performed in the encoding unit (2) given reference numeral 23 shown in Fig. 4 so that compressed information quantity B_2 is obtained. Encoding using control coefficient Q_3 is performed in the encoding unit (3) given reference numeral 24 shown in Fig. 4 so that compressed information quantity B_3 is obtained. Encoding using control coefficient Q_4 is performed in the encoding unit (4) given reference numeral 25 shown in Fig. 4 so that compressed information quantity B_4 is obtained. Then, the flow of the comparison and calculating unit 26 shown in Fig. 4 will now be described with reference to Fig. 6.

In the comparison and calculating unit 26 shown in Fig. 4, target compression information quantity B_0 is subjected to comparisons with B_1, B_2, B_3 and B_4 obtained by the above-described compressing and encoding trial such that $B_0 \leq B_1, B_0 \leq B_2, B_0 \leq B_3$ and $B_0 \leq B_4$, respectively (steps S1 to S4) so as to obtain N with which B_0 holds a relationship $B_N \leq B_0 \leq B_{N+1}$ (wherein N is a positive integer) (steps S5 to S7). If N is not obtained, an error is recognized (step S9).

At the time at which N is detected, straight line $Y = aK + b$ (where a and b are constants) which connects (Q_N, B_N)

and (Q_{N+1}, B_{N+1}) to each other is calculated in the comparison and calculating unit 26 shown in Fig. 4. As a result, control coefficient K is obtained from Equation (5):

$$K = \frac{(Q_{N+1} - Q_N) \cdot Y - Q_{N+1} \cdot B_N + Q_N \cdot B_{N+1}}{B_{N+1} - B_N} \quad (5)$$

Then, by making B_0 shown in Fig. 5 to correspond to the desired compression ratio (10.23%) so that optimum control coefficient Q_0 can be obtained by substituting B_0 into Y in Equation (5).

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$$Q_0 = \frac{(Q_{N+1} - Q_N) \cdot B_0 - Q_{N+1} \cdot B_N + Q_N \cdot B_{N+1}}{B_{N+1} - B_N} \quad (6)$$

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Actually, since the compressed information quantity generated with optimum control coefficient $K = Q_0$ has a value given by $Y = g(K)$, the actual quantity is B_0' . This means

that: $B_0' > B_0$ so that the desired compression ratio is not exceeded in any case. Therefore, a data overload of the transmission path is avoided.

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Among the above-described values, Q_1, Q_2, Q_3, Q_4 and B_0 are known constant values in the apparatus, therefore it is necessary to be capable of obtaining only B_1, B_2, B_3 and B_4 by trial encoding. Therefore, the encoding units (1), (2), (3) and (4) given reference numerals 22, 23, 24 and 25 shown in Fig. 4 are only required to generate the compressed information quantities.

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Although the above-described Equation (6) is calculated in the above-described comparison and calculating unit 26 shown in Fig. 4, the calculation may be performed by using a CPU or the like or a look-up table which uses a ROM or a RAM or the like. Although the above-described second embodiment is arranged in such a manner that the number of the encoding units for generating only the encoded information quantity is made to be four, the above-described number can be increased, resulting an effect to be obtained in that the optimum control coefficient infinitely approximates the desired compressed information quantity while being limited to be smaller than the same. As a result, encoding can efficiently be performed. Therefore, the present invention is not limited to the above-described number of the encoding units. Furthermore, although the above-described ordinary encoding system as shown in Fig. 8 is employed in the encoding unit for the purpose of easily making the description, another encoding system may be employed. In addition, in the above-described case, the DCT unit shown in Fig. 8 is commonly employed in the encoding units. Therefore, due to the necessity of providing a plurality thereof they can be unified into one unit.

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The frequency conversion is not limited to DCT since other types of orthogonal conversion may be employed.

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In addition, the present invention is not limited to the block size arranged to be 8 x 8 pixels.

Furthermore, the encoding method applied after the quantization has been completed is not limited to the Huffman encoding method. For example, an arithmetical encoding method or a run-length encoding method may be employed.

As described above, the quantity of compressed data can be satisfactorily controlled.

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Third Embodiment

The structure of the third embodiment is characterized by a means for adjusting the first-order term, or the zero order term, or both the zero and first order terms of the applied linear approximation.

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The basic block structure according to this embodiment is arranged to be similar to that shown in Fig. 1.

Fig. 10 illustrates a case in which control coefficient K and information quantity Y hold a special relationship.

In a case where the information quantities obtained by quantization using control coefficients Q_1 and Q_2 are B_1 and B_2 , respectively, and where the original information quantity is B_0 , the control coefficient which is obtained by linear approximation $Y = aK + b$ as shown in Fig. 10 becomes Q_0 . Furthermore, if the actual information quantity B_0 , obtained through the quantization is performed using control coefficient Q_0 , holds a relationship $B_0' > B_0$, data overload occurs.

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Therefore, by adding a predetermined information quantity β (a constant) to approximation curve $Y = aK + b$ obtained with information quantities B_1 and B_2 , approximation $Y' = aK + b + \beta$ can be obtained. Then, quantization with control coefficient $Q_{0\beta}$ obtained with desired information quantity B_0 is performed so that the actual information quantity becomes B_0'' . As a result, a relationship $B_0'' < B_0$ and thereby the quantity becomes the desired information quantity B_0 or less. Therefore, information can be quantized and compressed so as to be transmitted while preventing data overload.

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Since $Y = g(K)$ is, in Fig. 10, ordinarily a downward convex curve, it is preferable that the above-described constant β holds a relationship $\beta > 0$. By adding β thus-determined, the possibility of occurrence of a data overload can be decreased. The structure may be arranged in such a manner that β is set manually to the calculating unit 5 in accordance

with the supplied image or the same is automatically set in accordance with the characteristics of the image.

Fig. 11 illustrates control coefficient K and information quantity Y in a case where approximation $Y = aK + b$ shown in Fig. 10 is transformed (amended) into $Y' = (a + \alpha)K + b + \beta$. As described with reference to Fig. 3, by performing quantization with desired information quantity B_0 and control coefficient $Q_{0\alpha\beta}$ obtained by approximation $Y = (a + \alpha)K + b + \beta$, the actual information quantity becomes B_0'' which holds a relationship $B_0'' < B_0$. Since the information quantity does not exceed the desired information quantity B_0 , quantization and compression can be performed so as to transmit information.

Furthermore, it is preferable that α holds a relationship $\alpha > 0$, similarly to β .

According to the above-described embodiment of the present invention, the above-described adapted linear approximation is applied. As a result, quantization compression can be performed while preventing a data overload even if the image is an image of a type in which the quantization control coefficient and the information quantity holds a special relationship.

Fourth Embodiment

The fourth embodiment is characterized in that, in a case where the desired information quantity is larger than the information quantity generated by the trial made with the first control coefficient as a result of the trial of a plurality of variable-length compressing and encoding with M -types of control coefficients, or in a case where the information quantity is smaller than the information quantity generated by the trial made with the M -th control coefficient, variable-length encoding is performed using a predetermined constant value as the control coefficient.

Since the basic block structure according to this embodiment is the same as that shown in Fig. 1, its description is omitted here.

Fig. 13 is a flow chart for the calculation to be performed in the structure according to this embodiment.

In a case where the image is very simple such as a colour bar and the original information quantity is small as designated by curve (B) shown in Fig. 12 as a result of a trial performed by using two control coefficients Q_1 and Q_2 shown in Fig. 1, a relationship $B_0 > B_{1B}$ is held (S101) and the calculating unit 5 shown in Fig. 1 transmits Q_1 to the encoding unit 7 while making $Q_0 = Q_1$.

In a case where the image is, as designated by curve (A) shown in Fig. 12, very complicated such as a zone plate and the original information quantity is very large as a result of the trial performed by using two control coefficients Q_1 and Q_2 , a relationship $B_0 < B_{2A}$ is held (S102) and the calculating unit 5 shown in Fig. 1 transmits Q_{MAX} to the encoding unit 7 while making $Q_0 = Q_{MAX}$ (S104). In a case where $B_{2A} < B_0 \leq B_{1B}$, Q_0 is calculated similarly to the first embodiment (S105).

As a result, the desired compression ratio is not exceeded in any case and a data overload will not take place on the transmission path.

Fifth Embodiment

A fifth embodiment of the present invention is a modification to the second embodiment. Since the basic structure is the same as that shown in Fig. 4, its description is omitted here.

Fig. 15 is a flow chart for the calculation to be performed in the structure according to this embodiment, the flow chart being basically arranged to be the same as that shown in Fig. 6.

In a case where the image is very simple such as a colour bar and the original information quantity is small as designated by curve (B) shown in Fig. 14 as a result of a trial performed by using four control coefficients Q_1 , Q_2 , Q_3 and Q_4 shown in Fig. 14, a relationship $B_0 > B_{1B}$ is held and the calculating unit 26 shown in Fig. 4 performs a transmission to the encoding unit (0) while making $Q_0 = Q_1$ (S9).

In a case where the image is, as designated by curve (A) shown in Fig. 14, very complicated such as a zone plate and the original information quantity is very large as a result of the trial performed by using four control coefficients Q_1 , Q_2 , Q_3 and Q_4 , a relationship $B_0 < B_{4A}$ is held and the calculating unit 26 shown in Fig. 4 performs a transmission to the encoding unit 0 while making $Q_0 = Q_{MAX}$ (S10).

Although the above-described embodiment is arranged in such a manner that the relationship between the control coefficients and the compressed information quantities are expressed by a log curve, the actual relationship is sometimes different from this such that it can sometimes be approximated by a quadratic curve or a cubic curve depending upon the way of the quantization and the type of encoding employed in the encoding unit. However, any of the cases are commonly characterized in that each curve is a downward-convex curve (the tangent is always present below the curve). Therefore, the above-described method of determining the control coefficient can be effectively employed because of the above-described characteristics.

Sixth Embodiment

In general, in a case where an image signal is transmitted, the transmission path possesses a transmission capacity per unit time. Therefore, it is preferable that, in a case where one frame must be transmitted at a predetermined moment as in case of a moving image, the quantity of the code to be transmitted be a quantity fixed in units of frames or image blocks. Although the overall quantity of the code can be adjusted by changing the quantization step coefficient in the quantization process, the quantization step coefficient must be forecast in order to cause the overall quantity of encoded data to be included in the set code quantity because the quantity of encoded data is different depending upon the image. The relationship between the above-described quantization step coefficient and the overall quantity of the encoded data establish a monotone decreasing function. Furthermore, an average image is expressed by a logarithmic curve as shown in Fig. 18.

As a method of estimating the quantization step size by utilizing the above-described characteristics, there has, according to the above-described embodiments, been described a method in which different trial quantization step coefficients are applied and the quantity of code obtained for each trial coefficient is measured and a linear interpolation is then performed to determine the approximate value of the optimum quantization step coefficient.

Fig. 19 illustrates the above-described method of estimating the quantization step size.

However, the above-described method encounters a problem in that many trials must be provided in order to reduce the error from the set quantity of the code, a plurality of trials must be performed in parallel in order to shorten the time required for estimation and the size of hardware of the apparatus cannot be reduced if the number of the measuring points is increased in order to improve the accuracy of the measured results.

According to the sixth embodiment to be described below, there is provided an encoding apparatus for quantizing converted data obtained by converting image information into the spatial frequency domain in units of blocks composed of a plurality of pixels, and for variable-length encoding the quantized converted data, the encoding apparatus comprising means for measuring the quantity of code by, in parallel, performing quantization to variable-length encoding (VLC) with predetermined plural quantization step coefficients, and a calculating means for estimating a quantization step coefficient for a desired quantity of the code by a linear approximation, from the measured quantity of the code, wherein the intervals between the trial quantization step coefficients, for each of which the quantity of the code is measured, are widened in proportion to the value of the quantization step coefficient.

Accordingly, the approximation error of the estimated quantization quantity can be approximated to a substantially constant value in comparison to a case in which the trial coefficients are equispaced. In particular, in a case where the quantity of the quantized code is large, the intervals between the trial coefficients can be narrowed. Therefore, an effect can be obtained in that the approximation error of the above-described estimated quantization quantity can be reduced. As a result, the estimation accuracy of the quantity of the quantized code can be improved while necessitating a small number of trials coefficients.

Fig. 16 is a block diagram which illustrates the sixth embodiment of an encoding apparatus according to the present invention and structure in such a manner that the present invention is applied to a transmission apparatus for transmitting an image signal.

Referring to Fig. 16, reference numeral 322 represents an input terminal for receiving a digital image signal. The image signal supplied for each line is, in a block forming circuit 324, divided into blocks each of which is composed of, for example, 8 longitudinal pixels and 8 horizontal pixels.

Pixel data in each block is converted into spatial frequency data by a DCT conversion circuit 326. The above-described conversion data is temporarily stored in a memory 328 and as well as the same is linearly quantized in quantizing circuits 338a to 338n with different quantization step coefficients k_1 to k_n received from generating circuits 334a to 334n for generating the predetermined quantization step coefficients k_1 to k_n . According to this embodiment, quantization step coefficients k_1 to k_n generated in the generating circuits 334a to 334n are not made in such a manner that the step interval is equalized as shown in Fig. 19 but the same is widened in inverse proportion to the quantity of the quantized code as shown in Fig. 22.

Data quantized by the quantizing circuits 338a to 338n is variable-length encoded by VLCs 340a to 340n so that code quantities nb_1 to nb_n for each data are obtained. However, the actual encoded data is not transmitted here but only the quantity of the code is measured before it is transmitted to a calculating circuit 342.

In the calculating circuit 342, code quantities nb_1 to nb_n at each measuring point and set code quantity nb_0 determined from the transmission rate are subjected to a comparison so as to identify a measuring point which is larger than nb_0 and nearest nb_0 and a measuring point which is smaller than nb_0 and nearest nb_0 are approximated by a straight line. As a result, quantization step coefficient k_0 with respect to set code quantity nb_0 is estimated before it is transmitted to the quantizing circuit 330. The quantizing circuit 330 receives conversion encoding data transmitted after it has been delayed by a predetermined period by the memory 328 so as to perform the linear quantization with estimated quantizing step coefficient k_0 before its result is supplied to a VLC 332.

In the VLC 332, the variable-length encoding operation is performed so that its result is transmitted to the trans-

mission path through a terminal 336 while extremely reducing the error with respect to a predetermined transmission rate.

According to the above-described structure, the relationship between the total code quantity nb and quantization step coefficient k closely approximates a log curve. Therefore, the quantization step coefficient is selected in such a manner that the measuring points are set in an exponential function manner as shown in Fig. 20 so that, for example, the interval between the measured results of the code quantities is made to be equalized and the quantization error is made to be constant.

Furthermore, an image of a type which encounters a quantization error because of its large code quantity can be processed to improve it in such a manner that the measuring points are, as shown in Fig. 21, set adjacent to the points as each of which the quantization step coefficient is small.

Then, this embodiment will now be described in detail with reference to Figs. 16 and 22.

First, two quantization step coefficients k_3 and k_4 are selected, k_3 and k_4 being arranged to hold the following relationships with optimum quantization step coefficient k_0 :

$$k_3 < k_4, k_0 < k_4$$

Referring to Fig. 16, the linear quantization and the VLC are performed with the quantization step coefficients k_3 and k_4 so that compressed code quantities nb_3 and nb_4 are obtained. Referring to Fig. 22, point (k_3, nb_3) and point (k_4, nb_4) are connected to each other by a straight line so that estimated value k_0' of the quantization step coefficient is obtained from code quantity nb_0 set for each predetermined period.

Actually, since optimum quantization step coefficient k_0 with respect to nb_0 is on a curve shown in Fig. 22, compressed code quantity nb_0' with respect to k_0' and nb_0 always hold the following relationship:

$$nb_0' < nb_0$$

As a result, the desired code quantity cannot be exceeded in any case so that it can be quantized.

As a result of the above-described structure, in a case where the code quantity is small and thereby the estimated error of the quantization step coefficient becomes small, the measuring points is decreased. In a case where the code quantity is large and thereby the error becomes large, the measuring points are increased. Therefore, the estimation accuracy of the quantization step coefficient can be improved.

Although the above-described embodiments are arranged in such a manner that the size of the formed block is made to be 8 x 8, the size may be varied.

Furthermore, an orthogonal conversion (spatial frequency conversion) other than DCT may be employed.

As described above, according to the image processing apparatus according to the present invention, the data quantity for a predetermined region can be set to a desired data quantity while reducing the quantity of hardware and exhibiting satisfactory high accuracy.

The above-described embodiments are not limited to a moving image but the same can be applied to a still image.

The above described invention finds application not only in the processing of images to be displayed by a monitor, but also in image reproduction by printing such as by laser beam or ink jet.

Claims

1. An image processing apparatus comprising:

first encoding means (7;28;330;332) arranged to receive data representing an image, to produce a first amount (B_0') of encoded image data in response to a first control parameter (Q_0); and control means (3 to 5) to adapt said first control parameter (Q_0) so that said first amount (B_0') of encoded image data shall not exceed a predetermined amount (B_0); which apparatus is characterised in that:-

said control means (3 to 5) comprises:

second and third encoding means (3,4;22,23;338a and 340a,338b and 340b), arranged to receive data identical to that received by said first encoding means (7;28;330;332) to produce, in parallel, respective second and third different amounts ($B_1, B_2; nb_1, nb_2$) of encoded image data in response to respective second and third control parameters ($Q_1, Q_2; k_1, k_2$) different from each other; and determining means (5;26;342) responsive to said second and third control parameters ($Q_1, Q_2; k_1; k_2$), said measured second and third amounts

($B_1, B_2; nb_1, nb_2$) and said predetermined amount to determine said first control parameter (Q_0) so that said first amount (B_0) shall approximate but not exceed said predetermined amount (B_0).

- 5 2. An apparatus according to claim 1, wherein said determining means (5;26) is operable to determine said first control parameter by using a linear approximation.
3. An apparatus according to claim 1 or 2, wherein said first encoding means (7;28;330;332) includes quantizing means and the first control parameter (Q_0) is a quantizing step.
- 10 4. An apparatus according to any of claims 1 to 3, wherein the value of the second control parameter (Q_1) is larger than that of said first control parameter (Q_0) and said first amount (B_0) is larger than said second amount (B_1).
5. An apparatus according to claims 1 to 4, wherein said first encoding means (7;28;330;332) is adapted to perform encoding by employing an orthogonal transformation.
- 15 6. An apparatus according to any of claims 1 to 5, including input means to input data representing a sequence of pictures.
7. An apparatus according to any of claims 1 to 6, further comprising a buffer memory (8) for storing the image data encoded by said first encoding means (7).
- 20 8. An apparatus according to any of claims 1 to 7, further comprising transmitting means (9) for transmitting the image data encoded by said first encoding means (7) via a transmission path.
- 25 9. An apparatus according to any of claims 1 to 8, further comprising decoding means (11) for decoding the image data encoded by said first encoding means (7).
10. The apparatus as claimed in claim 2, wherein said linear approximation is based on use of the following formula:

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$$y = a k + b ; a = (B_1 - B_2) / (Q_1 - Q_2); b = (Q_2 B_1 - Q_1 B_2) / (Q_2 - Q_1)$$

where y and k represent said predetermined data amount (B_0) and said first control parameter (Q_0), B_1, B_2 represent said second and third data amounts corresponding to said second and third control parameters Q_1, Q_2 .

- 35 11. An apparatus as claimed in claim 2, wherein said linear approximation is based on use of the following formula:

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$$y = a k + b + \beta$$

where y, a, k and b are as defined in claim 10 and β is a constant selected manually, or automatically in accordance with the characteristics of the image.

- 45 12. An apparatus as claimed in claim 2, wherein said linear approximation is based on the following formula:

$$y = (a + \alpha) k + b + \beta$$

50 y, a, k, b and β being as defined in claim 11 and α being a constant.

- 55 13. An apparatus as claimed in claim 1 including additional encoding means responsive to at least one additional control parameter (Q_3, Q_4) in addition to said first, second and third encoding means; and comparison and selection means to compare the data amounts encoded by said first, second and additional encoding means and to select therefrom two data amounts nearest above and below said predetermined amount, and to select the corresponding control parameters for input to said determining means, as said second and third data amounts and as said second and third control parameters, respectively.
14. An apparatus as claimed in claim 13, including store means holding equispaced parameter values for use as said

control parameters of said second, third, and additional encoding means.

- 5 15. An apparatus as claimed in claim 13 including store means holding proportionate interval parameter values for use as said control parameters of said second, third and additional encoding means, the intervals between said parameter values increasing in proportion to the parameter value.
16. An apparatus as claimed in claim 1, including store means holding parameters for use as said second and third control parameters.
- 10 17. An apparatus as claimed in combined claims 4 and 16, wherein said store means also holds default maximum and minimum parameters (Q_{max} , Q_n) for use as said first control parameter; comparison means for comparing said second and third data amounts with said predetermined amount; and selection means for selecting said default maximum or minimum parameter as said first control parameter when said second data amount exceeds said predetermined amount or said predetermined amount exceeds said first data amount, respectively.
- 15 18. An apparatus according to claim 1, wherein said second and third encoding means perform full encoding operations to produce said second and third amounts of encoded image data.
- 20 19. A method of encoding received data representing an image wherein a first amount (B_o') of encoded image data is produced by a first encoding means (7) in response to a first control parameter (Q_o) and the first control parameter is adapted so that said first amount (B_o') shall not exceed a predetermined amount (B_o), which method is characterised by:
- 25 producing a second amount (B_1) of encoded image data from the received data by controlling a second encoding means (3) using a second control parameter (Q_1);
 producing a third amount (B_2) of encoded image data from the received data by controlling a third encoding means (4), in parallel with said second encoding means (3), using a third control parameter (Q_2) different from said second control parameter; and
 30 determining said first control parameter (Q_o) from said second and third data amounts (B_1 , B_2), said second and third control parameters (Q_1 , Q_2), and said predetermined data amount (B_o) as basis for approximation.

Patentansprüche

- 35 1. Bildverarbeitungsgerät mit
 einer ersten Kodiereinrichtung (7; 28; 330; 332) zum Empfang von ein Bild darstellenden Daten, damit eine erste Menge (B_o') von kodierten Bilddaten im Ansprechen auf einen ersten Steuerparameter (Q_o) erzeugt wird, und einer Steuereinrichtung (3 bis 5) zur Anpassung des ersten Steuerparameters (Q_o), so daß die erste Menge (B_o') von kodierten Bilddaten eine vorbestimmte Menge (B_o) nicht überschreitet,
 40 **dadurch gekennzeichnet, daß**
 die Steuereinrichtung (3 bis 5)
 zweite und dritte Kodiereinrichtungen (3; 4; 22; 23; 338a und 340a, 338b und 340b) zum Empfang von Daten aufweist, die identisch zu denen von der ersten Kodiereinrichtung (7; 28; 330; 332) empfangenen sind, damit
 45 jeweilige zweite und dritte unterschiedliche Mengen (B_1 , B_2 ; nb_1 , nb_2) von kodierten Bilddaten im Ansprechen auf jeweilige zweite und dritte voneinander verschiedene Steuerparameter (Q_1 , Q_2 ; k_1 , k_2) parallel erzeugt werden, und eine auf die zweiten und dritten Steuerparameter (Q_1 , Q_2 ; k_1 , k_2) ansprechende Bestimmungseinrichtung (5; 26; 342) aufweist, wobei die gemessenen zweiten und dritten Mengen (B_1 , B_2 ; nb_1 , nb_2) und die vorbestimmte Menge den ersten Steuerparameter (Q_o) derart bestimmen, daß die erste Menge (B_o') sich der vorbestimmten Menge (B_o) annähert, diese aber nicht überschreitet.
- 50 2. Gerät nach Anspruch 1,
dadurch gekennzeichnet, daß
 die Bestimmungseinrichtung (5; 26) der erste Steuerparameter unter Verwendung einer linearen Annäherung
 55 bestimmt ist.
3. Gerät nach einem der Ansprüche 1 oder 2,
dadurch gekennzeichnet, daß

die erste Kodiereinrichtung (7; 28; 330; 332) eine Quantisierungseinrichtung enthält und der erste Steuerparameter (Q_0) ein Quantisierungsschritt ist.

- 5 4. Gerät nach einem der Ansprüche 1 bis 3,
dadurch gekennzeichnet, daß
 der Wert des zweiten Steuerparameters (Q_1) größer als der des ersten Steuerparameters (Q_0) und die erste Menge (B_n) größer als die zweite Menge (B_1) ist.
- 10 5. Gerät nach einem der Ansprüche 1 bis 4,
dadurch gekennzeichnet, daß
 die erste Kodiereinrichtung (7; 28; 330; 332) die Kodierung unter Einsatz einer Orthogonaltransformation durchführt.
- 15 6. Gerät nach einem der Ansprüche 1 bis 5,
gekennzeichnet durch
 eine Eingabeeinrichtung zur Eingabe von eine Bildsequenz darstellenden Daten.
- 20 7. Gerät nach einem der Ansprüche 1 bis 6,
gekennzeichnet durch
 einen Pufferspeicher (8) zur Speicherung der von der ersten Kodiereinrichtung (7) kodierten Bilddaten.
- 25 8. Gerät nach einem der Ansprüche 1 bis 7,
gekennzeichnet durch
 eine Übertragungseinrichtung (9) zur Übertragung der von der ersten Kodiereinrichtung (7) kodierten Bilddaten über einen Übertragungsweg.
- 30 9. Gerät nach einem der Ansprüche 1 bis 8,
gekennzeichnet durch
 eine Dekodiereinrichtung (11) zur Dekodierung der von der ersten Kodiereinrichtung (7) kodierten Bilddaten.

10. Gerät nach Anspruch 2,
dadurch gekennzeichnet, daß

die lineare Annäherung auf der Verwendung der folgenden Formel beruht:

$$y = ak + b; a = (B_1 - B_2)/(Q_1 - Q_2); b = (Q_2 B_1 - Q_1 B_2)/(Q_1 - Q_2),$$

wobei y und k die vorbestimmte Datenmenge (B_0) und den ersten Steuerparameter (Q_0) darstellen und B_1 , B_2 die den zweiten und dritten Steuerparametern Q_1 , Q_2 entsprechenden zweiten und dritten Datenmengen darstellen.

11. Gerät nach Anspruch 2,
dadurch gekennzeichnet, daß

die lineare Annäherung auf der Verwendung der folgenden Formel beruht:

$$y = ak + b + \beta,$$

wobei y , a , k und b wie in Anspruch 10 angegeben definiert sind und β eine manuell oder automatisch entsprechend den Bildeigenschaften ausgewählte Konstante ist.

12. Gerät nach Anspruch 2,
dadurch gekennzeichnet, daß

die lineare Annäherung auf folgender Formel beruht:

$$y = (a + \alpha)k + b + \beta,$$

wobei y , a , k , b und β wie in Anspruch 11 angegeben definiert sind und α eine Konstante ist.

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13. Gerät nach Anspruch 1,
gekennzeichnet durch

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eine zusätzliche, auf mindestens einen zusätzlichen Steuerparameter (Q_3 , Q_4) ansprechende Kodiereinrichtung zusätzlich zur ersten, zweiten und dritten Kodiereinrichtung, und einer Vergleichs- und Auswahleinrichtung zum Vergleich der von der ersten, zweiten und zusätzlichen Kodiereinrichtung kodierten Datenmengen und zur Auswahl von zwei am nächsten oberhalb und unterhalb der vorbestimmten Menge liegenden Datenmengen daraus, sowie zur Auswahl der entsprechenden Steuerparameter zur Eingabe in die Bestimmungseinrichtung als die jeweiligen zweiten und dritten Datenmengen und die jeweiligen zweiten und dritten Steuerparameter.

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14. Gerät nach Anspruch 13,
gekennzeichnet durch

eine Parameterwerte mit gleichem Abstand zur Verwendung als Steuerparameter der zweiten, dritten und zusätzlichen Kodiereinrichtungen speichernde Speichereinrichtung.

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15. Gerät nach Anspruch 13,
gekennzeichnet durch

eine Parameterwerte mit einem proportionalen Intervall zur Verwendung als Steuerparameter der zweiten, dritten und zusätzlichen Kodiereinrichtungen speichernde Speichereinrichtung, wobei sich die Intervalle zwischen den Parameterwerten proportional zum Parameterwert vergrößern.

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16. Gerät nach Anspruch 1,
gekennzeichnet durch

eine Parameterwerte zur Verwendung als zweite und dritte Steuerparameter enthaltende Speichereinrichtung.

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17. Gerät nach den kombinierten Ansprüchen 4 und 16,
dadurch gekennzeichnet, daß

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die Speichereinrichtung auch Standard-Maximal- und Minimalparameter (Q_{max} , Q_n) zur Verwendung als ersten Steuerparameter, eine Vergleichseinrichtung zum Vergleich der zweiten und dritten Datenmengen mit der vorbestimmten Menge und eine Auswahleinrichtung zur Auswahl des Standard-Maximal- oder Minimalparameters als ersten Steuerparameter enthält, wenn die zweite Datenmenge die jeweilige vorbestimmte Menge übersteigt oder die vorbestimmte Menge die erste Datenmenge übersteigt.

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18. Gerät nach Anspruch 1,
dadurch gekennzeichnet, daß

die zweite und dritte Kodiereinrichtung vollständige Kodiervorgänge zur Erzeugung der zweiten und dritten Mengen von kodierten Bilddaten durchführen.

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19. Verfahren zur Kodierung von ein Bild darstellenden empfangenen Daten, wobei eine erste Menge (B_0) von kodierten Bilddaten im Ansprechen auf einen ersten Steuerparameter (Q_0) von einer ersten Kodiereinrichtung (7) erzeugt wird und der erste Steuerparameter derart angepaßt ist, daß die erste Menge (B_0) eine vorbestimmte Menge (B_0) nicht überschreitet,
gekennzeichnet durch die Schritte

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Erzeugen einer zweiten Menge (B_1) von kodierten Bilddaten aus den empfangenen Daten durch Steuerung einer zweiten Kodiereinrichtung (3) unter Verwendung eines zweiten Steuerparameters (Q_1),

Erzeugen einer dritten Menge (B_2) von kodierten Bilddaten aus den empfangenen Daten durch Steuerung einer zur zweiten Kodiereinrichtung (3) parallelen dritten Kodiereinrichtung (4) unter Verwendung eines vom zweiten Steuerparameter verschiedenen dritten Steuerparameters (Q_2) und

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Bestimmen des ersten Steuerparameters (Q_0) aus den zweiten und dritten Datenmengen (B_1 , B_2) mit den zweiten und dritten Steuerparametern (Q_1 , Q_2) und der vorbestimmten Datenmenge (B_0) als Grundlage für eine Annäherung.

Revendications

1. Appareil de traitement d'images comprenant :

- 5 des premiers moyens de codage (7;28;330;332) agencés de manière à recevoir des données représentant une image, pour produire une première quantité (B_0') de données d'images codées en réponse à un premier paramètre de commande (Q_0); et des moyens de commande (3 à 5) pour adapter ledit premier paramètre de commande (Q_0) de telle sorte que ladite première quantité (B_0') de données d'images codées ne dépasse pas une quantité prédéterminée (B_0); lequel appareil est caractérisé en ce que :
- 10 lesdits moyens de commande (3 à 5) comprennent :
des seconds et troisièmes moyens de codage (3,4;22,23;338a et 340a, 338b et 340b) agencés de manière à recevoir des données identiques à celles reçues par lesdits premiers moyens de codage (7;28;330;332) pour produire, parallèlement, des seconde et troisième quantités respectives différentes ($B_1, B_2; nb_1, nb_2$) de données d'images codées en réponse à des second et troisième paramètres respectifs de commande ($Q_1, Q_2; k_1, k_2$) différents l'un de l'autre; et des moyens de détermination (5;26;342) aptes à répondre auxdits second et troisième paramètres de commande (Q_1, Q_2, k_1, k_2), lesdites seconde et troisième quantités mesurées ($B_1, B_2; nb_1, nb_2$) et à ladite quantité prédéterminée, pour déterminer ledit premier paramètre de commande (Q_0) de telle sorte que ladite première quantité (B_0') doit approximer, mais ne pas dépasser ladite quantité prédéterminée (B_0).
- 20
2. Appareil selon la revendication 1, dans lequel lesdits moyens de détermination (5;26) peuvent fonctionner de manière à déterminer ledit premier paramètre de commande moyennant l'utilisation d'une approximation linéaire.
3. Appareil selon la revendication 1 ou 2, dans lequel lesdits premiers moyens de codage (7;28;330;332) incluent des moyens de quantification et le premier paramètre de commande (Q_0) est un échelon de quantification.
- 25
4. Appareil selon l'une quelconque des revendications 1 à 3, dans lequel la valeur du second paramètre de commande (Q_1) est supérieure à celle dudit premier paramètre de commande (Q_0) et ladite première quantité (B_0') est supérieure à ladite seconde quantité (B_1).
- 30
5. Appareil selon l'une des revendications 1 à 4, dans lequel lesdits premiers moyens de codage (7;28;330;332) sont adaptés pour l'exécution d'un codage en utilisant une transformation orthogonale.
6. Appareil selon l'une quelconque des revendications 1 à 5, comprenant des moyens d'entrée pour entrer des données représentant une séquence d'images.
- 35
7. Appareil selon l'une quelconque des revendications 1 à 6, comprenant en outre une mémoire tampon (8) pour mémoriser les données d'images codées par lesdits premiers moyens de codage (7).
8. Appareil selon l'une quelconque des revendications 1 à 7, comprenant en outre des moyens d'émission (9) pour émettre les données d'images codées par lesdits premiers moyens de codage (7), par l'intermédiaire d'une voie de transmission.
- 40
9. Appareil selon l'une quelconque des revendications 1 à 8, comprenant en outre des moyens de décodage (11) pour décoder les données d'images codées par lesdits premiers moyens de codage (7).
- 45
10. Appareil selon la revendication 2, dans lequel ladite approximation linéaire est basée sur l'utilisation de la formule suivante :
 $y = a k + b$; $a = (B_1 - b_2)/(Q_1 - Q_2)$; $b = (Q_2 B_1 - Q_1 B_2)/(Q_2 - Q_1)$ y et k représentant ladite quantité de données prédéterminée (B_0) et ledit premier paramètre de commande (Q_0), B_1, B_2 représentant lesdites seconde et troisième quantités de données correspondant auxdits seconds et troisièmes paramètres de commande Q_1, Q_2 .
- 50
11. Appareil selon la revendication 2, dans lequel ladite approximation linéaire est basée sur l'utilisation de la formule suivante :
- 55

$$y = a k + b + \beta$$

y, a, k et b étant tels que définis dans la revendication 10 et β étant une constante sélectionnée manuellement ou automatiquement en fonction des caractéristiques de l'image.

- 5 12. Appareil selon la revendication 2, dans lequel ladite approximation linéaire est basée sur la formule suivante :

$$y = (a + \alpha) k + b + \beta$$

10 y, a, k, b et β étant tels que définis dans la revendication 11 et α étant une constante.

- 15 13. Appareil selon la revendication 1, comprenant des moyens additionnels de codage aptes à répondre audit au moins un paramètre de commande additionnelle (Q_3, Q_4) en plus desdits premiers, seconds, et troisièmes moyens de codage; et des moyens de comparaison et de sélection pour comparer les quantités de données codées par lesdits premiers et seconds moyens de codage et lesdits moyens additionnels de codage et sélectionner, à partir de ces quantités, deux quantités de données les plus proches au-dessus et au-dessous de ladite quantité prédéterminée, et sélectionner les paramètres de commande correspondants pour les introduire dans lesdits moyens de détermination, respectivement en tant que lesdites seconde et troisième quantités de données et en tant que lesdits second et troisième paramètres de commande.

- 20 14. Appareil selon la revendication 13, comprenant des moyens de mémoire conservant des valeurs de paramètres équidistantes pour leur utilisation en tant que lesdits paramètres de commande desdits seconds et troisièmes moyens de codage et desdits moyens additionnels de codage.

- 25 15. Appareil selon la revendication 13, comprenant des moyens de mémoire conservant des valeurs de paramètres d'intervalles proportionnées, pour leur utilisation en tant que lesdits paramètres de commande desdits seconds et troisièmes moyens de codage et desdits moyens additionnels de codage, les intervalles entre lesdites valeurs de paramètres augmentant proportionnellement à la valeur du paramètre.

- 30 16. Appareil selon la revendication 1, comprenant des moyens de mémoire conservant des paramètres pour leur utilisation en tant que lesdits seconds et troisièmes paramètres de commande.

- 35 17. Appareil selon les revendications 4 et 16 combinées, dans lequel lesdits moyens de mémoire conservent également des paramètres maximum et minimum implicites (Q_{max}, Q_n) pour leur utilisation en tant que ledit premier paramètre de commande; des moyens de comparaison pour comparer lesdites seconde et troisième quantités de données à ladite quantité prédéterminée; et des moyens de sélection pour sélectionner ledit paramètre maximum ou minimum implicite en tant que ledit premier paramètre de commande lorsque ladite seconde quantité de données dépasse ladite quantité prédéterminée ou que ladite quantité prédéterminée dépasse ladite première quantité de données.

- 40 18. Appareil selon la revendication 1, dans lequel lesdits seconds et troisièmes moyens de codage exécutent des opérations de codage complet pour produire lesdites seconde et troisième quantités de données d'images codées.

- 45 19. Procédé pour coder des données reçues représentant une image, dans lequel une première quantité (B_0) de données d'images codées est produite par des premiers moyens de codage (7) en réponse à un premier paramètre de commande (Q_0) et le premier paramètre de commande est adapté de telle sorte que ladite première quantité (B_0) ne dépasse pas une quantité prédéterminée (B_0), lequel procédé est caractérisé par :

la production d'une seconde quantité (B_1) de données d'image codées à partir des données reçues par commande de seconds moyens de codage (3) en utilisant un second paramètre de commande (Q_1);

50 la production d'une troisième quantité (B_2) de données d'image codées à partir des données reçues par commande de troisièmes moyens de codage (4), en parallèle avec lesdits seconds moyens de codage (3), en utilisant un troisième paramètre de commande (Q_2) différent dudit second paramètre de commande; et

55 la détermination dudit premier paramètre de commande (Q_0) à partir desdites seconde et troisième quantités de données (B_1, B_2), desdits second et troisième paramètres de commande (Q_1, Q_2), et de ladite quantité prédéterminée de données (B_0) en tant que base pour l'approximation.

FIG. 1

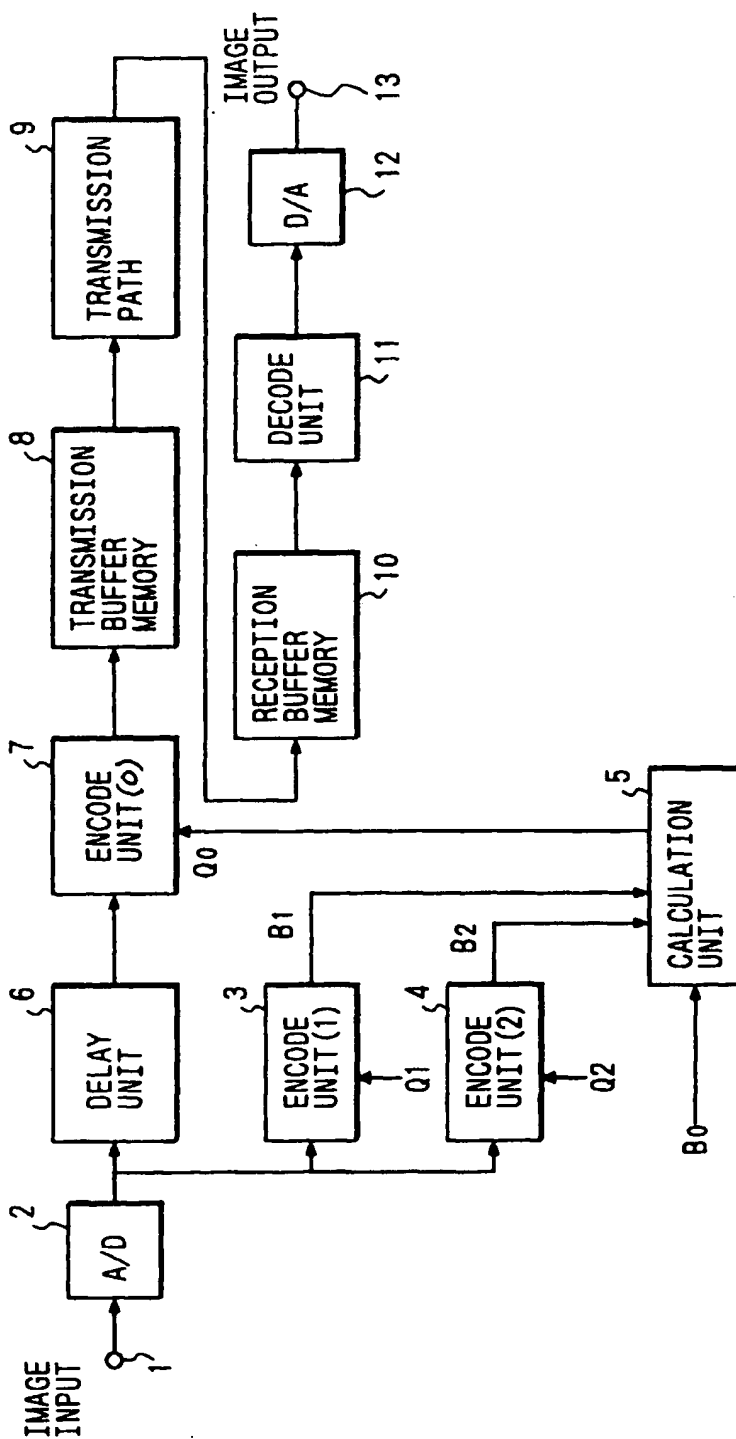


FIG. 2

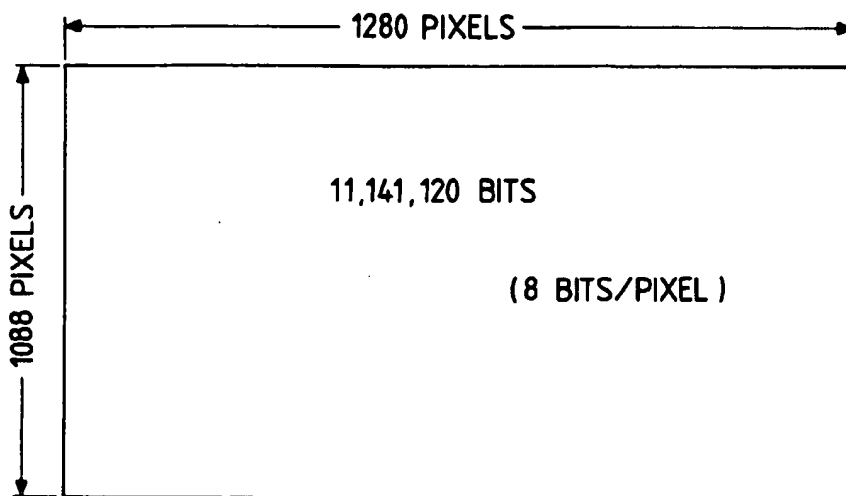


FIG. 3

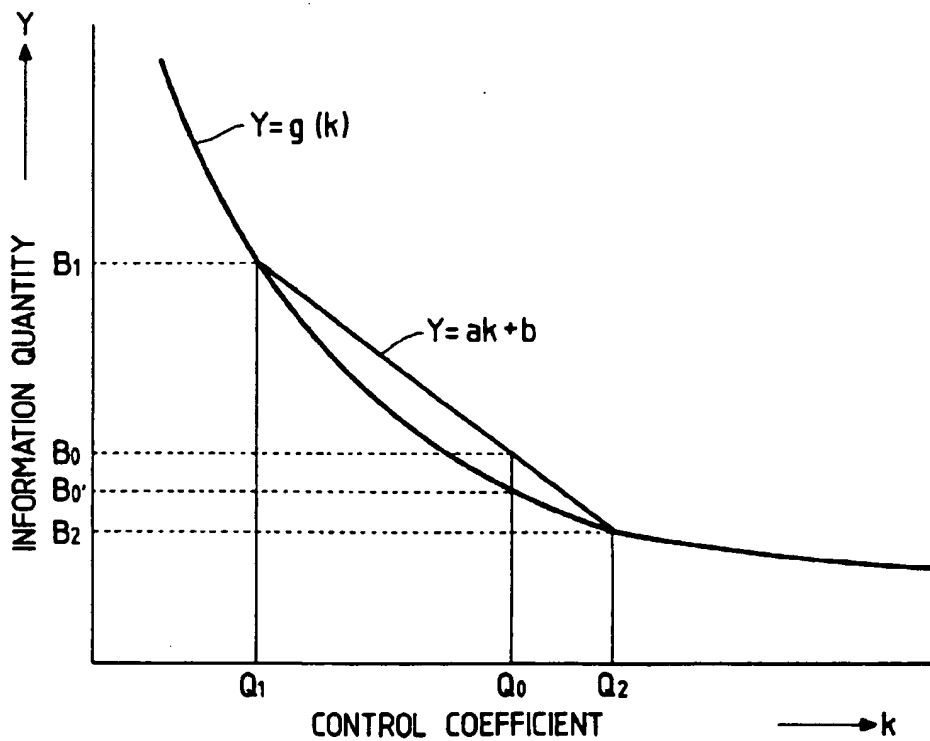


FIG. 4

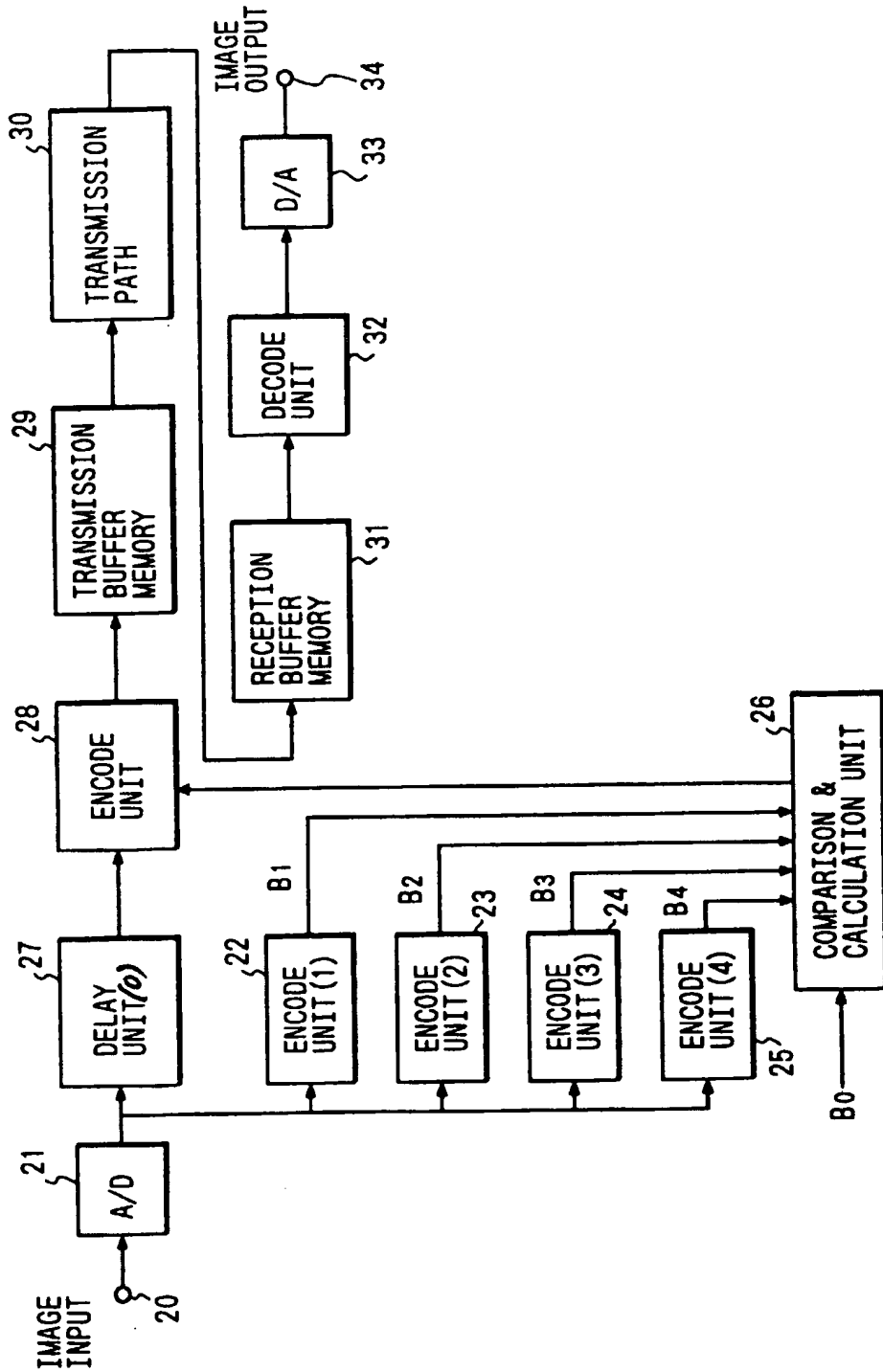


FIG. 5

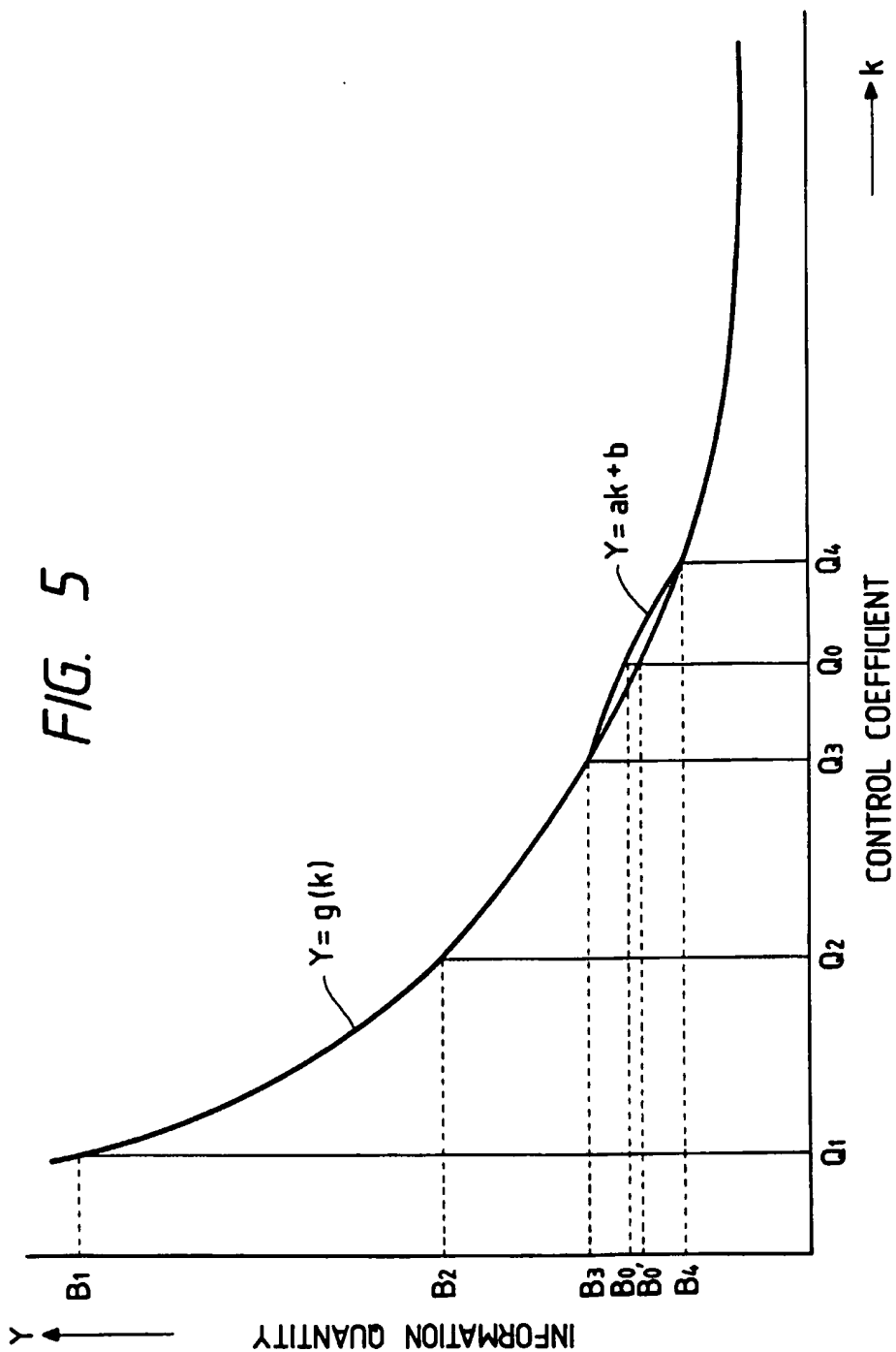
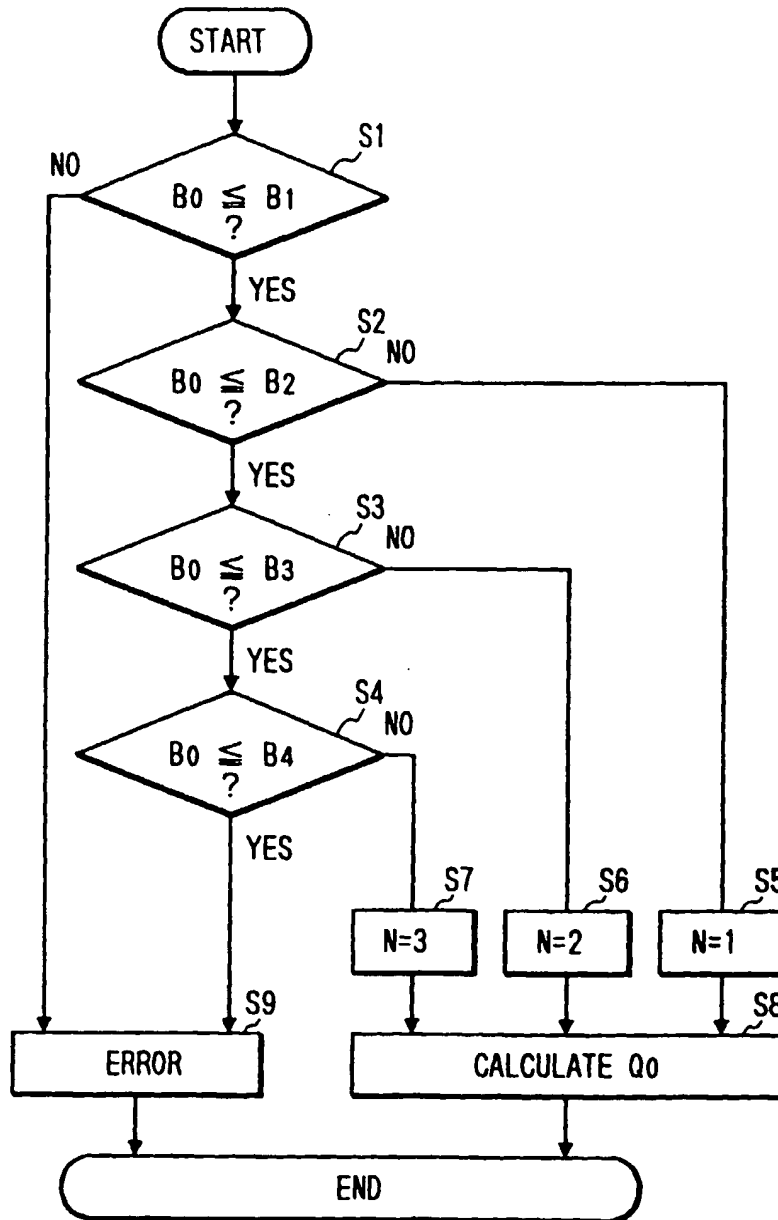


FIG. 6



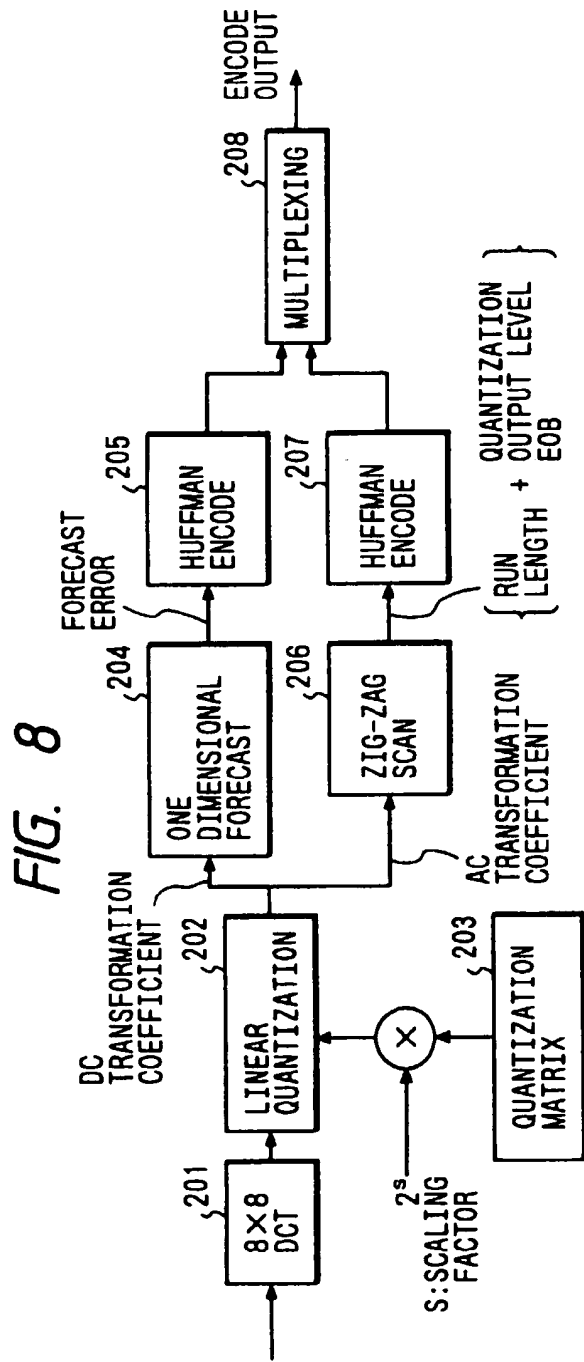
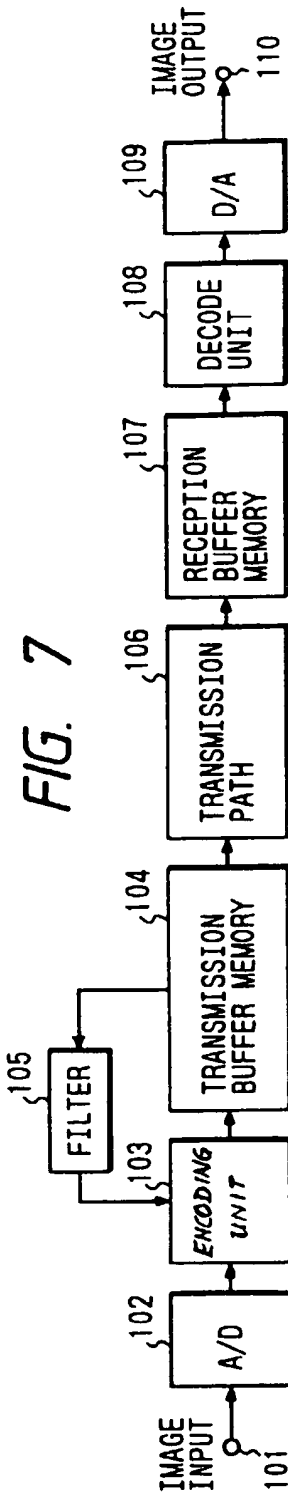


FIG. 9

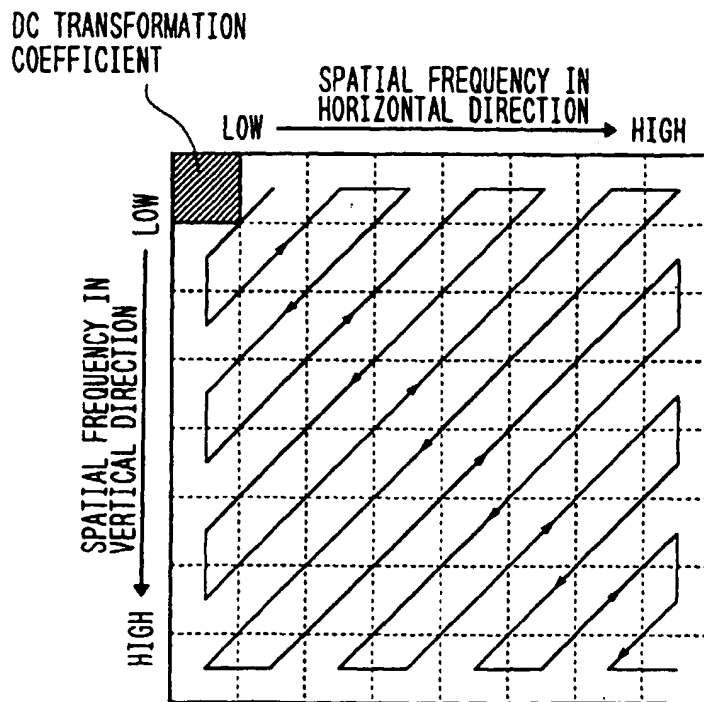
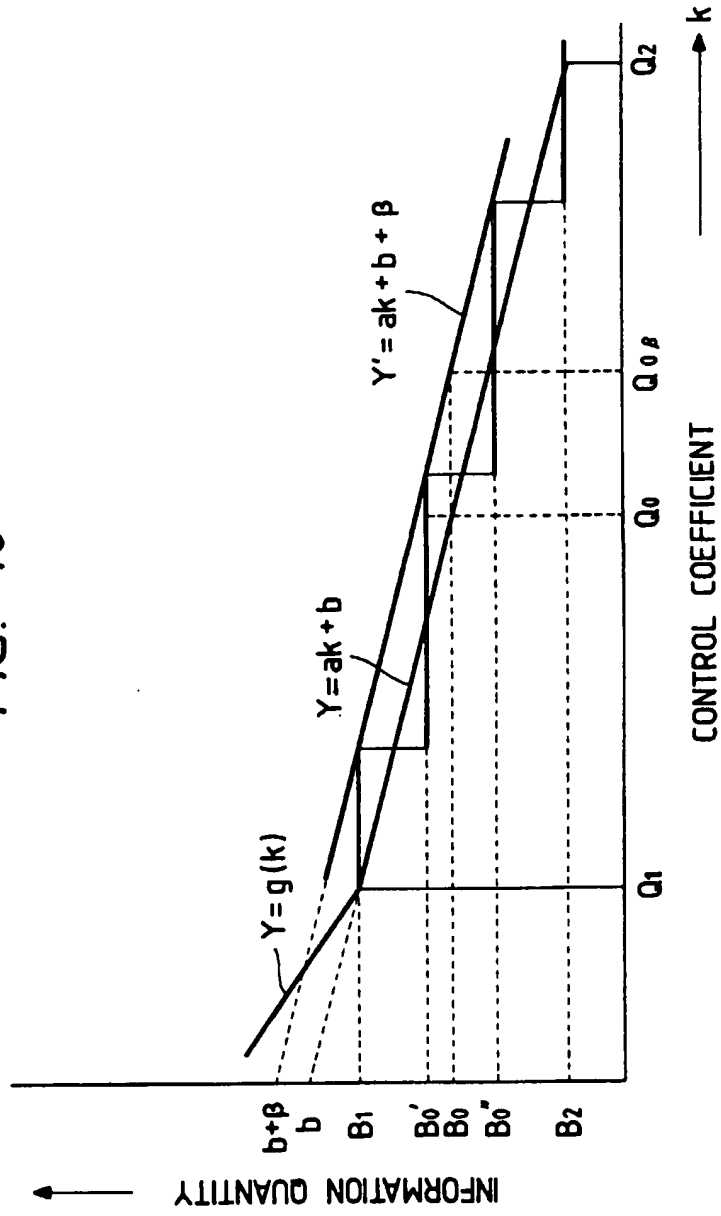
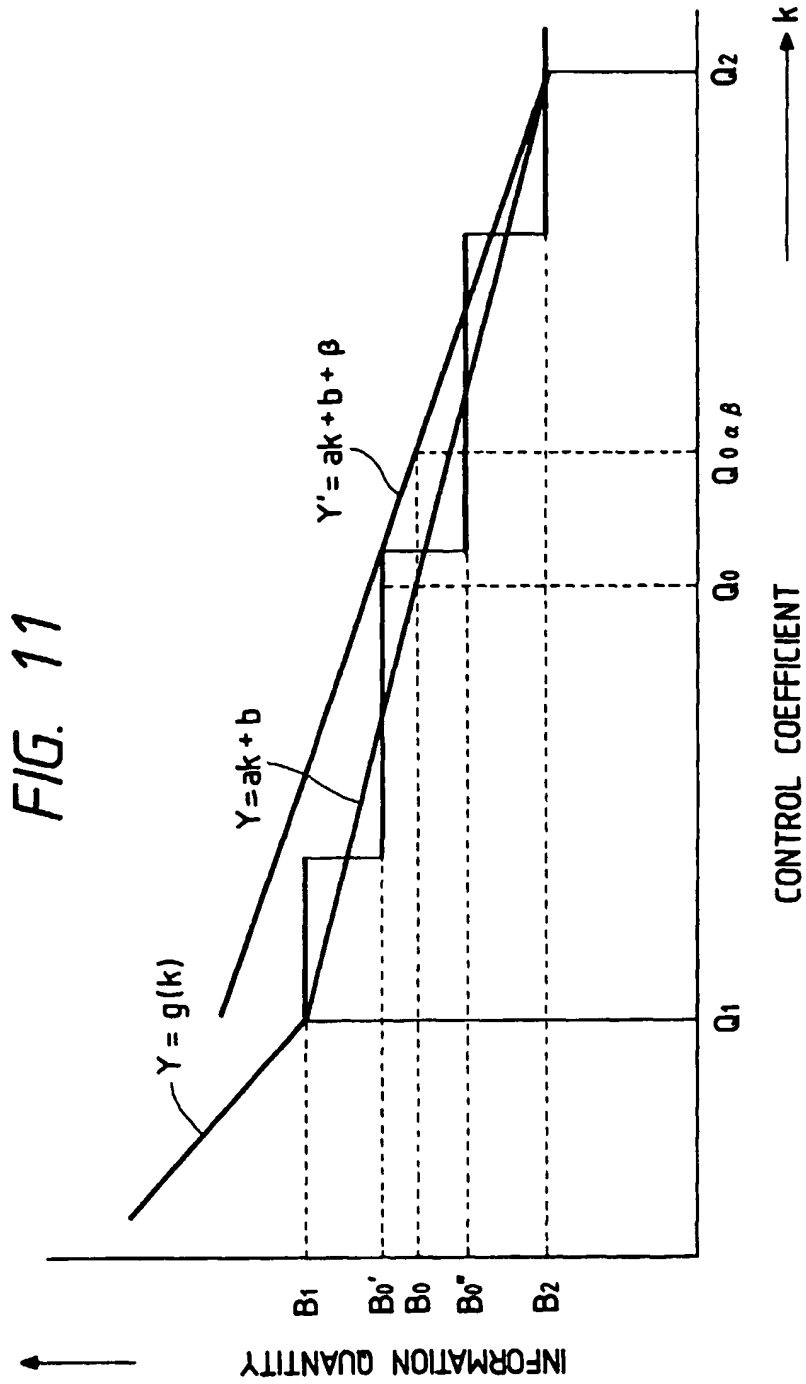


FIG. 10





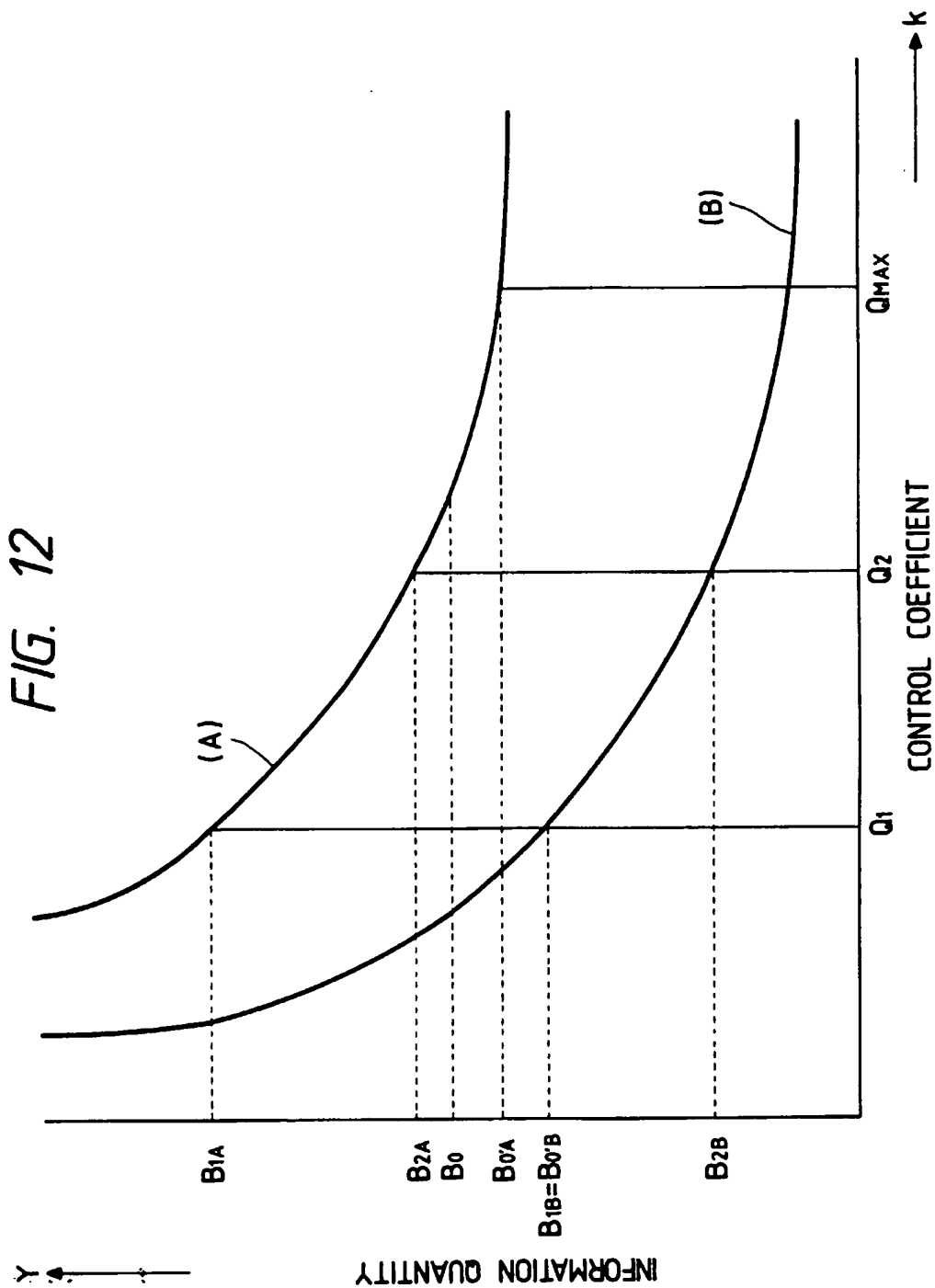


FIG. 13

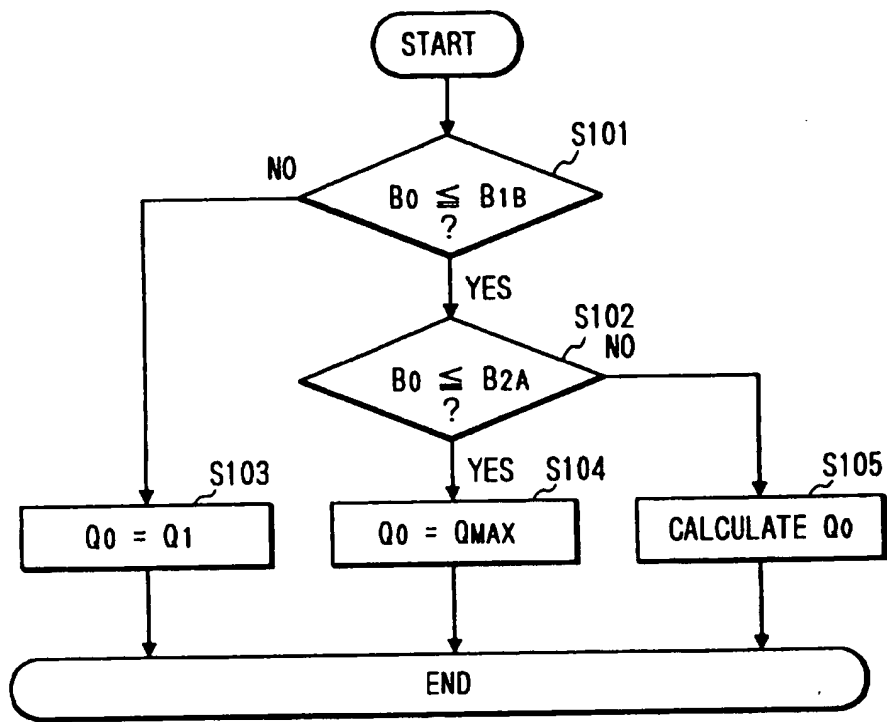


FIG. 14

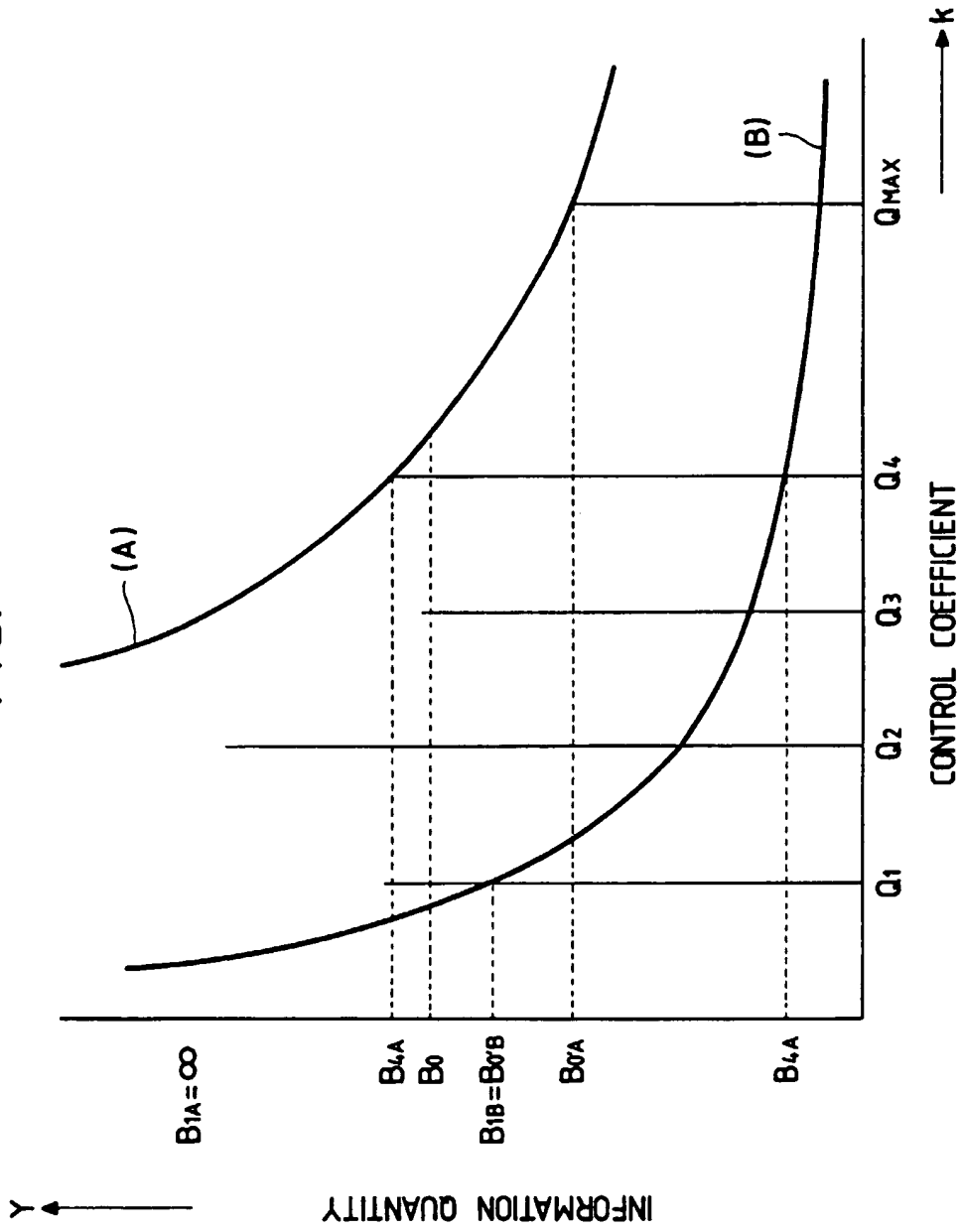


FIG. 15

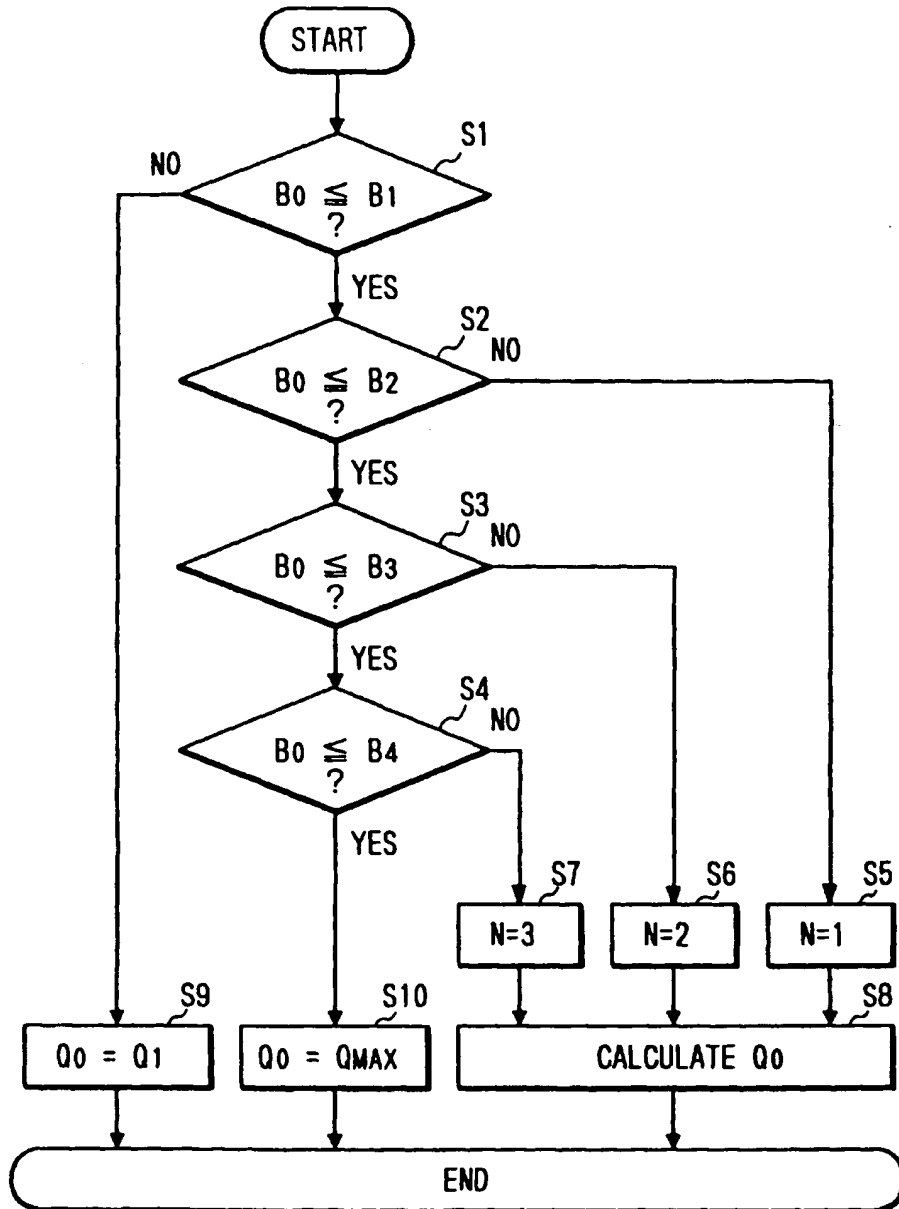


FIG. 16

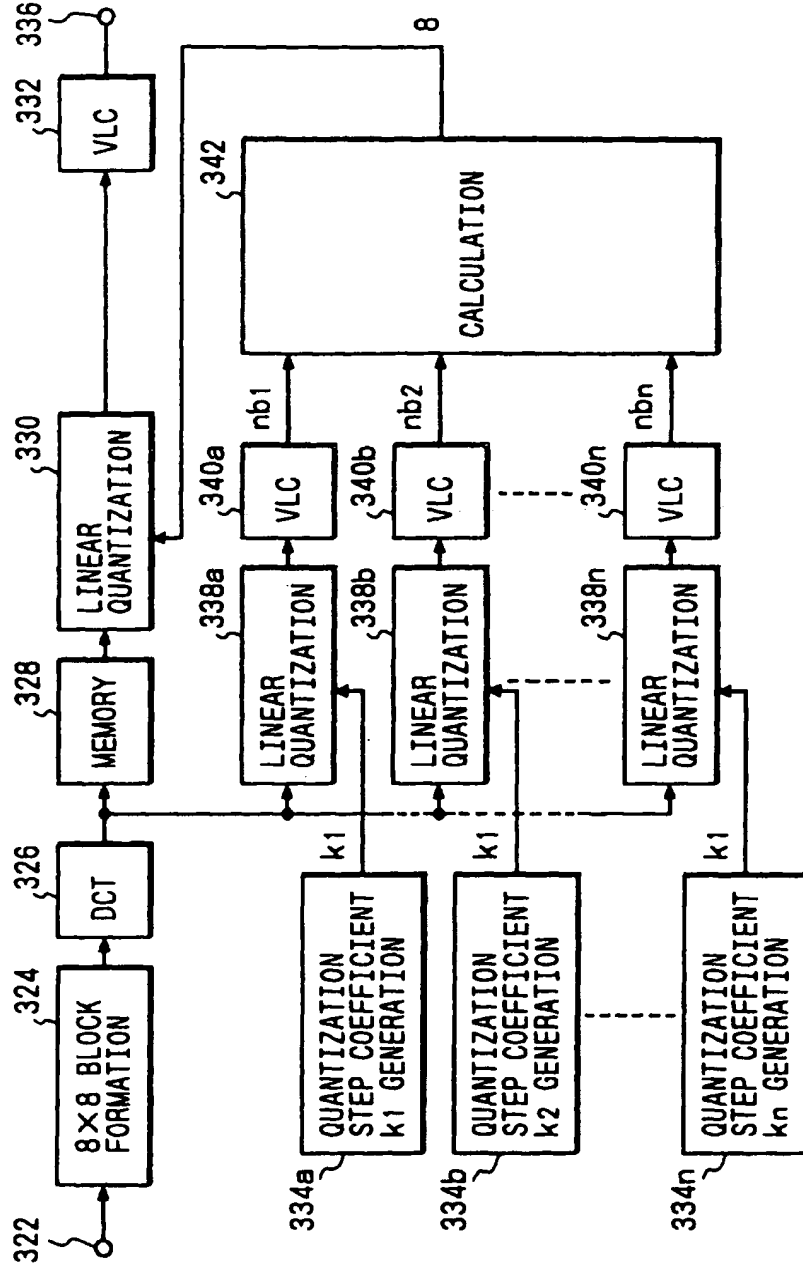


FIG. 17

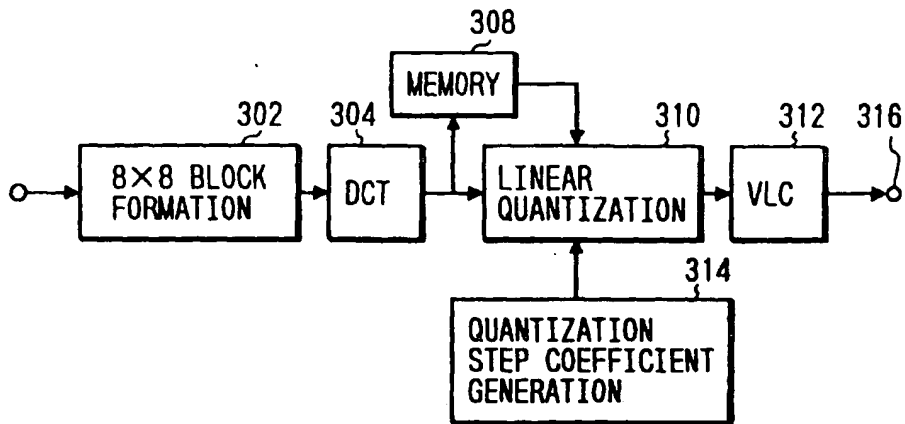


FIG. 18

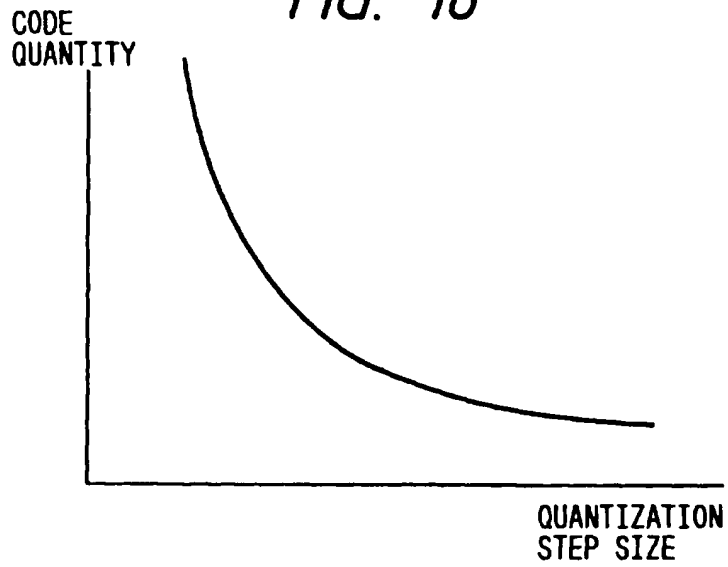


FIG. 19

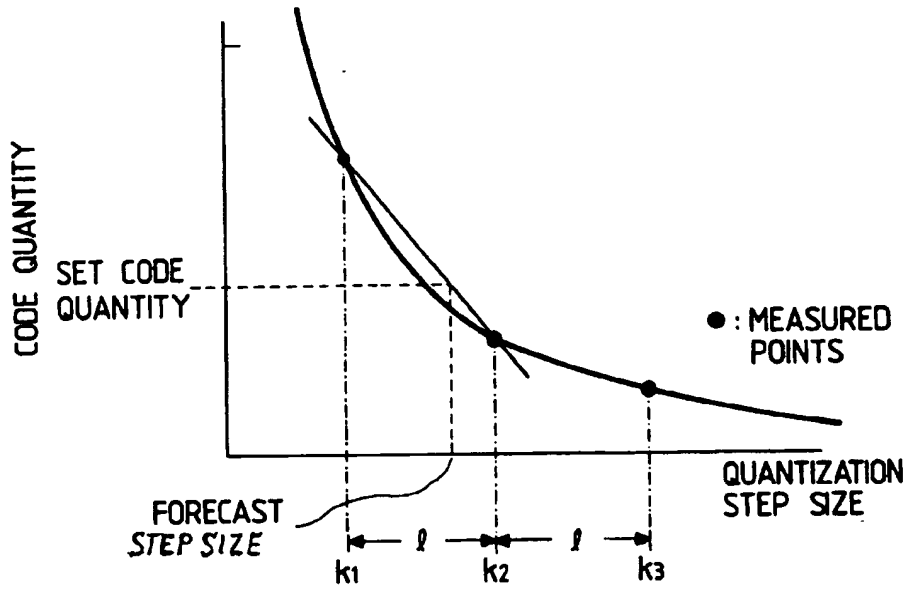


FIG. 20

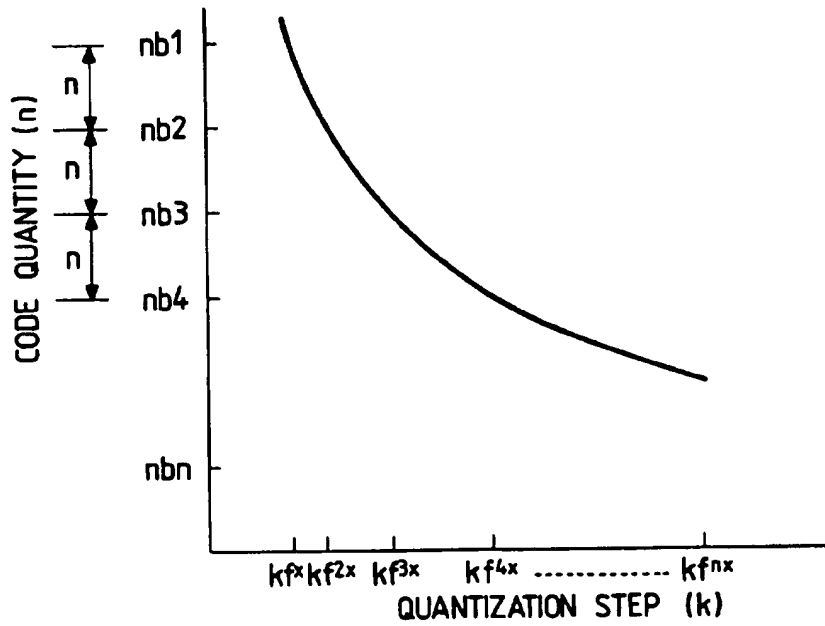


FIG. 21

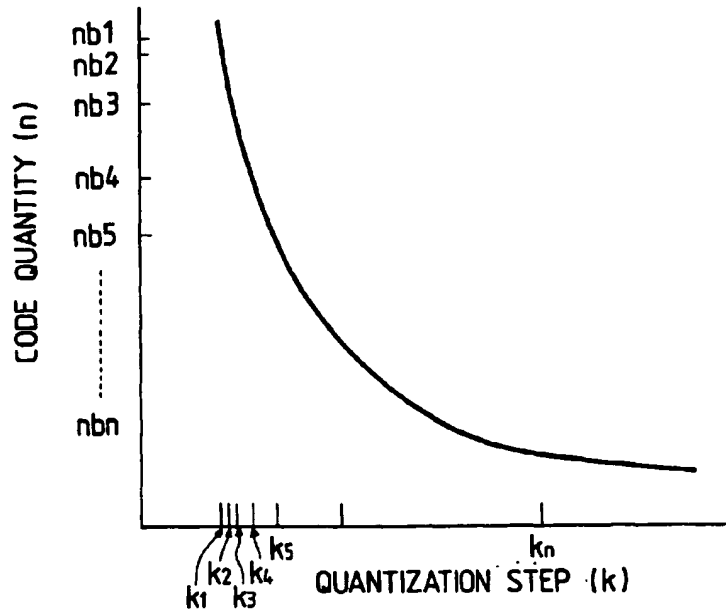
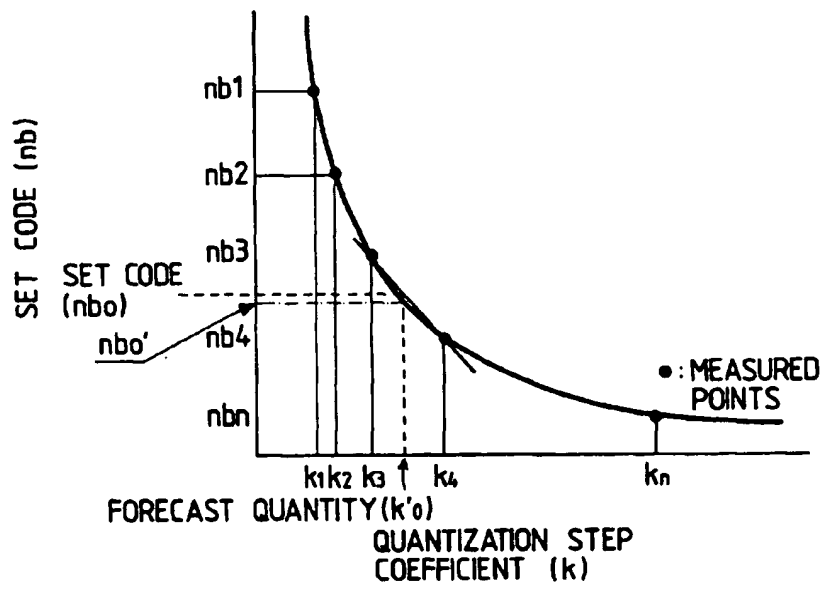


FIG. 22





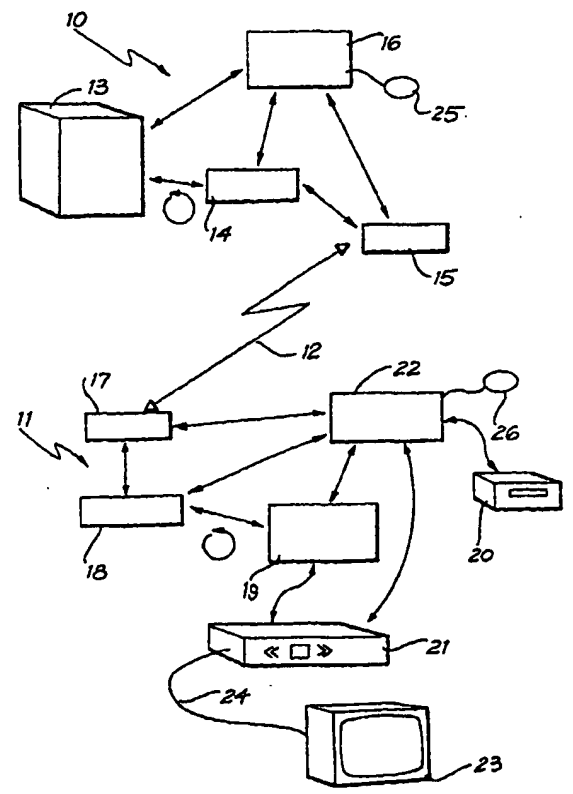
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(54) Title: AN INFORMATION TRANSMISSION SYSTEM FOR INCREASING THE EFFECTIVE RATE OF TRANSFER OF INFORMATION

(57) Abstract

An information delivery system comprises equipment located at a first or storage location (10) and additional equipment located at a second or utilization location (11). The locations are interconnected for transmission of information therebetween by a communication medium (12). The system includes means and methods for increasing the effective rate of transfer of information across information medium (12). These means and methods include data compression including iterative data compression. The means and methods further include the synchronised superposition of channels forming communication medium (12). Communication medium (12) can include a cellular mobile telephone network to permit transmission of information between mobile stations (311, 312) and to cellular receivers (217).



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An Information Transmission System for Increasing the Effective Rate of Transfer of Information

FIELD OF THE INVENTION

The present invention relates to improvements in information transmission systems and, more particularly, to such systems where it is desired to transmit relatively wide bandwidth data such as compressed or real time video data.

BACKGROUND ART

Electronic storage technology has reached the stage where large volumes of information can be stored relatively cheaply and accessed from storage relatively quickly.

There remain, however, problems in transmitting the large volumes of information over communication channels or networks sufficiently quickly and sufficiently conveniently to be readily usable by the consumer.

It is an object of the present invention to address or substantially ameliorate this problem.

DISCLOSURE OF THE INVENTION

Accordingly in one broad form of the invention there is provided an information delivery system for transmission of information from a first location to a second location, said system including first information processing means at said first location, second information processing means at said second location, and a communication channel adapted to transmit said information between said first location and said second location.

The information may be stored in digital form or in analog form at the first location.

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The information may be transmitted over the communications channel in digital form or in analog form.

Preferably, the first location comprises a storage location and includes a storage bank in which said information is stored and the second location comprises a utilization location and includes information output, display, presentation or playback means. The second location may also include a storage bank.

The communication channel may be implemented as a wide bandwidth data path by the establishment of a plurality of individual channels of predetermined bandwidth acting together to connect said first location to said second location whereby a bandwidth greater than the bandwidth of any one of said individual channels is available for transmission of said information.

The communication channel may comprise an apparent wide band channel by compression of said information prior to transmission over said channel.

The information is preferably transmitted over said communications channel in real time. The information may also be transmitted in compressed form in less than real time.

The first information processing means may include information storage means and information compression means and the data may be passed from said information storage means to said information compression means for compression of said data prior to return to said storage means. Preferably, the information is iteratively compressed by

repeated, adaptive and selective invocation of said compression means.

The second information processing means may include information decompression means and data storage means.

5 Preferably, such decompression means decompresses information prior to storage of said information in said storage means. The information may be iteratively decompressed by repeated adaptive and selective invocation of said decompression means, potentially involving repeated
10 passage between said decompression means and said storage means.

The communication channel may include at least part of a PSTN, ISDN, cellular telephone network, cable, satellite, microwave or optical fibre.

15 Preferably, the second information processing means includes audio, text, graphical or video presentation, playback, output and display means whereby information comprising such data transmitted over said communication channel can be provided to a user at said second location.

20 The display means may comprise a personal computer system, a television receiver, a video phone terminal or a hand-held mobile phone incorporating a video data display. Such a mobile phone may comprise a relatively high electromagnetic radiation emitting portion and a relatively
25 low electromagnetic radiation emitting portion, the low radiation emitting portion being adapted for placement at or near the head of a user and in communication with the high electromagnetic radiation

emitting portion; the high electromagnetic radiation emitting portion being adapted for location elsewhere on a user and being further adapted for communication with a cellular telephone network.

5 The present invention also relates to video compression techniques and, more particularly, to an advantageous usage of such techniques where a large volume of video data is to be transferred.

 Accordingly, in a further broad form of the invention,
10 there is provided a system for transmission of video information from a storage location to a utilisation location; said system including a storage bank at said storage location wherein said video information is stored in digital form; said system further including video
15 information playback means at said utilisation location; said system also including transmission means whereby said video information is transmitted from said storage location to said utilisation location on demand.

 A further storage bank may be located at said
20 utilization location.

 Preferably, the transmission means communicates said video information over a communications medium comprising either the public switched telephone network or unused or spare television channel band width.

25 According to another aspect of the invention there is provided an information delivery system comprising wide area signal delivery means delivering a signal containing information to a plurality of local receiver means

distributed throughout a wide area; each said local receiver means communicating said signal to respective local signal processing means whereby said signal is processed for transmission to a local cellular telephone network for reception by cellular receivers.

The information may be compressed by said local receiver means prior to transmission over the local cellular telephone network and the information is decompressed by each cellular receiver.

The information may be passed as wide band width information over more than one channel of said local cellular telephone network in a synchronised manner to a designated one of said cellular receivers.

The present invention also relates to communication of relatively wide-bandwidth information over cellular telephone networks and the like and, more particularly, to transmission of video information over such networks. Accordingly, there is provided a method for the establishment of a wide-bandwidth data path on a cellular telephone network.

The wide-bandwidth data path may be wide enough for real time video information for the purposes of establishment of a video phone connection between subscribers on said cellular telephone network.

The said data path may comprise a plurality of individual channels with portions of the bandwidth of the wide-bandwidth data signal being distributed across said plurality of individual channels.

In a further broad form of the invention there is

provided a wide-bandwidth data path on a cellular telephone network comprising the establishment of a plurality of individual channels of predetermined bandwidth acting together to connect subscribers together whereby a wide-
5 bandwidth data connection is established between subscribers having a bandwidth greater than the bandwidth of any one of said individual channels.

The invention further relates to a modular cellular telephone and, more particularly, to such a telephone
10 adapted to minimise the level of radiation emanating from the telephone near the head of a user.

Accordingly, in a further broad form of the invention, there is provided a mobile telephone communication device comprising a high radiated power portion and a low radiated
15 power portion; wherein the low radiated power portion is physically separate from said high radiated power portion; said high radiated power portion in wireless communication with base stations of a mobile telephone network to which said mobile telephone communication device is adapted to
20 connect; said high radiated power portion in communication with said low radiated power portion at a predetermined low radiated power and said low radiated power portion correspondingly in communication with said high radiated power portion also at said low radiated power.

25 BRIEF DESCRIPTION OF THE DRAWINGS

In order that the invention may be more readily understood and put into practical effect, reference will

now be made to the accompanying drawings in which;-

- 5
Fig. 1 is a block diagram of an information transmission system for a video movie on demand service according to a first embodiment of the present invention.
- Fig. 2 is a block diagram of a second embodiment of the invention implemented as a pay television delivery system.
- 10
Fig. 3 is a block diagram of a typical arrangement of a mobile telephone system;
- Fig. 4 is a block diagram illustrating a typical data path of an individual channel on a mobile telephone network;
- 15
Fig. 5 illustrates a wide-band interconnection across a mobile telephone network according to a particular implementation of the communication medium for the system of either Fig. 1 or Fig. 2;
- 20
Fig. 6 is a block diagram of a mobile telephone communication device adapted to perform at least some functions of either or both of the storage location equipment or utilization location equipment of Fig. 1; and
- 25
Fig. 7 is a location diagram illustrating a preferred form of use of the mobile telephone communication device of Fig. 6

MODES FOR CARRYING OUT THE INVENTION

The information transmission system illustrated in Fig. 1, includes equipment located at a storage or first location 10 and additional equipment located at a utilisation or second location 11. Communication of information takes place across a communication medium 12 between the two locations.

The equipment at the storage location 10 primarily comprises first information processing means comprising a storage bank 13, compression device 14 and transmitter/receiver 15 all controlled by system controller 16.

In this instance, the storage bank stores video movies in their entirety or in partly or fully compressed digital form. When a particular movie is selected, the digital information comprising that movie is passed to compressor 14 if compression is necessary and then transmitted by transmitter receiver 15 over medium 12 to the equipment at utilisation location 11.

The equipment at the second or utilisation location 11 comprises second information processing means comprising a corresponding receiver/transmitter 17, a decompression device 18, local digital storage 19, credit card reader (or user authentication device) 20 and video replay controller/modulator 21. These devices are controlled by system controller 22 in a manner whereby a selected video movie can be received from digital storage bank 13, stored locally on local digital storage 19 and played back onto

T.V./display 23 via the video replay controller/RF modulator 21.

The digital storage bank 13 can comprise a high capacity storage medium such as a WORM drive or CD ROM system having the capacity to store information equivalent to many video movies. The compressor 14 can comprise a digital processor specifically adapted to compress digital information prior to transmission and the decompressor 18 can decompress prior to display. The transmitter/receivers 15, 17 can incorporate modems where the public switched telephone network is to be used as the channel 12. Equivalent modulation/demodulation arrangements can be used where the transmission medium 12 comprises the unused or spare band width of a T.V. channel.

System controls 16, 22 can comprise microprocessor based control devices adapted to orchestrate information transmission between the various components at the storage location and at the utilisation location. Local storage 19 can comprise a high capacity magnetic disc drive whilst video replay controller and RF modulator 21 can comprise a modified video player adapted to receive video image input from local store 19 instead of from the read head of a cartridge based video player.

Credit card reader 20 can comprise any one of the commercially available readers available on the market and, for example, used as EFTPOS terminals.

In use, a consumer located at utilisation location 11 initiates a browse and select operation via system control

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22. System control 22 communicates over communication medium 12 to provide the appropriate summary information from digital storage bank 13. To make a selection and initiate a send operation, the consumer must provide the appropriate payment by entry of an appropriate credit or debit card into card reader 20.

Once successful payment has been signalled, the selected movie is passed in digital form from storage bank 13 via compressor 14 over communication medium 12 to local store 19 where it can be accessed by the consumer using the video player controls on video player 21. The controls would include those of the type typically found on a cartridge tape video player.

The storage system control 16 is capable of the following functions:-

- (a) accept and process user commands and provide messages in response;
- (b) accept and process supervisor interactions, including addition of functions;
- (c) maintain billing, accounting, usage, inventory and access authority (security) information to support operation of the system and use by utilization sites;
- (d) control of and transfer of data between 13, 14, 15;
- (e) recovery from incorrect commands, errors and catastrophic events (e.g. power cut);

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- (f) management of compression activities and data formats;
- (g) management of data storage layout, indexing and retrieval;
- 5 (h) interface to other possible associated systems for data and control interaction (e.g. computers, peripherals (e.g. printers), intelligent image or video generation devices, receiver stations).

The utilization system control 22 is capable of the
10 following functions:-

- (a) accept and process user commands and provide messages in response;
- (b) provide billing, accounting, usage information on demand;
- 15 (c) allow user access to inventory and billing information from storage site;
- (d) control of and transfer data between 17, 18, 19 and 21;
accept user payment and access authority input
20 from 20;
- (e) recovery from incorrect commands, errors and catastrophic events;
- (f) management of decompression activities for local format/formats;
- 25 (g) management of local data storage and retrieval;
- (h) interface to other possible associated devices for data and control interaction;

-12-

- (i) integration facilities for other systems sharing use of transmission link 12;
- (j) operation of appropriate components of utilization system in the absence of transmission link 12 (i.e. 18, 19, 21 to permit e.g. tape to local store transfers).

The video compression technique can cater for varying user needs such as different bandwidths for transmission link 12, different display characteristics and quality at TV/display 23, different storage modes or capacity at local store 19 or storage bank/data source 13 for different applications.

The video compression technique comprises several separate compression methods of which one will be selected prior to use, or several adaptively mixed during use. The methods described below could be selectively used and a record maintained of the selections made, to be transmitted to the decompressor along with the compressed data so that the same selections can be reproduced during decompression.

Some such selections may be deduced by the decoder if explicit conditions for selection switching are incorporated in the decompression algorithm which are identical to the decision criteria used by the compression algorithm (i.e. are based only on data already processed by the algorithm, not any future unseen data).

Various compression methods can be utilized including scene structure analysis, subsampling/quantization, compression standards and information theoretic coding.

In the context of this description, "pixel" means a single displayable sample (i.e. point) of digital image information, "frame" means a single complete digital image in the video sequence, "scene" means a succession of adjacent frames containing closely related data, "region" means a set of adjacent pixels within a frame that contain closely related information, "boundary" means the set of adjacent pixels that are each adjacent to other pixels in two or more regions, "block" means an adjacent rectangular group of pixels, "line" means a block of single pixel width, "texture" means the pattern relationships existing between groups of adjacent pixels, in either regular or irregular pattern form, and "neighbourhood" means a set of adjacent pixels relative to a specific single pixel.

With scene structure analysis, the successive frames of the video sequence will be analysed in digital form using a computer algorithm, to identify:-

- (i) scene changes, on the basis of more than a prescribed error tolerance between pixel values in adjacent frames;
- (ii) movements and changes affecting size, position, orientation, detail (sharpness), clarity, colour/intensity, texture and boundary shape of regions over pairs and sets of adjacent frames (including motion compensation and optical flow);
- (iii) mutual interaction of regions including overlap, transparency, warping, overlay.

Identification of regions will be undertaken by

intensity/colour and texture segmentation methods.

With subsampling/quantization, reduction in amount of pixel information per region or per frame will be undertaken by all or some of:-

- 5 (i) Spatial resolution reduction by subsampling or
 resampling of groups of pixels in blocks, lines,
 boundaries, regions using a regular (similar) or
 varying (irregular) size of input and output
 samples and sets of sample values, at regular or
10 irregular positions from region to region, from
 frame to frame or from scene to scene, or within
 half-frame alternate scow interlace.
- (ii) Visual quality reduction by subsampling or
 resampling of colour/intensity and texture,
15 definition of representative subsets of these,
 models for regional changes and importance of
 these to replace the specification of values
 pixel by pixel, and increasing visual effects
 associated with fast movement (such as motion
20 blur), regular/repeated motion (cycles of
 movement and kinephantom) and existence of
 multiple regions having different contributions
 to visual understanding of the scene (e.g. focus
 blur, random noise, relative intensity/colour as
25 perceived rather than as explicitly measured and
 represented).
- (iii) Temporal resolution by subsampling or resampling
 frames in a sequence to provide description of

changes pixel by pixel, region by region and
frame by frame over a separation of several
frames in time, and by quantizing types and
amounts of changes which can be represented as
described in (a)ii).

- (iv) Frequency resolution obtained by transforming
arbitrary groups of pixels, including blocks,
regions, frames and scenes, to alternative
representation providing frequency descriptions
for the group, such as Fourier and related
transforms, wavelet decomposition, sub-band
coding or signatures to permit selective
frequency bandwidth in the data. The
quantization techniques to be employed include
table lookup, vector quantization, probability
clustering, decimation, iterative improvement and
selection.

In the case of compression standards, the formats
established by existing ISO and CCITT standards would be
used (to allow ease of implementation, use of hardware
implementation and compatibility with different
decompressors). These formats might include:-

- (i) JPEG
(ii) MPEG, MPEG-2 and MPEG-4
(iii) H.261
(iv) FAX GROUP 3 and 4
(v) JBIG

With information theoretic coding, the use of methods

in conjunction with above techniques which will achieve optimally compact representation of compressed data streams or preprocessed data to produce compressed data streams including:-

- 5 (i) Entropy (probability) coding;
 (ii) Codebook or dictionary construction;
 (iii) Difference coding (residuals or errors);
 (iv) Predictive coding;
 (v) Context or neighbourhood based coding.

10 In addition to the above methods, the information describing which selection has been made and any variable parameters associated with that selection, might need to be specified for transmission to the decoder. This would be implemented by defining a set of symbols to represent each
15 different selection and inserting them prior to the compressed data stream, or in a separate sequence from the compressed data stream. These symbols may be subject to further compression by the methods immediately above.

 The decoder will reconstruct pixels, regions, frames
20 and scenes by first decoding the compressed data stream and selection symbols to provide an initial reconstructed version of a frame, then interpolating or estimating missing or approximated data values to achieve the full resolution required for replay or display, including
25 systematic or random dithering, blurring, sharpening or resampling to hide visual artifacts.

 Although the invention according to a first embodiment has been described somewhat specifically in relation to the

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delivery of video information from a conceptual storage location to a conceptual utilization location it is intended that the behaviour of the entire system described thus far should be viewed broadly functionally.

5 So, for example, transmission medium 12 can be realised using analog or digital techniques and could form part of a public, private or corporate network. For example transmission media 12 could be realised by any one of the following means:

10 twisted pair or other PSTN medium, including ISDN/B-ISDN lines, ADSL;
Optical fibre or other Telecom data service infrastructure lines;
Trunked radio;

15 Single or multiple channel cellular network;
Microwave links;
Satellite links;
Excess channel space on TV broadcast spectrum

In certain implementations the transmission medium 12 can support bidirectional communications. Perhaps the most ambitious use of bidirectional capability is where the system of Fig. 1 is mirror imaged and superposed upon itself so that at each location there is both storage and utilization capability. This aspect is described further

20 in later embodiments below in the context of personal communications devices communicating over the mobile telephone network and the like.

In less ambitious forms bidirectionality of

transmission medium 12 is required merely for exchange of commands, confirmations, data and video where necessary and appropriate.

Storage bank 13 can be implemented using either digital or analog means. Analog forms of storage can include video disc and video tape. Also included is the situation where information is produced in real time for passage from storage bank 13 to transmission medium 12 eg. relying on information produced by third parties. Composite or juke box arrangements are also envisaged where information passed to transmission medium 12 is derived from more than one such source in accordance with the requirements of a user at the utilisation location 11.

Data stored in storage bank 13 can be compressed in full or in part. Furthermore interactive compression procedure can be followed whereby data is passed from storage bank 13 to compression device 14 for return in compressed form to storage bank 13. The thus compressed data may again be passed to compression device 14 for further compression and return to storage bank 13. Similar activity may occur during decompression with 18 and 19. Furthermore the form in which the data is represented or stored may vary during each iteration eg. broadcast-compress-analog; broadcast-compress-digital; digital-compress-digital; analog-compress-digital.

In particular forms of the invention the degree of compression, the nature of compression, the number of iterations of compression and the manner of storage of

compressed data will be determined in conjunction with the specific nature of the transmission medium 12 to go with the nature of the requirements of a user at a utilization location 11. Transmission medium 12 can transport the information in a variety of forms ranging from uncompressed, real time video to compressed, real time data to packet or switched data to bidirectional controlled flow of data. As stated in respect of compression techniques, the choice of the nature of transmission of the information on transmission medium 12 is also dependent on the nature of the transmission medium 12 (particularly, but not exclusively, its bandwidth and whether it is bidirectional or not) and also upon the expectations and requirements of a user at a utilization location 11.

Accordingly the system provides a degree of flexibility whereby different combinations of compression procedure and transmission medium can be selected to satisfy different performance/control requirements and timing characteristics for different applications. In the specific application described with reference to Fig. 1 it is a specific requirement that video information be transported over transmission medium 12 in less time than is required to display or replay that information at normal video rates at the utilization location 11.

Selectivity in relation to decompression is also possible at utilization location 11. For example decompression device 18 may only partially decompress data arriving over transmission medium 12 whereby local store 19

can contain fully decompressed, partly decompressed and uncompressed data.

Furthermore, an iterative decompression procedure may be undertaken whereby compressed data or partly decompressed data is removed from local store 19 for subsequent decompression by decompression device 18. This procedure can occur in either real time or slower than real time.

Particularly where iterative decompression is to be utilized local store 19 is adapted to store more than one data entity whereby, whilst one data entity is being processed by replay controller 21 another data entity can be undergoing interative decompression. Furthermore video replay controller 21 can undertake limited final decompression of data in real time during replay.

Replay controller 21 may incorporate other means of capturing, copying or storing video information (eg. video tape, video disc or CD). Link 24 can be a straight RF aerial connection to a standard TV set. In the alternative other connection technologies can be used, particularly where visual display is to be performed by other than TV 23. For example, a display can be output via computer terminal screen, display panel, projection device, video phone, multimedia terminal, teleconferencing station, HDTV device, cellular mobile video telephone and the like. A mobile phone implementation is discussed specifically later in this specification.

Replay controller 21 can incorporate facilities for

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user control of the replay process either through local controls or via commands issued through system control 22. Typical controls are in the same manner as for a typical VCR and include fast forward play, fast forward advance, 5 fast reverse play, fast reverse advance, selected frame or playing time positioning, forward or reverse skip, freeze frame, split screen multiple video display, reduced simultaneous multiple frame display, insertion/superposition of multiple video displays or TV 10 broadcasts.

The facilities provided by card reader 20 can be implemented by other means. For example billing information can be input from in-built identification information at the utilization location or can be keyed in 15 by a user on a keypad associated with system control 22. In some applications billing can be omitted - for example where the entire system is owned and operated by the one entity. Where billing and like system usage accounting is required then, at least in some implementations, 20 management/logging information and access and authorisation information will need to be passed in either direction along communication medium 12 whereby system control 16 and system control 22 can orchestrate the availability of system facilities and the accounting for them, if necessary 25 in conjunction with further communication with external networks or databases.

System controls 16, 22 include a user interface 25, 26 respectively. Where the system control 16 or 22 forms part

of a computer system then the computer screen and keyboard of such system can provide the user interface 25, 26.

Alternatively other forms of interface such as keypad, touchpad/screen, mouse and LED or LCD display can be
5 utilized.

In order to ensure flexibility in utilization of the system, the system can be capable of handling video data in more than one standard format and also be capable of conversion between the formats eg. between PAL, NTSC, video
10 phone, teleconferencing, multimedia and HDTV format.

To facilitate this the system can define its own internal video data format for internal transmission between components of the system. In this event incoming data in any one of the above specified formats will be
15 converted at the time of first entry into the system into the standard internal format. This conversion can be undertaken within system control 16 implemented in either hardware or software. Alternatively, the conversion process can be attached to storage bank 13 and
20 transmitter/receiver 15.

Although it is envisaged that the data processed and transmitted according to various embodiments of the invention will be data intended for video display, it is to be expected that data destined for other purposes or other
25 forms of output can also be delivered by the system. Typically, however, such other data (for example control data or audio data) will form only a relatively small proportion of the total data to be transmitted per unit

time.

Further implementations and examples of the invention will now be described. In the examples to follow the communication medium 12 is implemented, at least in part, by a cellular mobile telephone transmission system. Also in these further examples TV 23 is replaced by video phone-type devices, whether hand held or otherwise. In many of the video phone implementations the video phone can be thought of as a superposition of storage location devices and utilization location devices as referenced with respect to Fig. 1. In these implementations less emphasis is placed on storage and replay capability with the majority of video data being generated in real time at one video phone location for transmission and immediate receipt (and "playback") at another video phone subscriber location.

Fig. 2 illustrates a system suitable for the delivery of pay television signals which utilises as part of the transmission path both satellites and a cellular telephone network. The satellite allows for broad coverage of a wide geographical area (for example one country) whilst the cellular telephone network provides localised information delivery combined with control of that information delivery.

In Fig. 2, a wide band width information delivery system 210 is arranged to deliver pay television services to a local subscriber's television set 211.

In this particular arrangement a satellite 212 arranged to cover a broad geographical foot print (such as Australia

as shown in the top inset) is fed digital compressed signals by a means not shown. The satellite retransmits the digital compressed signal to a ground based satellite dish 213. Ideally there is one satellite dish 213 for each STD telephone area, or like grouping of user devices.

The satellite dish 213 passes the digital compressed signal to a control and editing room 214 (where the digital compressed signal can be modified as appropriate for the purposes of delivering pay television services). The edited signal then passes from the control room 14 to the public switched telephone network 215 where it is routed to the digital cellular mobile telephone network 216 for reception by designated cellular receivers 217. The digital cellular mobile telephone network can be, for example, of type GSM or CDMA or TDMA. The information broadcast over this network can be in either compressed or decompressed format and over one channel or multiple channels up to 16 channels.

The cellular receiver 217 is adapted to receive the pay television signal transmitted over the digital cellular telephone network 216 and to decode, expand and enhance the information as appropriate.

The resultant data is then converted to RF for direct reception at the antenna input of television set 211.

The cellular receiver 217 includes controls whereby the viewer is able to select a television channel for viewing on television set 211 and be billed for the video information received. In one particular form debiting of a

smart card or debit card for the information received can be performed by the cellular receiver 217.

The cellular receiver 217 can be identified by way of its electronic serial numbers in a manner currently used by the standard cellular network for identification. By this arrangement both billing and identification information can be recorded within the cellular receiver 217 and, as appropriate, can be transmitted back to control room 214.

Fig. 3 illustrates a typical arrangement of a mobile cellular system (analogue or digital) comprising of a relatively large number of cells within which mobile telephone stations can communicate with each other. The cells are transmitting and receiving sites distributed in a network of locations separated typically by distances of between five kilometres and some hundreds of metres depending on the density of the expected telephone traffic.

It will be seen that a typical telephone connection between a first mobile station 311 and a second mobile station 312 is established via local transmitter/receiver base stations 313, 314 which are in direct communication respectively with first and second mobile stations 311, 312. In turn these base stations 313, 314 are in communication with main stations such as main stations 315, 316 either by landline or by radio/microwave link. These main stations 315, 316 can communicate, in turn, with the (generally land based) public switched network (not shown).

Fig. 4 illustrates the communication path between first mobile station 311 and second mobile station 312. The link

or individual channel 317 can be conceptualised as a data path established between the mobile stations 311, 312 of a predetermined bandwidth B.

5 A small portion of the bandwidth B is reserved as a control layer 318 however the majority of the bandwidth is reserved for user to user communications and is termed the signal layer 319.

10 Data compression techniques selected and modified from those described previously can be used to optimise/maximise the use of that available bandwidth B.

One particular method of increasing available bandwidth between two mobile stations on a cellular telephone network is illustrated in Fig. 5.

15 In this arrangement two video telephones 320, 321 are linked for wide-bandwidth data communication by means of four individual channels 317A, 317B, 317C, 317D simultaneously.

20 With this arrangement the effective bandwidth available for data transmission between the two video telephones 320, 321 is approximately 4 times B.

25 The simultaneous establishment of, in this case, 4 individual channels 317, interlinked so as to act as a single data path, can be orchestrated through signal layers 319 of the respective individual channels 317A, 317B, 317C, 317D.

With reference to Fig. 6 a mobile telephone communication device 410 comprises a high radiated power cellular phone module 411 physically separated and distinct

from a low radiated power handpiece module 412.

Phone module 411 incorporates the standard electronics of a mobile telephone including the receiver/transmitter portions adapted for communication with base station 413 by way of a high power signal 414.

Handpiece module 412 also includes a second low power receiver/transmitter adapted for communication with handpiece module 412 via low power signal 415.

Handpiece module 412 includes a corresponding low powered transmitter/receiver adapted for low range cordless communication.

Preferrably, the cordless communication between the handpiece module 412 and the phone module 411 can be selected from one of 40 channels in either the 800-900 MHz range or 30-46 MHz range.

The handpiece module includes a standard mobile telephone keypad 416 and digital display 417. The signal radiated by the handpiece module 412 will be in the range of 1mW - 4 milliwatts.

In use, as shown in Fig. 7, a user 418 can attach the phone module 411 to a belt or the like whereby the relatively high power transmissions from the phone module 411 to base station 413 are kept away from the head portion 419 of user 418.

Handpiece module 412 being in low power communication with phone module 411 can be used adjacent or against the head portion 419 of user 418 with reduced risk of harmful electromagnetic radiation exposure.

The mobile telephone 410 can operate as a cellular telephone of the analogue type, GSM type, CDMA type, TDMA type or digital type.

5 The modular arrangement of the mobile telephone 410 allows the incorporation of additional features such as a smart card, pager, diary and calculator into one or other of the phone module 411 or handpiece module 412..

INDUSTRIAL APPLICABILITY

10 The invention is applicable for communication of information, including particularly video information, over commercially available communication channels whereby relatively wide bandwidth information is available in convenient form to the consumer.

CLAIMS

1. An information delivery system for transmission of information from a first location to a second location, said system including first information processing means at said first location, second information processing means at said second location, and a communication channel adapted to transmit said information between said first location and said second location.
2. The system of claim 1 wherein said information is stored in either digital form or analog form at said first location.
3. The system of claim 1 wherein said information is transmitted over said communications channel in digital form.
4. The system of claim 1 wherein said information is transmitted over said communications channel in analog form.
5. The system of claim 1 wherein said first location comprises a storage location and includes a storage bank in which said information is stored.
6. The system of claim 1 wherein said second location comprises a utilization location and includes information, output, display, presentation or playback means.
7. The system of claim 1 wherein said second location includes storage means.
8. The system of claim 1 wherein said communication channel is implemented as a wide bandwidth data path by the establishment of a plurality of individual channels of

predetermined bandwidth acting together to connect said first location to said second location whereby a bandwidth greater than the bandwidth of any one of said individual channels is available for transmission of said information.

9. The system of claim 1 wherein said communication channel comprises an apparent wide band channel by compression of said information prior to transmission over said channel whereby said information is transmitted in compressed form in less than real time.

10. The system of claim 1 wherein said information is transmitted over said communications channel in real time.

11. The system of claim 1 wherein said first information processing means includes information storage means and information compression means.

12. The system of claim 11 wherein data is passed from said information storage means to said information compression means for compression of said data prior to return to said storage means.

13. The system of claim 12 wherein said information is iteratively compressed by repeated, adaptive and selective invocation of said compression means.

14. The system of claim 1 wherein said second information processing means includes information decompression means and data storage means.

15. The system of claim 14 wherein said decompression means decompresses information prior to storage of said information in said storage means.

16. The system of claim 15 wherein information is

iteratively decompressed possibly requiring repeated passage between said decompression means and said storage means.

17. The system of claim 1 wherein said information is transmitted over said communication channel in real time.

18. The system of claim 1 wherein said communication channel includes at least part of a cellular telephone network.

19. The system of claim 1 wherein said second information processing means includes video display means whereby information comprising video data transmitted over said communication channel can be displayed at said second location.

20. The system of claim 19 wherein said video display means comprises a television receiver.

21. The system of claim 19 wherein said video display means comprises a video phone terminal.

22. The system of claim 19 wherein said video display means comprises a hand-held mobile phone incorporating a video data display.

23. The system of claim 22 wherein said mobile phone is comprised of a relatively high electromagnetic radiation emitting portion and a relatively low electromagnetic radiation emitting portion, said low radiation emitting portion adapted for placement at or near the head of a user and in communication with said high electromagnetic radiation emitting portion; said high electromagnetic radiation emitting portion adapted for location around the

waist of a user and further adapted for communication with a cellular telephone network.

24. A system for transmission of information from a storage location to a utilisation location; said system including a storage bank at said storage location wherein said information is stored; said system further including information playback means at said utilisation location; said system also including transmission means whereby said video information is transmitted from said storage location to said utilisation location on demand.

25. A system according to claim 24 wherein the transmission means communicates said information over a communications medium comprising either the public switched telephone network or unused or spare television channel band width.

26. A system according to claim 24 wherein the utilisation location includes storage means for temporary storage of said information during playback of said information by a replay controller which provides an RF modulated signal to the antenna input of a T.V. set.

27. A system according to claim 24 wherein the information is compressed by compression means prior to transmission from the storage location and decompressed by decompression means upon reception at said utilisation location.

28. An information delivery system comprising wide area signal delivery means delivering a signal containing information to a plurality of local receiver means distributed throughout a wide area; each said local receiver means communicating said signal to respective

local signal processing means whereby said signal is processed for transmission to a local cellular telephone network for reception by cellular receivers.

29. An information delivery system according to claim 28 wherein each of said cellular receivers are uniquely identifiable by said local signal processing means.

30. An information delivery system according to claim 28 wherein each of the cellular receivers is in communication with a television receiver and said information comprises video and audio information adapted to be output to said television receiver.

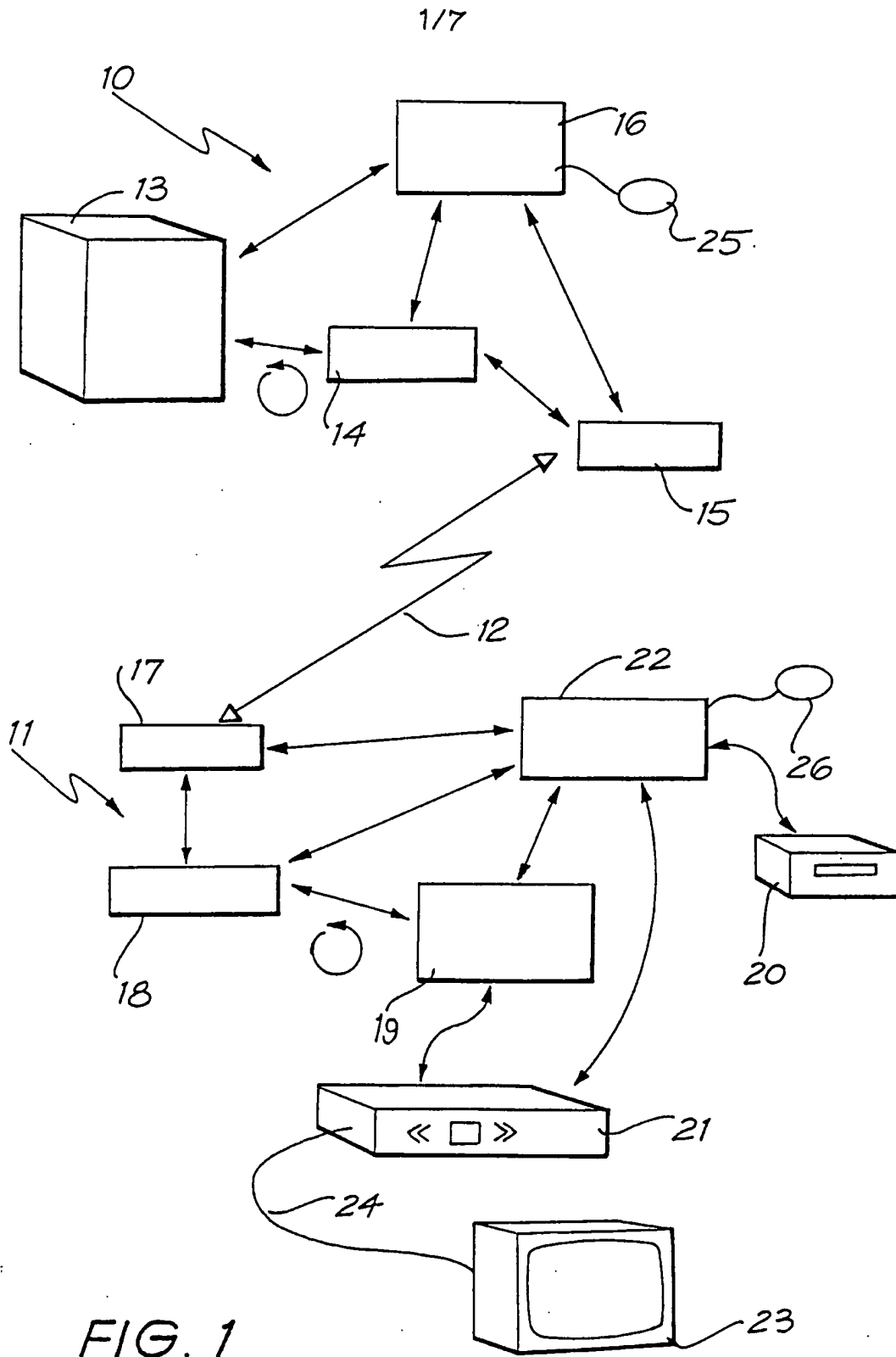
31. An information delivery system according to claim 30 wherein each cellular receiver is adapted to selectively control said information output therefrom.

32. An information delivery system according to claim 31 wherein the information comprises pay television information which can be selectively obtained by a user manipulating controls on each said cellular receiver.

33. An information delivery system according to claim 32 wherein each cellular receiver includes control means whereby said information output therefrom is monitored and an account of the value attributed to said information is maintained.

34. A wide-bandwidth data path on a cellular telephone network comprising the establishment of a plurality of individual channels of predetermined bandwidth acting together to connect subscribers together whereby a wide-

bandwidth data connection is established between subscribers having a bandwidth greater than the bandwidth of any one of said individual channels.



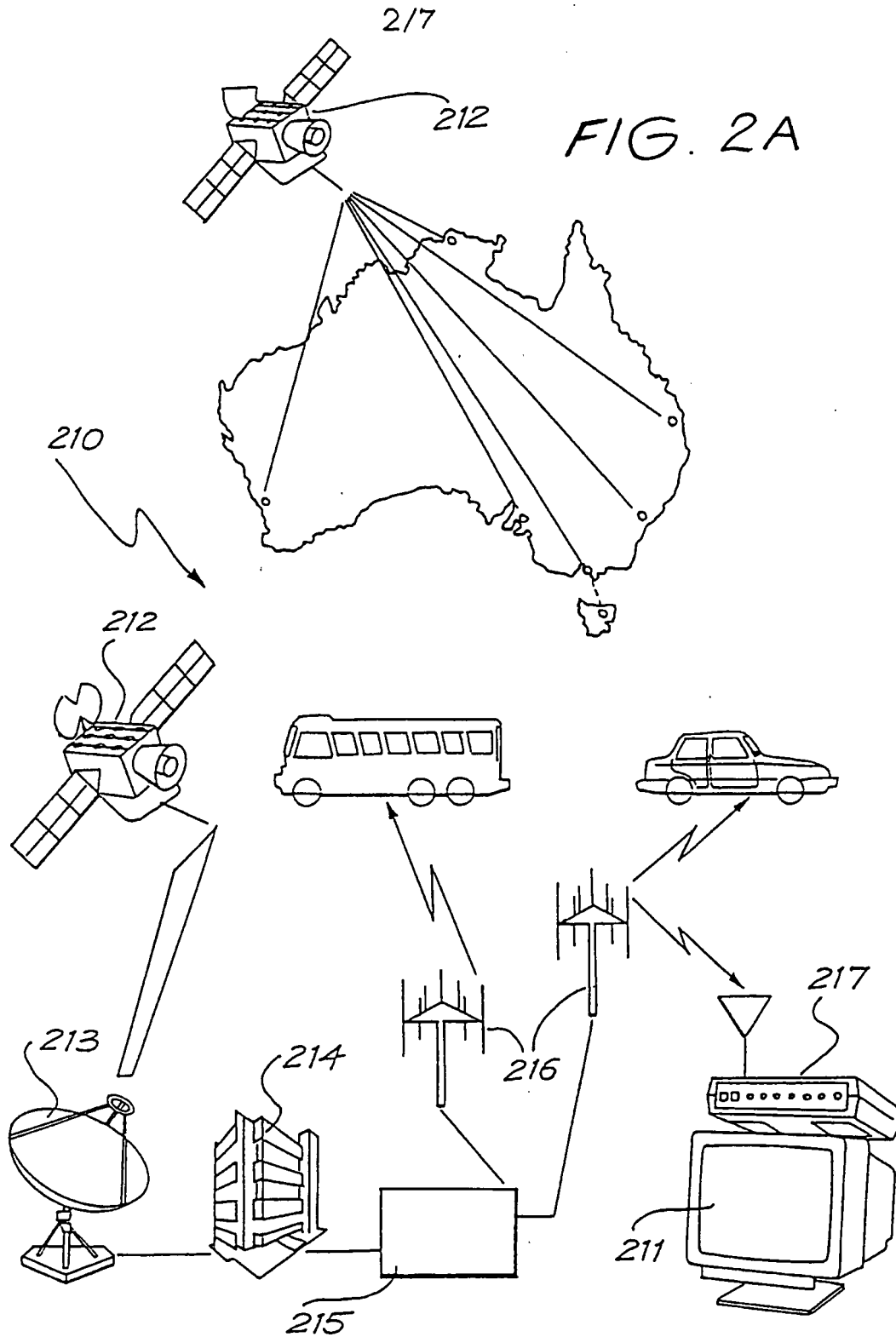


FIG. 2A

FIG. 2

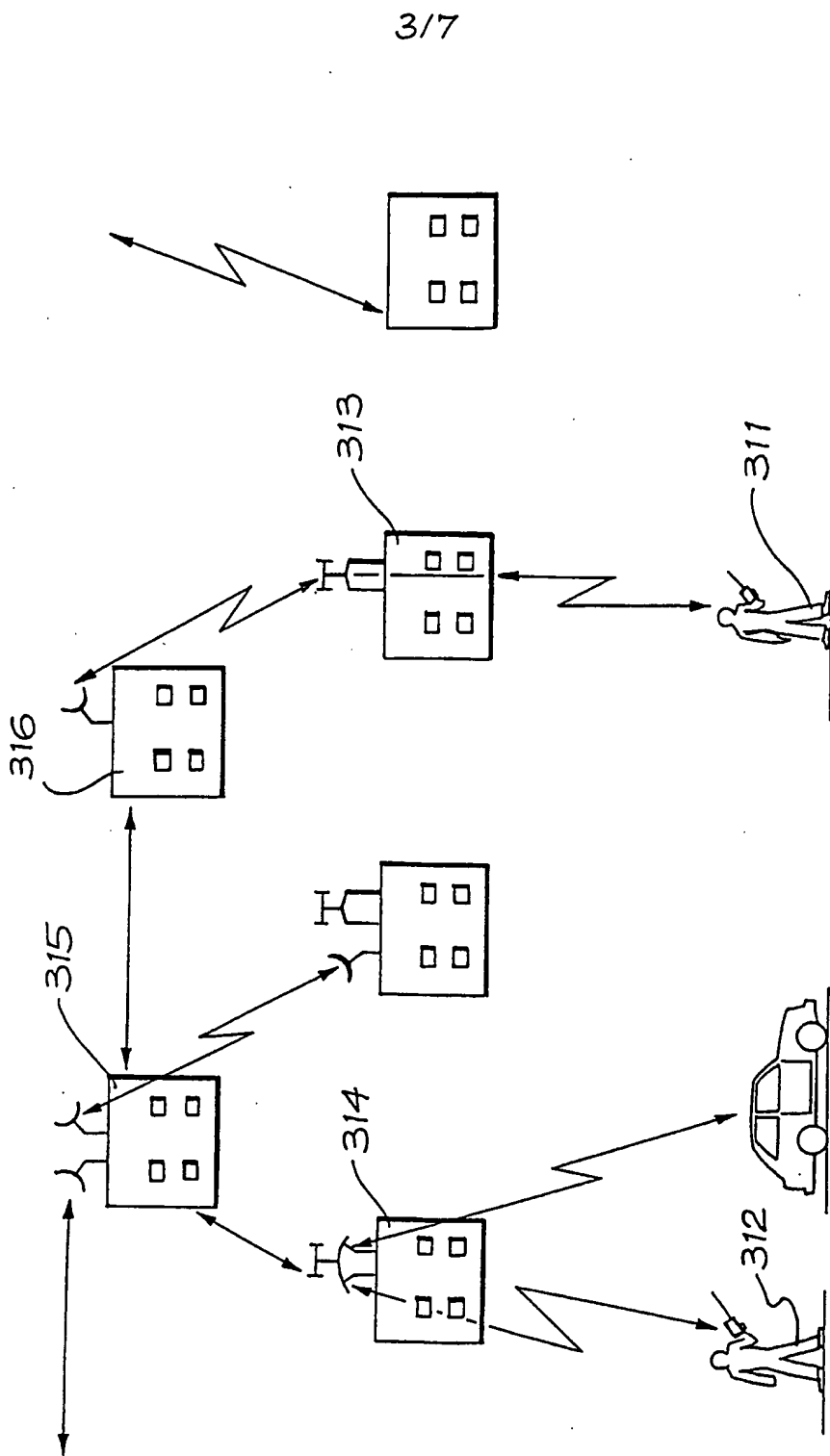


FIG. 3

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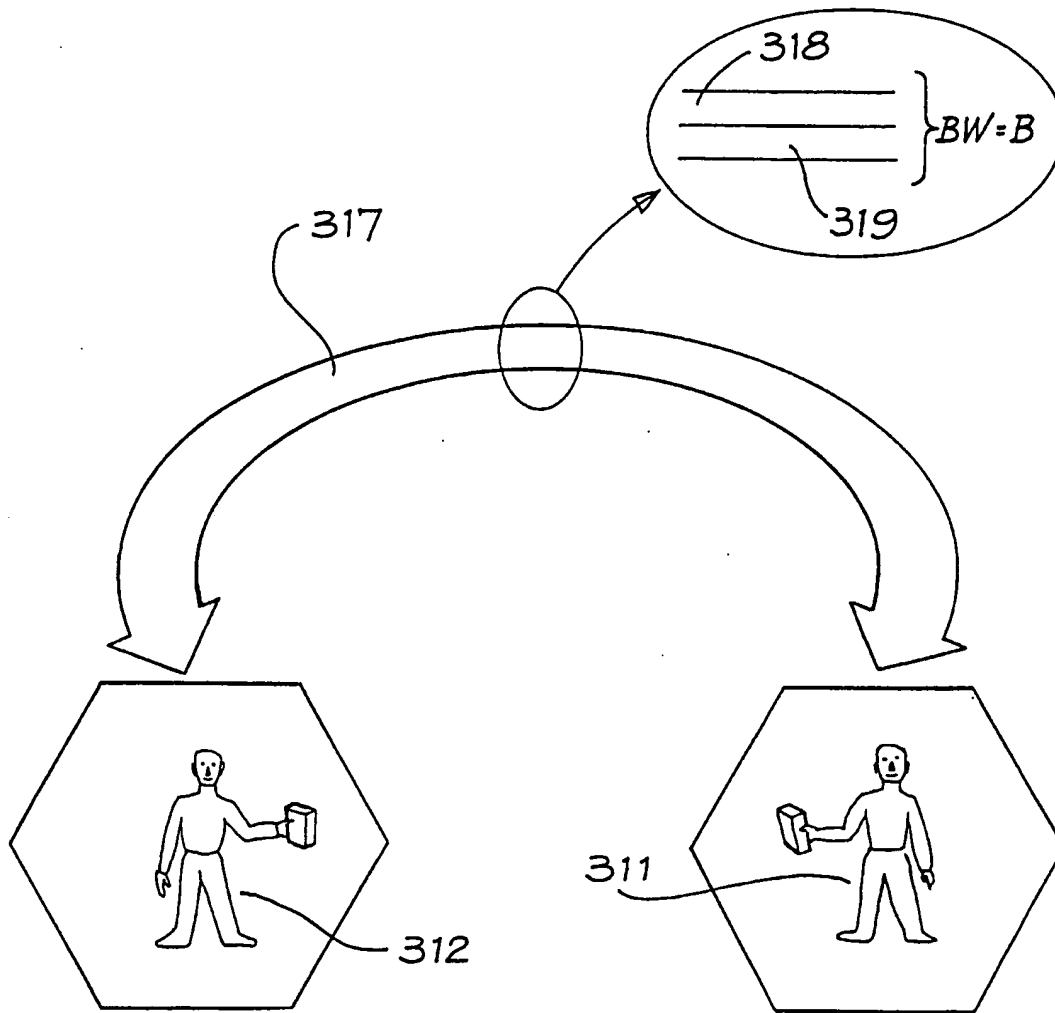


FIG. 4

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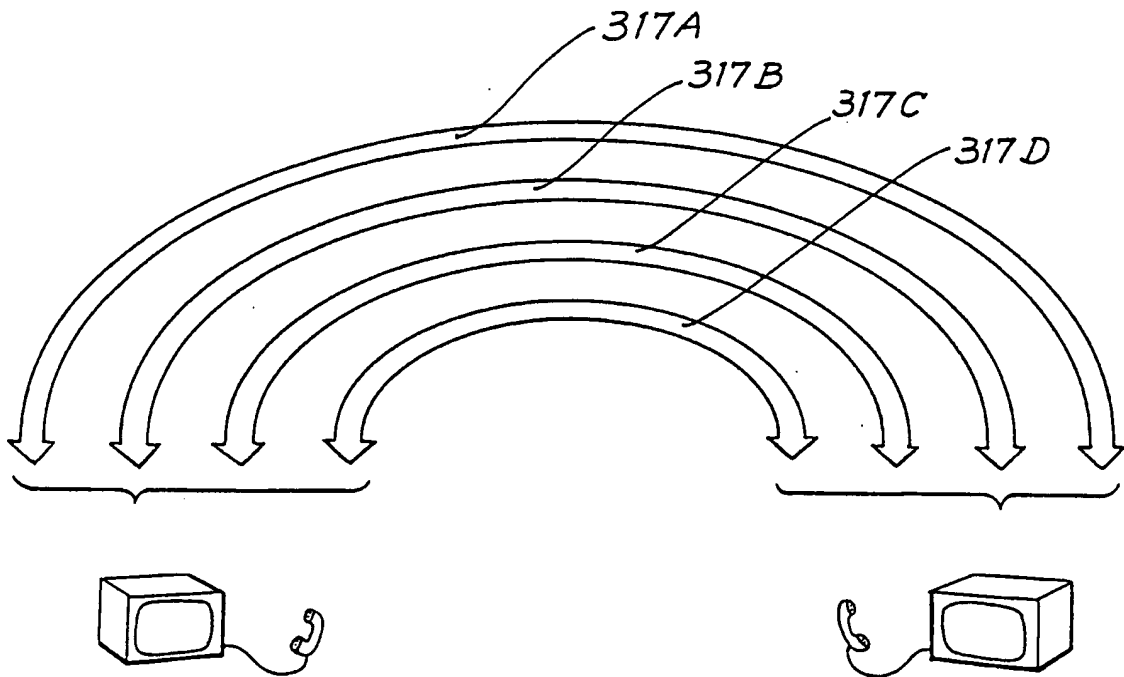


FIG. 5

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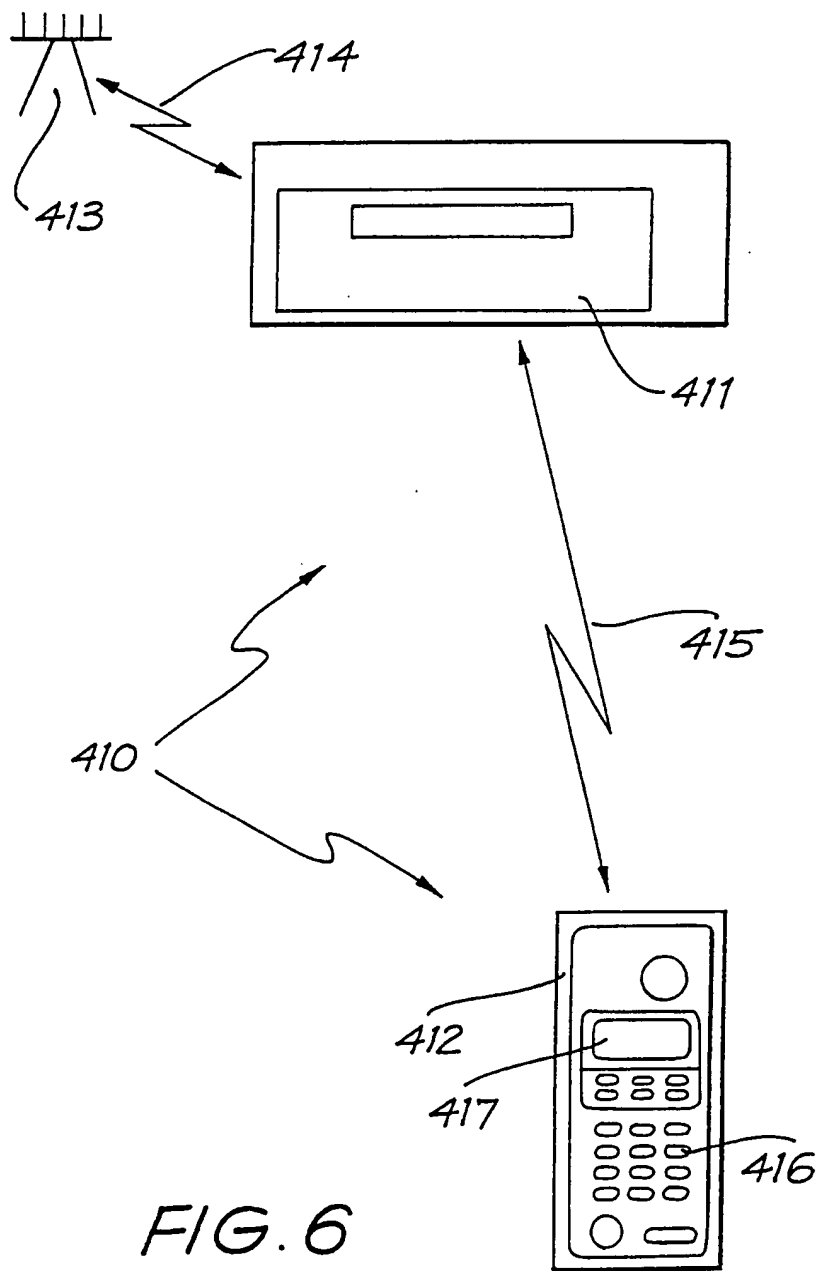


FIG. 6

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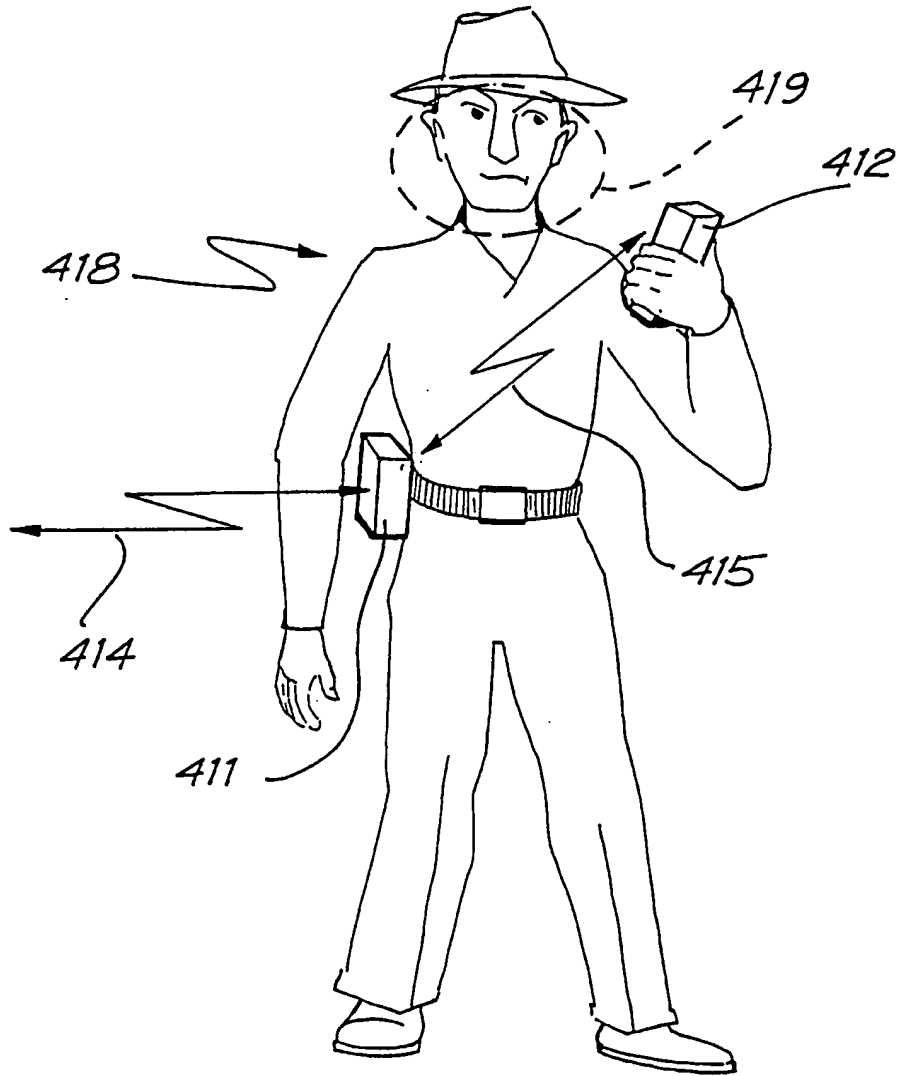


FIG. 7

A. CLASSIFICATION OF SUBJECT MATTER Int. Cl. ⁵ H04M 11/08, H04N 7/173, H04Q 7/04 According to International Patent Classification (IPC) or to both national classification and IPC																						
B. FIELDS SEARCHED Minimum documentation searched (classification system followed by classification symbols) IPC H04M 11/08, H04N 7/173, 7/16, H04H 1/08, H04Q 7/04 Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched AU : IPC as above Electronic data base consulted during the international search (name of data base, and where practicable, search terms used)																						
C. DOCUMENTS CONSIDERED TO BE RELEVANT																						
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to Claim No.																				
X Y	WO,A, 92/12599 (YURT) 23 July 1992 (23.07.92) Abstract, page 7 lines 17-27, Figs. 1(a), 1(b), 1(g) and 2(b) Fig. 1(a)	1-7,9-20,24-29 8																				
X Y	WO,A, 89/12370 (MONSLOW) 14 December 1989 (14.12.89) Fig. 1, page 7 line 6 - page 10 line 24 page 4 lines 20-25	1-7,10,17,19-20,24-26 28-33																				
X	WO,A, 92/21211 (VIDEO TELECOM CORPORATION) 26 November 1992 (26.11.92) page 2 lines 4-13, pages 8-9, Fig. 1	1-7,10,17,19-20,24-26																				
<input checked="" type="checkbox"/> Further documents are listed in the continuation of Box C.																						
<input checked="" type="checkbox"/> See patent family annex.																						
* Special categories of cited documents : <table border="0"> <tr> <td>"A"</td> <td>document defining the general state of the art which is not considered to be of particular relevance</td> <td>"T"</td> <td>later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention</td> </tr> <tr> <td>"E"</td> <td>earlier document but published on or after the international filing date</td> <td>"X"</td> <td>document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone</td> </tr> <tr> <td>"L"</td> <td>document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)</td> <td>"Y"</td> <td>document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art</td> </tr> <tr> <td>"O"</td> <td>document referring to an oral disclosure, use, exhibition or other means</td> <td>"&"</td> <td>document member of the same patent family</td> </tr> <tr> <td>"P"</td> <td>document published prior to the international filing date but later than the priority date claimed</td> <td></td> <td></td> </tr> </table>			"A"	document defining the general state of the art which is not considered to be of particular relevance	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention	"E"	earlier document but published on or after the international filing date	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone	"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art	"O"	document referring to an oral disclosure, use, exhibition or other means	"&"	document member of the same patent family	"P"	document published prior to the international filing date but later than the priority date claimed		
"A"	document defining the general state of the art which is not considered to be of particular relevance	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention																			
"E"	earlier document but published on or after the international filing date	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone																			
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art																			
"O"	document referring to an oral disclosure, use, exhibition or other means	"&"	document member of the same patent family																			
"P"	document published prior to the international filing date but later than the priority date claimed																					
Date of the actual completion of the international search		Date of mailing of the international search report 29 March 1994 (29.03.94)																				
Name and mailing address of the ISA/AU AUSTRALIAN INDUSTRIAL PROPERTY ORGANISATION PO BOX 200 WODEN ACT 2606 AUSTRALIA Facsimile No. 06 2853929		Authorized officer R. CHIA Telephone No. (06) 2832185																				

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate of the relevant passages	Relevant to Claim No.
X Y	AU,B, 56937/90 (634242) (TV ANSWER INTERNATIONAL, INC) 20 December 1990 (20.12.90) Figs. 1-4, pages 4-6 Figs. 3-4	1-7,10,17,19-20,24-30 8
X	US,A, 5130792 (TINDELL et al) 14 July 1992 (14.07.92) Column 2 lines 3-15, Figs. 1-3	1-7,9-20,24-27
X	EP,A, 104456 (SIEMENS AG) 4 April 1984 (04.04.84) Fig. 2, Abstract	1-7,10,17,19-22,24-26
X Y	AU,A, 34835/84 (SONY CORPORATION) 16 May 1985 (16.05.85) Fig. 4, page 15 lines 1-10 Fig. 4	1-7,10,17,19-20,24-26 28-33
P,X P,Y	US,A, 5260989 (JENNESS et al) 9 November 1993 (09.11.93) Column 2 lines 51-68 Fig. 1	1-7,10,17,19-20 8,34
Y	US,A, 4704716 (BOWERS et al) 3 November 1987 (03.11.87) Column 2 lines 4-34	8,34
A	EP,A, 425145 (AMERICAN TELEPHONE AND TELEGRAPH COMPANY) 2 May 1991 (02.05.91) page 3 lines 1-35	34

Box I Observations where certain claims were found unsearchable (Continuation of Item 1 of first sheet)

This international search report has not established in respect of certain claims under Article 17(2)(a) for the following reasons:

- 1. Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

- 2. Claim Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

- 3. Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box II Observations where unity of invention is lacking (Continuation of item 2 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

- 1. Claims 1-33
Information delivery system/method,
- 2. Claim 34
Wide bandwidth data path on a cellular telephone network,
as reasonewd on the extra sheet.

- 1. As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims
- 2. As all searchable claims could be searched without effort justifying an additional fee, this Authority did not invite payment of any additional fee.
- 3. As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

- 4. No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

- The additional search fees were accompanied by the applicant's protest.
- No protest accompanied the payment of additional search fees.

(continuation)

Box II (continued)

The international application does not comply with the requirements of unity of invention because it does not relate to one invention or to a group of inventions so linked as to form a single general inventive concept. In coming to this conclusion the International Searching Authority has found that there are two inventions:

- 1 Claims 1-33 are directed to an information delivery system. It is considered that the transmission of information from a first information processing means at a first location to a second information processing means at a second location through a communication medium comprises a first "special technical feature".
- 2 Claim 34 is directed to a wide-bandwidth data path on a cellular telephone network. It is considered that the use of a bandwidth greater than the bandwidth of individual channels to establish communication between a plurality of subscribers comprises a second separate "special technical feature".

Since the abovementioned groups of claims do not share either of the technical features identified, a "technical relationship" between the inventions, as defined in PCT rule 13.2 does not exist. Accordingly the international application does not relate to one invention or to a single inventive concept.

This Annex lists the known "A" publication level patent family members relating to the patent documents cited in the above-mentioned international search report. The Australian Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

Patent Document Cited in Search Report		Patent Family Member					
WO	9212599	AU	11970/92	EP	566662	MX	9200041
WO	8912370	AU	38481/89	AU	636848	EP	422074
		US	4890320	US	4995078		
AU	56937/90	CN	1048136	CS	9002906	EP	402809
		IL	94519	JP	3064286	NO	902571
		NZ	233837	PT	94361	US	5101267
		US	5223923	US	5257099	DD	297041
		ZA	9004436				
US	5260989	BR	9301307	EP	571104	EP	571125
		JP	6037858	EP	571124	JP	6037695
		EP	565229				
US	5130792						
EP	104456	DE	3232198	ZA	8306380		
WO	9221211	AU	20101/92				
AU	34835/84	CA	1223335	EP	144770	JP	60102080
		US	4805014				
US	4704716	CA	1260588	CN	86108890	EP	229365
		JP	62189895	US	4885738		
EP	425145	JP	3265257	US	5042062		
END OF ANNEX							



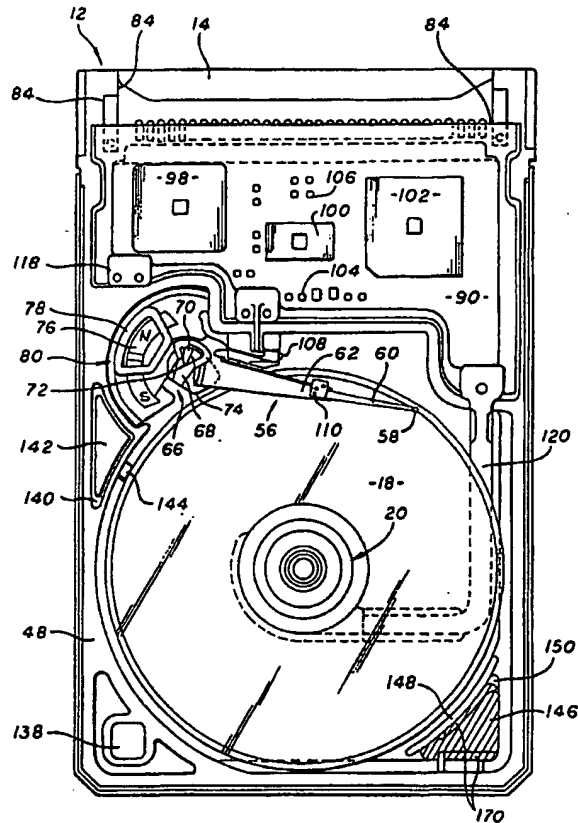
INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

<p>(51) International Patent Classification ⁵ : G11B 5/012</p>	<p>A1</p>	<p>(11) International Publication Number: WO 94/29852 (43) International Publication Date: 22 December 1994 (22.12.94)</p>
<p>(21) International Application Number: PCT/US94/04981 (22) International Filing Date: 28 April 1994 (28.04.94) (30) Priority Data: 08/075,697 11 June 1993 (11.06.93) US (71) Applicant: MAXTOR CORPORATION [US/US]; 211 River Oaks Parkway, San Jose, CA 95134 (US). (72) Inventors: CUCCIO, Allen; 5291 Idylwild Trail, Boulder, CO 80503 (US). BRUNER, Curt; P.O. Box 1022, Longmont, CO 80502 (US). BEECROFT, Harold; 18375 Chisman Lane, Colorado Springs, CO 80928 (US). HUTSELL, Larry; 2326 Judson Street, Longmont, CO 80503 (US). REH, Jeff; 6450 Eagle Court, Longmont, CO 80503 (US). METZ, Robert; 9052 Perry Street, Westminster, CO 80030 (US). (74) Agents: BEREZNAK, Bradley, J. et al.; Blakely, Sokoloff, Taylor & Zafman, 7th floor, 12400 Wilshire Boulevard, Los Angeles, CA 90025 (US).</p>	<p>(81) Designated States: AT, AU, BB, BG, BR, BY, CA, CH, CN, CZ, DE, DK, ES, FI, GB, GE, HU, JP, KG, KP, KR, KZ, LK, LU, LV, MD, MG, MN, MW, NL, NO, NZ, PL, PT, RO, RU, SD, SE, SI, SK, TJ, TT, UA, UZ, VN, European patent (AT, BE, CH, DE, DK, ES, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, ML, MR, NE, SN, TD, TG).</p> <p>Published <i>With international search report.</i></p>	

(54) Title: **TYPE II PCMCIA HARD DISK DRIVE CARD**

(57) Abstract

A hard disk drive which meets the type II PCMCIA specifications is provided. The disk drive has an outer housing (12) and a connector (14) which allow the drive to be plugged into a host computer. All of the electrical components of the drive are mounted to a single printed circuit board (90). The circuit board is approximately one-third the length of the housing and is located between the disk (18) and the connector. The reduction in the board length allows the circuit board to be placed in the same plane as the disk and therefore does not add to the thickness of the overall assembly.



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TYPE II PCMCIA HARD DISK DRIVE CARD

BACKGROUND OF THE INVENTION

1. FIELD OF THE INVENTION

The present invention relates to a hard disk drive assembly which complies with the PCMCIA type II specifications.

2. DESCRIPTION OF RELATED ART

Most computer systems contain a massive memory storage device such as a hard disk drive. Hard disk drive units include a magnetic disk that is capable of storing a large amount of binary information. The magnetic disk is typically coupled to a hub that is rotated by an electric motor, commonly referred to as a spin motor. The drive unit also has a head that magnetizes and senses the magnetic field of the disk. The head is typically located at the end of a cantilevered actuator arm which can pivot about a bearing assembly mounted to the base plate of the disk drive. The actuator arm has a coil which cooperates with a magnet mounted to the base plate. Providing a current to the coil creates a torque on the arm and moves the head relative to the disk. The coil and magnet are commonly referred to as a voice coil motor or VCM. The actuator arm, motors and other components of a typical disk drive unit are relatively small and fragile, and are therefore susceptible to damage when subjected to excessive external shock loads or vibration. For this

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reason, hard disk drives are usually rigidly mounted to the housing of the computer system by screws or other fastening means.

Hard disk drives contain programs and other information that are vital to the user. It is sometimes desirable to transfer such information to a different computer system. Transferring programs from a hard disk typically requires loading the information onto a floppy disk, or sending such information over a phone line. Such methods can be time consuming, particularly if the program is long, or there is a large amount of data. There have been developed portable hard disk drives which can be plugged into a slot in the computer. To reduce the amount of possible component damage to the drive unit, the housing and disk assembly are constructed to be quite rugged. These rugged assemblies are typically heavy and bulky, and generally impractical to carry and store.

The Personal Computer Memory Card International Association (PCMCIA) has recently promulgated specifications for portable memory cards which can be plugged into slots within a computer. The PCMCIA standard includes a type I format, a type II format and a type III format, each format being distinguished by a different card thickness. Memory can be added to a computer by merely plugging in an additional card. Similarly, a modem or facsimile (FAX) card can be added to a system with the push of the hand. The standardized format of the cards allow a user to plug the memory card of one computer into another computer, regardless of the type or make of either system.

The standardized PCMCIA cards are approximately the size of a credit card and include a connector which mates with a corresponding connector in the computer. The small size of the card provides an electronic assembly that is easy to carry and store. It is very desirable to

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have a hard disk drive unit which conforms with the PCMCIA format, so that the disk drive can be readily carried and plugged into an existing slot of a computer. Such a hard disk card must be rugged enough to withstand the large shock loads that may be applied to the drive unit, such as by dropping the card onto a hard surface. The existence of such a card would also allow the user to accumulate memory in the same manner that floppy disk are used today.

Hard disk drive units contain a number of integrated circuits that control the operation of the drive. The circuits typically include a read/write channel that is coupled to the transducers of the actuator arm assembly. The read/write channel is connected to a interface controller which is coupled to the host computer. The interface controller is coupled to a random access memory device that is used as a buffer to store data transferred between the disk and the host.

Disk drives also contain circuitry that provide current to the voice coil to maintain the head(s) on the center of a track (servo routine) and to move the head(s) from track to track (seek routine). Additionally, a disk drive typically contains circuitry to commutate the motor, and to insure that the motor and disk rotate at a uniform speed.

The operation of the above described circuits is typically controlled by a microprocessor based controller. Conventional disk drive also contain a separate circuit which interfaces the controller with the other circuits. This chip is commonly referred to as glue logic. U.S. Patent No. 4,979,056 issued to Squires et al., discloses a hard disk architecture which has a microprocessor based controller that controls the operation of the interface controller, read/write channel, actuator and spin motor circuitry. The Squires system utilizes an embedded servo format which

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stores the servo information in the same sector of a track as the data. During each sector the processor services the voice coil and spin motor circuitry of the drive. The processor employs a hierarchy that allows the spin motor and the voice coil to be serviced in conjunction with the transfer of data between the host computer and the disk. Although a Squires type system provides a controller based system to efficiently transfer data between the disk and the host, such systems typically require a large amount of electrical components that must be mounted onto a printed circuit board.

U.S. Patent No. 4,933,785 issued to Morehouse et al. and U.S. Patent No. 5,025,335 issued to Stefansky et al., disclose conventional hard disk drives which have a printed circuit board mounted to a disk drive housing commonly referred to as a HDA. The HDA is typically sealed and contains the disk, actuator arm and spin motor of the assembly. The HDA may also contain a pre-amplifier that is connected to the heads of the drive. The remaining electrical components (interface controller, read/write channel, actuator circuitry, etc.) are located on the external printed circuit board. The circuit board extends along the entire length and width of the HDA. Therefore the thickness of the overall assembly is determined by the thickness of the HDA, the thickness of the printed circuit board and the height of the electrical components.

Application Serial No. 07/975,008 filed on November 13, 1992 and assigned to the same assignee as the present application, discloses a hard disk drive which contains a 1.8 inch diameter disk and meets the type III requirements of the PCMCIA specifications. Like the Morehouse and Stefansky patents, the '008 application contains a printed circuit board

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that extends across the length and width of the HDA. It has been found that using such a board arrangement will not provide a disk drive that meets the type II PCMCIA specification. It is desirable to provide a hard disk drive assembly which meets the type II PCMCIA specifications.

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SUMMARY OF THE INVENTION

The present invention is a hard disk drive which meets the type II PCMCIA specifications. The disk drive contains a low profile spin motor that rotates a disk. The rotation of the spin motor is controlled by spin motor circuitry within a servo chip. The disk rotates relative to an actuator arm assembly which has transducers that store and retrieve information from the disk. The actuator arm is rotated by a voice coil that is controlled by actuator circuitry within the servo chip.

The disk drive has an outer housing and a connector which allows the drive to be plugged into a host computer. The transducers are coupled to a read/write chip which transfers information between the disk and the host computer through a data manager chip. The data manager, read/write and servo chips are all controlled by a controller chip. All of the electrical components of the drive are mounted to a single printed circuit board. The circuit board is approximately one-third the length of the housing and is located between the disk and the connector. The reduction in board length allows the circuit board to be placed in the same plane as the disk and therefore does not add to the thickness of the overall assembly. The compact assembly provides a hard disk drive which meets the type II PCMCIA thickness requirements.

It is therefore an object of the present invention to provide a hard disk drive that will meet the type II PCMCIA specifications.

It is also an object of the present invention to provide an architecture which will reduce the size of the printed circuit board of a hard disk drive assembly.

BRIEF DESCRIPTION OF THE DRAWINGS

The objects and advantages of the present invention will become more readily apparent to those ordinarily skilled in the art after reviewing the following detailed description and accompanying drawings, wherein:

Figure 1 is a perspective view of a hard disk drive of the present invention;

Figure 2 is a top cross-sectional view of the hard disk drive;

Figure 3 is a bottom view of the cover of the hard disk drive;

Figure 4 is a cross-sectional view of the actuator arm assembly;

Figure 5 is a cross-sectional view of the hard disk drive showing the printed circuit board and the connector of the drive;

Figure 6 is a cross-sectional view of the spin motor;

Figure 7 is a bottom view of the printed circuit board;

Figure 8 is a schematic of the system architecture of the disk drive;

Figure 9 is a schematic of the data manager chip of the system;

Figure 10 is a schematic of the servo chip of the system;

Figure 11 is a representation of a sector of the disk;

Figure 12 is a schematic of the controller chip of the system;

Figure 13 is a schematic of the R/W chip of the system;

Figures 14a-g are flowcharts of the operation of the disk drive.

DETAILED DESCRIPTION OF THE INVENTION

Referring to the drawings more particularly by reference numbers, Figure 1 shows a hard disk drive 10 of the present invention. The disk drive 10 is constructed as a card which can be plugged into a host computer (not shown). The unit 10 includes a housing 12 and a connector 14. In the preferred embodiment, the housing has the dimensions of 85.6 x 54.0 x 5.0 millimeters. The dimensions conform with the specifications issued by the Personal Computer Memory Card International Association (PCMCIA) for a type II electronic card. The PCMCIA is an association that has promulgated a specification which lists dimensions and other requirements for a standard electronic card. Each computer that conforms with the PCMCIA specification will contain slots that can receive a standardized card. With such a standard, electronic cards of one computer can be readily plugged into another computer, regardless of the model or make of the systems. A copy of the PCMCIA standard can be obtained by writing to the Personal Computer Memory Card International Association at 1030 G East Duane Avenue, Sunnyvale, California 94086.

The PCMCIA standard includes three types of cards which each have varying thicknesses. A type I card is approximately 3.3 millimeters thick, a type II card is approximately 5.0 millimeters thick and a type III card is approximately 10.5 millimeters thick. The computer has a plurality of adjacent slots that are wide enough to receive a type II card. Both the type I and II cards occupy a single slot, while the type III card occupies two slots. Each computer slot contains a 68 pin connector that is typically mounted to a motherboard to provide an interconnect to the

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computer system. The PCMCIA standards were originally established for memory and/or logic cards including internal modem and facsimile boards. The present invention provides a hard disk drive unit that can conform to the PCMCIA type II card format.

In the preferred embodiment, the connector 14 of the card assembly 10 has 68 pins which can mate with the 68 pin connector located in the computer. The connector 14 is typically constructed from a dielectric material that has a plurality of sockets 16 which mate with pins (not shown) located in the computer connector. The connector has certain pins designated for power, ground and data. As required by the PCMCIA specification, the sockets dedicated to ground are longer than the sockets dedicated to power, and the sockets dedicated to power are longer than the sockets dedicated to data. Such an arrangement allows the card to be plugged into an operating "live" system, without creating voltage spikes or power surges within the card.

Referring to Figures 2-7, the hard disk drive contains a disk 18 that is rotated by a spin motor 20. The disk 18 is typically constructed from a metal, glass, ceramic or composite substrate that is covered with a magnetic coating as is known in the art. As shown in Fig. 6, the spin motor 20 includes a hub 22 coupled to a spindle magnet 24 by a pair of conical bearings 26. Within the hub 22 is a stator 28 and a number of windings 30 which cooperate with magnets 32 attached to the inner surface of the hub 22. Providing a current to the windings 30 creates a magnetic flux which passes through the magnets 32 and induces a rotation of the hub 22 and the disk 18. The hub 22 has a pair of tapered inner surfaces 34 which slide along corresponding tapered surfaces 36 of the conical bearings 26. Between the tapered hub surfaces 36 and

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bearings 26 is a thin layer of fluid which allows relatively frictionless rotation between the two members 22 and 26. Between the conical bearings 26 is a space 38 which provides a reservoir for the bearing fluid. The bearing fluid is preferably a ferro-fluid lubricant which is maintained between the hub 22 and bearings 26 by the magnetic flux of the spindle magnet 24. The conical bearings 26 provide a low profile spin motor 20 which can withstand the type shock loads that could be applied to a hand held computer and/or disk drive.

The disk 18 is clamped against a hub shoulder 40 by a disk clamp 42. The disk clamp 42 is preferably constructed from a thermoplastic material that is ultrasonically melted onto the motor 20. The thermoplastic flows into a plurality of grooves 44 located in the hub 22. The plastic in the grooves 44 prevent movement of the disk 18 in the z axis. A portion of the clamp 42 also flows into a space between the inner diameter of the disk 18 and the hub 22 to prevent lateral movement of the disk 18.

The fixed spindle 24 is captured by a pair of caps 45 and 46. The bottom cap 45 is mounted to a base plate 48 by a layer of adhesive 50. In the preferred embodiment the adhesive is a material sold by Minnesota Manufacturing & Mining Co. ("3M") under the designation AF46. The film 50 is also used to mount the lower conical bearing 26 to the cap 45. The upper cap 46 is mounted to the fixed spindle 24. In the preferred embodiment, the cap 46 and cover 52 are coupled together by an adhesive viscoelastic film material 54 mounted on the cover 52. The viscoelastic material 54 compensates for tolerances between the height of the motor 20 and the space between the base plate 48 and cover 52.

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The viscoelastic 54 also dampens shock and vibrational loads applied to the motor 20.

As shown in Fig. 2, the disk 18 rotates relative to an actuator arm assembly 56 which has a pair of transducers 58 commonly referred to as heads. The transducers 58 contain a coil (not shown) which can magnetize and sense the magnetic field of each corresponding adjacent surface of the disk 18. Each head 58 is supported by a flexbeam 60 that is attached to an actuator arm 62. In the preferred embodiment, each flexbeam 60 is constructed from one or more conductive plates (not shown) that are separated by a relatively elastic dielectric material (not shown). The metal plates may provide a conductive path for the signals that are sent to the transducers 58. The heads 58 each contain a slider (not shown) which cooperate with the air stream produced by the rotation of the disk 18 to create an air bearing between the surface of the disk and the transducer. The air bearing lifts the head 58 off of the surface of the disk 18. The flexbeams are constructed to be flexible enough to allow the heads to be separated from the disk surface by the air bearings and take up the disk 18 and motor 20 axial runout. The heads 58 can be constructed to provide either horizontal or vertical recording.

The flexbeams 60 are inserted into slots of the actuator arms 62 by an adhesive. In the preferred embodiment, the adhesive can be cured by a primer, heat, or a UV light source. The actuator arms 62 are preferably constructed from a silicon carbide which is both light and strong. The actuator arms 62 pivot about a bearing assembly 66. As shown in Fig. 4, the bearing assembly 66 includes a bearing block 68 which extends from the base plate 48. Referring to Fig. 2, the actuator arms 62 have a triangular shaped roller bearing 70 which extends into a V shaped slot 72

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in the block 68. The roller bearing 70 is pressed into contact with the block 68 by a C shaped spring clip 74. The apex of the roller bearing 70 engages the apex of the slot 72 such that the bearing rolls relative to the block 68 when the actuator arms 62 are rotated about the bearing assembly 66. The roller bearing of the present invention provides a low profile bearing assembly that produces a relatively small amount of friction and which can withstand the typical shock loads applied to a hand held disk drive.

At the end of the actuator arms 62 is a magnet 76 located between a pair of stationary coils 78. The magnet has north (N) and south (S) poles, so that when a current is sent through the coils in one direction the north pole experiences a force perpendicular to the coils, and when current is provided in an opposite direction the south pole experiences a force in the same direction. The magnet and coils, commonly referred to as a voice coil motor or VCM 80, rotate the actuator arms 62 and move the heads 58 relative to the disk 18. As shown in Fig. 4, the coils 78 are mounted to a C shaped shield plate 82 that is constructed from a ferrite material which provides a return path for the magnetic flux, and maintains the flux in the area of the voice coil 80.

As shown in Figs. 2 and 5, the connector 14 is located at one end of the housing 12 and is captured by indent surfaces 84 in the base plate 48 and cover 52. The indent surfaces 84 prevent the connector 14 from moving in any direction relative to the housing 12. The connector sockets 16 each have tails 86 that are soldered to conductive surface pads 88 on a printed circuit board 90 (PCB). As shown in Fig. 4, the printed circuit board 90 is supported by the base plate 48 and contains

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all of the electrical components required to operate the disk drive assembly 10.

As shown in Fig. 7, mounted to the printed circuit board 90 is a controller chip 92, a read/write channel chip 94 and a servo chip 96. Each chip is housed within an integrated circuit package that is soldered to the board 90 by conventional techniques well known in the art. As shown in Fig. 2, the opposite side of the circuit board 90 contains a data manager chip 98, a pre-amplifier chip 100 and a read only memory (ROM) chip 102. The board 90 also contains passive elements such as resistors 104 and capacitors 106 to complete the electrical system of the drive assembly. The board 90 is located between the disk 18 and the connector 14. As shown in Fig. 5, the printed circuit board 90 is located in a plane essentially parallel with the disk 18. Locating the board 90 essentially "in-plane" with the disk 18 reduces the overall thickness of the disk drive assembly.

As shown in Fig. 2, the printed circuit board 90 is coupled to the actuator arm assembly 56 by a flexible circuit board 108. The flexible circuit board 108 is typically constructed from polyimide sheets commonly sold under the trademark KAPTON, which encapsulate conductive traces that extend throughout the circuit. One end of the flexible circuit 108 has contact pads 110 that are soldered or ultrasonically to the flexbeam 60. As shown in Fig. 5, the opposite end of the circuit 108 has contact pads that are pressed into operative contact with corresponding pads on the printed circuit board 90 by clamp down strips 116 located on the cover plate 52. The clamp down strips 116 are adapted to apply a pressure to the contact pads of the flexible circuit 108 when the cover plate 52 is attached to the base plate 48. The clamp

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down strips 116 provide a means of coupling/decoupling the flexible circuit 108 to the printed circuit board 90 without having to solder together the two members. As shown in Fig. 2, the disk drive assembly also contains flexible circuits 126 and 128 that couple the printed circuit board 90 to the coils 78 of the voice coil 80 and the windings 30 of the spin motor 20, respectively. The flexible circuits 126 and 128 have contact pads that are pressed into contact with corresponding pads on the circuit board 90 by clamp down strips 116.

As shown in Figs. 3 and 4, mounted to the cover 52 is an elastomeric seal 122 that is pushed against a corresponding surface 124 in the base plate 48. The elastomer 122 seals the disk 18, spin motor 20 and actuator arm assembly 56 in an area which is commonly referred to as the HDA 126. The cover plate 52 is attached to the base plate 48 by a clamp 128. The clamp 128 has a number of spring tabs 130 which extend into corresponding slots 132 in the plates 48 and 52. The clamp 128 may have an elastomeric strip 134 which absorbs external shock and vibrational loads that are applied to the edges of the disk drive assembly 10. The disk drive 10 is typically loaded into a host computer so that the edges of the card are supported by the computer housing. Any shock or vibrational loads applied to the computer are therefore typically transmitted to the disk drive through the edge of the drive. The elastomeric strip 134 dampens these loads to prevent damage or an interruption to the operation of the drive. The clamp provides a means for attaching the base plate 48 to the cover 52 without using screws or other equivalent fastening means. The elimination of threaded fasteners assist in the reduction of the overall height of the assembly. As shown in Figs. 2 and 3, the cover 52 has a rectangular pin 136 that is inserted into

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a corresponding groove 138 in the base plate 48 to align the two members 48 and 52.

The base plate 48 has a filter chamber 140 which contains a breather filter 142 located external to the HDA 126. The base plate 48 has a slot 142 which provides fluid communication between the HDA 126 and the chamber 140. When the pressure of the air within the HDA 126 is lower than the ambient air outside of the drive 10, the differential pressure will pump air past the clamp 128, through the interface of the cover 52 and base plate 48 and into the HDA area 126 and base 48. This HDA area 126 is in fluid communication with the filter chamber 140 which also is in fluid communication with the HDA. The pumped air flows into the HDA 126 through the filter chamber 140. Hydrocarbon, acid-gas and other impurities in the air are captured by the breather filter 142. The breather filter may also have a humidity control element.

The disk drive assembly 10 also has a recirculation filter 146 that removes impurities within the HDA. The recirculation filter 146 is located in the center of chamber separated from the HDA by a wall 146. The filter 146 separates an upstream chamber 150 from a downstream chamber 151. Rotation of the disk 18 induces a flow of air into the upper chamber 151, through the filter 146, into the lower chamber 146 and back into the HDA area 126 of the disk 18. The disk drive may also have an environmental control assembly 180 constructed from materials that absorb hydrocarbons, acid-gas and water.

Figure 8 shows a schematic of the system architecture of the hard disk drive assembly 10. The system controls the operation of the disk drive. Data is typically stored on a magnetic disk 12 along annular tracks concentric with the diameter of the disk. In the preferred embodiment,

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the disk is 1.8 inches in diameter. Although a 1.8 inch disk is described, it is to be understood that the present invention can be used with disks having other diameters such as 1.3", 2.5", 3.5", etc. For a 1.8" disk, the system will typically store data on 130 tracks per disk surface. Each track contains a plurality of servo sectors. Each sector is capable of storing up to 768 bytes of data. The total assembly is capable of storing up to 130 Mbytes of data.

As shown in Fig. 8, the system 10 includes the data manager chip 98, the controller chip 92, the servo chip 96 and the read/write ("R/W") chip 94. The system also has the read only memory ("ROM") device 102 coupled to the controller 92, and the pre-amplifier circuit ("pre-amp") 100 connected to the heads 58 and the R/W chip 94. The controller 92 is coupled to the servo 96 and R/W 94 chips through serial lines 204 and 206, respectively. The controller 92 is coupled to the data manager 98 by address/data bus 208 and to the ROM 202 by instruction bus 210. The data manager 98 is coupled to a host 212 by address/data bus 214 and to the R/W chip 94 by data bus 216. The R/W chip 94 is connected to the pre-amplifier chip by lines 218. The servo chip 96 is coupled to the R/W chip 94 through servo lines 220. The servo chip 96 is also connected to the voice coil 80 and spin motor 20 through lines 222 and 224, respectively. The pre-amp chip 100 is connected to the heads 58 through lines 226. The controller 92 is also coupled to the R/W chip 94 by raw data line 228. The serial lines and address/data busses contain control signal lines which are needed to transfer information between the respective chips. Although the term line is used through this specification, it is to be understood that the term line may include multiple lines.

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As shown in Figure 9, the data manager 98 is coupled to the host 212 by a host interface controller circuit 230. The interface controller 230 contains hardware to interface with the host 212 by providing return handshakes, etc. in accordance with the host protocol. In the preferred embodiment, the interface controller 230 complies with the PCMCIA protocol. The interface controller 230 is coupled to a random access memory (RAM) device 232 through data bus 234. The RAM 232 provides a data buffer to store the data transferred between the host 212 and the disk 18. In the preferred embodiment, the RAM can store up to 4.0 Kbytes of data. 3.5 Kbytes of memory is typically dedicated to storing data transferred between the host and the disk. The remaining 0.5 Kbytes of memory provide a scratch pad which is typically dedicated to storing certain predetermined disk drive characteristics. When each disk drive is assembled, various characteristics of the drive unit are determined and stored on the disk. When the disk drive is powered up, the controller performs an initialization routine. Part of the routine retrieves the drive characteristics from the disk and stores the same in the scratch pad portion of the RAM.

The management of the RAM 232 is controlled by a memory controller circuit 236 which provides addresses to the memory device 232 on address bus 238 and an enable control signal on line 240. The memory controller circuit 236 receives access request from the interface controller circuit through lines 242. The controller circuit 236 also receives access request from a disk controller circuit 244 through lines 246. The disk controller circuit 244 provides an interface between the disk manager chip 98 and the R/W chip 94. The disk controller circuit 244 receives read/write control signals on lines 248 from the interface

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circuit 236 which are relay to the R/W chip 94 on read and write gate lines 250 and 252. The interface, memory and disk controller circuits is also connected to the controller chip 92 through lines 254, 256 and 258.

The memory controller 256 controls the storage and retrieval of data between the RAM 232 and interface controller circuit 230, between the RAM 232 and the disk controller circuit 244 and between the controller chip 92 and the data manager chip 98. The RAM 232 and controller chip 92 are coupled together by dedicated data bus 208. The controller chip provides addresses and a data manager chip select (DMCS) control signal when the controller chip 92 wants access to the RAM 232.

To write data onto the disk 18, the host 212 initially provides a write request that is received by the interface controller circuit 230, which executes the requisite handshaking sequence. The interface controller circuit 230 generates an access request to the memory controller circuit 236 to store the logical addresses and data from the host to the memory buffer 232. The memory controller circuit 236 then stores the data in the buffer 232 in accordance with a memory mapping scheme. The interface controller circuit 230 generates a HOSTINT interrupt signal that is sent to the controller chip 92.

After acknowledging the HOSTINT signal, the controller chip 92 will request access to the RAM 232 to read the logical addresses provided by the host 212. The controller chip 92 converts the logical addresses to physical disk addresses. The controller chip 92 may then initiate a seek routine to move the heads 58 to the proper location on the disk 18. When the voice coil 80 has moved the transducers 58 to the desired disk sector, the controller chip 92 provides a Z sector signal to

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the data manager 98. Upon receiving the Z sector signal, the disk controller circuit 244 provides a data access request to the memory controller circuit 236. The memory controller circuit 236 initiates a write sequence onto the disk 18 by placing the corresponding contents of the RAM 232 onto the bus 216.

To read data, the host 212 provides a read request that is received by the interface controller circuit 230. The requested logical addresses are stored in the buffer 232. A HOSTINT signal is generated and the logical addresses are retrieved by the controller chip 92. The controller chip 92 converts the physical addresses to the actual sectors on the disk and then initiates a seek routine to move the actuator arm, accordingly. When the transducers are above the proper disk location, the controller chip 92 provides a Z sector signal to the data manager 98. The disk controller circuit 244 then generates a memory access request to the memory controller circuit 236 which enables the RAM 232. Data is then transferred from the R/W chip 94 to the buffer 232 through the disk controller circuit 244. The memory controller circuit 236 then transfers the data from the RAM 232 to the host 212 through the interface controller circuit 230.

As shown in Figure 10, the servo chip 96 contains a voice coil control circuit 270 and a spin motor control circuit 272 to drive the voice coil 80 and spin motor 20, respectively. The servo chip 96 is coupled to the controller chip 92 by a bi-directional 16 bit synchronous serial port 274. The serial port 274 is coupled to a digital to analog (Dac) converter by lines 278. The Dac 278 contains a spin motor Dac port 280, a voice coil Dac port 282 and an analog to digital (Ad) Dac port 284.

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The voice coil port provides three signals $V_{vc}offset$, $V_{vc}track$ and V_{vc} gain range to the voice control circuit 270 on lines 288-292. The three signals are summed within a summing circuit 294. The $V_{vc}offset$ signal provides the bias voltage for the voice coil 80. The $V_{vc}track$ signal provides a secondary voltage signal, that will vary the bias signal to more accurately control the driving signal of the voice coil 80. The V_{vc} gain range signal is another secondary signal that provides a higher resolution of the bias signal and is typically employed during a servo routine of the drive. The amplitudes of the V_{vc} signals are determined by a 8 bit data stream which is provided by the controller chip 92 to the voice coil port 280 through the bi-directional serial port 274. The data command is accompanied by a 7 bit address and a read/write bit which are decoded by the serial port. The data is directed to the appropriate Dac port in accordance with the contents of the 7 bit address.

The summation circuit 294 provides a signal to an operational amplifier 296 which biases a driver circuit 298. The driver circuit 298 is connected to the coils 78 of the voice coil through pins V_{cmP} 300 and V_{cmN} 302. The voice coil control circuit 270 also contains a current sensor 304 which is fed back to the operational amplifier 296 to provide a direct current control of the current supplied to the voice coil 80.

The spin motor port 280 provides signals $V_{spn}offset$, $V_{spn}track$ and V_{spn} gain range to the spin motor control circuit 272 through lines 306-310. The signals are received by the spin motor circuit which contains essentially the same components, summation circuit 312, op-amp 314, driver circuit 316 and current sensor 318, as the voice coil circuit 270. The summing circuit sums the $V_{spin}()$ signals as described

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above. Like the voice coil signals, the offset signal provides a bias voltage and the other signals provide an adjustment of the bias voltage. The driver circuit 316 is connected to the windings of the spin motor through pins A, B and C on lines 320-324, respectively. The driver circuit 316 is controlled by spindle control logic 326 which sequentially enables the proper combination of drivers of the output lines A, B and C after receiving a commutation advance signal provided by the controller chip 92 on the Vcomm line 328. Each time a commutation advance signal Vcomm is provided, the control logic 326 sequentially enables the correct drivers, so that a current is provided to the spin motor in the proper combination of lines A, B or C.

The spin motor control circuit 272 has a back emf sensor 330 connected to the lines A, B and C and the center tap (CT) of the motor on line 332. The sensor 330 provides a back emf signal to a comparator 334 which compares the signal to a reference voltage. The comparator 334 provides a Vphase signal to the controller chip 92 on line 336. The controller chip 92 utilizes the Vphase signal to commutate the spin motor 20 through the Vcomm line 328. In the preferred embodiment, the driver circuit 316 has additional lines SpnGa, SpnGb and SpnGc which can be connected to additional drivers to increase the current level provided to the motor. This feature allows the servo chip 96 to be used in disk drives which contain additional disk that require higher rotating torque.

The servo chip 96 has an analog multiplexer 338 which receives various input signals. The signals are multiplexed to an analog to digital (Adc) converter 340 which utilizes the digital to analog circuits of the Dac converter 276. The Adc includes a comparator 342, and a serial

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approximation register (SAR) 344 which generates a series of 8-bit data strings.

In operation, the multiplexer 338 provides an analog signal to the comparator 342. The SAR 344 generates successive 8 bit words that are sent to the Ad DAC port 284 which converts the word to an analog comparator signal. The analog comparator signal is compared with the analog signal from the multiplexer 338. The first word has the most significant bit set to 1 and all other bits set to 0. If the most significant bit is greater than the analog signal, then a bit 1 is provided to the serial port 274. The SAR 344 generates the next 8 bit word which is again converted to an analog signal and compared by the comparator 342. The new word has the next least significant bit set to 1. This routine is continued until 8 bits are provide to the serial port 274 to define the amplitude of the analog signal. The serial port 274 then sends the bits to the controller chip 92 through the serial line 304.

The multiplexer 338 receives input signals Vbemf and Vispn from the back emf sensor 330 and current sensor 318 on lines 346 and 348, respectively. A-B and C-D servo signals from the R/W chip 94 are provided to the multiplexer 338 through lines 350 and 352. The output signal Vivcm of the voice coil current sensor 304 is provided to the multiplexer 338 on line 354. These feedback signals are transmitted to the controller chip 92 through the Adc 340 and the serial port 274.

The voice coil control circuit 270 positions the heads 58 relative to the disk in response to commands from the controller chip 92. The controller chip 92 and control circuit 270 move the actuator pursuant to either a seek routine or a servo routine. In a seek routine the heads 58 are moved from a first track location on the disk to a second track

location on the disk. The servo routine is used to maintain the transducers 58 on the centerlines of the tracks.

In the preferred embodiment, the disk 18 contains embedded servo information. Figure 11 shows a typical sector on a track of a disk. Each sector initially contains a servo field followed by an ID field. The ID field includes a header address that identifies the sector. The ID field is followed by a data field and error correction code information. The ECC field is followed by another ID field which identifies a subsequent data field D1 that contains a fraction of the data of data field D0.

The servo field initially contains a write to read field and then an automatic gain control (AGC) field that is followed by a period of no data (DC gap). At the end of the DC gap is a sync pulse. The servo field also includes a gray code to identify the particular cylinder (tracks) of the sector and a number of servo bursts A, B, C and D. Servo bursts A and B have an outer edge at the centerline of the track. Servo burst C is centrally located on the centerline of the track for even numbered tracks. Servo burst D has a bottom edge located at the top edge of servo burst C. The position of the transducer relative to the centerline of the track can be determined by reading the amplitudes of servo bursts A-D. The AGC field is used to set the reference voltage value of the servo bursts.

The sync pulse is identified as the first voltage transition that is sensed after a predetermined number of clock cycles having no transitions after the AGC field. For example, after the transducer senses the AGC field, three clock cycles may occur without any voltage transitions, before detection of the sync pulse. As an alternate scheme, the beginning of the gray code may provide a voltage transition which signifies the sync pulse.

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Figure 12 shows a schematic of the controller chip 92 which contains a core microprocessor 360. In the preferred embodiment, the core is a modified version of a processor sold by Texas Instruments Inc. ("TI") under the part designation DSP TMS320C25. The processor 360 operates with less instruction sets than a conventional hard disk drive controller such as the controller chip sold by Intel Corp. under the family designation 80C196. The decrease in instruction sets results in less memory access request. The processor block 360 includes RAM memory (not shown). Conventional RAM devices operate with a 5.0 V nominal power supply. It is desirable to provide a hard disk drive that will run on 3.3 V nominal, a voltage level that is commonly used in portable laptop computers. Conventional RAM devices respond to processor memory access request at a slower speed when operating at 3.3 V, than when the RAM device is operating at 5.0 V. The slower RAM speed degrades the performance of the processor. Utilizing a processor which requires fewer memory access request for a given function provides a system that can operate on 3.3 V without appreciably affecting the performance of the processor.

The DSP microprocessor has two separate internal busses (not shown) for transferring instructions and data. The dual bus architecture allows the processor to execute fetching, decoding, reading and execution routines in parallel. The pipeline feature of the DSP significantly increases the performance of the processor. The DSP processor has on board memory that functions as both registers and a RAM device.

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The controller chip also has supporting "on-chip" hardware coupled to the processor 360. The supporting hardware includes a bi-directional 16 bit synchronous serial port 362 that is coupled to the servo 96 and R/W chips 94 through the serial lines 204 and 206. The serial port 362 is also connected to the processor 360 through bus 364. The serial port 362 contains registers that provide a buffer between the processor 360 and the chips 94 and 96. The port 362 also generates chip select signals for the R/W chip 94 and the servo chip 96 in response to addresses provided by the processor 360. The serial port 362 is connected to a register file 366.

The controller chip 96 has a state machine 368 which contains a gray code circuit 370, servo strobe circuit 372, burst demod circuit 374, automatic gain control (AGC) circuit 376 and a write disable circuit 378. The burst demod 374 controls the operation of the other circuits through lines 380. The demod circuit 374 is connected to a timer circuit 382 through line 384. Both the gray code circuit 370 and the burst demod circuit 376 are connected to a raw data line 328 to receive raw data from the R/W chip 94.

The timer circuit 382 has a number of timers, one of which "times out" prior to the servo burst of a sector. When the pre-servo timer times out, the timer circuit 382 provides an AGC signal to the AGC circuit 376 on line 386. The AGC signal enables the AGC circuit 376, which enables the automatic gain control circuitry of the R/W chip 94 through line 388. The timer circuit 382 also provides a search signal to the burst demod 374 on line 384. The search signal enables the burst demod 374 to begin searching for the sync pulse within the servo burst of the sector. Upon receipt of the search signal, the burst demod 374 enables an

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internal sync mark field when no signal transitions (from the raw data line 228) occur within a predetermined number of clock cycles. If a transition occurs within a predetermined time after the field is enabled, the burst demod 374 generates a H sector signal which signifies the detection of a sync pulse.

The H sector signal is provided to a Z sector circuit 392 on line 394 and to the processor 360 on line 390. The H sector signal from the demod circuit 374 sets a pair of timers within the z sector circuit 392. The z sector circuit 392 provides a z sector signal to the data manager 98 and R/W 94 chips on line 258 when a timer "times out". There is preferably a timer for each data field Do and D1. The z sector circuit 392 only generates a z sector signal if the circuit 392 has been enabled by the processor 360 through enable line 396.

The burst demod 374 circuit enables the gray code circuit 372 after detection of the sync pulse. The gray code circuit 372 contains shift registers which store the gray code provided on the raw data line 228. The gray code is then stored in a dedicated address in the register file 366 through bus 398, for subsequent retrieval by the processor 360. The detection of the sync pulse also sets an internal timer in the burst demod 374. When the timer times out the burst demod 374 disables the gray code circuit 370 and enables the servo strobe circuit 372. The servo strobe circuit 372 sends out a series of two bit signals on line 399, to enable internal circuits within the R/W chip 94 to provide the A-B and C-D signals to the servo chip 96. The A-B and C-D signals are then sent to the register file 366 through the Adc converter 340 and the serial ports 374 and 362.

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When the timer 382 generates the search signal, the burst demod 374 also enables the write disable circuit 378. The write enable line 252 from the data manager chip 98 is routed to the preamp 100 through the write disable circuit 378, so that the write disable circuit 378 can disable the write signal and prevent writing of data onto the disk. The write disable circuit 378 disables the write signal during the servo burst to prevent any writing of data onto the servo field. The write disable circuit 378 is also enabled by a shock sensor (not shown) through line 400. The shock sensor provides an enabling signal when the disk drive is accelerated beyond a predetermined value. The shock sensor and write disable circuit 378 prevent writing of data when the drive is subjected to an excessive shock.

The controller chip 92 contains an interface module 402 that is coupled to the processor 360 and register file 366 through busses 404 and 406. The interface module 402 provides a memory map between the processor 260 and the register file 366. The modular interface 402 allows the supporting on-chip hardware to be coupled to different types of processors. The module 402 is coupled to a decoder 408 through line 410. The decoder 408 decodes addresses provided by the processor 360 to enable chip select control signals ROM and DM that select either the ROM 102 or data manager chip 98 through lines 412 and 256.

The controller chip 92 contains an oscillator 412 which receives a clock signal from a system clock on line 414. The oscillator 412 provides a clocking signal to clock circuit 416 on line 418. The clock circuit 416 provides clocking signals for the R/W chip 94, data manager chip 98, servo chip 96, microprocessor 360 and the support hardware of the

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controller 92 on lines 420-428. In the preferred embodiment, the oscillator 412 generates a 30 MHz clock signal. The oscillator 412 is connected to a sleep circuit 430 through line 432. The sleep circuit 430 disables the oscillator 412 when an INTb signal is provided to the circuit 430 on line 434. The INTb signal is typically provided by the host processor (not shown). The host processor typically provides the sleep signal when a disk access request has not been generated for a predetermined time interval, by setting a bit within a register of the register file 366.

The support hardware also contains a spin circuit 436 which is connected to the servo chip 96 through the Vphase and Vcomm lines 336 and 328. The spin circuit 436 is connected to both the register file 366 and the processor 360 by lines 438 and 440. When the spin circuit 336 receives a Vphase signal, the circuit 436 provides an interrupt signal to the processor 360 on the SPININT line 440. The Vphase signal also sets an internal Vcomm timer within the spin circuit 436. Additionally, the spin block circuit 436 also reads a dedicated register(s) in the register file 366. The contents of the register file 366 provide a time interval between when the spin circuit 436 receives the Vphase signal and when the circuit 436 generates the Vcomm signal for the spin control circuit 272 of the servo module 96.

The processor 360 has a continuously running internal timer (not shown). When the processor 360 acknowledges the SPININT pin 440 and the line is activated by the spin circuit 436, the processor 360 reads the time of the internal timer and the value of the Vcomm timer in the spin circuit 436. The Vcomm timer value signifies the amount of time elapsed between the reception of the Vphase signal and the

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acknowledgment by the processor 360 of the SPININT interrupt signal. The Vcomm time is subtracted from the time value of the internal processor timer. The resulting time is compared to a theoretical time to determine if there is an error in the speed of the spin motor 20. The spin motor 20 typically has 12 poles wherein there are created 36 Vphase signals per revolution.

The processor acknowledges the interrupt signals H sector, SPININT, HOSTINT and DISKINT in accordance with a hierarchy that responds to the H sector interrupt first (voice coil subtask), SPININT interrupt signal second (spin motor subtask) and then either the HOSTINT or DISKINT interrupt signals (data subtask). Accordingly, when the burst demod 374 detects a sync pulse signal, a pulse is sent to the processor 360 on the H sector line 390. Upon receiving the H sector signal the processor 360 may initiate a servo routine. The processor 360 initially reads the registers within the register file 366 that contain the gray code information. The processor 360 determines the cylinder location of the head 58 and then writes data containing voice coil control information to the serial port 362. The serial port 362 then sends the data to the servo chip 96. If the gray code corresponds to a desired track location (eg. for a read or write of data from the disk) the processor enables the Z sector circuit 392 through the enable line 396.

After the gray code is read, the processor 360 contain the A-B and C-D servo information. The servo burst information is processed by the processor 360 to determine the location of the head 58 relative to the centerline of the track. The processor 360 then writes data to the serial port 362 for subsequent transmittal to the servo chip 96. If the

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processor 360 is in a seek routine the servo information is not fetched from the register file 366.

After the servo routine, the processor acknowledges any SPININT signal from the spin circuit 436 and computes the difference between the actual motor speed and the theoretical motor speed. In the preferred embodiment, the processor stores the error values of each sector and computes a mean spin motor error each revolution of the disk. The processor 360 then writes control data to the servo chip 96 through the serial port 362 to control the speed of the spin motor 20, typically during an index sector that occurs once per revolution of the disk 18.

After the spin routine the processor 360 acknowledges any HOSTINT or DISKINT interrupt signals. If the HOSTINT pin is active the processor 360 retrieves the logical addresses stored in the buffer 232 of the data manager 98. The processor 360 converts the logical addresses to actual sector locations on the disk. The processor 360 initiates a seek routine if the heads 58 are not above the desired track. Once the head reaches a desired sector of the head, the controller chip 92 provides the Z sector signal to the data manager 98 which then transfer, data with the R/W chip 94. An active DISKINT signal indicates the end of a data transfer or an error in the process of transferring data. The register file 366 typically has a error bit that is set when an error has occurred. The processor 360 reads the error bit and performs an error correction routine if there is an error.

Figure 13 shows a schematic of the R/W chip 94. The R/W chip 94 contains a bi-directional 16 bit synchronous serial port 450 that is coupled to the serial port 362 of the controller chip 92. The serial port 450 is coupled to a controller circuit 452 through line 454. The

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controller 452 is connected to a multiplexer 456 through line 458. The multiplexer 456 multiplexes the various lines of the heads in accordance with instructions received from the controller chip 92 through the serial port 450 and the controller circuit 452.

The R/W chip 94 has a data port 460 that is coupled to a detection circuit 462 through bus 464. The detection circuit 462 is coupled to the multiplexer 456 and controller circuit 452 by lines 466 and 468, respectively. The circuit 462 detects transitions in the voltage provided by the transducers and provides a digital output to the data port 246 through line 370. The R/W chip 94 has a decoder 472 connected to the servo strobe circuit 372 of the controller chip 92. The decoder 472 is coupled to a servo burst circuit 474 through line 476. The decoder 472 enables the servo burst circuit 474 in response to pulses received from the servo strobe. The servo burst circuit 474 provides the servo signals A-B and C-D to the servo chip 96 on lines 350 and 352.

In the preferred embodiment, the R/W chip 94 is an integrated circuit similar to a product sold by Silicon Systems Inc. ("SSI") under the part designation 32P4730. The pre-amplifier chip is preferably a conventional integrated circuit sold by TI under the part designation TLV2234.

Figures 14a-g provide a flowchart of a typical operating sequence of the disk drive. In processing block 500 the host 212 has provided the disk drive with a request to write data to logical addresses A0-A63. The other condition is a head position at the end of a sector of the disk. In block 502 the data manager 98 stores the physical addresses and data from the host into the RAM buffer 232 and activates the HOSTINT interrupt signal. As the disk spins the servo field of a sector the

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approaches the head. In block 404, the search timer of the timer circuit 382 times out and provides the search signal and H sector signal to the burst demod circuit 374 and processor 360, respectively. The AGC circuit is also enabled to provide a control signal to the R/W chip 94 to initiate automatic gain control in block 506.

Along a parallel path the spin motor control circuit of the servo chip 96 generates a Vphase signal that is received by the spin circuit 436 of the controller chip 92 in block 508. The spin circuit 436 generates a SPININT interrupt signal for the processor 360 and initiates an internal timer in block 510. The spin circuit 436 also accesses the register file 366 to determine the time interval between the Vphase signal and the generation of the Vcomm signal. In block 512, the spin circuit 336 generates the Vcomm signal after the predetermined time interval.

After block 506, the burst demod circuit 374 reads raw data from the R/W chip 94 and enables the gray code circuit 370 upon the detection of the sync pulse in block 514. In block 516, the burst demod circuit 374 disables the gray code circuit 370 and enables the servo strobe circuit 372, which provides servo strobe pulses to the R/W chip 94. The R/W chip 94 provides the servo signals A-B and C-D to the servo chip 96 in block 518. The servo chip 96 converts the analog servo signals to digital data strings, which are transmitted to the controller chip 92 and stored in the register file 366 in blocks 518 and 520. The ID field of the servo burst is subsequently stored in the register file 366 in block 522.

In processing block 524, the processor 360 acknowledges the H sector interrupt signal. In decision block 526, the processor 360 determines whether the disk drive is in a seek routine. If the drive is in

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a seek routine, the processor reads the contents of the register file 366 which contain the gray code information, in processing block 528. In blocks 530-531, the processor 360 compares the gray code data with a desired track location, computes a seek current and generates a write command which is transmitted to the servo chip 96 through the serial ports 274 and 362. If the disk is in a servo routine the processor 360 reads the contents of the register file 366 which contain the servo burst information in processing block 534. The servo burst information is used to determine whether the heads 58 are on the centerline of the tracks and to calculate a voice coil correction command. in processing block 537-8. The processor 360 then generates a write command containing voice coil control data to the servo chip 96 through the serial ports in block 532. The digital voice coil control data is converted to analog signal by the Dac of the servo chip and provided to the voice coil to move the actuator arm and heads of the assembly.

In block 538, the processor 260 acknowledges the SPININT interrupt signal, if one exists. The processor 360 reads the processor internal timer and the Vcomm timer of the spin circuit 436 to compute the time interval between the Vphase signals in processing block 540 and adds the time interval to an accumulated time. In accordance with decision block 542, if the number of interrupts equals one revolution, a spin correction command is computed and the processor 360 generates a write command to the servo chip 96 through the serial ports in processing blocks 544 and 546. The spin correction command is calculated from the difference between a reference time and the accumulated time. The accumulative time is reset to zero in block 547. A new time interval value is also stored in the register file 366 for

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subsequent use by the spin circuit 436. The write command is transmitted to the servo chip which converts the digital string into analog signals which are provided to the spin motor control circuit. If the number of interrupts does not equal a revolution, the accumulative time is stored by the processor 360 in block 548.

In processing block 550, the processor 360 acknowledges the HOSTINT interrupt signal from the data manager 98. The processor 360 then retrieves the physical addresses from the buffer 332 within the data manager 98 and the ID field data in the register file 366 in processing block 552. In block 554, the processor 360 converts the logical addresses to actual sector locations. In accordance with decision block 556, if the heads 58 are not above the actual sector location, the processor 360 initiates a seek routine and generates a write command to the servo chip 96 to move the voice coil in processor block 558. The actuator arm is moved until the head is in the proper track. The processor 360 continually reads gray code until the actual sector location is adjacent to the head. In block 560, the processor 360 enables the Z sector circuit 392 which activates the Z sector pin after the servo field of the sector. The activation of the Z sector pin initiates a write of data from the data manager 98 to the R/W chip 94, which writes the data into the data field of the sector in processing block 562.

While certain exemplary embodiments have been described and shown in the accompanying drawings, it is to be understood that such embodiments are merely illustrative of and not restrictive on the broad invention, and that this invention not be limited to the specific constructions and arrangements shown and described, since various other modifications may occur to those ordinarily skilled in the art.

What is claimed is:

1. A hard disk drive, comprising:
 - a disk;
 - a spin motor that rotates said disk;
 - an actuator arm assembly coupled to said disk;
 - a printed circuit board that is essentially in a same plane as said disk;
 - a controller chip attached to said printed circuit board;
 - a data manager chip attached to said printed circuit board;
 - a read/write chip attached to said printed circuit board;
 - a servo chip attached to said printed circuit board; and,
 - a housing that encloses said disk, said spin motor, said actuator arm assembly and said printed circuit board.

2. The hard disk drive as recited in claim 1, further comprising a pre-amplifier chip mounted to said printed circuit board.

3. The hard disk drive as recited in claim 1, wherein said spin motor includes a spindle, a hub and a conical bearing couple to said spindle and said hub.

4. The hard disk drive as recited in claim 1, wherein said housing includes a cover plate and a base plate that are connected by a clamp which has a C shaped cross-section.

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5. The hard disk drive as recited in claim 1, wherein said actuator arm assembly includes an actuator arm which has a roller bearing that extends into a V-shaped slot of a bearing block, said roller bearing being coupled to said bearing block by a bearing capture member.

6. The hard disk drive as recited in claim 1, wherein said housing has a thickness of approximately 5 millimeters.

7. The hard disk drive as recited in claim 6, wherein said housing has a width of approximately of 54 millimeters and a length of approximately 85 millimeters.

8. A portable hard disk drive card, comprising:
a housing having a first end and a second end;
a connector located at said first end of said housing;
a disk located within said housing;
a spin motor that rotates said disk;
an actuator arm assembly coupled to said disk;
a printed circuit board located between said disk and said first end of said housing;
a controller chip mounted to said printed circuit board;
a data manager chip mounted to said printed circuit board;
a read/write chip mounted to said printed circuit board; and,
a servo module chip to said printed circuit board.

9. The hard disk drive as recited in claim 8, further comprising a pre-amplifier chip mounted to said printed circuit board.

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10. The hard disk drive as recited in claim 8, wherein said spin motor includes a spindle, a hub and a conical bearing couple to said spindle and said hub.

11. The hard disk drive as recited in claim 8, wherein said housing includes a cover plate and a base plate that are connected by a clamp which has a C shaped cross-section.

12. The hard disk drive as recited in claim 8, wherein said actuator arm assembly includes an actuator arm which has a roller bearing that extends into a V-shaped slot of a bearing block, said roller bearing being coupled to said bearing block by a bearing capture member.

13. The hard disk drive as recited in claim 8, wherein said housing has a thickness of approximately 5 millimeters.

14. The hard disk drive as recited in claim 13, wherein said housing has a width of approximately of 54 millimeters and a length of approximately 85 millimeters.

15. A hard disk drive that can be coupled to an external device, comprising:

housing means having a first end and a second end;

disk means for storing information;

spin motor means for rotating said disk;

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actuator arm assembly means for transferring information with said disk;

data manager means for transferring information with the external device;

read/write means for transferring information between said actuator arm assembly means and said data manager means;

servo module means for controlling said actuator arm assembly means and said spin motor means;

controller means for controlling said data manager means, said read/write means and said servo module means;

printed circuit board means for supporting said controller means, said data manager means, said read/write means and said servo module means, said printed circuit board means being located between said disk means and said first end of said housing.

16. The hard disk drive as recited in claim 15, further comprising pre-amplifier means for amplifying a signal from said actuator arm assembly means, said pre-amplifier means being mounted to said printed circuit board means.

17. The hard disk drive as recited in claim 15, wherein said spin motor means includes a spindle, a hub and a conical bearing couple to said spindle and said hub.

18. The hard disk drive as recited in claim 15, wherein said housing means includes a cover plate and a base plate that are connected by a clamp which has a C shaped cross-section.

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19. The hard disk drive as recited in claim 15, wherein said actuator arm assembly means includes an actuator arm which has a roller bearing that extends into a V-shaped slot of a bearing block, said roller bearing being coupled to said bearing block by a bearing capture member.

20. The hard disk drive as recited in claim 15, wherein said housing means has a thickness of approximately 5 millimeters.

21. The hard disk drive as recited in claim 20, wherein said housing means has a width of approximately of 54 millimeters and a length of approximately 85 millimeters.

22. A portable hard disk drive card that can be coupled to an external device, comprising:

housing means having a first end and a second end;

a connector located at said first end of said housing means;

disk means for storing information;

spin motor means for rotating said disk;

actuator arm assembly means for transferring information with said disk;

data manager means for transferring information with the external device;

read/write means for transferring information between said actuator arm assembly means and said data manager means;

servo module means for controlling said actuator arm assembly means and said spin motor means;

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controller means for controlling said data manager means, said read/write means and said servo module means;

printed circuit board means for supporting said controller means, said data manager means, said read/write means and said servo module means, said printed circuit board means being located between said disk means and said first end of said housing.

23. The hard disk drive as recited in claim 22, further comprising pre-amplifier means for amplifying a signal from said actuator arm assembly means, said pre-amplifier means being mounted to said printed circuit board means.

24. The hard disk drive as recited in claim 22, wherein said spin motor means includes a spindle, a hub and a conical bearing couple to said spindle and said hub.

25. The hard disk drive as recited in claim 22, wherein said housing means includes a cover plate and a base plate that are connected by a clamp which has a C shaped cross-section.

26. The hard disk drive as recited in claim 22, wherein said actuator arm assembly means includes an actuator arm which has a roller bearing that extends into a V-shaped slot of a bearing block, said roller bearing being coupled to said bearing block by a bearing capture member.

27. The hard disk drive as recited in claim 22, wherein said housing means has a thickness of approximately 5 millimeters.

28. The hard disk drive as recited in claim 27, wherein said housing means has a width of approximately of 54 millimeters and a length of approximately 85 millimeters.

29. A hard disk drive that can be coupled to an external device, comprising:

a housing that is approximately 10 millimeters thick;

a disk located within said housing;

a spin motor that rotates said disk;

an actuator arm assembly coupled to said disk;

electronic means for transferring information between said disk and the external device and for controlling said spin motor and actuator arm assembly, said electronic means being located within said housing.

30. The hard disk drive as recited in claim 29, wherein said housing means has a width of approximately of 54 millimeters and a length of approximately 85 millimeters.

31. The hard disk drive as recited in claim 29, wherein said electronic means includes data manager means for transferring information with the external device, read/write means for transferring information between said actuator arm assembly means and said data manager means, servo module means for controlling said actuator arm assembly means and said spin motor means, controller means for controlling said data manager means, said read/write means and said servo module means.

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32. The hard disk drive as recited in claim 29, wherein said spin motor includes a spindle, a hub and a conical bearing couple to said spindle and said hub.

33. The hard disk drive as recited in claim 29, wherein said housing includes a cover plate and a base plate that are connected by a clamp which has a C shaped cross-section.

34. The hard disk drive as recited in claim 29, wherein said actuator arm assembly includes an actuator arm which has a roller bearing that extends into a V-shaped slot of a bearing block, said roller bearing being coupled to said bearing block by a bearing capture member.

35. The hard disk drive as recited in claim 30, wherein said electronic means includes data manager means for transferring information with the external device, read/write module for transferring information between said actuator arm assembly means and said data manager means, servo module means for controlling said actuator arm assembly means and said spin motor means, controller means for controlling said data manager means, said read/write means and said servo module means.

36. The hard disk drive as recited in claim 35, wherein said spin motor includes a spindle, a hub and a conical bearing couple to said spindle and said hub.

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37. The hard disk drive as recited in claim 36, wherein said housing includes a cover plate and a base plate that are connected by a clamp which has a C shaped cross-section.

38. The hard disk drive as recited in claim 37, wherein said actuator arm assembly includes an actuator arm which has a roller bearing that extends into a V-shaped slot of a bearing block, said roller bearing being coupled to said bearing block by a bearing capture member.

39. The hard disk drive as recited in claim 29, further comprising a connector located at said first end of said housing.

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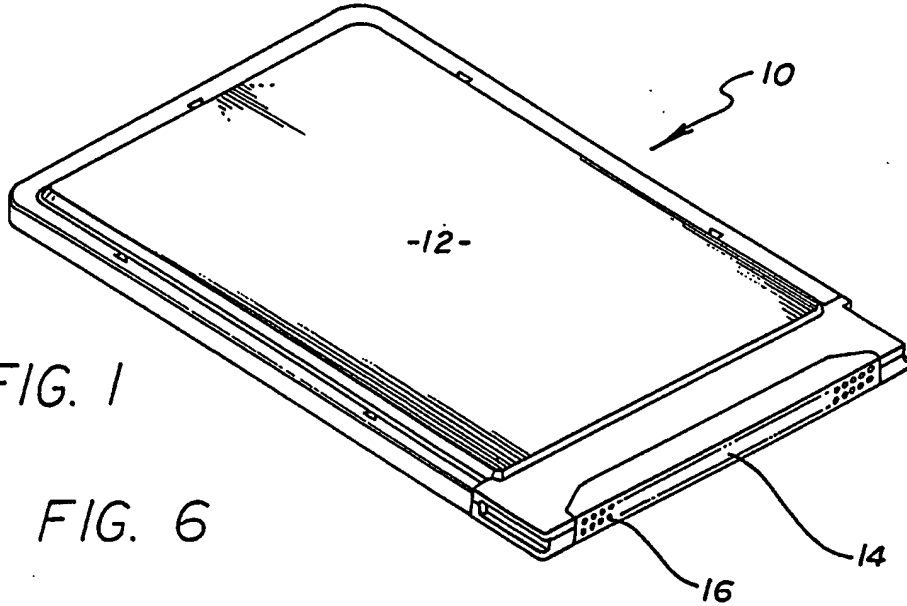


FIG. 1

FIG. 6

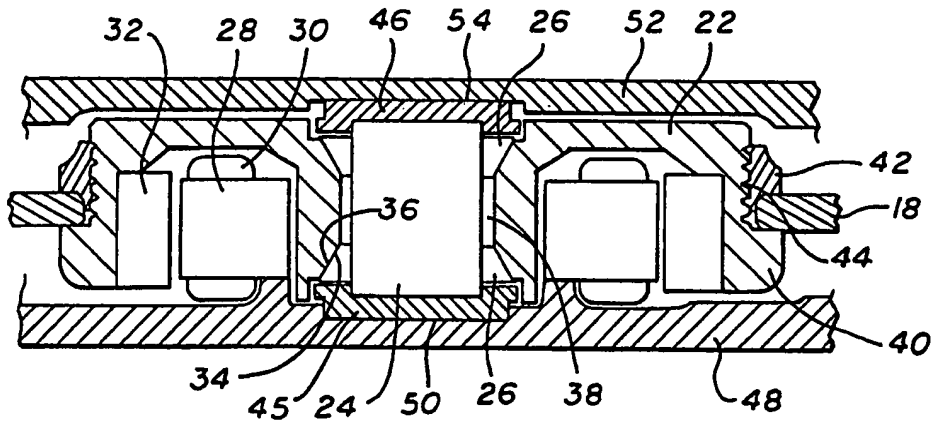


FIG. 7

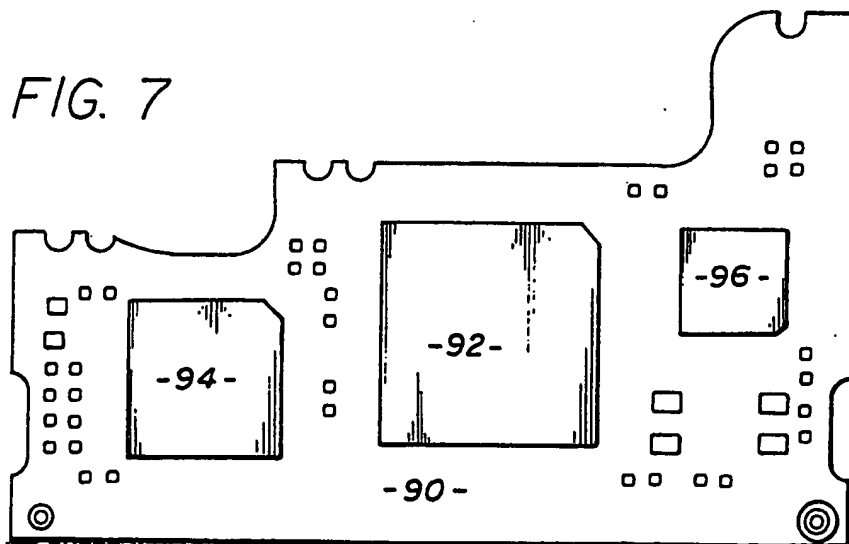
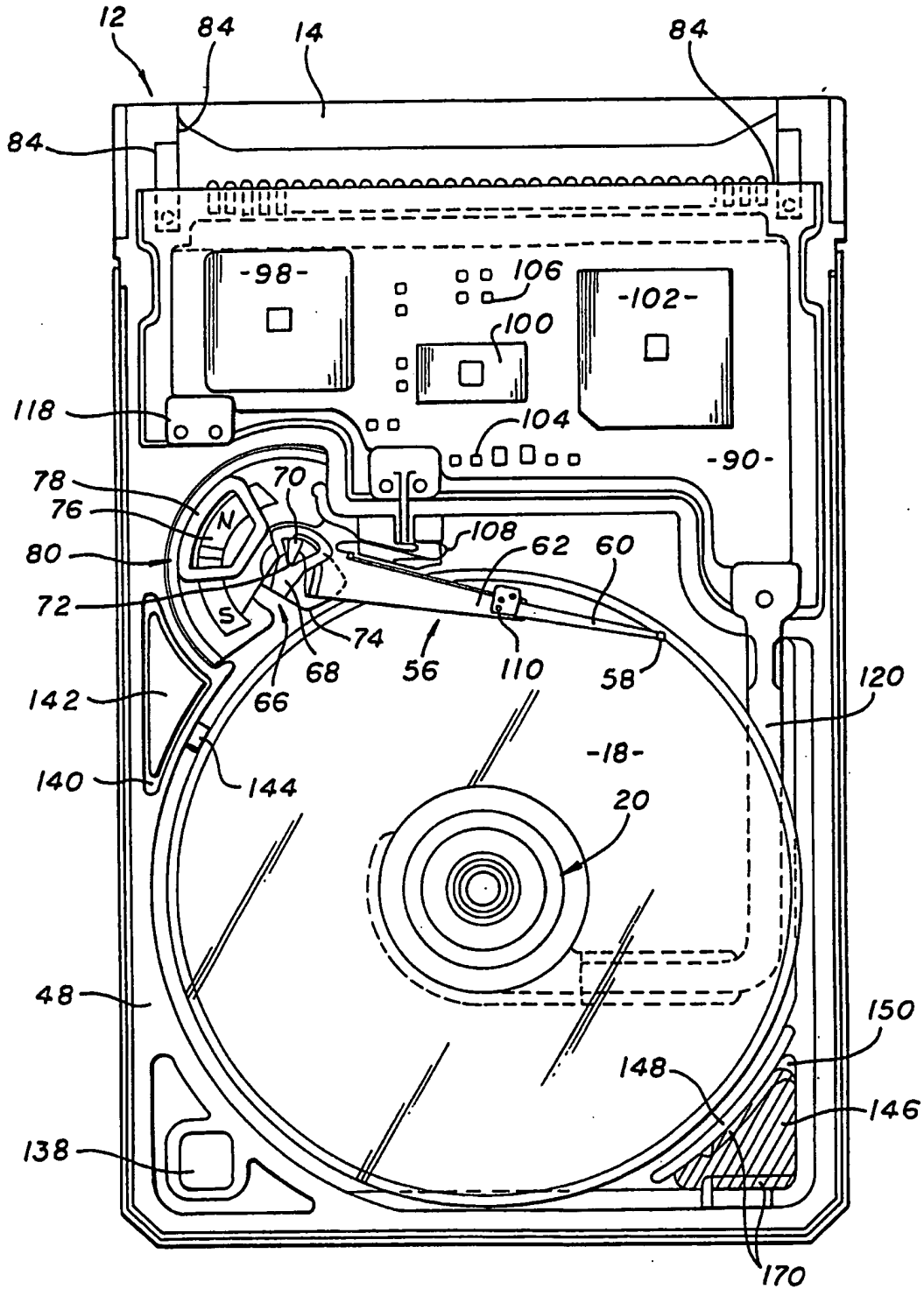
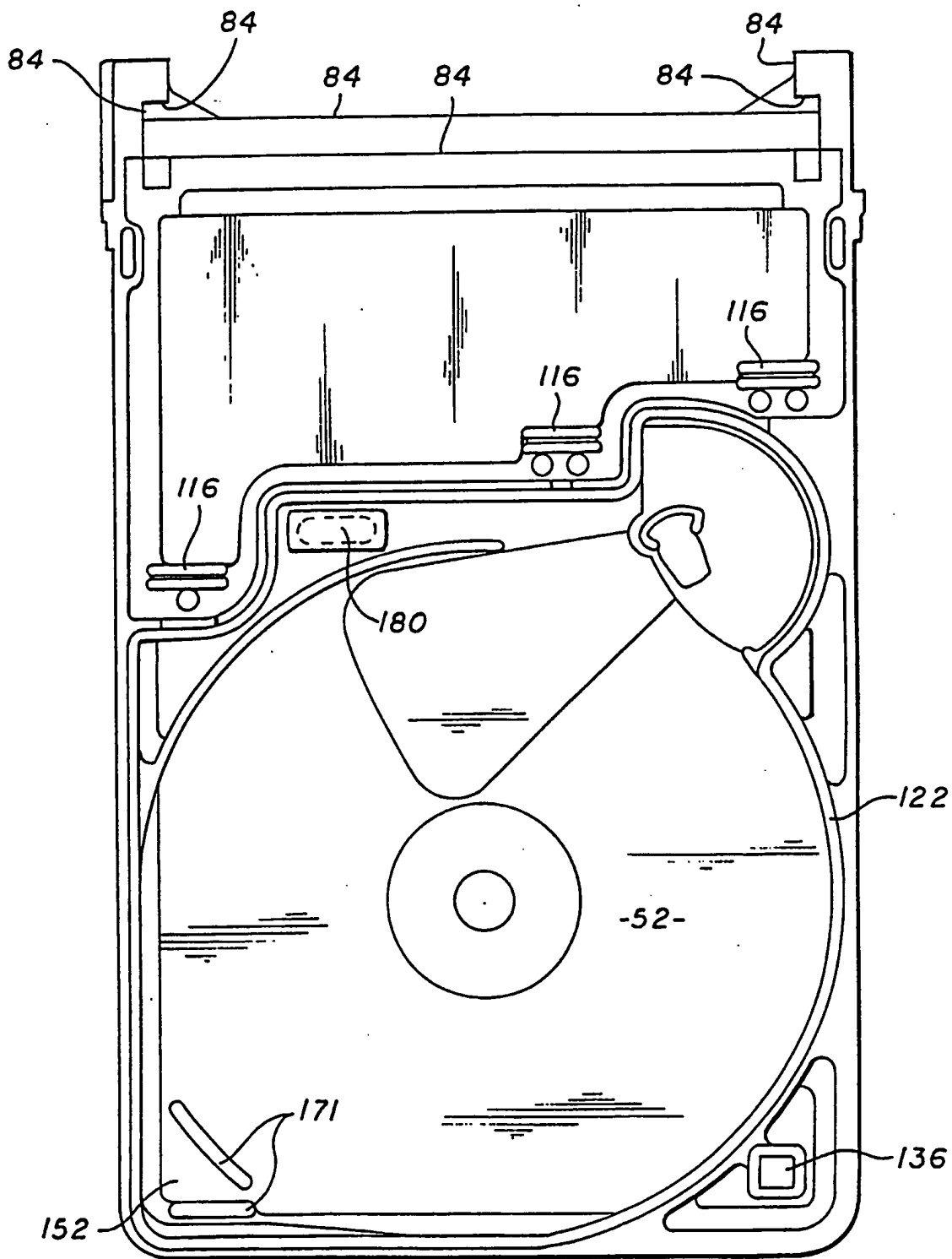


FIG. 2



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FIG. 3



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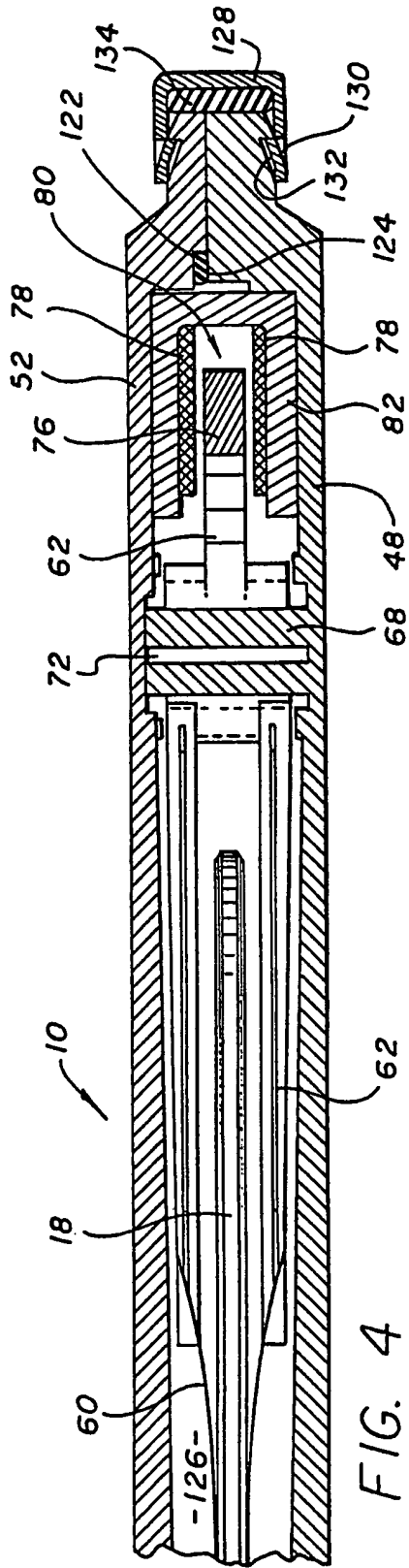


FIG. 4

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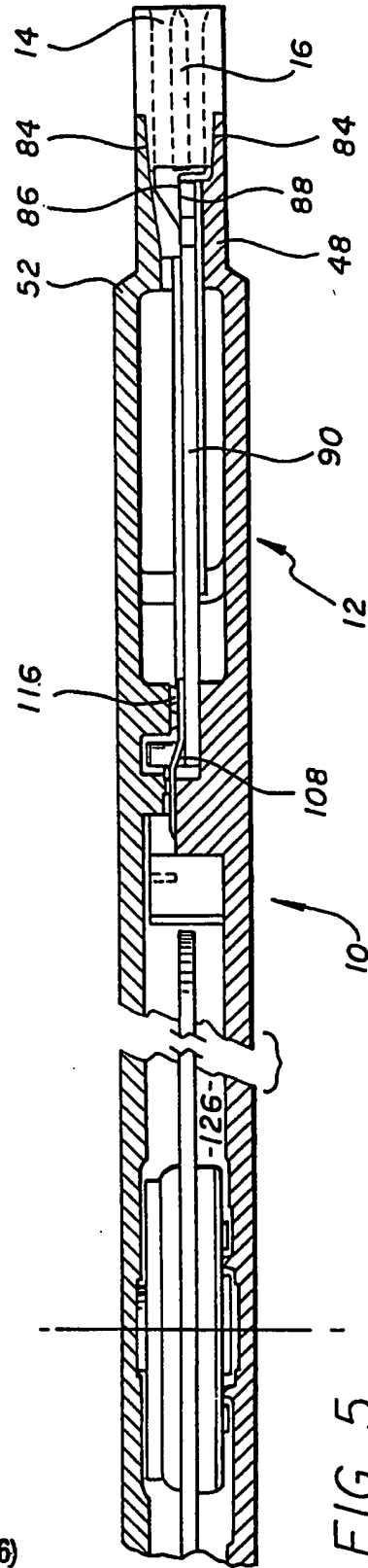


FIG. 5

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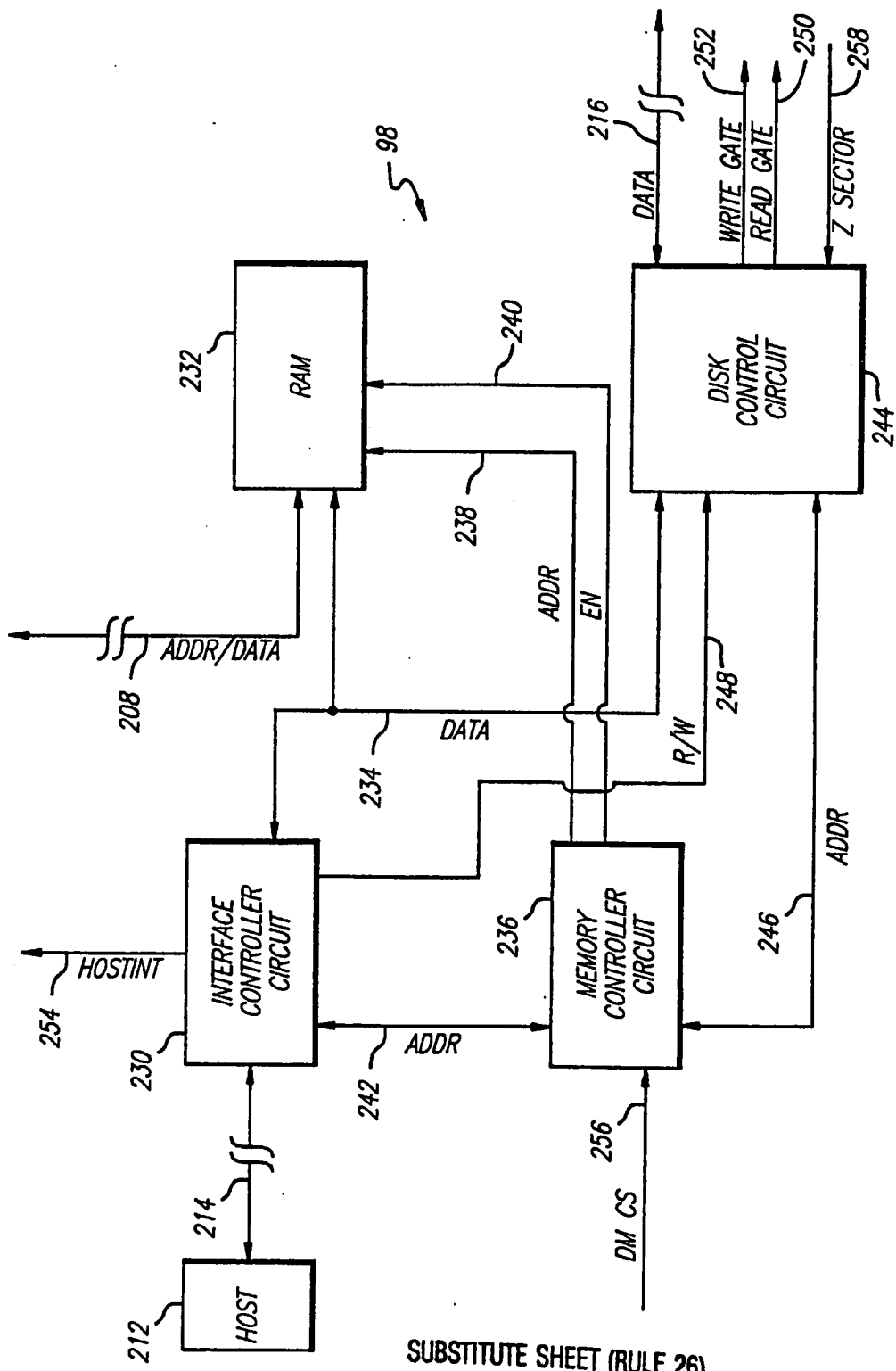


FIG. 9

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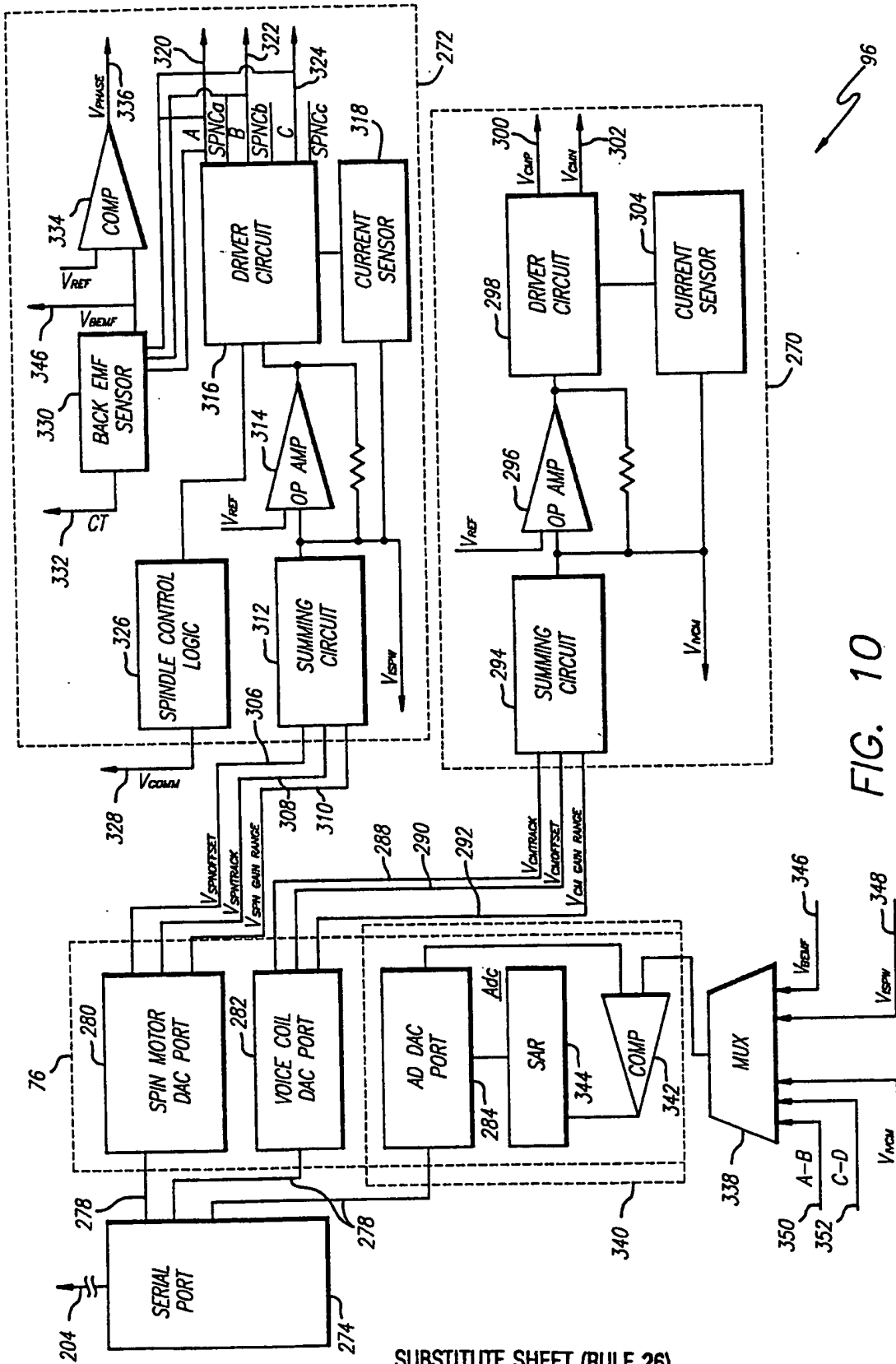


FIG. 10

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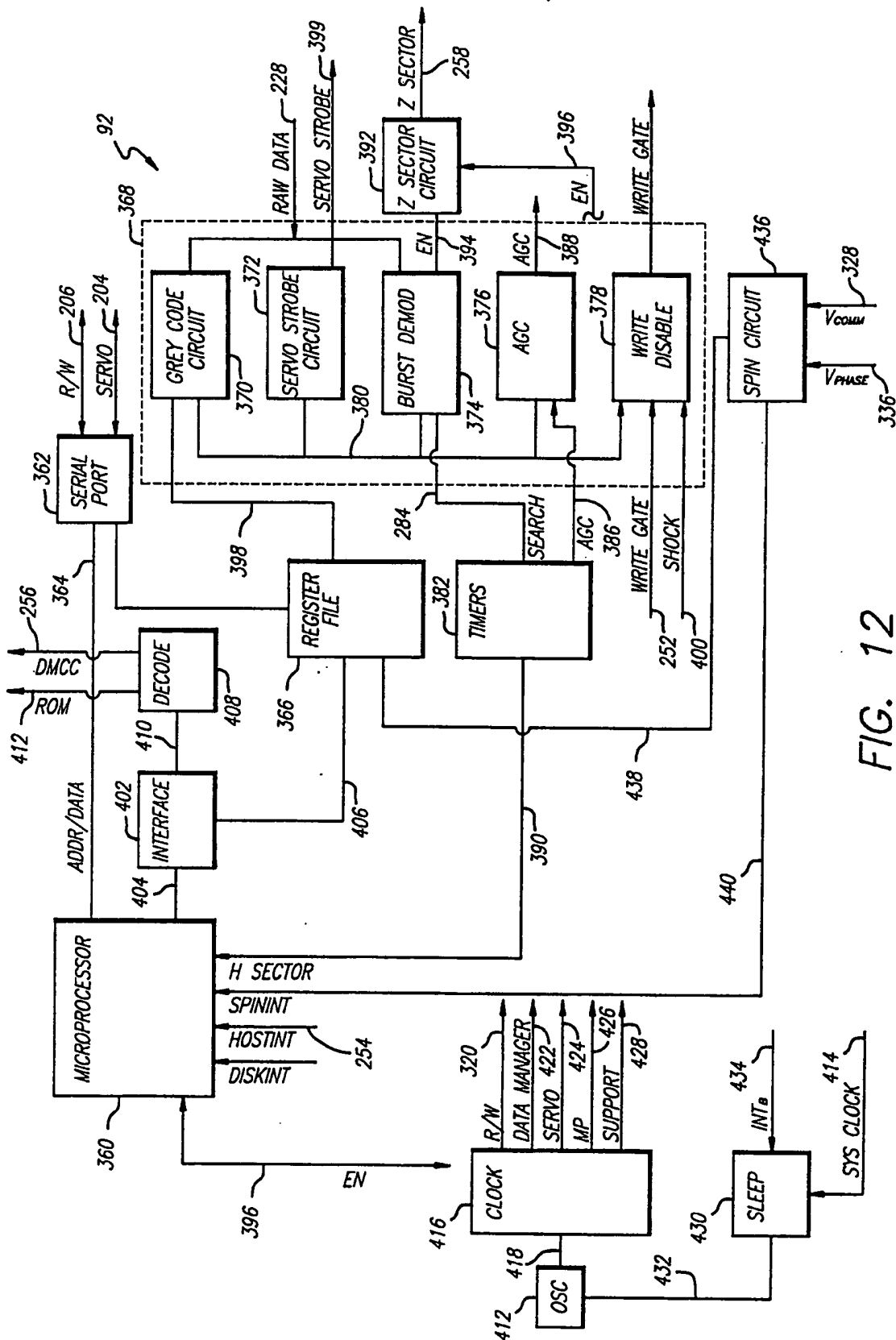


FIG. 12

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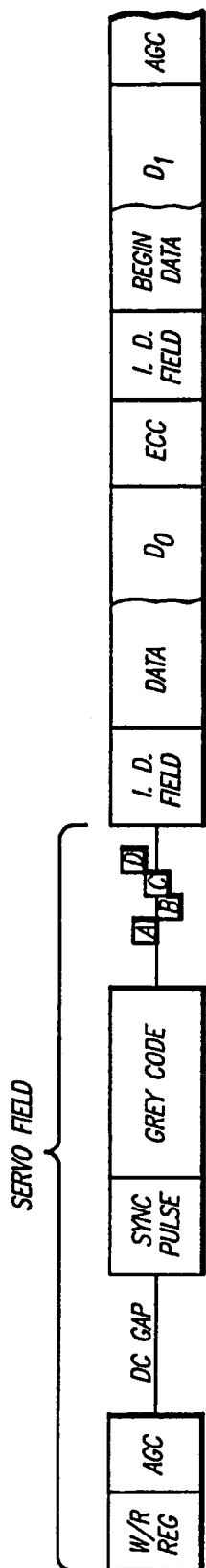


FIG. 11

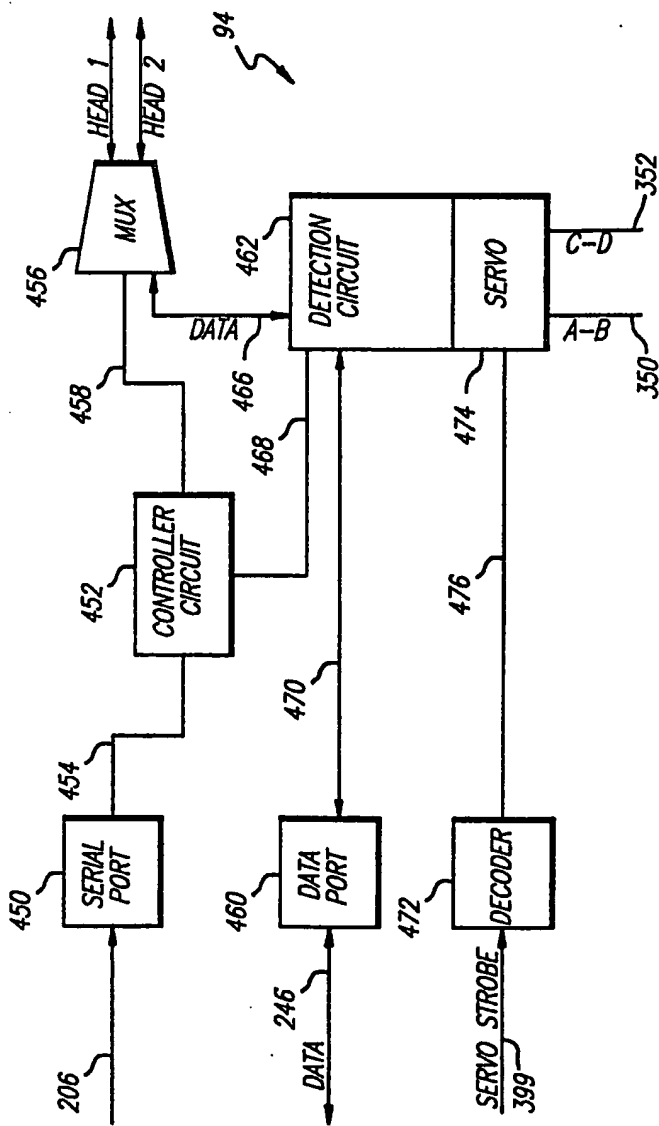


FIG. 13

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FIG. 14a

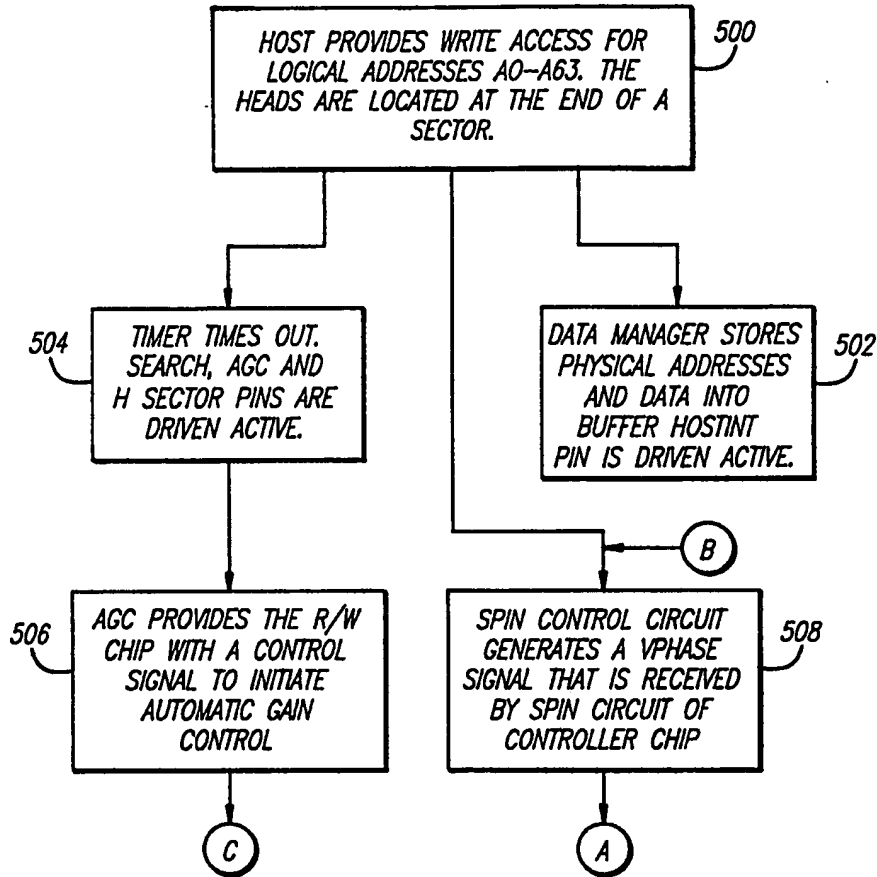
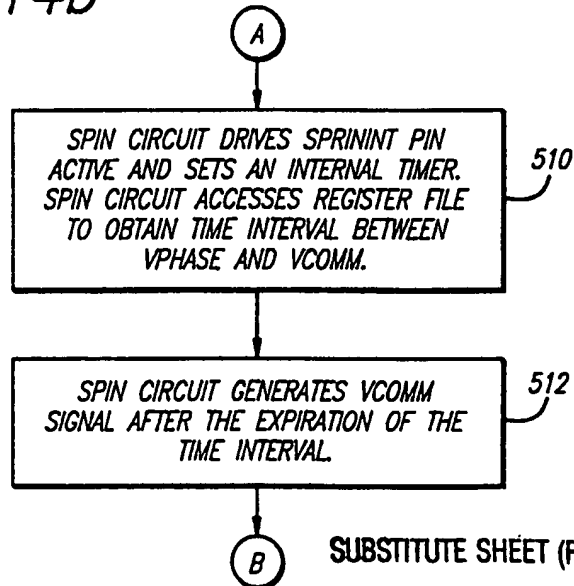


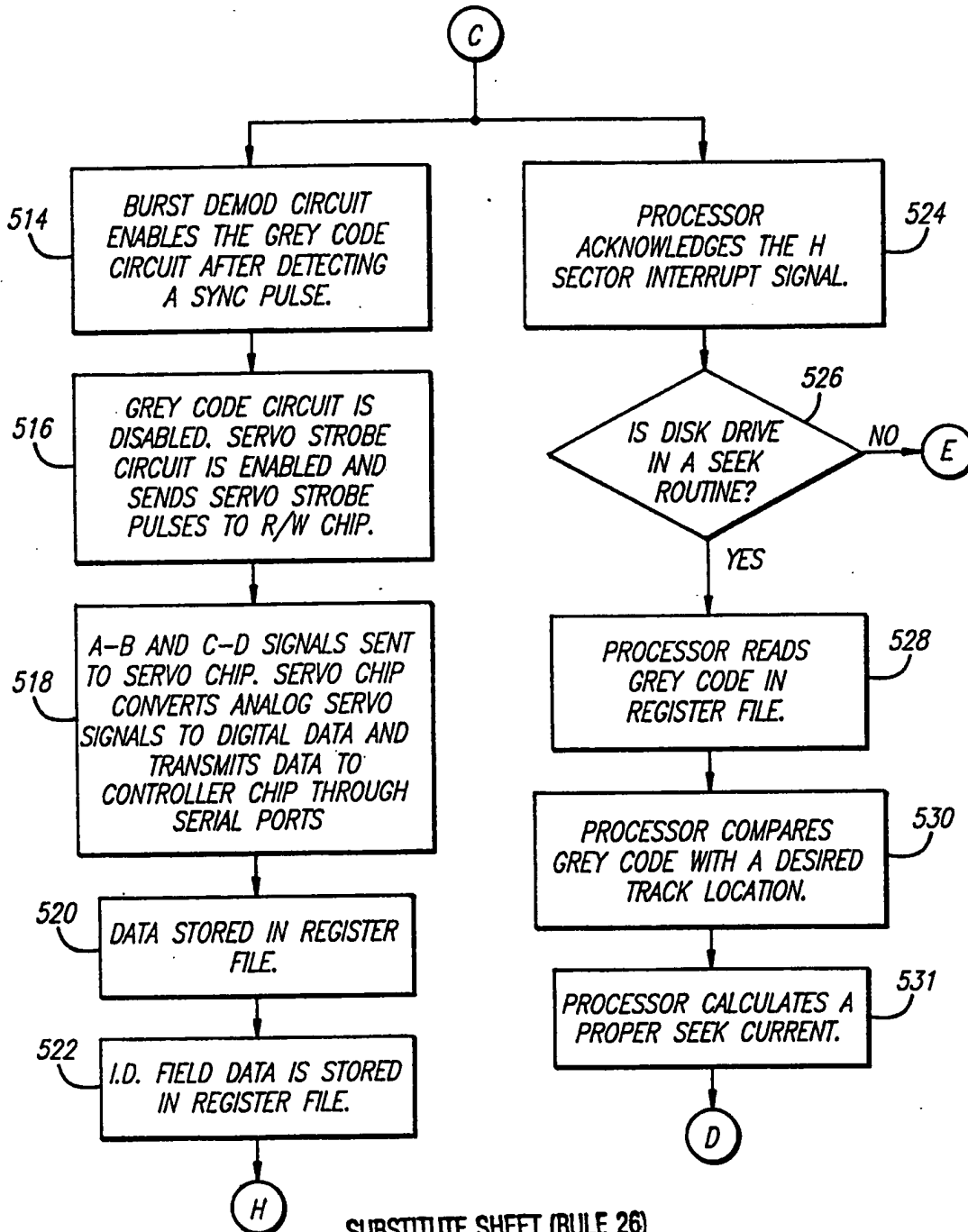
FIG. 14b



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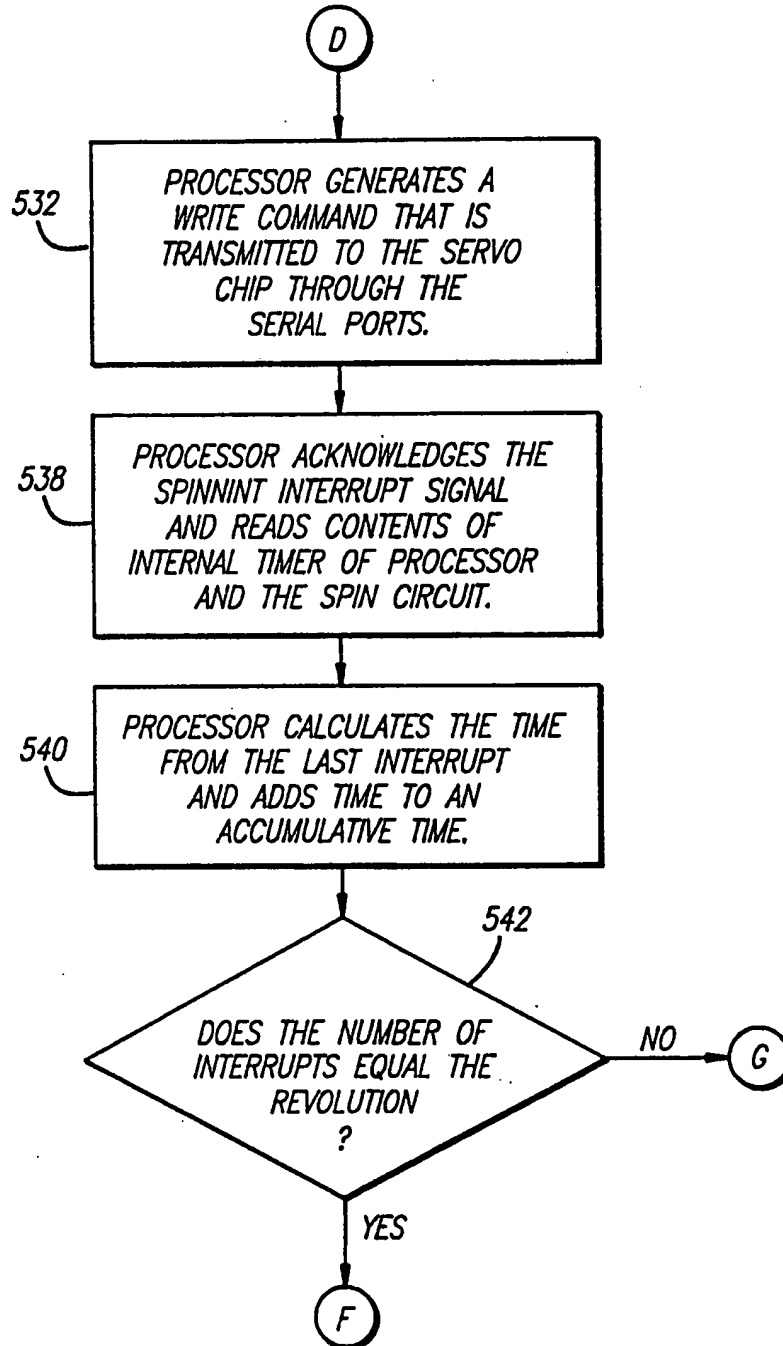
FIG. 14c



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FIG. 14d



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FIG. 14e

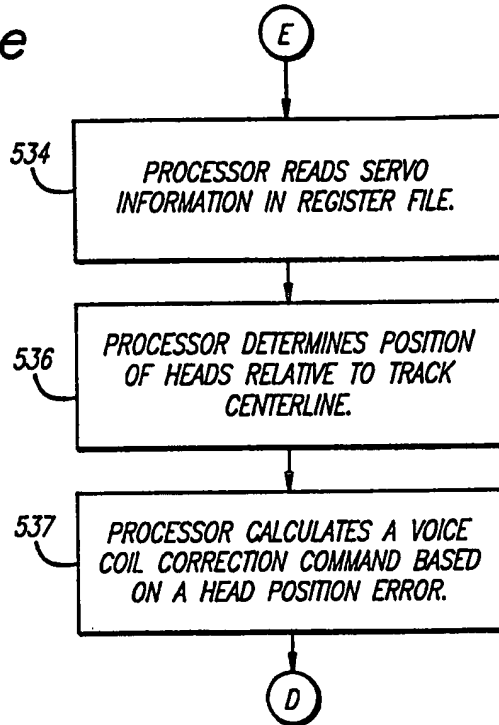
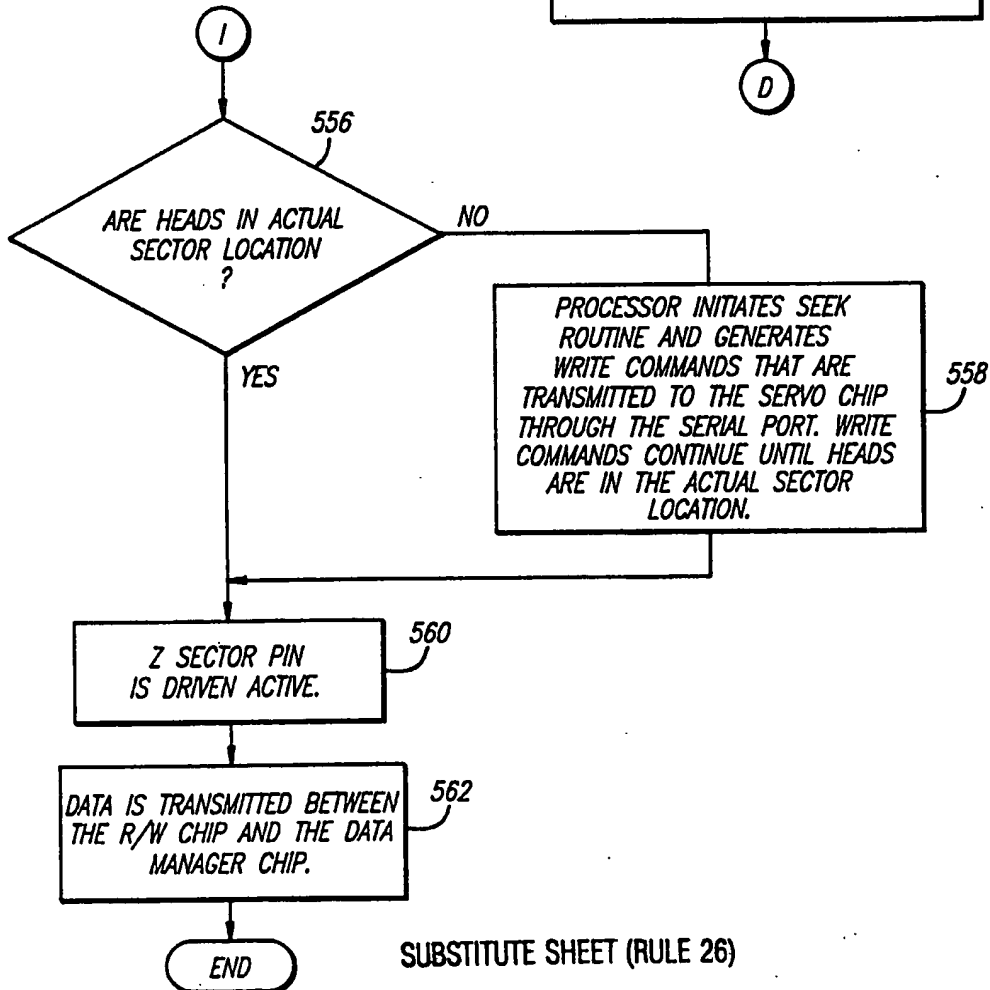
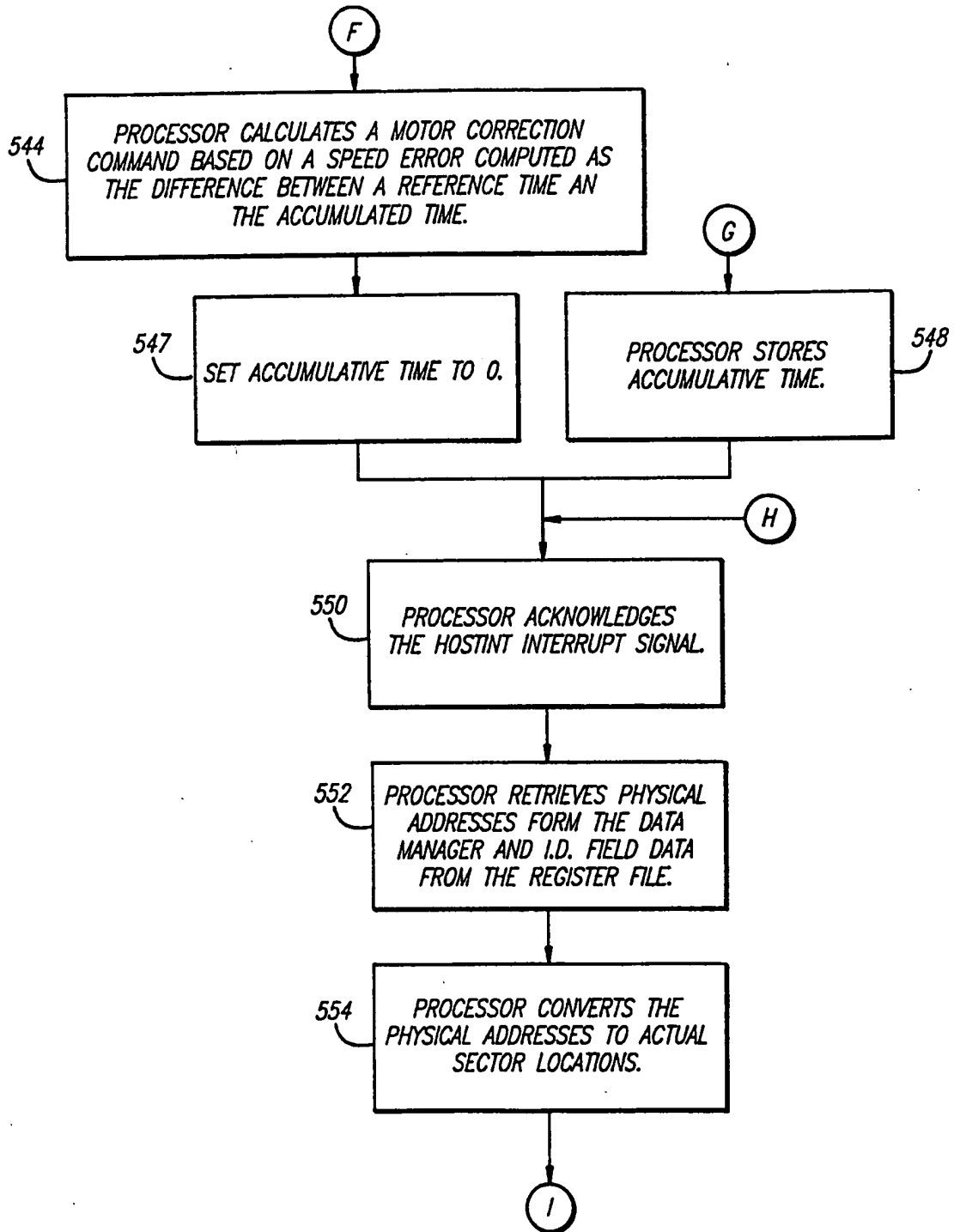


FIG. 14g



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FIG. 14f



INTERNATIONAL SEARCH REPORT

International application No.
PCT/US94/04981

A. CLASSIFICATION OF SUBJECT MATTER
 IPC(5) :G11B 5/012
 US CL :360/97.01. 903
 According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED
 Minimum documentation searched (classification system followed by classification symbols)
 U.S. : 360/97.01, 903

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
 APS (Search Terms: (disc or disk) drive#, preamplifier#, amplifier#, (cone or conical) bearing#, pin bearing#)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X/Y	US, A, 4,639,863 (Harrison et al) 27 January 1987, Figure 1	1-2, 8-9, 15-16, 22-23, 29, 31 & 39/ 3-7, 10-14, 17-21, 24-28; 30 & 32-38
Y	US, A, 4,919,547 (Schwartzman) 24 April 1990, Figure 1 and col. 1, lines 63-66.	3, 10, 17, 24, 32 & 36-38
Y	US, A, 5,030,260 (Beck et al) 09 July 1991, Figure 1 and col. 5, lines 15-17.	4, 11, 18, 25, 33 & 37-38

Further documents are listed in the continuation of Box C. See patent family annex.

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Date of the actual completion of the international search 22 June 1994	Date of mailing of the international search report 05 JUL 1994
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INTERNATIONAL SEARCH REPORT

International application No.
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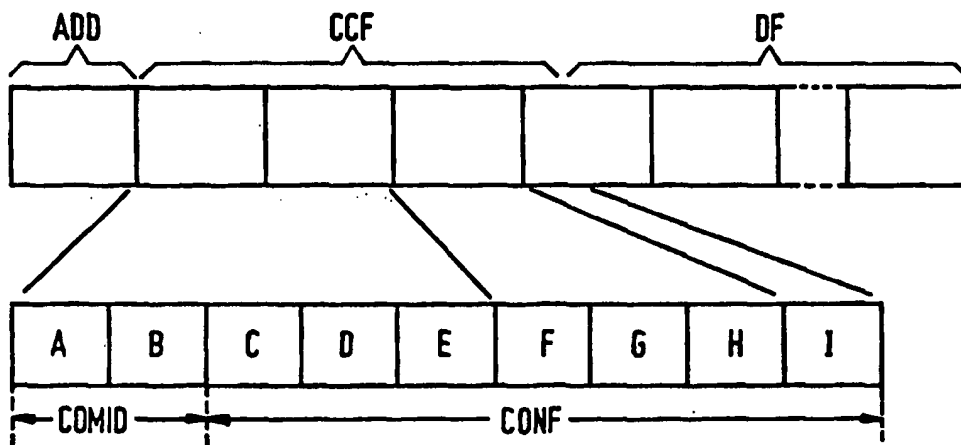
C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	EP, A, WO92/09945 (Schulze) 11 June 1992, Figure 1	5, 12, 19, 26, 34 & 38
Y	US, A, 5,025,336 (Morehouse et al) 18 June 1991, Figure 5	6-7, 13-14, 20- 21, 27-28, 30 & 35-38
A,P	US, A, 5,264,975 (Bajorek et al) 23 November 1993, Figures 2 and 7	6-7, 13-14, 20- 21, 27-28, 30 & 35
Y,P	US, A, 5,243,495 (Read et al) 07 September 1993, Figure 1 and col. 5, lines 4-28.	8 & 22



INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

<p>(51) International Patent Classification ⁶ : G08B 5/22, H04Q 7/02</p>	<p>A1</p>	<p>(11) International Publication Number: WO 95/02873 (43) International Publication Date: 26 January 1995 (26.01.95)</p>
<p>(21) International Application Number: PCT/IB94/00189 (22) International Filing Date: 4 July 1994 (04.07.94) (30) Priority Data: 9314516.7 13 July 1993 (13.07.93) GB (71) Applicant: PHILIPS ELECTRONICS N.V. [NL/NL]; Groenwoudseweg 1, NL-5621 BA Eindhoven (NL). (71) Applicant (for GB only): PHILIPS ELECTRONICS U.K. LIMITED [GB/GB]; 420-430 London Road, Croydon CR9 3QR (GB). (71) Applicant (for SE only): PHILIPS NORDEN AB [SE/SE]; Kottbygatan 7, Kista, S-164 85 Stockholm (SE). (72) Inventor: SHARPE, Anthony, Keith; 75 High Street, Teversham, Cambridge CB1 5AG (GB). (74) Agent: DE JONGH, Cornelis, Dominicus; Internationaal Octrooibureau B.V., P.O. Box 220, NL-5600 AE Eindhoven (NL).</p>		<p>(81) Designated States: CN, JP, KR, RU, European patent (AT, BE, CH, DE, DK, ES, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE). Published With international search report.</p>

(54) Title: DIGITAL COMMUNICATIONS SYSTEM, A TRANSMITTING APPARATUS AND A RECEIVING APPARATUS FOR USE IN THE SYSTEM



(57) Abstract

In digital communication systems such as digital paging, alpha-numeric messages are normally encoded character-by-character using say the ASCII bit character set. The number of bits concerned in sending such messages can be reduced by arranging the primary and secondary stations in a communications system to have ROMs which store a common dictionary. If a word to be sent is stored in the ROM then its location address is transmitted as a 7-bit character pair. However, if a word is not present in the ROM then it is encoded using ASCII characters. The data field (DF) of the transmitted message signal is preceded by and concatenated with a command and control field (CCF) which includes an indication that word compression has been used and indications which can be used by a receiver to determine when the ASCII characters begin and end in the data field.

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DESCRIPTION**DIGITAL COMMUNICATIONS SYSTEM, A TRANSMITTING APPARATUS
AND A RECEIVING APPARATUS FOR USE IN THE SYSTEM**

5

TECHNICAL FIELD

The present invention relates to a digital communications system and to a transmitting apparatus and a receiving apparatus for use in the system. More particularly, the present invention relates to the compression of alpha-numeric messages for transmission in digital communication systems such as digital radiopaging system.

10

For convenience of description the present invention will be described with reference to a digital radiopaging system but it is to be understood that the present invention is applicable to other digital transmission systems.

15

BACKGROUND ART

An internationally used digital paging code is the CCIR Radiopaging Code No 1 which is also known as POCSAG (Post Office Code Standardisation Advisory Group). Details of this radiopaging code are given in a book entitled "The Book of the CCIR Radiopaging Code No 1" published by the Radiopaging Code Standards Group (RCSG) in 1986. Appendix 1 discloses the specification for a standard Code Format for use in Wide Area Radiopaging Systems the details of which will be known by those skilled in the art. However, for the sake of completeness the signal format used comprises a batch structure consisting of preamble and a succession of concatenated batches. Each batch consists of a synchronisation code word plus 8 frames each comprising 2 code words, making a total of 17 code words. There are two types of code words, address code words and message code words each comprising 32 bits. In the case of a message code word 20 bits, that is bit 2 to bit 21 inclusive, form a data field and these are followed by parity check bits. Bits 20 and

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21 of an address code word, which precedes the message code word(s), are function bits and are used to select the format of decoding of concatenated message code words. Appendix 1, subsection 4.1 states that for the sole transmission of messages in decimal numbers, 4 bits per character are used and the function bits are set to 00. Subsection 4.2 refers to an Alpha-numeric or General Data Format and states that the ISO 7-bit coded character set is used and that the function bits are set to 11. When sending a message, the batch structure is maintained. Thus a message comprises an address code word and concatenated message code words plus a synchronisation code word at the beginning of each batch. As Appendix 1 is quite specific in stating that the formats shall not be mixed within any one message then the function bits in the address code word effectively condition the paging receiver to the method of deformatting the received message.

European Patent Specification EP-A1-0 536 831 discloses a method of compressing messages by means of storing words in a ROM dictionary and transmitting two 7 bit characters identifying the location of the word in the dictionary. The receiver has an identical ROM dictionary. In the case of a word not being in the dictionary then this is sent letter by letter as 7 bit ASCII characters. Switch characters are inserted into an encoded message to indicate the change from dictionary references to ASCII characters and vice versa. By using pairs of switch characters a wider range of options is available such as being able to use several dictionaries. A disadvantage of using a switch character or switch characters inserted into a message is that if its or their occurrence coincides with a fade in the received signal, the receiver will decode the subsequently received part of the message incorrectly.

DISCLOSURE OF INVENTION

An object of the present invention is to compress a message signal by a method which is robust against signal fading.

According to a first aspect of the present invention there is provided

a digital communications system comprising a transmitting means and a receiving means, in which the transmitting means has means for encoding alpha-numeric messages in at least two formats, at least one of which formats is a compressed format, characterised in that a data field of a message is preceded by a command and control field and in that the first character of the command and control field is indicative of whether a compressed format has been used in the data field.

According to a second aspect of the present invention there is provided a digital communications system comprising a transmitting means and a receiving means, in which the transmitting means has means for encoding alpha-numeric messages in at least two modes which may switch from one mode to the other mode and vice versa during the encoding of a message, characterised in that a data field of a message is preceded by a command and control field comprising indications which can be used by a receiving means to switch from one decoding mode to another decoding mode and vice versa in order to recover the message data.

According to a third aspect of the present invention there is provided a receiving apparatus for use in the digital communications system in accordance with the present invention, the receiving apparatus comprising means for receiving and recovering the command and control field and the data field, and means for decoding the code words in the data field in accordance with the indications given in the command and control field which are used to enable the decoding of the data field to be compatible with the encoding of the message data.

According to a fourth aspect of the present invention there is provided a transmitting apparatus for use in the digital communications system in accordance with the present invention, the transmitting apparatus comprising means for encoding alpha-numeric messages in at least two formats, at least one of which formats is a compressed format, characterised in that a data field of a message is preceded by a command and control field and in that the first character of the command and control field is indicative of whether a compressed format has been used in the

data field:

One of said at least two modes may comprise the transmission of two 7 bit characters identifying the location of a word in a ROM dictionary and another of said at least two modes may comprise the transmission of ASCII characters representing letters of words not included in the ROM dictionary. By the command and control field containing indications which a receiver can use to switch between dictionary locations and ASCII characters, then provided this field is received correctly, any fades occurring during the receipt of a data field will not affect the decoding operation but only the data to be decoded.

The indications may indicate the location of, and number of, ASCII characters in a series of ASCII characters in the data field.

In order to avoid the command and control field being excessively long, thereby reducing the benefits obtained by word compression, the number of series of ASCII characters may be limited to a maximum n. When there are n series of ASCII characters, the nth series terminates the data message.

If desired the command and control field may include an indication of the number of code words in a message.

BRIEF DESCRIPTION OF DRAWINGS

The present invention will now be described, by way of example, with reference to the accompanying drawings, wherein:

Figure 1 is a block schematic diagram of a base or primary station for a digital radiopaging system,

Figure 2 is a block schematic diagram of a paging receiver or secondary station,

Figure 3 in a diagram A illustrates diagrammatically the various fields in a compressed word message and in diagram B illustrates details of a Command and Control field CCF related to the format shown in Table 1,

Figure 4 is a flow chart relation to a receiver protocol for processing received data messages, and

Figure 5 illustrates how a widely used group of words may be transmitted in the system in accordance with the present invention.

In the drawings, the same reference numerals have been used to indicate corresponding features.

5

MODES FOR CARRYING OUT THE INVENTION

The present invention will be described with reference to a digital radiopaging system which can be overlaid transparently on a system operating in accordance to the CCIR Radiopaging Code No 1 but the encoding principles disclosed can be applied to any other data message system having a primary station and secondary station which are linked by cable, optical fibre and/or radio or a data storage and retrieval system.

In the case of a digital radiopaging system, such as one operating in accordance with CCIR Radiopaging Code No 1, messages to be relayed to secondary stations may be sent orally to a paging centre whereat an operator at a keyboard 10 types in the addresses and messages which are encoded in accordance with the ASCII or ISO-7 bit coded character set and sent to a control stage 14. Alternatively, a subscriber with a personal computer and MODEM 11 is able to send messages directly to the control stage 14 by way of a landline connection. The control stage 14 includes spell checking means and a dictionary in the form of a ROM 12 containing a vocabulary of say 16380 commonly used words. The dictionary is interrogated to see if it includes the word which has just been stored in the control stage, if it does then the address of the location of the word in the ROM is read-out. This address for the sake of description comprises two ASCII or ISO 7-bit characters. A message format stage 16 is coupled to the control stage 14 which feeds encoded data to the stage 16 either in the form of concatenated ROM addresses each representative of a compressed word, assuming that the words are in the dictionary, or ASCII-7 bit coded characters for words not in the dictionary. As will be explained later with reference to Figure 3 the completed message will include the

30

Address Field ADD and a Command and Control Field CCF which comprises indications of where a change from a ROM address to ASCII characters and vice versa occurs. Optionally an extended address field may be included between the Address Field ADD and the Command and Control Field CCF.

5 Once the encoded message string has been assembled in say a buffer store, it is analysed to determine where the changes from ROM dictionary addresses to ASCII characters and vice versa occur and the occurrences of these changes are included in the Command and Control Field CCF which together with the Address Field ADD is concatenated with
10 a Data Field DF. The message format stage 16 then forms code words from successive 20 bit blocks of the assembled, compressed message in accordance with the CCIR Radiopaging Code No 1. Since the format has been described briefly in the preamble of this specification then in the interests of brevity it will not be repeated. The string of code words is
15 then applied to a transmitter 18 for onward transmission.

Figure 2 illustrates a secondary station or paging receiver which comprises a radio receiver 20 which is periodically energised to be able to receive an address code word, if sent, in its appropriate frame. If the address code word is followed by message code words, the addressed
20 paging receiver remains energised to receive the message code words which are passed to a decoding stage 22 which includes means for error checking and correction within the limits permitted by the CCIR Radiopaging Code No 1. The decoding stage 22 checks addresses of paging signals received in the appropriate frame for a paging message
25 being transmitted to the particular pager. If a match is detected between a received address and an internally stored address then the paging receiver remains energised so that the concatenated message data is stored in a buffer memory 23 in the decoding stage 22. Once all the code words have been received, the Command and Control Field CCF is decoded and
30 checked for errors. If this field contains uncorrectable errors, the Data Field DF of the received message is discarded because without the knowledge of where the changes from dictionary references to ASCII characters and

vice versa occur the Data Field cannot be decoded. Assuming that the Command and Control Field CCF is decoded correctly and the Data Field DF is subsequently decoded the stream of bits is applied to a microcontroller 24 which stores the message data in a RAM 26.

5 When the user of the paging receiver wants to read-out the message(s) stored in the RAM 26, the microcontroller 24 is activated and reads out the data bits of the stored message. In the case of a ROM address, this is supplied to a ROM 28 which comprises the same dictionary as is stored in the ROM 12 (Figure 1) of the primary station. Assuming
10 that the address corresponds to an entry in the ROM 28 then the relevant word including an end space character is read-out in the form of ASCII characters and is supplied to a display driver 30.

 Alternatively, in the case of some of the bits being read-out of the RAM 26 being ASCII characters then the microcontroller 24 supplies these
15 directly to the display driver 30.

 The read-out from the ROM 28 has to be controlled such that word characters ASCII form are supplied in the correct sequence to the display driver 30. One way of doing this is for the space character at the end of a word to be detected by the microcontroller 24. A liquid crystal display
20 (LCD) panel 31 is connected to the display driver 30.

 In its most elementary form only two methods of encoding alpha-numeric data are used, namely as a ROM address comprising two ASCII 7-bit coded characters when a dictionary reference is used and character by character using ASCII 7-bit coded characters where a dictionary reference
25 cannot be used.

 Figure 3 illustrates in diagram A the message compression control format and message structure and in diagram B the format of the Command and Control Field CCF. As indicated already the code word structure of the Address Field ADD, Command and Control Field CCD and the Data Field DF is in accordance with the CCIR Radiopaging Code No 1 and in consequence
30 is transparent to those users of a paging system having paging receivers capable of receiving uncompressed alpha-numeric messages only. As the

format of the Address Field is conventional then in the interests of brevity it will not be discussed. The Command and Control Field CCF which follows the Address Field ADD comprises a series of 7-bit characters which as shown in diagram B comprise the Command Identity COMID and the Control Field CONF. The Data Field DF is a series of code words constituted by a string of 7-bit characters defining either the character identities in a ROM dictionary words or ASCII characters contained in the message. Optionally, an extended address field comprising a sequence of characters and digits is transmitted immediately after the Address Field ADD and before the Command and Control Field CCF.

Termination of the Data Field DF will be indicated by the receipt of another address or an idle code word but optionally an end of message code word may be included.

Referring to diagram B, the Command Identity COMID comprises a 7-bit character pair which can only occur in the first two character positions A,B of the Command and Control Field CCF in order to instruct the pager to operate in the appropriate compressed word mode. The Control Field CONF is a field comprising a plurality of character positions up to a predetermined maximum number. This field CONF gives to a pager the decoding information about the message, for example where the pager should switch from decoding character identities to ASCII characters and vice versa and the length of the message. This field will not exceed five code words. The Control Field CONF increases in steps of 14 bits (2x7 bits) because each pair of 7-bit numbers defines the start and end locations of each ASCII character series or island in the Data Field DF. The Control Field can have an even or odd number of 7-bit characters. In the case of the format of the Command and Control Field shown in Table 3 below an odd number of 7-bit characters defines the length of the message and an even number means that the last two characters define the length.

The Command and Control Field CCF may have various formats and examples are given below.

TABLE 1

Character		Function	Values	
5	C O M I D	A	Command Character. Word compressed message.	xx
		B	Language and case identity. Language 1 - upper case Language 1 - mixed case Language 2 - upper case Language 2 - mixed case	01 02 03 04
10	C O N T R O L	C	Number of 7 bit characters in Command and Control Field.	0 to 12 binary
		D	Location of first ASCII character in Data Field DF, for example the number of 7-bit characters from the end of the address code word.	4 to 128 binary
15	C O N T R O L	E	Number of ASCII characters following and including location "D" before word coding begins again.	1 to 128 binary
20		F	Location of the first of a second series of ASCII characters in DF	5 to 12 binary
		G	Number of ASCII characters following and including location F.	1 to 12 binary
		H	Location of the first of a third series of ASCII characters in DF.	6 to 12 binary
		I	Number of ASCII characters following and including location H.	1 to 12 binary

TABLE 2

Character		Function	Values	
5	C O M I D	A	Command Character. Word compressed message.	xx
		B	Language and case identity. Language 1 - upper case Language 1 - mixed case Language 2 - upper case Language 2 - mixed case	01 02 03 04
10 15 20	C O N F	C	Number of code words in the message including the address code word (not including any terminating code word).	3 to 128 binary
		D	Number of 7 bit characters in Command and Control message.	0 to 12
		E	Location of first ASCII character in Data Field DF, for example the number of 7-bit characters from the end of the address code word.	4 to 128 binary
		F	Number of ASCII character following and including location "C" before word coding begins.	1 to 128 binary
		G	Location of the first of a second series of ASCII characters in DF	5 to 12 binary
		H	Number of ASCII characters following and including location F.	1 to 12 binary
		I	Location of the first of a third series of ASCII characters in DF.	6 to 12 binary
		J	Number of ASCII characters following and including location F.	1 to 12 binary

TABLE 3

Character	Function	Values	
5 C O M M I D	A	Command Character. Dictionary A - mixed case Dictionary A - upper case Dictionary B - mixed case Dictionary B - upper case ASCII only	0000001 0000010 0000011 0000100 0001001
	B	Number of 7-bit characters in Control Field.	3 to 12 binary
10 C O N F 20	C	Number of Word Identities from the end of the Control Field to the first ASCII series	0 to 127 binary
	D	Number of ASCII characters in the first series of ASCII characters.	0 to 127 binary
	E	Number of Word Identities in the second series of Word Identities.	0 to 127 binary
	F	Number of ASCII characters in the second series of ASCII characters	0 to 127 binary
	G	Number of Word Identities in the third series of Word Identities.	0 to 127 binary
	H	Number of ASCII characters in the third series of ASCII characters.	0 to 127 binary
	I	Number of Word Identities in the fourth series of Word Identities.	0 to 127 binary
	J	Number of ASCII characters in the fourth series of ASCII characters.	0 to 127 binary
@	Number of code words in the total message excluding the address code word.	2 to 128 bin or 2 to 16384 bin	

25 Comparing Tables 1, 2 and 3 character positions A and B comprise a command character indicating that a word compressed message is following and optionally an indication of the number of characters in the Command and Control Field CCF (Table 3). Thus if a pager determines that the first character is not a command character, it will assume that the appended message is a normal alpha-numeric message and will decode it accordingly.

Table 1 is able to indicate a greater number of locations of, and

numbers of, ASCII characters than are Tables 2 and 3 because in Tables 2 and 3 character position C and @ respectively comprise an indication of the total number of code words in a message in one case (Table 2) including the address code word and in the other case (Table 3) excluding the address code word, whereas this indication is omitted from Table 1.

Since the Control Field CONF has a maximum number of character positions, for example positions C to I in diagram B of Figure 3 which relates to the format of Table 1, this imposes a limit on the number of "islands" of ASCII characters which can be identified. If the message when assembled at the primary station has more than say 4 islands of ASCII characters, the user can either rearrange the message or accept the fact that the final island of ASCII characters extends to the end of the message even though it contains words which could otherwise be sent as a 7-bit character pair.

The Command and Control Field CCF has to obey the following rules:

1. The Command and Control Field must be received without error. If the uncorrectable code words are received during the command and control message the paged message cannot be accepted.

2. All pagers capable of receiving word compressed messages must receive the first ASCII character after the address code word without error when receiving non word compressed (ASCII) messages (that is the first message code word) in order to accept the paged message.

3. If the first 7-bit character of the message after the address code word (and any associated extended format information) is not a command character the pager accepts the message as a conventional alpha-numeric message conforming to the CCIR Radiopaging Code No 1 standard.

4. The Control Field CONF will have a maximum of twelve 7-bit characters. This means that the complete Command and Control Field CCF will have a maximum length of five code words. The Data Field DF will thus contain a string of word identities in which a maximum of four islands of ASCII character strings are permitted.

5. If the message to be sent contains more words that are not in the dictionary than can be conveniently fitted into four islands then words in

the dictionary will be chosen by the encoding computer to be sent in ASCII character format in order to restrict the strings of ASCII characters to four while maintaining maximum possible compression.

5 6. If the Data Field DF is to be concluded with one string of ASCII characters that terminates the message then the number of ASCII characters in this last island need not be included in the Control Field CONF.

7. In the case of Table 3 the value corresponding to C will be set to zero if the message starts with ASCII characters. Further the values corresponding to D to I may be set to zero to extend the effective word or
10 character count of the preceding series.

Rules 1 to 3 apply to the pager and can be summarised by the flow chart shown in Figure 4. Block 32 denotes the pager being energised in its predetermined frame period as required by CCIR Radiopaging Code No 1. Block 34 denotes checking if the received address is one of those assigned
15 to the pager, if it is not (N) the pager is de-energised until the beginning of the next batch. If the address does belong to the pager (Y), the pager remains energised to receive the message concatenated with the address code word which is stored in a buffer store, block 36. A check is made to see if the first ASCII character is correct, block 38, and if it is not (N) then
20 the pager reverts to its de-energised state for the remainder of the batch. If it is correct (Y), then in block 40 a check is made if the first ASCII character is a command character (see Tables 1, 2 and 3) and if the answer is negative (N) then the stored message is decoded as a normal alpha-numeric message, block 42. If the first character is a command character (Y), then
25 in block 44, a check is made to see if the Command and Control Field (CCF) has been received correctly, if not (N), the flow chart reverts to the block 32 and the data in the buffer store is erased, but if it is, the data field is decoded as a compressed message block 46.

30 Referring now to the Data Field DF, the capacity of the ROM based word dictionary within the pager is limited to 16380 words. This limitation results from the addressing capacity within two 7-bit characters which are used to identify the location of a word in the dictionary. The dictionary may

be specialised to a certain technical field but alternatively may be of a more general application. The nature of and limitation in the size of the word dictionary does not affect the message content because the words which are not in the dictionary can be transmitted as ASCII characters. The total system compression ratio will be that achieved by the average message content and not the worst case. As mentioned previously when a ROM dictionary word is decoded it usually includes a space. However, there are some exceptions when the ROM dictionary word relates to punctuation characters such as parenthesis. The number of words which can be stored in the ROM dictionary can be increased by adding suffixes, such as plurals and different tenses, to singular nouns and verbs thus avoiding the need to store the plurals of all the nouns and all the tenses of verbs.

In order to add a suffix it is necessary to delete the space and add the suffix together with a space. In the following examples a space delete character is represented by [#] and a space character by []. Every suffix word or word extension is transmitted by its own two 7-bit word identify which is held in the dictionary as such.

For the addition of word plurals, the following suffixes can be stored:

[#es] and [#s].

In the case of verbs, the suffixes can be:

[#ing] and [#ed].

Punctuation can be represented as follows:

[#)]; [# .]; [#?]; [#'] and [(].

Words not normally held in the dictionary may be constructed by joining together two stored words and deleting the space between them.

Thus:

[Bird] [#] [wood] = Birdwood

[Hay] [#] [ward] = Hayward

Messages which contain a mixture of upper and lower case characters can be handled by using the following rules:

1. The first character of a message is always upper case.
2. The first character of a word following a sentence terminator,

such as a full stop, question mark or exclamation mark, is always upper case.

3. Real names, these are words held in the dictionary with the first character always upper case.

4. Some words are classed as special names (e.g. acronyms) and are held in the dictionary with all characters upper case.

5. When it is necessary to present words held as lower case in the dictionary with the first or all characters in upper case this can be achieved with the Case Identities.

There are three case change Case Identities that can occur within the Data Field DF:

- a. Change to upper case the first character of the next word,
- b. Change to upper case for all following words,
- c. Change to mixed case for all following words.

It is noted that Case Identities will not be transmitted in messages with command characters in the Control Field that specify all characters in the message be upper case. A command character "upper case" overrides Case Identities.

The transmission of the two 7-bit word identity characters in the Data Field DF conforms to the CCIR Radiopaging Code No 1, that is the characters will be transmitted in bit order, least significant bit (LSB) first and in character order, most significant character first, as a message is presented in word order. This is illustrated in Table 4 below in respect of the message "Please call the".

TABLE 4

WORD ORDER	WORD IDENTITIES	
	b7,b6,b5,b4,b3,b2,b1	b7,b6,b5,b4,b3,b2,b1
	Most Sig. Character	Least Sig. Character
5 1	character 1. 7 6 5 4 3 2 1	character 2 [Please_] 14 13 12 11 10 9 8
	10 2	character 3. 21 20 19 18 17 16 15
15 3	character 5. 35 34 33 32 31 30 29	character 6. [the_] 42 41 40 39 38 37 36

In order to illustrate the word compression method in accordance with the present invention the following short message will be considered:

"Please call Fred urgently."

20 If this was encoded as 7-bit ASCII characters including space characters and the full stop it will require 182 bits. On the basis of 20 bits to a code word, such a message will require 10 code words plus an address code word.

25 If it is assumed that "Please", "call", "urgently" and the full stop [#._] are each stored as two 7-bit characters and "Fred+space" are ASCII 7-bit characters then the Data Field DF will be $(4 \times 14) + (5 \times 7)$ bits which equal 91 bits. Additionally, the number of bits in the Command and Control Field (CCF) using Table 1 will be $A+B+C+D+E = 5 \times 7 = 35$. The total number of bits is $91 + 35 = 126$ which corresponds to 7 code words plus an address code word. Three code words are saved compared to an all 7 bit ASCII character message. In this particular example, if "urgent" and "ly" [#ly_] are stored separately the additional 14 bits when added to 126 will still not increase the number of code words required.

Figure 5 illustrates a method by which commonly used phrases or

groups of words may be encoded to save bits. In a sentence "The time is 4 p.m.", the first three words frequently will be used as a group and the words "the", "time" and "is" will be stored at respective locations in the ROM. Instead of sending three address locations totalling 42 bits, a single ROM address for the phrase "The time is" is sent, for example 0001. At memory location 0001, there is stored the memory locations, say 0003, 0004 and 0005 of the respective words "the", "time" and "is" which at the paging receiver are read-out in that order from the ROM. Thus only a 14 bit address location need be transmitted thereby saving 28 bits. Other phrases like "as soon as possible" could be handled in a similar way, although it may be possible to store the abbreviation "asap" as a single item in the ROM.

Compressing the alpha-numeric message data in the information field of a paging message reduces the message length for a given message content and thus increases the capacity of a paging channel and thereby the number of subscribers. Reducing the message length also has the advantages of increasing the message success rate in a given rf environment and enhancing the battery life of the pagers.

Although the error correction and detection capability of the CCIR Radiopaging Code No 1 will be usable in the system in accordance with the present invention, the effect of errors on the compressed words may be more serious so that, for example, if a ROM address cannot be decoded satisfactorily then rather than reproduce a word which may be completely nonsensical, an indication, such as a start, may be displayed to indicate to a user that a non-decodable word has been received.

Many variations of the described embodiments are possible. For example, a dictionary can be divided into say 3 or 4 sections, one section comprising say one thousand of the most frequently used words which are used and the subsequent sections comprising differing degrees of less frequently used words. The most frequently used words may include single alphabetical letters and well known combination of letter such as "ly", "ley", "ph" and "es" and numbers.

If say a dictionary of say one thousand words, letters and numbers is

usable then the dictionary locations can be represented as pairs of 5-bit characters and when a message is encoded if a word is not present in the dictionary section it is encoded letter by letter using pairs of 5-bit characters. Word locations in larger dictionary sections can be represented by pairs of
5 6-bit characters.

Alternatively, ASCII 7-bit characters may be used to represent letters of a word not present in the dictionary section rather than pairs of 5-bit characters. In any event the relevant information required by a receiver to decode a data message is contained in the Command and Control Field, which comprises 7-bit ASCII characters, the first character A (Figure 3)
10 always is used to indicate that a form of message compression is used. Different dictionary sections can be indicated in the CONF field by using non-printable ASCII 7-bit characters.

If an intelligent encoder is used, it can encode a message according to various formats and decide which one gives the best message
15 compression. The Command and Control Field is then generated to contain the required information that a receiver will require to decode the message field.

The system in accordance with the present invention enables message words to be encoded in a transparent, effective and flexible manner which
20 increases the message capacity of a CCIR Radiopaging Code No 1 system beyond that envisaged at its introduction. The present invention can be applied to other digital radiopaging systems using paging codes such as GOLAY and ERMES.

In describing the present invention in the context of a digital paging system, no discussion has been made of sending tone only alert signals, that is address signals only, and of the facility of producing audio, optical or vibrational alert signals at the receiver as they do not form a part of the invention step disclosed herein.
25

From reading the present disclosure, other modifications will be apparent to persons skilled in the art. Such modifications may involve other features which are already known in the design, manufacture and use of
30

alpha-numeric message communication systems and component parts thereof and which may be used instead of or in addition to features already described herein. Although claims have been formulated in this application to particular combinations of features, it should be understood that the scope
5 of the disclosure of the present application also includes any novel feature or any novel combination of features disclosed herein either explicitly or implicitly or any generalisation thereof, whether or not it relates to the same invention as presently claimed in any claim and whether or not it mitigates any or all of the same technical problems as does the present invention. The
10 applicants hereby given notice that new claims may be formulated to such features and/or combinations of such features during the prosecution of the present application or of any further application derived therefrom.

INDUSTRIAL APPLICABILITY

15 Transmission of alpha-numeric messages, such as digital paging messages.

CLAIMS

1. A digital communications system comprising a transmitting means and a receiving means, in which the transmitting means has means for encoding alpha-numeric messages in at least two formats, at least one of which formats is a compressed format, characterised in that a data field of a message is preceded by a command and control field and in that the first character of the command and control field is indicative of whether a compressed format has been used in the data field.
2. A system as claimed in claim 1, characterised in that said first character is an ASCII 7 bit character.
3. A system as claimed in Claim 1, characterised in that said encoding means, when in said compressed format, is adapted to encode alpha-numeric messages in at least two modes which may switch from one mode to another mode and vice versa during encoding of a message and in that the command and control field comprises indications which can be used by a receiving means to switch from one decoding mode to another decoding mode and vice versa in order to recover the message data.
4. A digital communications system comprising a transmitting means and a receiving means, in which the transmitting means has means for encoding alpha-numeric messages in at least two modes which may switch from one mode to the other mode and vice versa during the encoding of a message, characterised in that a data field of a message is preceded by a command and control field comprising indications which can be used by a receiving means to switch from one decoding mode to another decoding mode and vice versa in order to recover the message data.
5. A system as claimed in Claim 2, 3 or 4 characterised in that one encoded mode comprises a first type data structure indicative of at least one spoken language word and in that another encoded mode comprises a second type data structure indicative of an individual alpha character.
6. A system as claimed in Claim 5, characterised in that the first type data structure comprises a data structure indicative of at least one spoken language word and a space character.

7. A system as claimed in Claim 5, characterised in that the receiving means comprises a non-volatile memory storing words at predetermined storage locations and in that the first type data structure comprises pairs of characters identifying storage locations in the memory, and in that when said storage location is interrogated the corresponding at least one spoken language word is read out character by character in the form of the second type data structure.

8. A system as claimed in Claim 5, characterised in that said indications indicate the location of, and number of characters in a series of individual alpha characters in the data field.

9. A system as claimed in Claim 8, characterised in that the number of series of individual alpha characters is limited to a maximum n , and that when there are n series of individual alpha characters, the n th series terminates the data message.

10. A system as claimed in any one of Claims 1 to 4, characterised in that the command and control field includes an indication of the number of code words in a message.

11. A receiving apparatus for use in a communications system as claimed in any one of Claims 1 to 4, comprising means for receiving and recovering the command and control field and the data field, and means for decoding the code words in the data field in accordance with the indications given in the command and control field which are used to enable the decoding of the data field to be compatible with the encoding of the message data.

12. A transmitting apparatus for use in a communications system as claimed in any one of claims 1 to 4, comprising means for encoding alphanumeric messages in at least two formats, at least one of which formats is a compressed format, characterised in that a data field of a message is preceded by a command and control field and in that the first character of the command and control field is indicative of whether a compressed format has been used in the data field.

1/2

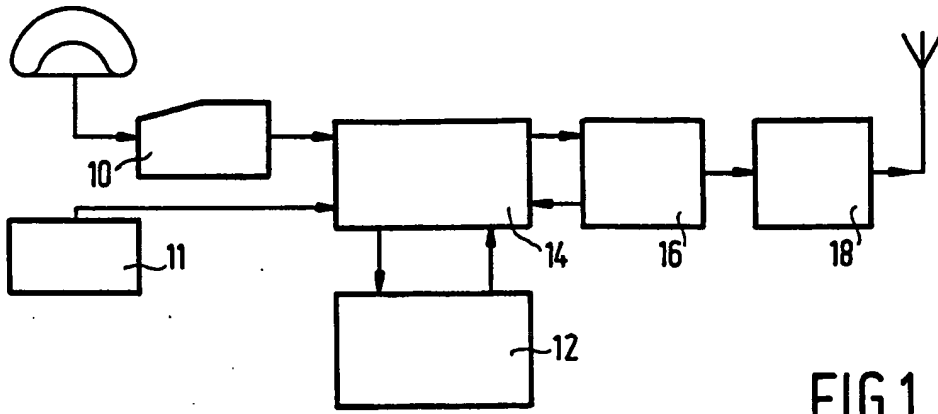


FIG.1

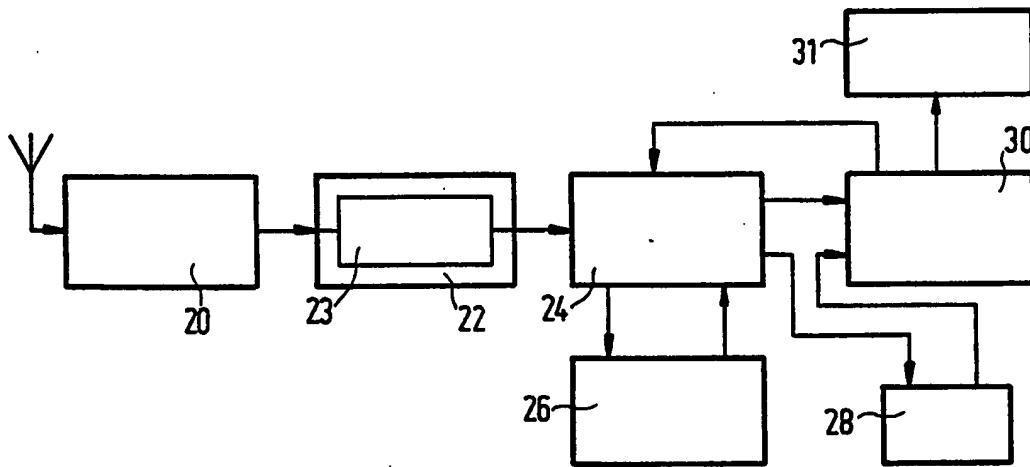


FIG.2

0001	0003 , 0004 , 0005
0002	
0003	THE
0004	TIME
0005	IS
0006	
0007	

FIG.5

2/2

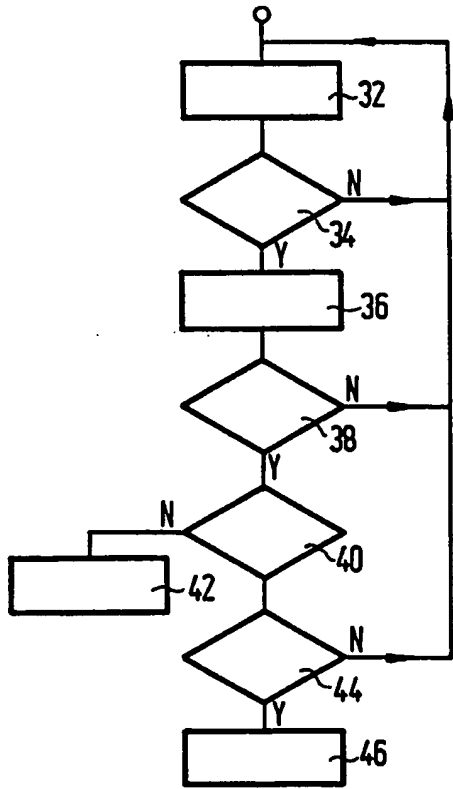
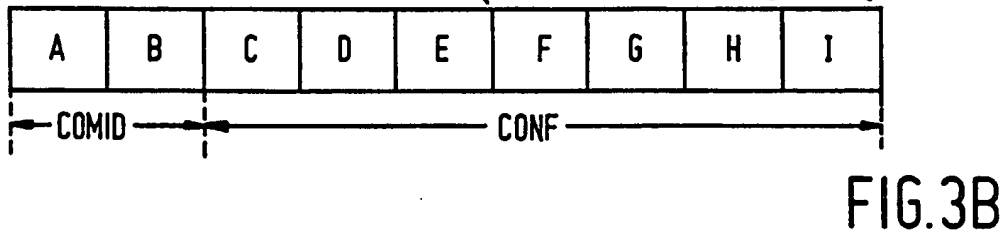
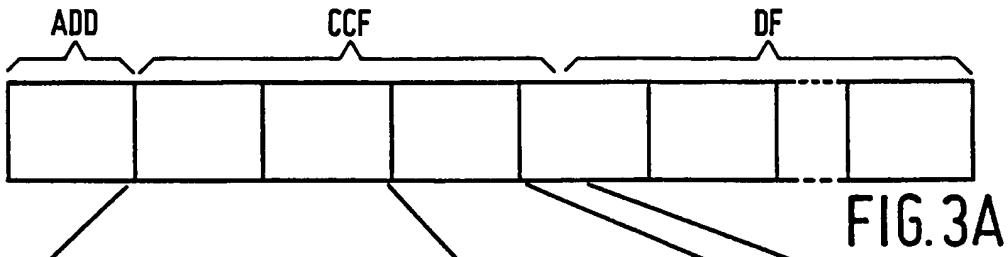


FIG.4

INTERNATIONAL SEARCH REPORT

International application No.

PCT/IB 94/00189

A. CLASSIFICATION OF SUBJECT MATTER		
IPC6: G08B 5/22, H04Q 7/02 According to International Patent Classification (IPC) or to both national classification and IPC		
B. FIELDS SEARCHED		
Minimum documentation searched (classification system followed by classification symbols)		
IPC6: G08B, H04Q		
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Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)		
WPIL, CLAIMS		
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Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	EP, A1, 0536831 (PHILIPS ELECTRONICS UK LIMITED), 14 April 1993 (14.04.93), column 2, line 4 - column 3, line 24 --	1-7,11-12
Y	EP, A2, 0342638 (CASIO COMPUTER COMPANY LIMITED), 23 November 1989 (23.11.89), column 4, line 58 - column 5, line 33; column 7, line 7 - line 18, abstract --	1-7,11-12
A	US, A, 4369443 (F.V. GIALLANZA ET AL), 18 January 1983 (18.01.83), column 2, line 12 - line 42, figure 2, claim 1 -- -----	8-10
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01/10/94

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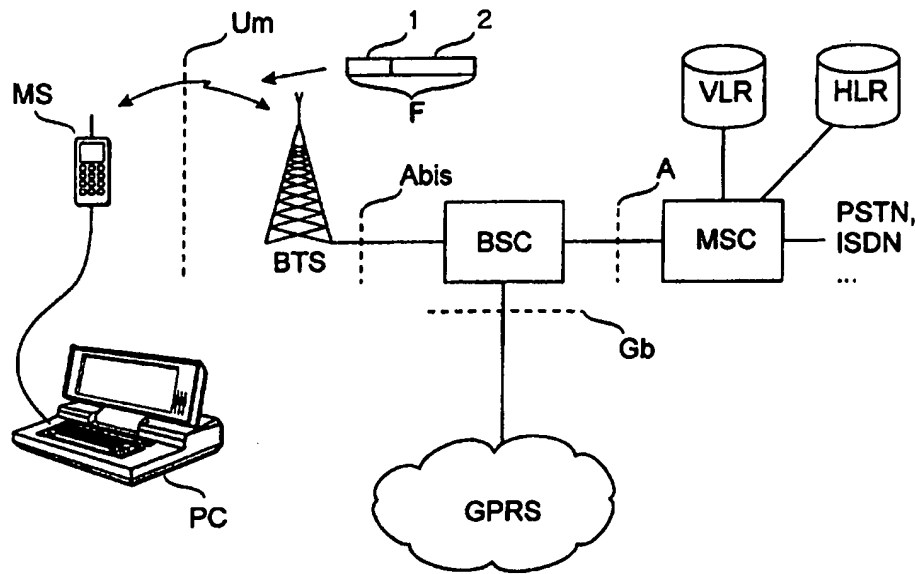
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US-A- 4369443	18/01/83	US-A- 4383257	10/05/83



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<p>(21) International Application Number: PCT/FI97/00345 (22) International Filing Date: 3 June 1997 (03.06.97) (30) Priority Data: 962381 7 June 1996 (07.06.96) FI (71) Applicant (for all designated States except US): NOKIA TELECOMMUNICATIONS OY [FI/FI]; Keilalahdentie 4, FIN-02150 Espoo (FI). (72) Inventor; and (75) Inventor/Applicant (for US only): KARI, Hannu, H. [FI/FI]; Kullervonkuja 9 B 9, FIN-02880 Veikkola (FI). (74) Agent: KOLSTER OY AB; Iso Roobertinkatu 23, P.O. Box 148, FIN-00121 Helsinki (FI).</p>		<p>(81) Designated States: AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CU, CZ, DE, DK, EE, ES, FI, GB, GE, GH, HU, IL, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, TJ, TM, TR, TT, UA, UG, US, UZ, VN, YU, ARIPO patent (GH, KE, LS, MW, SD, SZ, UG), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, ML, MR, NE, SN, TD, TG). Published <i>With international search report. Before the expiration of the time limit for amending the claims and to be republished in the event of the receipt of amendments.</i></p>

(54) Title: DATA COMPRESSION ON A DATA CONNECTION



(57) Abstract

The invention relates to compressing and transmitting data on a connection between two parties in a telecommunication system comprising at least one slow transmission channel, such as the air interface Um of the radio network. The data to be transmitted are assembled into frames (F) comprising a header section (1) and a data section (2). Prior to transmission, at least the header (1) or the data section (2) of at least some of the frames (F) are compressed. The transmitting party has available at least two different compression algorithms and the receiving party has available at least two different decompression algorithms. The transmitting party compresses at least one section (1, 2) of at least some of the frames (F) with at least two different algorithms, and transmits the frame (F) compressed with the algorithm that produced the best compression ratio.

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DATA COMPRESSION ON A DATA CONNECTION

BACKGROUND OF THE INVENTION

The invention relates to improving the capacity of data transfer in a communication system, or more specifically a mobile communication system.

5 Figure 1 shows, from the point of view of the invention, the essential parts of a cellular mobile communication system. Mobile stations (MS) communicate with base transceiver stations (BTS) over an air interface Um. The base stations are controlled by base station controllers (BSC) which are connected to mobile switching centers (MSC). A subsystem under control of a
10 base station controller BSC, including the base stations BTSn it controls, is commonly referred to as a base station subsystem (BSS). The interface between the mobile switching center MSC and the base station subsystem BSS is referred to as an A-interface. The part of the mobile communication system at the MSC side of the A-interface is referred to as a network
15 subsystem (NSS). Correspondingly, the interface between the BSC and the BTS is referred to as an Abis interface. The mobile switching center MSC handles the connecting of incoming and outgoing calls. It performs functions similar to those of an exchange of a public switched telephone network (PSTN). In addition to these, it also performs functions characteristic of mobile
20 communications only, such as subscriber location management, jointly with the subscriber registers VLR and HLR of the network. As an alternative to the circuit switched connection described above, the connection to the mobile station MS may also take place via a packet network GPRS (General Packet Radio Service).

25 One of the growing fields of application for mobile stations is to establish data links in connection with portable computers. Such a computer is represented by the computer PC in Figure 1. The computer PC and the mobile station MS may be separate units or they may form an integrated whole. The data to be transmitted on data links is assembled into frames (F) that typically
30 contain a header section 1 and a data section 2. If an increase occurs in the number and/or use of mobile stations, a bottleneck will be met in the form of the transfer capacity of the air interface Um. The transfer capacity of the air interface may be increased by compressing the data to be transmitted over the air interface. The compression is based on some bit patterns in the data stream
35 being frequent and some occurring only once. The bit patterns which occur frequently may be sent only once as a whole, and later it is possible to send only

a reference to the bit pattern sent earlier. A number of such compression algorithms has been developed, including RLE (Run Length Encoding) and LZ (Lempel-Ziv) with its different variants, JPEG, MPEG etc. Within the scope of this application, compression ratio of an algorithm refers to the ratio between the length of an uncompressed bit string (e.g. a frame) and the length of the bit string compressed with the algorithm in question.

The conventional packet communication described above encounters the problem that data of a specific type may be compressed more efficiently with a particular compression algorithm whereas data of some other type may be compressed more efficiently with another algorithm. Also such bit patterns exist that cannot be compressed with any algorithm, whereby the identifier indicating the algorithm used just adds to the length of the bit string. A further problem with the prior art compression carried out with a fixed algorithm is that it does not offer optimal protection against eavesdropping because the algorithm does not change.

For example, PCT application WO 94/14273 discloses a system for compressing data to be transmitted with a number of different compression means. However, the WO 94/14273 application mainly relates to transmission of video information to several receivers simultaneously. Because the same information is transmitted to several receivers, such a system does not comprise a bottleneck comparable to the air interface of a cellular packet radio network wherein unique information is transmitted between each pair of transmitter and receiver. Also the WO 94/14273 application assumes that the best compression method can be determined by the contents of the transmitted information. This assumption may be correct if it is known before transmission that the information will be video information.

BRIEF SUMMARY OF THE INVENTION

It is consequently the object of the invention to develop a method by means of which the limited capacity of the air interface or another low-speed telecommunication resource may be utilized as efficiently as possible, thereby simultaneously enhancing traffic encryption against unauthorized listening. The objects of the invention are achieved by a method which is characterized by that which is set forth in the independent claims. The preferred embodiments of the invention are set forth in the dependent claims.

The invention is based on the notion that in a general case, when the contents of the data to be transmitted may be arbitrary, the most efficient

compression algorithm can be established only experimentally. Because of this, the data to be transmitted are, according to the invention, compressed with a number of different algorithms, and the best of the compression results is transmitted to the receiving party. The invention is further based on the view that
5 it is worth while in a telecommunication system which contains a slow telecommunication resource, such as an air interface limiting the capacity, to carry out a lot of extra computation in a location where that is cheap and where capacity enlargements may result from such an action.

The method according to the invention utilises the bandwidth of the
10 bottleneck (such as the air interface in a telecommunication system) in the most effective manner possible because the compression algorithm is selected on the basis of actual testing between different algorithms. The method is applicable to several types of telecommunication systems. The method according to the invention may be used adaptively so that the transmitting party learns to apply a
15 specific algorithm on a specific connection. A further advantage of the inventive method is provided by improvements regarding the protection of telecommunication as an eavesdropper will have difficulties in interpreting a message whose compression algorithm may change in the middle of the connection, even between successive packets.

20 BRIEF SUMMARY OF THE FIGURES

In the following, the invention will be described in closer detail in connection with its preferred embodiments and with reference to the accompanying drawings in which:

Figure 1 shows the parts of the mobile communication network that
25 are significant to the invention,

Figures 2A and 2B illustrate the steps of the inventive compression.

DETAILED DESCRIPTION OF THE INVENTION

With reference to Figure 1, the invention will be described in an environment in which there is a mobile station MS and a computer PC
30 connected thereto at the first end of the transmission channel, and at the other end a network subsystem NSS of which is shown a base station BTS, a base station controller BSC and a mobile switching center MSC. To keep the description simple, it is assumed that the compression and decompression algorithm according to the invention is implemented in the MS, but it may equally
35 well be implemented in the PC. The preferred embodiment of the invention

relates to enhancing the traffic that takes place over the air interface Um, but in place of the air interface there may also be some other transmission channel having a limited capacity.

In its simplest form, the invention may be applied so that a fixed set
5 of compression and decompression algorithms are implemented in the mobile station MS and the network subsystem NSS. This set of algorithms is the same in the MS and the NSS. The transmitting party compresses each frame F with each algorithm it knows, and selects the algorithm that yields the best compression ratio. In addition, the transmitting party inserts an information field
10 in the frame to be transmitted, indicating which algorithm the data have been compressed with. On the basis of this information field, the receiving party will know which algorithm to use in order to decompress the data.

This simple implementation has at least two problems. Firstly, when using different equipments, the transmitting and receiving parties do not know in
15 advance which algorithms have been installed at the counterpart. In addition, it is not possible to add new algorithms in the system without simultaneous updating of all the equipments in the system. Secondly, compressing each frame with all possible algorithms considerably increases requirements for computation capacity. The first of the problems may be solved by a negotiation
20 protocol between the transmitting and receiving parties. The latter problem may be solved by optimizing the compression procedure, e.g. by making it adaptive.

In a mobile communication system, it could in principle be speculated that the negotiation for finding out the capabilities of the parties is unnecessary and that the features of each mobile station could be stored in a home location
25 register or a similar equipment register. This arrangement would involve a lot of problems, the biggest of which probably having to do with the GSM type of systems maintaining the subscriber location by means of SIMs (Subscriber Identity Modules). If a SIM is shifted to another, for example a rented, terminal equipment, the system will assume that the second terminal equipment has the
30 same capabilities as the original one. This assumption is not necessarily correct.

For this reason, it is better to identify the capabilities of the transmitting and receiving parties at the beginning of the communication. In mobile communication systems, the negotiation must be carried out anew when the mobile station roams to a new area. A suitable and simple negotiation
35 protocol is, for example, such that when taking new algorithms in use they are issued a running number, and at the beginning of the connection or in

association with a location area change the calling equipment transmits an inquiry to the called equipment, concerning the available algorithms, to which the called equipment responds by sending a bitmap in which a bit set at an algorithm means that the algorithm is available. According to an alternative negotiation protocol, the calling equipment transmits a short test message compressed with all the algorithms being tested, and the called equipment responds with an affirmative acknowledgment if it is capable of decompressing the message, and if it is not, with a negative acknowledgment. If there is installed, for each compression algorithm, both a compressing and a decompressing algorithm in the transmitting party as well as the receiving party, the common capabilities of the transmitting party and the receiving party may be identified so that e.g. the calling equipment identifies the capabilities of the called equipment. It is unnecessary for the called equipment to identify the capabilities of the calling equipment as the latter cannot have capabilities other than those it has already inquired of the called equipment.

On the other hand, it is mathematically considerably simpler to decompress a packet than to compress it. This holds particularly well true regarding compression of live video images and fractal algorithms, especially. Consequently, it could also be conceivable to implement e.g. in mobile stations a larger number of algorithms for decompressing a packet than for compressing it. In such a case, the negotiation protocol may be supplemented so that also the called equipment identifies the capabilities of the calling equipment.

For an efficient compression of data, the compression must take place prior to encryption and splitting the data into frames. According to an embodiment of the invention, the header sections 1 of the frames F are compressed with a specific type of algorithm and the data sections 2 of the frames F are compressed with at least two different algorithms of which the one is selected that provides the best compression ratio. The header section is compressed with an algorithm optimized for this purpose, said algorithm being substantially the same from one frame to another.

For example, when transmitting user-entered characters in TCP/IP frames in a Telnet connection, each character entered is normally sent in its own frame. This is because the user awaits a relatively quick response, after no more than approximately 0.2 seconds from entering the character. On the other hand, the transmitting program does not know at which moment the next

entering is to take place, which means that each character has to be sent as a separate frame consisting of 40 bytes of header and 1 byte of data. The reference [1] discloses a method for compressing the header sections of TCP/IP frames into 3 - 5 bytes. The method according to the reference [1] utilizes the fact that in the header sections of TCP/IP frames a lot of information is sent that the receiving party is able to form by itself on the basis of the header section in the previous frame. Similar redundancy is present e.g. in header sections of ATM cells.

The compression algorithm employed may be indicated to the receiving party for example by transmitting, in each compressed frame F, an identifier indicative of the compression algorithm used. Alternatively, the receiving party may be sent information on the change in the compression algorithm. This information may be a separate frame, or a field or a peculiar bit pattern inserted to a frame normally transmitted.

To utilize the air interface as efficiently as possible, it is advantageous to carry out the compression procedure during those moments when the transmitting party for a reason or another may not transmit. In the GSM system, for example, the data are transmitted over the air interface as bursts in TDMA timeslots. Between the bursts, the transmitting party can perform the necessary computations and thus utilize its computation capacity that it would otherwise waste just waiting for the next timeslot. At the allocated timeslot, it is possible to interrupt the compression and to transmit the frame compressed with the algorithm that up to that point has produced the best result.

The following discusses various options for reducing the computation requirements. The compression procedure can be optimized by for example compressing a frame F with all the algorithms used, i.e. those that were in the negotiations found to be supported by both parties.

The frame F that is compressed with all the algorithms employed is preferably the first one representing a specific type of data, i.e. when the data type changes, the testing with the algorithms may be started from the beginning. The subsequent frames are each first compressed with the algorithm that at the previous frame yielded the best result. The other compression algorithms are not necessarily completed. Their processing may be interrupted immediately as the length of the compressed frame obtains the length of the algorithm compressed with the optimal algorithm.

According to another embodiment, a sliding average of the compression ratio is maintained for each algorithm with which a frame has been compressed. The frames are compressed with different algorithms in an order determined by the compressing ratio obtained with the algorithms. If the compression ratio of a frame with some algorithm exceeds a predetermined threshold value, the frame in question will not be compressed with the other algorithms. The predetermined threshold value may be a fixed multiplier, for example a number between 3 - 6. Alternatively, the threshold value may be a specific percentage, for example 80 - 90% of the compression ratio achieved with the best algorithm up to that point.

If the time available is not sufficient for compressing each frame with each algorithm, the individual frames may be compressed for example with those 1 - 3 algorithms that up to that point show the best sliding average for the compression ratio. The remaining time - e.g. when waiting for the transmission turn - is spent on testing the remaining algorithms one at a time. This is illustrated by the following example. It is assumed that there are 7 different algorithms available, and when waiting for each transmission timeslot there is time to test four of them. In such a case, at each timeslot, compression may be carried out with those two algorithms that up to that point have yielded the best result. Of the other five algorithms, two are tested at each timeslot.

Encryption may further be improved if the algorithms are during the negotiation numbered in an order determined on the basis of a pseudorandom number known only to the parties. The same outcome may be reached by changing the identifiers of the algorithms at a specific algorithm during the connection. It is advantageous to carry out the negotiation in an encrypted form. With these methods the advantage is obtained that the compression algorithm identifiers transmitted along with the frames are not unequivocal to eavesdroppers.

Figures 2A and 2B illustrate some of the steps in the compression method of the invention. At step 200, the compression routine receives the data to be transmitted and compressed from the application producing them. Step 205 illustrates the operations in which time supervision is set to ensure that the data are transmitted on time, for example in the next transmission timeslot. At step 210, the header 1 of the frame F is compressed with an algorithm optimized for this purpose. At step 215, the data section 2 is

compressed by a few, in this case three, of the best algorithms up to that point. In association with the compression, a parameter is maintained for each algorithm, illustrating its efficiency, such a parameter being for example the sliding average of the compression ratio. At step 220, the data section 2 is
5 compressed with as many of the remaining algorithms as possible within the time supervision, in this example with two algorithms. The identifiers of the algorithms tested at this step are stored in memory, and next time at step 220, other algorithms are tested. The testing may be begun with the algorithm that follows the one tested last. When the time supervision 225 expires, for
10 example when a transmission turn approaches, the order from best to worst of the algorithms is updated at step 230, and the data are transmitted at step 235 compressed with the algorithm that produced the best result within the time available.

The preferred embodiment of the invention relates to compressing
15 data on a communication link and particularly in a packet radio network. The invention is applicable for use in other types of telecommunication systems and in data processing systems which have at least one distinct bottleneck restricting the capacity of the entire system. Therefore, it is obvious for a person skilled in the art that upon advancements in technology the basic idea
20 of the invention may be implemented in many ways. The invention and its embodiments are consequently not restricted to the examples described above but they may vary within the scope of the claims.

References:

- 25 [1] V. Jacobson: Compressing TCP/IP headers for low-speed serial links (Request For Comments 1144).

CLAIMS

1. A method for compressing and transmitting data on a connection between two parties in a telecommunication system comprising at least one
5 slow transmission channel (Um), the method comprising:
assembling the data to be transmitted into frames (F) which contain at least a header section (1) and a data section (2), and
compressing at least one section (1, 2) of at least some of the frames (F) prior to transmission,
10 making at least two different compression algorithms available to the transmitting party,
making at least two different decompression algorithms available to the receiving party,
characterized in that the transmitting party:
15 compresses at least one section (1, 2) of at least some of the frames (F) with at least two different compression algorithms;
selects the compression algorithm that yielded the best compression ratio; and
transmits the frame (F) over the slow transmission channel (Um) to
20 the receiving party, compressed with said selected compression algorithm.
2. A method as claimed in claim 1, **characterized** in that the parties negotiate the compression algorithms to be used on the connection at least at the beginning of the connection.
3. A method as claimed in claim 2, **characterized** by the first
25 party sending to the second party an inquiry concerning the available algorithms, to which the second party responds by sending a list containing information on the algorithms available to the second party.
4. A method as claimed in claim 2, **characterized** by the second party selecting the algorithms that both the parties support from the list
30 sent by the first party.
5. A method as claimed in claim 2, **characterized** by the second party transmitting a list of the algorithms available to it regardless of which algorithms the first party has available.
6. A method as claimed in claim 2, **characterized** by the first
35 party transmitting a brief test message compressed separately with each algorithm being tested, and the second party responding with an affirmative ac-

knowledge if it is capable of decompressing the message, and if not, with a negative acknowledgment.

7. A method as claimed in any one of claims 2 - 6, **characterized** in that both parties have a decompression algorithm available for
5 substantially each compression algorithm.

8. A method as claimed in any one of claims 2 - 6, **characterized** in that at least one of the parties may have available a decompression algorithm without a corresponding compression algorithm or vice versa, and that the parties negotiate separately the compression and decompression
10 algorithms available to them.

9. A method as claimed in any one of claims 2 - 8, **characterized** in that the negotiation between the parties is transmitted on an encrypted channel.

10. A method as claimed in any one of claims 2 - 9, **characterized** in that the identifiers of the compression algorithms are changed
15 between successive connections and/or during one connection.

11. A method as claimed in any one of claims 1 - 10, **characterized** by
compressing the header sections (1) of the frames (F) with an algo-
20 rithm which is substantially the same between two successive frames (F), and
compressing the data sections (2) of the frames (F) with at least two
different algorithms of which the one is selected that yields the best compression result.

12. A method as claimed in any one of claims 1 - 11, **characterized** by transmitting, with each compressed frame (F), an identifier indicative of the compression algorithm used.
25

13. A method as claimed in any one of claims 1 - 11, **characterized** in that when the compression algorithm changes the transmitting party separately transmits information on the change to the receiving party.
30

14. A method as claimed in any one of the previous claims, **characterized** by
compressing a frame (F), which is advantageously the first one representing a specific type of data, with substantially all the algorithms known to both parties,
35
compressing the subsequent frames (F) first with the algorithm that at the previous frame (F) produced the best result,

discontinuing to carry out the other algorithms if the length of the frame (F) compressed with the algorithm in question exceeds the length of the frame (F) compressed with up to that point the best algorithm.

15 **characterized** by the transmitting party being assigned a restricted time for the compression, such as the time between two successive transmit turns in time division multiple access systems.

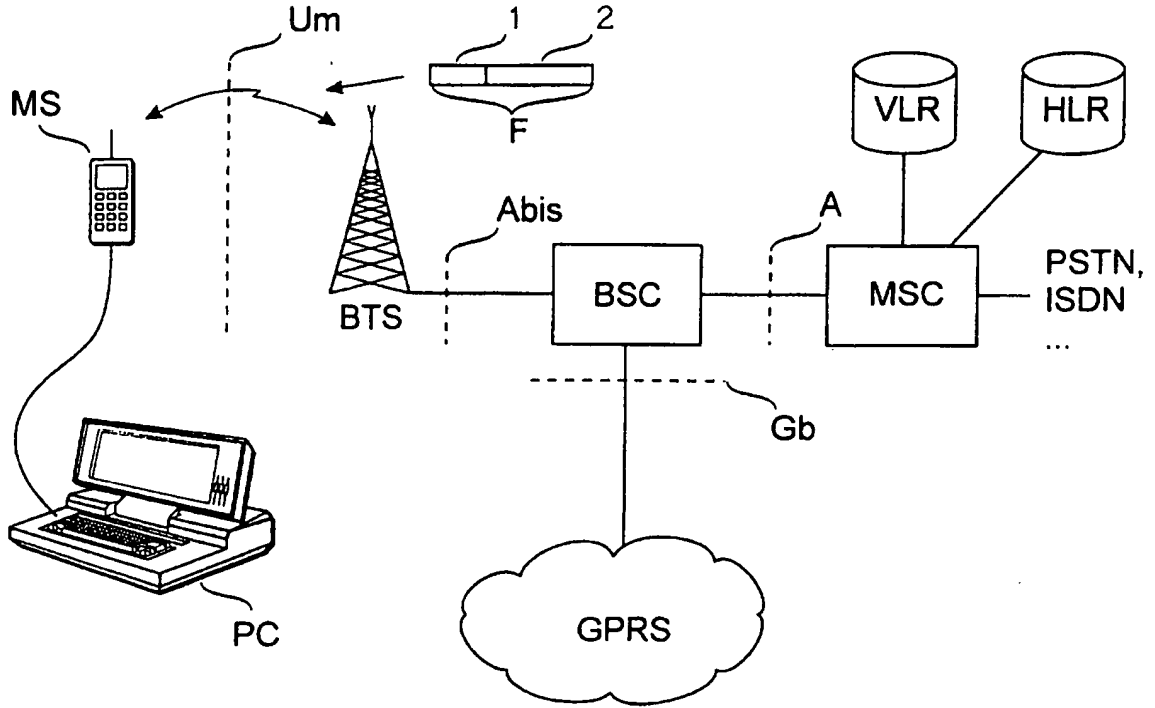
16. A method as claimed in claim 15, **characterized** in that at the end of the restricted time the transmitting party discontinues testing the
10 compression algorithms and transmits the frame (F) compressed with the algorithm that up to that point has yielded the best compression result.

17. A method as claimed in claim 16, **characterized** by
maintaining, for the different compression algorithms, a parameter
indicating efficiency, advantageously a sliding average of the compression ra-
15 tio,

compressing each frame (F) or a section (1, 2) thereof with a few, advantageously 1 - 3 of the best compression algorithms up to that point, in an order determined by the parameter indicating efficiency, and

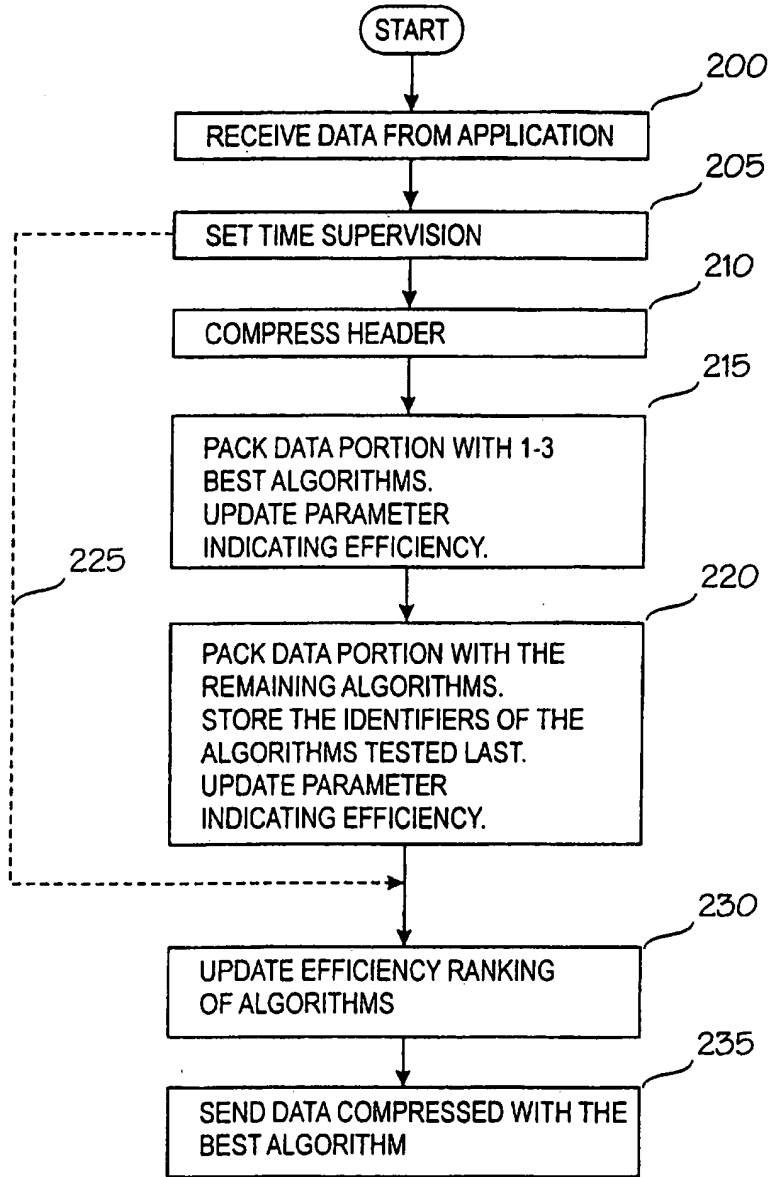
20 testing, in the remaining part of the restricted time, the remaining algorithms alternately so that at successive frames (F) different algorithms are tested.

Fig. 1



2/2

Fig. 2A



- ALGORITHM 1
- ALGORITHM 2
- ALGORITHM 3
-
- ALGORITHM 4
- ALGORITHM 5
- ALGORITHM 6
- ALGORITHM 7
- ALGORITHM 8
- ALGORITHM 9
- ALGORITHM 10
- ALGORITHM 11
- ALGORITHM 12

Fig. 2B

INTERNATIONAL SEARCH REPORT

International application No.
PCT/FI 97/00345

A. CLASSIFICATION OF SUBJECT MATTER

IPC6: H04L 12/56, H04Q 7/30, H04Q 7/32
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC6: H04L, H04Q

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

SE,DK,FI,NO classes as above

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EDOC, WPIL, JAPIO

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	WO 9414273 A1 (VOXON INTERNATIONAL PTY. LIMITED), 23 June 1994 (23.06.94), page 3, line 12 - line 14; page 5, line 6 - line 9; page 12, line 13 - line 28, page 15, line 18-27, page 18 line 26 - page 19, line 14.	1,11-13
Y		2-5,7-10
A		6,14-17
	--	
Y	US 5452287 A (STEPHEN DICECCO), 19 Sept 1995 (19.09.95), column 2, line 51 - column 3, line 2, abstract	2-5,7-10
A		6,11-17
	--	

 Further documents are listed in the continuation of Box C.
 See patent family annex.

- * Special categories of cited documents:
- "A" document defining the general state of the art which is not considered to be of particular relevance
- "B" earlier document but published on or after the international filing date
- "L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
- "O" document referring to an oral disclosure, use, exhibition or other means
- "P" document published prior to the international filing date but later than the priority date claimed
- "T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
- "X" document of particular relevance: the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
- "Y" document of particular relevance: the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
- "&" document member of the same patent family

Date of the actual completion of the international search

3 November 1997

Date of mailing of the international search report

05-11-1997

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INTERNATIONAL SEARCH REPORT

International application No.

PCT/FI 97/00345

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 5396228 A (MASOOD GARAH), 7 March 1995 (07.03.95), abstract --	1-17
A	EP 0595406 A1 (PHILIPS ELECTRONICS N.V.), 4 May 1994 (04.05.94), column 1, line 1 - line 16; column 1, line 52 - column 2, line 14 --	1-17
A	WO 9502873 A1 (PHILIPS ELECTRONICS N.V.), 26 January 1995 (26.01.95), page 1, line 7 - line 11; page 3, line 25 - page 4, line 10 -- -----	1-17

INTERNATIONAL SEARCH REPORT

International application No.

PCT/FI97/00345

Box I Observations where certain claims were found unsearchable (Continuation of Item 1 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

- 1. Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

- 2. Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

- 3. Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box II Observations where unity of invention is lacking (Continuation of Item 2 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

See next sheet!

- 1. As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.
- 2. As all searchable claims could be searched without effort justifying an additional fee, this Authority did not invite payment of any additional fee.
- 3. As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

- 4. No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

- The additional search fees were accompanied by the applicant's protest.
- No protest accompanied the payment of additional search fees.

The technical feature common to all of claims 1 to 17 is the negotiation of compression algorithms to be used. This technical feature is expressed in claim 1.

However, the search has revealed that this technical feature is not novel since it is disclosed in patent application WO, 94 14273, A1, (VOXSON INTERNATIONAL PTY. LIMITED), 23 June 1994 (23.06.94), page 12, lines 13 - 28 and page 18, line 26 - page 19, line 14.

Consequently the common feature is not a special technical feature within the meaning of PCT Rule 13.2 since it makes no contribution over the prior art.

Claims 2 - 13 are directed to a method for negotiating which compression algorithm to use and claims 14 - 17 are directed to a method for data compression. Consequently it appears that, a posteriori, claims 2 - 13 and 14 - 17 do not comply with the requirement of unity of invention.

INTERNATIONAL SEARCH REPORT
Information on patent family members

01/10/97

International application No.
PCT/FI 97/00345

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
WO 9414273 A1	23/06/94	AU 5804994 A	04/07/94
		CA 2151581 A	23/06/94
		CN 1092578 A	21/09/94
		EP 0679312 A	02/11/95
		JP 8505015 T	28/05/96
		NZ 259281 A	24/04/97
		ZA 9309454 A	07/09/94
US 5452287 A	19/09/95	AU 7557894 A	10/04/95
		CA 2148914 A	30/03/95
		EP 0671087 A	13/09/95
		WO 9508880 A	30/03/95
US 5396228 A	07/03/95	NONE	
EP 0595406 A1	04/05/94	AU 663234 B	28/09/95
		AU 5030993 A	12/05/94
		JP 6244887 A	02/09/94
WO 9502873 A1	26/01/95	CN 1112378 A	22/11/95
		EP 0659292 A	28/06/95
		JP 8501673 T	20/02/96



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8011-15

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants : James J. Fallon et al.

Application No.: 09/776,267

Confirm. No. : 9730

Filing Date : February 2, 2001

Title : SYSTEMS AND METHODS FOR ACCELERATED LOADING
OF OPERATING SYSTEMS AND APPLICATION
PROGRAMS

Art Unit : 2115

Examiner : Suresh Suryawanshi

Commissioner for Patents
P.O. Box 1450 New York, NY 10020
Alexandria, VA 22313-1450 August 14, 2006

REPLY TO OFFICE ACTION

This is in response to the Office Action mailed February 14, 2006. A three-month extension of time is applicable hereto. Applicants hereby amend the application as follows.

Amendments to the Claims begin on page 2 of this paper; and

Arguments/Remarks being on page 12 of this paper.

08/17/2006 GWORDDF1 00000043 061075 09776267

01 FC:2201 100.00 DA
02 FC:2202 475.00 DA

Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of the Claims

1. (Currently Amended) A method for providing accelerated loading of an operating system, comprising the steps of:

maintaining a list of boot data used for booting a computer system;

initializing a central processing unit of the computer system;

preloading the boot data into a cache memory prior to completion of initialization of the central processing unit of the computer system, wherein preloading the boot data comprises accessing compressed boot data from a boot device; and

servicing requests for boot data from the computer system using the preloaded boot data after completion of initialization of the central processing unit of the computer system, wherein servicing requests comprises accessing compressed boot data from the cache and decompressing the compressed boot data at a rate that increases the effective access rate of the cache.

2. (Original) The method of claim 1, wherein the boot data comprises program code associated with one of an operating

system of the computer system, an application program, and a combination thereof.

3. (Canceled)

4. (Currently Amended) The method of claim 1, wherein the preloading ~~the method steps are~~ is performed by a data storage controller connected to the boot device.

5. (Currently Amended) The method of claim 1, further comprising ~~the step of~~ updating the list of boot data ~~during the boot process.~~

6. (Original) The method of claim 5, wherein the step of updating comprises adding to the list any boot data requested by the computer system not previously stored in the list.

7. (Original) The method of claim 5, wherein the step of updating comprises removing from the list any boot data previously stored in the list and not requested by the computer system.

8-12. (Cancelled)

13. (Currently Amended) A system boot device controller for providing accelerated loading of an operating system of a host system system, ~~the boot device controller~~ comprising:

~~a digital signal processor (DSP) or controller comprising a data compression engine (DCE) for compressing boot data stored to a boot device and for decompressing compressed boot data retrieved from the boot device;~~

~~a programmable volatile logic device, wherein the programmable volatile logic device is programmed by the DSP or controller prior to completion of initialization of a central processing unit of the host system, to (i) instantiate a first interface for operatively interfacing the boot device controller to the boot device and to (ii) instantiate a second interface for operatively interfacing the boot device controller to the host system;~~

a cache memory device; and

a non-volatile memory device, for storing logic code associated with the DSP or controller, ~~the first interface and the second interface~~, wherein the logic code comprises instructions executable by the DSP or controller for maintaining a list of boot data used for booting the host system, for preloading the compressed boot data into the cache memory device prior to completion of initialization of the central processing unit of the host system, and for decompressing the preloaded

compressed boot data, at a rate that increases the effective access rate of the cache, to service requests for boot data from the host system after completion of initialization of the central processing unit of the host system.

14. (Canceled)

15. (Currently Amended) The ~~boot device controller~~ system of claim 13, wherein the logic code in the non-volatile memory device further comprises program instructions executable by the DSP or controller for maintaining a list of application data associated with an application program; preloading the application data upon launching the application program, and servicing requests for the application data from the host system using the preloaded application data.

16. (Canceled)

17. (Previously presented) The method of claim 1, further comprising:

maintaining a list of application data associated with an application program;

preloading the application data into the cache memory prior to completion of initialization of the central processing unit

of the computer system, wherein preloading the application data comprises accessing compressed application data from a boot device; and

servicing requests for application data from the computer system using the preloaded application data after completion of initialization of the central processing unit of the computer system, wherein servicing requests comprises accessing compressed application data from the cache and decompressing the compressed application data.

18. (New) The method of claim 1, further comprising a data compression engine for compressing, wherein the compressing provides the compressed boot data and the data compression engine provides the compressed boot data to the boot device.

19. (New) The method of claim 1, wherein the decompressing is provided by a data compression engine.

20. (New) The method of claim 1, further comprising a data compression engine for compressing, wherein the compressing provides the compressed boot data, the data compression engine provides the compressed boot data to the boot device, and the decompressing is provided by the data compression engine.

21. (New) The method of claim 1, wherein the compressed boot data is accessed via direct memory access.

22. (New) The method of claim 1, wherein Huffman encoding is utilized to provide the compressed boot data.

23. (New) The method of claim 1, wherein Lempel-Ziv encoding is utilized to provide the compressed boot data.

24. (New) The method of claim 1, wherein a plurality of encoders are utilized to provide the compressed boot data.

25. (New) The method of claim 1, wherein a plurality of encoders in a parallel configuration are utilized to provide the compressed boot data.

26. (New) The system of claim 13, wherein Huffman encoding is utilized to provide the compressed boot data.

27. (New) The system of claim 13, wherein Lempel-Ziv encoding is utilized to provide the compressed boot data.

28. (New) The system of claim 13, wherein a plurality of encoders are utilized to provide the compressed boot data.

29. (New) The system of claim 13, wherein a plurality of encoders in a parallel configuration are utilized to provide the compressed boot data.

30. (New) A method comprising:

maintaining a list of boot data used for booting a computer system;

initializing a central processing unit of the computer system;

preloading boot data in compressed form, based on the list of boot data, from a boot device into a cache memory prior to completion of initialization of the central processing unit;

servicing requests for boot data from the computer system using the preloaded compressed boot data after completion of initialization of the central processing unit, wherein servicing requests comprises accessing the compressed boot data from the cache and decompressing the compressed boot data with a data compression engine and the data compression engine being operable to compress additional boot data and store the additional compressed boot data to the boot device.

31. (New) The method of claim 30, wherein Huffman encoding is utilized by the data compression engine to compress the additional boot data.

32. (New) The method of claim 30, wherein Lempel-Ziv is utilized by the data compression engine to compress the additional boot data

33. (New) The method of claim 30, wherein a plurality of encoders are utilized by the data compression engine to compress the additional boot data.

34. (New) The method of claim 30, wherein a plurality of encoders in a parallel configuration are utilized by the data compression engine to compress the additional boot data.

35. (New) A system comprising:
a boot device;
a processor;
cache memory; and
non-volatile memory for storing logic code for use by the processor, the logic code being used for:

maintaining a list associated with boot data, wherein the boot data is used in booting a first system;

preloading compressed boot data associated to the list into the cache memory prior to completion of initialization of a central processing unit of the first system; and

servicing requests for the compressed boot data from the first system after completion of initialization of the central processing unit; and

a data compression engine for decompressing the compressed boot data accessed from the cache memory for use in responding to the servicing requests and for compressing additional boot data and storing the additional compressed boot data to the boot device.

36. (New) The system of claim 35, wherein Huffman encoding is utilized by the data compression engine to compress the additional boot data.

37. (New) The system of claim 35, wherein Lempel-Ziv is utilized by the data compression engine to compress the additional boot data

38. (New) The system of claim 35, wherein a plurality of encoders are utilized by the data compression engine to compress the additional boot data.

39. (New) The system of claim 35, wherein a plurality of encoders in a parallel configuration are utilized by the data compression engine to compress the additional boot data.

ARGUMENTS/REMARKS

Summary of Office Action

The drawings were objected to for lacking formal drawings.

Claims 1-2, 4-7, 9, 13, and 15 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Kroeker et al. U.S. Patent No. 6,073,232 (hereinafter "Kroeker") in view of Stewart U.S. Patent No. 6,539,456 (hereinafter "Stewart") and further in view of Esfahani et al. U.S. Patent No. 6,434,695 (hereinafter "Esfahani").

Summary of Applicant's Amendments

Applicants have amended claims 1 and 13 solely to expedite prosecution.

Applicants have amended claims 4, 5, and 15 in order to more particularly point out and distinctly claim the subject matter that applicant regards as the invention.

Applicants have cancelled claim 9 solely to expedite prosecution.

Applicants have added new claims 18-39 in order to more particularly point out and distinctly claim the subject matter that applicant regards as the invention.

Applicants reserve the right to claim any subject matter lost by the above amendments in a divisional or continuation application.

Applicant's Reply to the Drawing Objection

The drawings were objected to for lacking formal drawings. The Examiner stated that when "the application is allowed, applicant will be required to submit new formal drawings" (Office Action, page 2). Applicant will file formal drawings when the application is allowed.

Applicant's Reply to the 35 U.S.C. § 103(a) Rejections

The Examiner stated that:

"Kroeker and Stewart do not disclose ... accessing compressed boot data and decompressing the compressed boot data. However, Esfahani ... [discusses] loading a compressed boot data into a RAM cache and then the boot data is decompressed and executed."
(Office Action, page 5).

Claims 1 and 13 have been amended solely to expedite prosecution. Claims 1 and 13 include decompressing the compressed boot data at a rate that effectively increases the data access rate of the cache.

None of the prior art, used either alone or in combination, shows or suggests a decompression process that is able to effectively increases the data access rate of

the cache. The mere discussion of decompression in no way suggests decompression operable to effectively increase the data access rate of the cache.

For at least the above reasons, applicants respectfully request that the Examiner's rejection of claim 13 under 35 U.S.C. § 103(a), and any claims dependent therefrom, be withdrawn.

New Claims 18-25

As shown above, claim 1 is patentable. Claims 18-25 depend from claim 1. Accordingly, applicants respectfully submit that claims 18-25 are patentable because claims 18-25 depend from claim 1.

New Claims 26-29

As shown above, claim 13 is patentable. Claims 26-29 depend from claim 13. Accordingly, applicants respectfully submit that claims 26-29 are patentable because claims 26-29 depend from claim 13.

New Claims 30-34 and 35-39

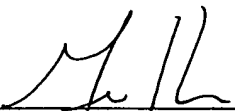
New claims 30 and 35 include a data compression engine for compressing additional boot data stored to a boot device and decompressing compressed boot data retrieved from the cache.

None of the prior art, used either alone or in combination, shows or suggests a data compression engine for compressing additional boot data stored to a boot device and decompressing compressed boot data retrieved from the cache. Claims 31-34 and 36-39 are patentable because claims 31-34 and 36-39 depend from patentable claims 30 and 35, respectively.

Conclusion

In light of the foregoing, applicant respectfully submits that this application, including the pending claims, is in condition for allowance. A favorable action is respectfully requested.

Respectfully submitted,



Jeffrey D. Mullen

(Reg. No. 52,056)

Agent for Applicants

Submitted under 37 C.F.R. § 1.34

Fish & Neave IP Group

Ropes & Gray

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1251 Avenue of the Americas

New York, NY 10020

(212) 596-9000

08-66-06

TFU 2157



8011-15

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants : James J. Fallon et al.
 Application No. : 09/776,267
 Confirm. No. : 9730
 Filing Date : February 2, 2001
 Title : SYSTEMS AND METHODS FOR ACCELERATED LOADING
 OF OPERATING SYSTEMS AND APPLICATION
 PROGRAMS
 Art Unit : 2115
 Examiner : Suresh Suryawanshi

Commissioner for Patents
 P.O. Box 1450
 Alexandria, VA 22313-1450

New York, NY 10020
 August 14, 2006

TRANSMITTAL LETTER

Sir:

Transmitted herewith to be filed in the above-identified
 patent application is a:

Reply to an Office Action.

FEE FOR ADDITIONAL CLAIMS

A fee for additional claims is not required.

A fee for additional claims is required.

Express Mail: EV669671832US

The additional fee has been calculated as shown below:

	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PAID FOR		PRESENT PREVIOUSLY		RATE	ADD'L FEES
TOTAL CLAIMS	39	-	20	*	= 19	X	\$25 =	\$475.00
INDEPENDENT CLAIMS	4	-	3	**	= 1	X	\$100 =	\$100.00
FIRST PRESENTATION OF A MULTIPLE DEPENDENT CLAIM						+	\$180 =	\$000.00
							TOTAL	<u>\$575.00</u>

* If less than 20, insert 20.

** If less than 3, insert 3.

[] A check in the amount of \$0.00 in payment of the filing fee is transmitted herewith.

[X] Please charge \$575.00 to Deposit Account No. 06-1075, Order No. 103532-0002, in payment of the filing fee. A duplicate copy of this transmittal letter is transmitted herewith.

[X] The Director is hereby authorized to charge payment of any additional filing fees required under 37 C.F.R. § 1.16, in connection with the paper(s) transmitted herewith, or credit any overpayment of same, to deposit Account No. 06-1075, Order No. 103532-0002. A duplicate copy of this transmittal letter is transmitted herewith.

EXTENSION FEE

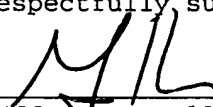
[X] A three-month extension fee of \$510.00 is applicable to the Response filed herewith pursuant to 37 C.F.R. § 1.136(a).

[] A check in the amount of \$_____ in payment of the extension fee is transmitted herewith.

[X] The Director is hereby authorized to charge the \$510.00 extension fee pursuant to 37 C.F.R. § 1.136(a) to Deposit Account No. 06-1075, Order No. 103532-0002. A duplicate copy of this transmittal letter is transmitted herewith.

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Respectfully submitted,



Jeffrey D. Mullen
(Reg. No. 52,056)
Agent for Applicants
[X] Submitted under 37 C.F.R. § 1.34
Fish & Neave IP Group
Ropes & Gray
Customer No. 1473
1251 Avenue of the Americas
New York, NY 10020
(212) 596-9000



PATENTS
Attorney Docket No. 8011-15

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants : James J. Fallon et al.
Application No. : 09/776,267 Confirmation No. : 9730
Filing Date : February 2, 2001
Title : SYSTEMS AND METHODS FOR ACCELERATED LOADING
OF OPERATING SYSTEMS AND APPLICATION PROGRAMS
Art Unit : 2115
Examiner : Suresh Suryawanshi

New York, New York 10020
August 14, 2006

Hon. Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

EXPRESS MAIL CERTIFICATION

Sir:

"Express Mail" mailing label number EV669671832US

Date of Deposit August 14, 2006

I hereby certify that the papers and fees identified below are being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 C.F.R. § 1.10 on the date indicated above and are addressed to Hon. Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Transmittal Letter (in duplicate);

Reply to Office Action; and,

Return Postcard.


Isatta B. Smith

08-66-06

TFU 2157



8011-15

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants : James J. Fallon et al.
 Application No. : 09/776,267
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 Alexandria, VA 22313-1450

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TRANSMITTAL LETTER

Sir:

Transmitted herewith to be filed in the above-identified
 patent application is a:

Reply to an Office Action.

FEE FOR ADDITIONAL CLAIMS

A fee for additional claims is not required.

A fee for additional claims is required.

Express Mail: EV669671832US

The additional fee has been calculated as shown below:

	CLAIMS REMAINING AFTER AMENDMENT	-	HIGHEST NUMBER PAID FOR	*	=	PRESENT PREVIOUSLY	X	RATE EXTRA	=	ADD'L FEES
TOTAL CLAIMS	39	-	20	*	=	19	X	\$25	=	\$475.00
INDEPENDENT CLAIMS	4	-	3	**	=	1	X	\$100	=	\$100.00
FIRST PRESENTATION OF A MULTIPLE DEPENDENT CLAIM							+	\$180	=	\$000.00
* If less than 20, insert 20.										TOTAL
										<u>\$575.00</u>

** If less than 3, insert 3.

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[X] Please charge \$575.00 to Deposit Account No. 06-1075, Order No. 103532-0002, in payment of the filing fee. A duplicate copy of this transmittal letter is transmitted herewith.

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EXTENSION FEE

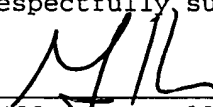
[X] A three-month extension fee of \$510.00 is applicable to the Response filed herewith pursuant to 37 C.F.R. § 1.136(a).

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Respectfully submitted,



Jeffrey D. Mullen
(Reg. No. 52,056)
Agent for Applicants
[X] Submitted under 37 C.F.R. § 1.34
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PATENTS
Attorney Docket No. 8011-15

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants : James J. Fallon et al.
Application No. : 09/776,267 Confirmation No. : 9730
Filing Date : February 2, 2001
Title : SYSTEMS AND METHODS FOR ACCELERATED LOADING
OF OPERATING SYSTEMS AND APPLICATION PROGRAMS
Art Unit : 2115
Examiner : Suresh Suryawanshi

New York, New York 10020
August 14, 2006

Hon. Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

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Date of Deposit August 14, 2006

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Transmittal Letter (in duplicate);

Reply to Office Action; and,

Return Postcard.


Isatta B. Smith

PATENT APPLICATION FEE DETERMINATION RECORD
Effective December 8, 2004

09/776267

CLAIMS AS FILED - PART I

	(Column 1)	(Column 2)
TOTAL CLAIMS		
FOR	NUMBER FILED	NUMBER EXTRA
TOTAL CHARGEABLE CLAIMS	minus 20= *	
INDEPENDENT CLAIMS	minus 3 = *	
MULTIPLE DEPENDENT CLAIM PRESENT <input type="checkbox"/>		

* If the difference in column 1 is less than zero, enter "0" in column 2

CLAIMS AS AMENDED - PART II

	(Column 1)	(Column 2)	(Column 3)
AMENDMENT A	8-14-06		
	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
Total	* 39	Minus ** 20	= 19
Independent	* 4	Minus *** 3	= 1
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM <input type="checkbox"/>			

SMALL ENTITY TYPE

OR OTHER THAN SMALL ENTITY

RATE	FEE		RATE	FEE
BASIC FEE		OR	BASIC FEE	
X\$ 25=		OR	X\$50=	
X100=		OR	X200=	
+180=		OR	+360=	
TOTAL		OR	TOTAL	

SMALL ENTITY

OR OTHER THAN SMALL ENTITY

RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X\$ 25=	475	OR	X\$50=	
X100=	160	OR	X200=	
+180=		OR	+360=	
TOTAL ADDIT. FEE	575	OR	TOTAL ADDIT. FEE	

(Column 1)

(Column 2)

(Column 3)

	(Column 1)	(Column 2)	(Column 3)
AMENDMENT B			
	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
Total	*	Minus **	=
Independent	*	Minus ***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM <input type="checkbox"/>			

RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X\$ 25=		OR	X\$50=	
X100=		OR	X200=	
+180=		OR	+360=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

(Column 1)

(Column 2)

(Column 3)

	(Column 1)	(Column 2)	(Column 3)
AMENDMENT C			
	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
Total	*	Minus **	=
Independent	*	Minus ***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM <input type="checkbox"/>			

RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X\$ 25=		OR	X\$50=	
X100=		OR	X200=	
+180=		OR	+360=	

Document code: WFEE

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01 FC:2253 510.00 DA



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UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/776,267	02/02/2001	James J. Fallon	8011-15	9730

22150 7590 02/14/2006
F. CHAU & ASSOCIATES, LLC
130 WOODBURY ROAD
WOODBURY, NY 11797

EXAMINER

SURYAWANSHI, SURESH

ART UNIT PAPER NUMBER

2115

DATE MAILED: 02/14/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No. 09/776,267	Applicant(s) FALLON ET AL.	
Examiner Suresh K. Suryawanshi	Art Unit 2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 12/08/05 amendments.
- 2a) This action is **FINAL**.
- 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1,2,4-7,9,13,15 and 17 is/are pending in the application.
4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 1,2,4-7,9,13,15 and 17 is/are rejected.
- 7) Claim(s) _____ is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on 02 February 2001 is/are: a) accepted or b) objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) All b) Some * c) None of:
1. Certified copies of the priority documents have been received.
2. Certified copies of the priority documents have been received in Application No. _____.
3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) Notice of References Cited (PTO-892)
- 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) Notice of Informal Patent Application (PTO-152)
- 6) Other: _____

DETAILED ACTION

1. Claims 1-2, 4-7, 9, 13, 15 and 17 are presented for examination.

Drawings

2. This application, filed under former 37 CFR 1.60, lacks formal drawings. The informal drawings filed in this application are acceptable for examination purposes. When the application is allowed, applicant will be required to submit new formal drawings. In unusual circumstances, the formal drawings from the abandoned parent application may be transferred by the grant of a petition under 37 CFR 1.182.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Art Unit: 2115

4. Claims 1-2, 4-7, 9, 13, 15 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kroeker et al (US Patent 6,073,232¹; hereinafter Kroeker) in view of Stewart (US Patent 6,539,456¹) and further in view of Esfahani et al (US Patent 6,434,695 B1¹; hereinafter Esfahani).

5. As per claim 1, Kroeker discloses

maintaining a list of boot data used for booting a computer system [col. 2, lines 30-47; col. 5, lines 1-7; a prefetch table containing a listing of the disk locations and length of data records that were requested by the host computer in the immediately previous power-on/reset];

initializing a central processing unit of the computer system [col. 2, lines 30-35; inherent to the system during power-up process];

preloading the boot data into a cache memory prior to completion of initialization of the computer system [col. 1, lines 58-64; col. 2, lines 36-41; col. 3, lines 30-39; col. 5, lines 17-21; data is preloaded into the RAM cache according to the prefetch table prior to completion of initialization of the host computer as shown in Fig. 3]; and

¹ Prior art cited by the examiner in the prior office action.

Art Unit: 2115

servicing requests for boot data from the computer system using the preloaded boot data after completion of initialization of the host computer system [col. 2, lines 41-47; col. 3, lines 30-39; data is communicated from the cache to the host computer as soon as the host computer requests the data].

Kroeker does not expressly disclose that the completion of initialization of the host computer includes the completion of initialization of a central processing unit too. However, a routineer in the art would know that a host computer will not be called having completed its initialization without having its central processing unit initialized. The central processing unit is a brain of a host computer that must be initialized in order to have a successful initialization of the host computer. However, Stewart clearly discloses that the stored boot data is for access by the central processing unit of the host computer [Fig. 1; col. 1, lines 28-35; col. 1, line 63 -- col. 2, line 3; col. 3, lines 20-37]. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the cited references as both are directed for speeding the boot-up process in computers. Moreover, one cannot have a host computer without having a central processing unit or some sort of processing unit performing the job of the central processing unit. The central processing unit will be initialized in the process of initialization of the host computer.

Kroeker and Stewart do not disclose about accessing compressed boot data and decompressing the compressed boot data. However, Esfahani et al clearly disclose about loading a compressed boot data into a RAM cache and then the boot data is decompressed and executed [col. 2, lines 5-13, 63, 67; col. 10, line 65 – col. 11, line 4]. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the cited references as they are directed to minimize a computer's initial program load time or shortening the load time of the computer programs from a hard disk drive to a host computer. Moreover, the shortening load time method of Kroeker by loading the program codes into the RAM cache according to the prefetch table will definitely be benefited with the method of reading compressed data into the RAM cache and then decompressing and executing as needed. This way, one may not only have needed data into a fast access memory but also a large amount of data to avoid frequent accessing the storage device(s).

6. As per claim 2, Kroeker discloses that the boot data comprises program code associated with one of an operating system of the computer system, an application program, and a combination thereof [col. 5, lines 41-51; requesting data records are part of a computer program such as DOS or Windows].

7. As per claim 4, Kroeker discloses that the method steps are performed by a data storage controller connected to the boot device [fig. 1; controller].

8. As per claim 5, Kroeker discloses the step of updating the list of boot data during the boot process [col. 8, lines 63-65; the prefetch table is updated].

9. As per claim 6, Kroeker discloses the step of updating comprises adding to the list any boot data requested by the computer system not previously stored in the list [col. 8, lines 63-68; the prefetch table is updated].

10. As per claim 7, Kroeker discloses that the step of updating comprises removing from the list any boot data previously stored in the list and not requested by the computer system [col. 8; lines 63-65; updating the prefetch table].

11. As per claim 9, Kroeker discloses that the method steps are program instructions that are tangibly embodied on a program storage device and readable by a machine to execute the method steps [col. 9, lines 27-30; computer program].

12. As per claim 13, Kroeker discloses

a digital signal processor (DSP) [fig. 1; host computer];

a programmable volatile logic device [fig. 1, RAM cache], wherein the programmable volatile logic device is programmed by the DSP or controller prior to completion of initialization of a central processing unit of the host system [col. 1, lines 58-64; col. 2, lines 36-41; col. 3, lines 30-39; col. 5, lines 17-21; data is preloaded into the RAM cache according to the prefetch table prior to completion of initialization of the central processor unit as shown in Fig. 3 that the method enters an idle state to await a command from the host computer since the CPU of the host computer is not ready] to (i) instantiate a first interface for operatively interfacing the boot device controller to a boot device [fig. 1; controller] and to (ii) instantiate a second interface for operatively interfacing the boot device controller to the host system [inherent to the system as a bus interface is used to interface the controller with host computer];

a cache memory device [Fig. 1; RAM cache]; and

a non-volatile memory device, for storing logic code associated with the DSP, the first interface and the second interface, wherein the logic code comprises instructions executable by the DSP for maintaining a list of boot data used for booting the host system [fig. 1; col. 4, lines 10-28; instructions are embodied as microcode in a ROM; col. 5, lines 1-7; a prefetch table is read from a reserved area of the disks], for preloading the boot data into the cache memory

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device prior to completion of initialization of the host system [col. 1, lines 58-64; col. 2, lines 36-41; col. 3, lines 30-39; col. 5, lines 17-21; data is preloaded into the RAM cache according to the prefetch table prior to completion of initialization of the host computer as shown in Fig. 3 that the method enters an idle state to await a command from the host system], and servicing requests for boot data from the host system after completion of initialization of the host system using the preloaded boot data [col. 2, lines 41-47; col. 3, lines 30-39; data is communicated from the cache to the host computer as soon as the host computer requests the data].

Kroeker does not expressly disclose that the completion of initialization of the host system includes the completion of initialization of a central processing unit too. However, a routineer in the art would know that a host system will not be called having completed its initialization without having its central processing unit initialized. The central processing unit is a brain of a host system that must be initialized in order to have a successful initialization of the host system. However, Stewart clearly discloses that the stored boot data is for access by the central processing unit of the host system [Fig. 1; col. 1, lines 28-35; col. 1, line 63 -- col. 2, line 3; col. 3, lines 20-37]. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the cited references as both are directed for speeding the boot-up process in computers. Moreover, one cannot have a host system without having a central processing unit or some sort of processing unit performing the job of the central processing unit. The central processing unit will be initialized in the process of initialization of the host system.

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Kroeker and Stewart do not disclose about accessing compressed boot data and decompressing the compressed boot data. However, Esfahani et al clearly disclose about loading a compressed boot data into a RAM cache and then the boot data is decompressed and executed [col. 2, lines 5-13, 63, 67; col. 10, line 65 – col. 11, line 4]. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the cited references as they are directed to minimize a computer's initial program load time or shortening the load time of the computer programs from a hard disk drive to a host computer. Moreover, the shortening load time method of Kroeker by loading the program codes into the RAM cache according to the prefetch table will definitely be benefited with the method of reading compressed data into the RAM cache and then decompressing and executing as needed. This way, one may not only have needed data into a fast access memory but also a large amount of data to avoid frequent accessing the storage device(s).

13. As per claim 15, Kroeker discloses that the logic code in the non-volatile memory device further comprises program instructions executable by the DSP for maintaining a list of application data associated with an application program [col. 11; lines 30-34; a prefetch table containing disk storage location and length of the data records requested by the application program]; preloading the application data upon launching the application program [col. 11, lines 46-50; preloading the data cache prior to receiving a read command from the application], and servicing requests for the application data from the host system using the preloaded application data col. 11, lines 51-57; communicating the prestored data records of the application from the data cache to the host computer].

14. As per claim 17, Kroeker discloses

maintaining a list of application data associated with an application program [col. 2, lines 30-47; col. 5, lines 1-7; a prefetch table containing a listing of the disk locations and length of data records that were requested by the host computer in the immediately previous power-on/reset; col. 5, lines 41-51; requesting data records are part of a computer program such as DOS or Windows; claims 28 and 32];

preloading the application data into the cache memory prior to completion of initialization of the central processing unit of the computer system, wherein preloading the application data comprises accessing application data from a boot device [col. 1, lines 58-64; col. 2, lines 36-41; col. 3, lines 30-39; col. 5, lines 17-21; data is preloaded into the RAM cache according to the prefetch table prior to completion of initialization of the central processor unit as shown in Fig. 3 that the method enters an idle state to await a command from the host computer since the CPU of the host computer is not ready]; and

servicing requests for application data from the computer system using the preloaded application data after completion of initialization of the central processing unit of the computer system, wherein servicing requests comprises accessing application data from the cache [col. 2, lines 41-47; col. 3, lines 30-39; data is communicated from the cache to the host computer as soon as the host computer requests the data upon completion of initialization of the CPU].

Kroeker does not expressly disclose that the completion of initialization of the computer system includes the completion of initialization of a central processing unit too. However, a routineer in the art would know that a computer system will not be called having completed its initialization without having its central processing unit initialized. The central processing unit is a brain of a computer system that must be initialized in order to have a successful initialization of the computer system. However, Stewart clearly discloses that the stored boot data is for access by the central processing unit of the computer system [Fig. 1; col. 1, lines 28-35; col. 1, line 63 -- col. 2, line 3; col. 3, lines 20-37]. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the cited references as both are directed for speeding the boot-up process in computers. Moreover, one cannot have a computer system without having a central processing unit or some sort of processing unit performing the job of the central processing unit. The central processing unit will be initialized in the process of initialization of the computer system.

Response to Arguments

15. Applicant's arguments with respect to claims 1-2, 4-7, 9, 13, 15 and 17 have been considered but are moot in view of the new ground(s) of rejection.

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Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Suresh K. Suryawanshi whose telephone number is 571-272-3668. The examiner can normally be reached on 9:00am - 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas C. Lee can be reached on 571-272-3667. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

sks
February 6, 2006



THOMAS LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

Notice of References Cited	Application/Control No. 09/776,267	Applicant(s)/Patent Under Reexamination FALLON ET AL.	
	Examiner Suresh K. Suryawanshi	Art Unit 2115	Page 1 of 1

U.S. PATENT DOCUMENTS

*	Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A US-5,307,497	04-1994	Feigenbaum et al.	713/1
*	B US-6,003,115	12-1999	Spear et al.	711/137
*	C US-6,463,509	10-2002	Teoman et al.	711/137
*	D US-6,704,840	03-2004	Nalawadi et al.	711/118
	E US-			
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FOREIGN PATENT DOCUMENTS

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NON-PATENT DOCUMENTS

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*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
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CONFIRMATION NO. 9730

SERIAL NUMBER: 09/776,267	FILING DATE 02/02/2001 RULE	CLASS 713	GROUP ART UNIT 2182	ATTORNEY DOCKET NO. 8011-15
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APPLICANTS
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 Paul F. Pickel, Bethpage, NY;
 Stephen J. McErlain, New York, NY;

**** CONTINUING DATA ****
 THIS APPLN CLAIMS BENEFIT OF 60/180,114 02/03/2000
yes yes

**** FOREIGN APPLICATIONS ****
None yes

IF REQUIRED, FOREIGN FILING LICENSE GRANTED ** 03/09/2001 **** SMALL ENTITY ****

Foreign Priority claimed <input type="checkbox"/> yes <input checked="" type="checkbox"/> no	STATE OR COUNTRY NY	SHEETS DRAWING 13	TOTAL CLAIMS 10	INDEPENDENT CLAIMS 2
35 USC 119 (a-d) conditions met <input type="checkbox"/> yes <input type="checkbox"/> no <input type="checkbox"/> Met after Allowance				
Verified and Acknowledged <i>yes</i>	Examiner's Signature <i>sls</i>	Initials	<i>SPS 2/4/06 SP3 12/18/04 SP8 5/27/05 SP4 2/16/06</i>	

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TITLE
 Systems and methods for accelerated loading of operating systems and application programs

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INDEX OF CLAIMS

- ✓ Rejected
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- (Through numeral) ... Canceled
- ± Restricted
- N Non-elected
- I Interference
- A Appeal
- O Objected

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