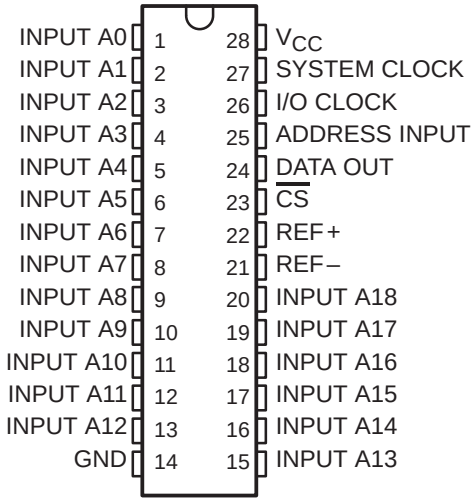
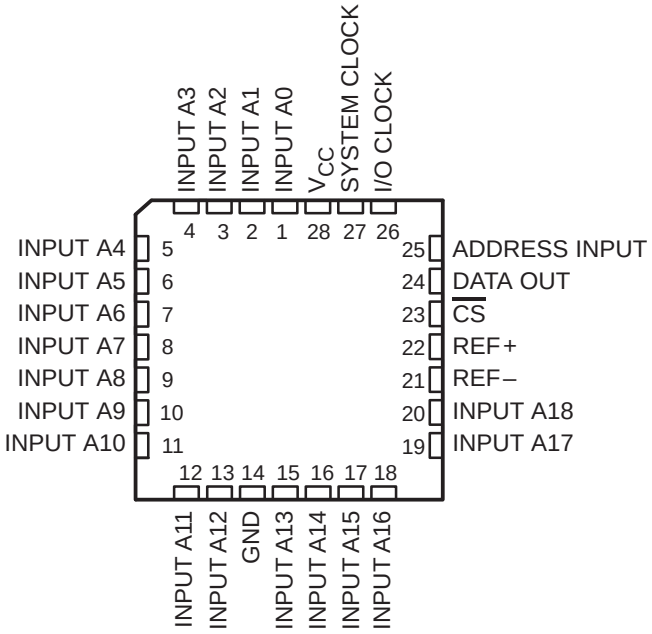
- **8-Bit Resolution A/D Converter**
- **Microprocessor Peripheral or Stand-Alone Operation**
- **On-Chip 20-Channel Analog Multiplexer**
- **Built-in Self-Test Mode**
- **Software-Controllable Sample and Hold**
- **Total Unadjusted Error . . . ±0.5 LSB Max**
- **Timing and Control Signals Compatible With 8-Bit TLC540 and 10-Bit TLC1540 A/D Converter Families**
- **CMOS Technology**

PARAMETER	TL545	TL546
Channel Acquisition Time	1.5 µs	2.7 µs
Conversion Time (Max)	9 µs	17 µs
Sampling Rate (Max)	76 x 10^3	40 x 10^3
Power Dissipation (Max)	15 mW	15 mW

N PACKAGE
(TOP VIEW)



FN PACKAGE
(TOP VIEW)



description

The TLC545 and TLC546 are CMOS analog-to-digital converters built around an 8-bit switched capacitor successive-approximation analog-to-digital converter. They are designed for serial interface to a microprocessor or peripheral via a 3-state output with up to four control inputs including independent SYSTEM CLOCK, I/O CLOCK, chip select ($\overline{CS}$), and ADDRESS INPUT. A 4-MHz system clock for the TLC545 and a 2.1-MHz system clock for the TLC546 with a design that includes simultaneous read/write operation allowing high-speed data transfers and sample rates of up to 76,923 samples per second for the TLC545, and 40,000 samples per second for the TLC546.

In addition to the high-speed converter and versatile control logic, there is an on-chip 20-channel analog multiplexer that can be used to sample any one of 19 inputs or an internal self-test voltage, and a sample-and-hold that can operate automatically or under microprocessor control.

The converters incorporated in the TLC545 and TLC546 feature differential high-impedance reference inputs that facilitate ratiometric conversion, scaling, and analog circuitry isolation from logic and supply noises. A totally switched capacitor design allows low-error (±0.5 LSB) conversion in 9 µs for the TLC545, and 17 µs for the TLC546, over the full operating temperature range.

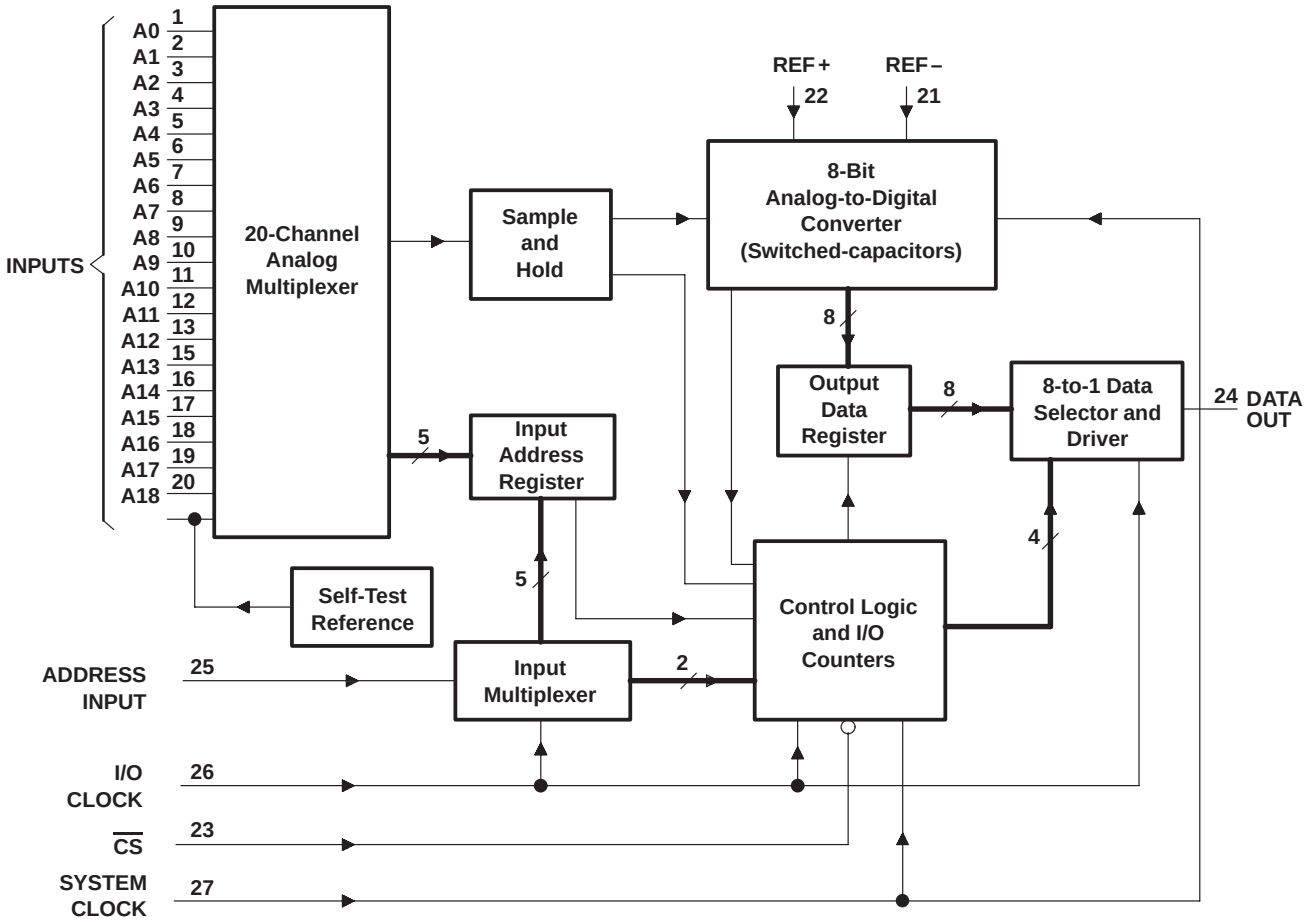
AVAILABLE OPTIONS

T_A	PACKAGE	
	CHIP CARRIER (FN)	PLASTIC DIP (N)
0°C to 70°C	TLC545CFN —	TLC545CN —
–40°C to 85°C	TLC545IFN TLC546IFN	TLC545IN TLC546IN

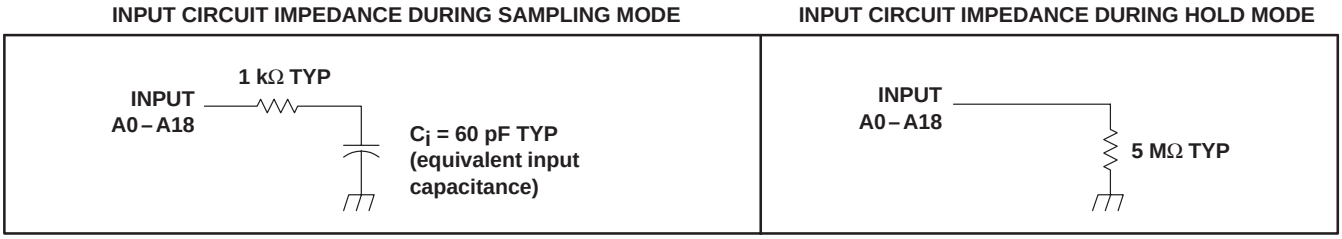
description (continued)

The TLC545C and the TLC546C are characterized for operation from 0°C to 70°C. The TLC545I and the TLC546I are characterized for operation from –40°C to 85°C.

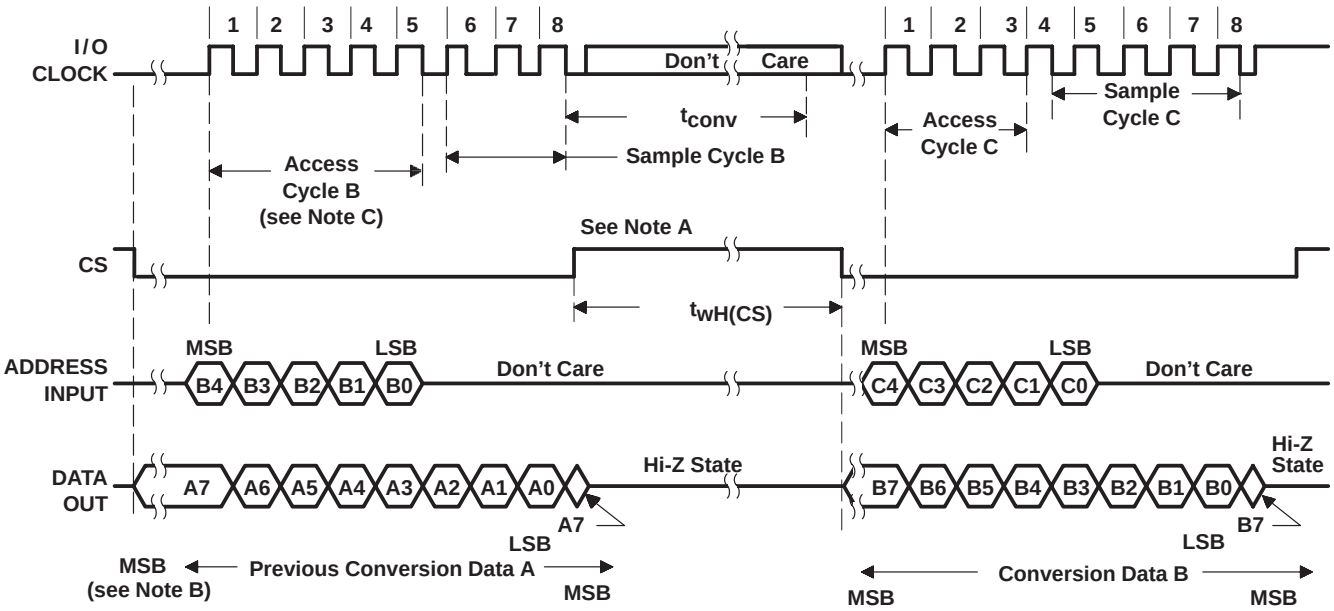
functional block diagram



typical equivalent inputs



operating sequence



NOTES: A. The conversion cycle, which requires 36 system clock periods, is initiated with the eighth I/O CLOCK↓ after $\overline{CS}$↓ for the channel whose address exists in memory at that time.

B. The most significant bit (MSB) will automatically be placed on the DATA OUT bus after $\overline{CS}$ is brought low. The remaining seven bits (A6–A0) will be clocked out on the first seven I/O CLOCK falling edges.

C. To minimize errors caused by noise at the $\overline{CS}$ input, the internal circuitry waits for three system clock cycles (or less) after a chip select transition before responding to control input signals. Therefore, no attempt should be made to clock-in address data until the minimum chip-select setup time has elapsed.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) . . . . . 6.5 V
Input voltage range, V_I (any input) . . . . . –0.3 V to V_{CC} +0.3 V
Output voltage range, V_O . . . . . –0.3 V to V_{CC} +0.3 V
Peak input current range (any input) . . . . . ±10 mA
Peak total input current (all inputs) . . . . . ±30 mA
Operating free-air temperature range, T_A: TLC545C, TLC546C . . . . . 0°C to 70°C
TLC545I, TLC546I . . . . . –40°C to 85°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Case temperature for 10 seconds, T_C: FN package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: N package . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to network ground terminal.

recommended operating conditions

			TLC545			TLC546			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}			4.75	5	5.5	4.75	5	5.5	V
Positive reference voltage, V_{ref+} (see Note 2)			0	V_{CC}	V_{CC} +0.1	0	V_{CC}	V_{CC} +0.1	V
Negative reference voltage, V_{ref-} (see Note 3)			−0.1	0	V_{CC}	−0.1	0	V_{CC}	V
Differential reference voltage, $V_{ref+} - V_{ref-}$ (see Note 3)			0	V_{CC}	V_{CC} +0.2	0	V_{CC}	V_{CC} +0.2	V
Analog input voltage (see Note 3)			0		V_{CC}	0		V_{CC}	V
High-level control input voltage, V_{IH}			2			2			V
Low-level control input voltage, V_{IL}					0.8			0.8	V
Setup time, address bits at data input before I/O CLOCK↑, $t_{su(A)}$			200			400			ns
Address hold time, t_h			0			0			ns
Setup time, $\overline{CS}$ low before clocking in first address bit, $t_{su(CS)}$ (see Note 2)			3			3			System clock cycles
I/O CLOCK frequency, $f_{clock(I/O)}$			0		2.048	0		1.1	MHz
SYSTEM CLOCK frequency, $f_{clock(SYS)}$			$f_{clock(I/O)}$		4	$f_{clock(I/O)}$		2.1	MHz
Pulse duration, $\overline{CS}$ high during conversion, $t_{wH(CS)}$			36			36			System clock cycles
Pulse duration, SYSTEM CLOCK high, $t_{wH(SYS)}$			110			210			ns
Pulse duration, SYSTEM CLOCK low, $t_{wL(SYS)}$			100			190			ns
Pulse duration, I/O CLOCK high, $t_{wH(I/O)}$			200			404			ns
Pulse duration, I/O CLOCK low, $t_{wL(I/O)}$			200			404			ns
Clock transition time (see Note 4)	System	$f_{clock(SYS)} \le 1048$ kHz			30			30	ns
		$f_{clock(SYS)} > 1048$ kHz			20			20	
	I/O	$f_{clock(I/O)} \le 525$ kHz			100			100	ns
		$f_{clock(I/O)} > 525$ kHz			40			40	
Operating free-air temperature, T_A		TLC545C, TLC546C	0		70	0		70	°C
		TLC545I, TLC546I	−40		85	−40		85	

NOTES: 2. To minimize errors caused by noise at $\overline{CS}$, the internal circuitry waits for three system clock cycles (or less) after a chip select falling edge or rising edge is detected before responding to control input signals. Therefore, no attempt should be made to clock-in address data until the minimum chip select setup time has elapsed.

3. Analog input voltages greater than that applied to REF+ convert as all “1”s (11111111), while input voltages less than that applied to REF– convert as all “0”s (00000000). As the differential reference voltage decreases below 4.75 V, the total unadjusted error tends to increase.

4. This is the time required for the clock input signal to fall from V_{IH} min to V_{IL} max or to rise from V_{IL} max to V_{IH} min. In the vicinity of normal room temperature, the devices function with input clock transition time as slow as 2 µs for remote data acquisition applications where the sensor and the A/D converter are placed several feet away from the controlling microprocessor.

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