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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

KINGSTON TECHNOLOGY COMPANY, INC.,
Petitioner,

v.

POLARIS INNOVATIONS LTD.,
Patent Owner.

Case IPR2016-01623
Patent 7,315,454 B2

Before SALLY C. MEDLEY, JEAN R. HOMERE,
and KEN B. BARRETT, *Administrative Patent Judges*.

BARRETT, *Administrative Patent Judge.*

FINAL WRITTEN DECISION
35 U.S.C. § 318(a) and 37 C.F.R. § 42.73

I. INTRODUCTION

A. Background and Summary

Kingston Technology Company, Inc. ("Petitioner") filed a Petition requesting *inter partes* review of claims 1–7 of U.S. Patent No. 7,315,454 B2 ("the '454 patent," Ex. 1001). Paper 2 ("Pet."). The Board instituted *inter partes* review of claims 1–5 and 7. Paper 7 ("Inst. Dec."), 32. Polaris Innovations Ltd. ("Patent Owner")[1] filed a Response to the Petition. Paper 16 ("PO Resp."). Petitioner filed a Reply. Paper 21 (Pet. Reply). The parties filed papers addressing Patent Owner's identification of allegedly improper arguments and evidence in Petitioner's Reply. Papers 23, 24. An oral hearing was held on November 14, 2017, and a transcript of the hearing is included in the record. Paper 32 ("Tr.").

This Final Written Decision is entered pursuant to 35 U.S.C. § 318(a). For the reasons discussed below, we determine that Petitioner has *not* shown by a preponderance of the evidence that claims 1–5 and 7 of the '414 patent are unpatentable.

B. Related Proceedings

According to the parties, the '454 patent is involved in *Polaris Innovations Ltd. v. Kingston Tech. Co., Inc.*, Case No. 8:16-cv-300 (C.D. Cal.). Pet. 1; Paper 4, 1.

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[1] Patent Owner identifies Polaris Innovations Ltd., Wi-LAN Inc., and Quarterhill Inc. as real parties-in-interest. Paper 4, 1; Paper 20, 1.

C. The '454 Patent

The '454 patent, titled "Semiconductor Memory Module," issued January 1, 2008, from U.S. Patent Application No. 11/439,443. Ex. 1001, [54], [45], [21].

The '454 patent generally relates to a semiconductor memory module including an electronic printed circuit board with a contact strip and a plurality of semiconductor memory chips of identical type. *Id.* at Abstract. "The semiconductor memory chips are rectangular in shape and are arranged, in at least two rows with the adjacent chips being oriented perpendicular to one another, such that the area used on the PC [printed circuit] board is optimized." *Id.*

According to the '454 patent, semiconductor memory chips of a conventional memory module are arranged symmetrically with respect to the center of the semiconductor memory module. *See id.* at 1:42–45. Figure 1A is reproduced below.

FIG 1A
PRIOR ART

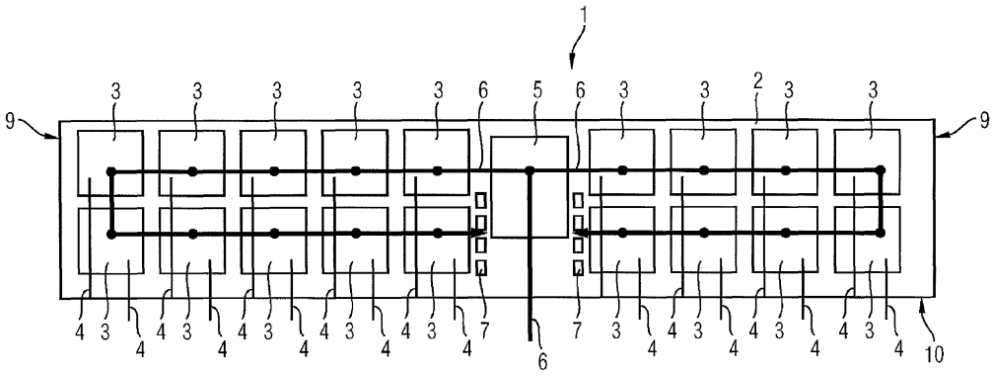


Figure 1A shows a front side of a conventional memory module. *Id.* at 4:14–16. As shown in Figure 1A, printed circuit board 2 has two rows of square-shaped semiconductor memory chips 3 arranged symmetrically around register component 5. *Id.* at 4:41–5:12. According to the '454

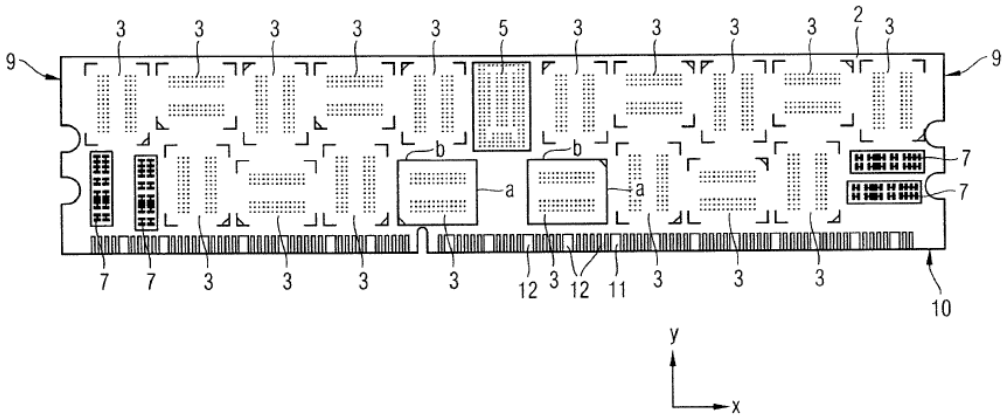
patent, "[t]he problem arises that the electronic printed circuit boards for semiconductor memory modules . . . have a standard size . . . [such that] rectangular memory chips with a large storage capacity, e.g., DDR3-DRAM[2] memory chips, can no longer be arranged in two rows, lying one above another." *Id.* at 1:62–67. The '454 patent also states:

> Moreover, when arranging the memory chips, care must be taken to ensure that an arrangement is found which exhibits the occurrence of signal propagation times that are as uniform as possible to all of the semiconductor memory chips in conjunction with conductor track lengths that are, to the greatest extent possible, identical in length. Meanwhile, the conductor track lengths are also desired to be as short as possible to keep the signal propagation times as short as possible.

Id. at 2:1–9.

To address these concerns, the '454 patent discloses a memory module in which "successive semiconductor memory chips in a row are in each case rotated by 90º relative to one another." *Id.* at 2:56–58. Figure 2 is reproduced below.

FIG 2



[2] "DDR" refers to Double Data Rate, and "DRAM" refers to Dynamic Random Access Memory. Ex. 1014 ¶ 3.

Figure 2 shows an embodiment of the memory module according to the '454 patent. *Id.* at 4:17–19. "In each of the two rows, the semiconductor memory chips 3 of identical type are mounted next to one another . . . wherein the semiconductor memory chips 3 of the two adjacent rows are respectively arranged in an opposite position." *Id.* at 5:29–34. Such an arrangement "maximiz[es] the utilization of the space available on the electronic printed circuit board 2." *Id.* at 5:67–6:2. Additionally, the arrangement allows for conductor track[3] lengths that are identical and that are comparatively short between the semiconductor memory chips. *Id.* at 7:36–39, Fig. 5; *see also id.* at 7:11–14 (explaining that Figure 5 includes a schematic illustration of a configuration of the line bus of the Figure 2 embodiment).

D. Illustrative Claim

Of the challenged claims of the '454 patent, claim 1 is an independent claim. The remaining challenged and instituted claims depend directly from claim 1. Claim 1, reproduced below with emphasis added, is illustrative:

> 1. A semiconductor memory module, comprising:
> an electronic printed circuit board including a contact strip that extends at a first edge of the printed circuit board along a first lateral direction and a plurality of electrical contacts disposed along the first lateral direction between two second edges that extend in a second lateral direction that is perpendicular to the first lateral direction; and
> a plurality of semiconductor memory chips of substantially identical type mounted on at least one external area of the printed circuit board and having a rectangular form with a shorter dimension and a longer dimension in a direction

[3] According to Patent Owner's expert, Dr. Bernstein, "[e]ach component on a memory module is connected via wires known interchangeably as 'traces,' 'conductor tracks,' 'line tracks,' or even simply 'wires.'" Ex. 2012 ¶ 38.

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