PC SDRAM Serial Presence Detect (SPD) Specification

REVISION 1.2B
November, 1999

Changes:

Revision 1.2B:

Updated Table 5, Serial Present Detect Data format, for consistency:
- Definitions of bytes 32-35 were added to this summary table since they were already defined in the specs

Added Section 5.0, SPD data format example.

Revision 1.2A:

Modified specification name
Corrects the typos in Rev1.2 revision history
Byte 127 bit 3 definition reserved for thermal information, values are TBD

Revision 1.2 adds:

Bytes 126, 127: Additional Information for "backward compatibility"
Bytes 93-94: Manufacturing Date Code
Bytes 32-35: Additional Timing Information
Byte 5: Changed the nomenclature from Bank to Row on the DIMM to remove confusion of Rows vs. Banks on a DIMM

Revision 1.1 adds comments to clarify several Bytes:

Bytes 3-4: Note added to clarify address row/column 1/16 rollup usage.
Bytes 5,17: Note added to clarify Module, SDRAM Device bank usage.
Bytes 23-26: Note added to clarify timing1/16ns rollup usage.

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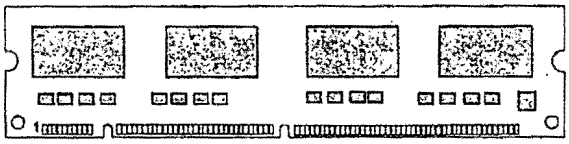
1.0 Introduction

This specification defines the Serial Presence Detect (SPD) electrical and Data Structure requirements for Synchronous DRAM Dual In-Line Memory Modules (SDRAM DIMMs) and Small-outline Memory Modules (SO-DIMM). These SDRAM DIMMs are intended for use as main memory installed on personal computer, ***work-station, and/or server*** motherboards.



168-DIMM reference

This specification largely follows the JEDEC defined 168-pin and SO-144 SDRAM DIMM SPD specs as of July 1996. *Changes in process are currently shown in italics.*

2.0 SDRAM Module Performance Grades

Three performance grades are defined in the SPD matrix:

CAS Latency x	highest latency, lowest performance
CAS Latency x-1	2nd highest latency
CAS Latency x-2	3rd highest latency, highest performance (may restrict freq)

This is a relative series of three latencies, CL x being the most commonly available at this speed grade.
The performance grade of the module is determined by the read data access time (Tac), and RAS cycle time (Trc) supported by the SDRAM components.

Latency numbers in the sequence will depend on the speeds which are supported by the module.

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