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**133 MHz PC SDRAM 64-Bit Non-ECC/Parity 144 Pin
UNBUFFERED SO-DIMM SPECIFICATION**

REVISION 1.0C

August 2000

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Revision 1.0C



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Changes:**Revision 1.0c Aug. 23, 2000**

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Added "Y" field in label to help specify if SO-DIMM is buffered or un-buffered (Optional)

Removed wiring table from page 16.

Revision 1.0b June 23, 2000

Review copy.

Added Gerber release note stating that PC133 Unbuffered SO-DIMM Gerber is backward compatible with the PC100 Unbuffered SO-DIMM.

Removal of the pull-up/pull-down on WP.

Require SPD EEPROM to be strapped to allow for write (WP to be shorted to GND).

Revision 1.0a May 23, 2000

Updated SO-DIMM naming convention (Added extra characters for the "d" and "e" field.)

Removed mixed-mode configuration table.

Revision 1.0 April 28, 2000

Added support for 512Mb

Removed A12/256Mb serial resistor.

Removed support for 50 pin TSOP package.

Removed support for 1MX16 devices.

Removed support for PC100/66 SDRAM for better clarity.

Copied from PC100/66 SO-DIMM Spec. Rev 1.1

Revision 1.1 January 25, 2000

Added pull-up/pull-down option on SPD write protect pin.

Revision 1.0 October, 1998

Added 256Mbit support, and changed decoupling.

Revision 0.7 August 14, 1998

Added clock trace length data, and PB marking information.

Revision 0.51 July 15, 1998

Added figures 14 and 15

Revision 0.5 July 14, 1998

Add support for 66MHz

Revision 0.3 June 12, 1998

Removed support of X8 components

Revision 0.22 April 15, 1998

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