IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent of: Benisek et al.
US Patent No.: 6,850,414 Attorney Docket No.: 37307-0007IP1
Issue Date: February 1, 2005
Appl. Serial No.: 10/187,763
§ 371 (c)(1) Date: July 2, 2002
Title: ELECTRONIC PRINTED CIRCUIT BOARD HAVING A PLURALITY OF IDENTICALLY DESIGNED, HOUSING-ENCAPSULATED SEMICONDUCTOR MEMORIES

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DECLARATION OF VIVEK SUBRAMANIAN

I, Vivek Subramanian, declare as follows:

I. Introduction.

1. I am making this declaration at the request of the Real Party in Interest (Kingston Technology Company, Inc.) in the matter of *Inter Partes* Review of U.S. Patent No. 6,850,414 (the "'414 patent").

2. I am being compensated for my work. My compensation does not depend on the outcome of this proceeding.

3. I have been asked to consider whether certain references disclose or render obvious the claims of the '414 Patent, either alone or in combination with each other.

4. I have been advised that a patent claim may be invalid as obvious if the differences between the subject matter patented and the prior art are such that the subject matter as a whole would have been obvious at the time of the invention to a person having ordinary skill in the art. I have also been advised that several factual inquiries underlie a determination of obviousness. These inquiries include the scope and content of the prior art, the level of ordinary skill in the field of the invention, the differences between the claimed invention and the prior art, and any objective evidence of non-obviousness.

5. I have been advised that objective evidence of non-obviousness directly attributable to the claimed invention, known as "secondary considerations of non-obviousness," may include commercial success, satisfaction of a long-felt but unsolved need, failure of others, copying, skepticism or disbelief before the invention, and unexpected results. I am not aware of any such objective evidence of non-obviousness that is directly attributable to the subject matter claimed in the '414 patent at this time.

6. In addition, I have been advised that the law requires a "common sense" approach of examining whether the claimed invention is obvious to a person skilled in the art. For example, I have been advised that combining familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results. I have further been advised that this is especially true

in instances where there are a limited numbers of possible solutions to technical problems or challenges.

7. I have been informed that all claims of the '414 Patent are subject to this *inter partes* review.

II. Materials Reviewed

8. In forming the opinions that I express below, I considered my own knowledge of the art plus at least the following references:

a. The '414 Patent

b. UK Patent Application GB 2 289 573 A ("Simpson")

c. U.S. Patent Application Publication No. 2002/0006032 A1 ("Karabatsos")

d. U.S. Patent No. 5,973,951 ("Bechtolsheim")

e. U.S. Patent No. 6,038,132 ("Tokunaga")

f. PC SDRAM Unbuffered DIMM Specification, Version 1.0 ("Intel Specification")

g. English Translation of German Publication No. DE 101 42 361 A1 ("Kiehl")

h. Intel Small Outline Package Guide

i. Micron 64Mb: x32 SDRAM Features

j. U.S. Patent No. 4,954,088 ("Fujizaki")

k. The File History of U.S. Patent No. 6,850,414

III. Qualifications

9. I summarize my relevant knowledge and experience below. My *Curriculum Vitae* contains additional information and is attached as Exhibit 1010.

10. I received a B.S. in electrical engineering from Louisiana State University in 1994, an M.S. in electrical engineering from Stanford University in 1996, and a Ph.D. in electrical engineering from Stanford University in 1998.

11. I co-founded Matrix Semiconductor, Inc. in 1998 to develop high density memory technology.

12. I have been teaching in the Electrical Engineering and Computer Sciences Department at the University of California, Berkeley since 2000. I was an Assistant Professor from 2000 to 2005, an Associate Professor from 2005 to 2011, and a Professor from 2011 to the present.

13. I have been an adjunct professor at the Sunchon National University in Sunchon, Korea since 2009, leading research in printed electronics.

14. I have been an independent consultant in the semiconductor industry since 2000, focusing on memory technology, flexible electronics, and RFID technology.

15. I have published more than 200 technical papers in journals and at conferences.

16. I am a named inventor on over 40 U.S. Patents, many of which are in the field of memory design.

IV. Simpson Memory Module Layout is not limited to use with memory chips of a particular physical size.

17. Simpson's teachings are clearly not limited to a memory module that contains only a particular size or type of memory chip. For instance, Simpson states that while, "[t]he first example is based on a standard 72 terminal DRAM memory module but . . . this technique can equally be applied to . . . 30, 144 and 168 terminal modules, and also to other types of memory." Simpson at 13:3-6. From this, one of skill in the art would understand that Simpson's layout of memory chips is not limited to chips with a particular physical size, memory capacity, or number of terminals. Instead, Simpson's layout is more broadly applicable, and may be implemented using any memory chips available at the time or that might be developed later. In fact, Simpson even invites artisans to modify of its example embodiment. *Id*. at 14:10-12 ("The quantity, position and type [of memory chips and sockets] are dependent upon the design preferences of the module designer.")

18. In addition, Simpson does not even mention physical dimensions of either its memory chips or its memory module. Consequently, it would be obvious to one of skill in the art to look to a standards document such as the Intel Specification to

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