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The following details have been taken from the documents submitted by the applicant

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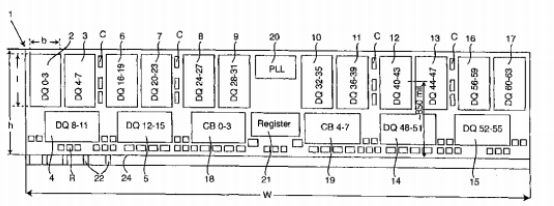
(54) Memory module

(57) The invention relates to a memory module, wherein memory chips (4-19) are arranged both horizontally (4, 5, 14, 15, 18, 19) and vertically (2, 3, 6 to 13, 16, 17) on a circuit board (1).



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Description

[0001] The present invention relates to a memory module, made of a plurality of memory chips which are arranged on at least one first surface of a substantially rectangular circuit board, which has pins along at least one side which forms a connector edge, said pins connected via a resistor to DQ terminals (and/or data terminals) of the memory chip, wherein the likewise substantially rectangular memory chips are arranged with their shorter sides in a row in the longitudinal direction of the circuit board in such a manner that the longer sides of the semiconductor chips run parallel to each other and perpendicular to the longitudinal direction of the circuit board.

[0002] Such memory modules with pins on both sides are, for example, DIMMs (DIMM = dual in-line memory modules). The existing types of DIMMs, such as RDIMMs (RDIMM = registered DIMM) with 184 pins and UDIMMs (UDIMM = unbuffered DIMM) with a length and/or width of 5.25 in (13.33 cm), should have a width and/or height of less than 1.2 in (3.048 cm), or preferably less than 1.125 in (2.85 cm). The goal is to preserve these dimensions while accommodating 36 DRAMs on one PCB (PCB = Printed Circuit Board).

[0003] To-date, DRAMs (DRAM Dynamic Random Access Memory and/or dynamic RAM or read/write memory) have been housed in so-called TSOP packages (TSOP = Thin Small Outline Package) which enable stacking. This means that two DRAMs can be mounted on top of each other, wherein in each case the pins are connected to each other. This makes it possible, for example, to accommodate 36 DRAMs on both sides of a PCB with solder pads for 18 DRAMs on each surface. Future DRAMs such as DDR333 (DDR = Double Data Rate) are made for better electrical performance in BGA packages (BGA = Ball Grid Array); however, these cannot be stacked easily. However, it is not possible to accommodate a plurality of 36 chips on a module in a straight line without stacking.

[0004] Modules which do not require stacking the memory chips use, for this purpose, two superimposed, spaced sub-PCBs in, for example, so-called FEMMA technology (FEMMA = Flexible Memory Module Assembly). Ultimately, then, two PCBs are stacked on top of each other, each equipped on both sides with DRAMs.

[0005] In modules with a construction including, for example, 36 DRAMs, the cable length between the DQ terminals and their respective pins must not be too large, since otherwise delay and resistance problems can arise. This distance should therefore be, in any case, less than about 1000 mils (25.4 mm; 1 mil = 10^{-3}). Such values are not achieved even with the FEMMA technology.

[0006] In memory modules with two physical banks, the configuration is known in which two DQ ports of different DRAMs are connected to each other and to a shared resistor, the other terminal of which is connected to DQ pins of a PCB connector (see JEDEC document: ddrregrev 1_0.pdf, page 11). In other words, a DQ terminal of a first DRAM, and a corresponding DQ terminal of a second DRAM are connected to each other, and connected via a shared resistor to a pin of the PCB. Such a resistor, also called a "stub resistor", serves the purpose of decoupling the load posed by the memory chips together with the cables - and more precisely the load of the currently inactive banks - from a DQ signal path.

[0007] **Fig.** 4 shows DIMMs 0 to DIMMs N from memory chips B0, B1, ..., BN, BN+1, which can comprise one or two banks each. Two memory chips are connected via a resistor r to a DQ bus, which is connected to a memory controller MC.

[0008] The problem addressed by the present invention is that of providing a memory module, wherein a plurality of DRAMs can be accommodated on a circuit board while preserving low height and short signal paths.

[0009] This problem is addressed according to the invention, in a memory module of the type named above, in that at least one further memory chip is mounted on the circuit board between the row of memory chips and the connector edge, the longer side of which is parallel to the longitudinal direction of the circuit board.

[0010] In the invention, therefore, some memory chips are arranged with their longitudinal direction perpendicular to the memory chips which are oriented in the usual manner on the circuit board. These memory chips are then positioned between the memory chips aligned in the usual way and the connector edge and/or the side of the memory module facing the pins.

[0011] In this way, the distance between the DQ terminals of the memory chips and the connector edge of the PCB is restricted to a maximum of about 990 mils (2.51 cm). The resulting signal path therefore turns out to be shorter than in other solutions - such as, in particular, in FEMMA technology.

[0012] This short signal path is achieved by aligning the several memory chips which are rotated by 90° with respect to the conventionally oriented memory chips - such that they are also referred to below as rotated memory chips - with their longitudinal direction parallel to the longitudinal direction of the circuit board. As a result, these rotated memory chips are positioned with their width, and not their length, between the pins and the memory chips which are present in the conventional manner on the circuit board. The signal path is therefore ultimately short as a result of the rotated memory chips running transverse to the same.

[0013] Optionally, it is possible to provide, in the memory module according to the invention, 18 memory chips on each side of the circuit board, by way of example. The thickness of the accordingly obtained memory module is then in any case less than the thickness of existing memory modules with dual PCBs, and less than when stacked TSOP housings are used.

[0014] In the memory module according to the invention, the individual memory chips therefore have a different orientation: the memory chips arranged in the conventional manner lie parallel to each other with their longitudinal direction perpendicular to the longitudinal direction of the circuit board. The rotated memory chips are pivoted 90° relative to these parallel memory chips, and lie with their longitudinal direction parallel to the longitudinal direction of the circuit board. This makes it possible to shorten the signal path significantly, as has already been explained above.

[0015] Furthermore, in the memory module according to the invention, a separate resistor can be assigned to each DQ terminal such that the DQ terminals of two different memory chips are only brought together and connected to a pin after these resistors. It has been found that such a "doubled" design of the resistors can further improve the decoupling.

[0016] It should be noted that the assignment of one stub resistor to each DQ terminal is an independent feature of the present invention. That means that this feature can also be advantageously applied if the memory chips are not oriented with respect to each other in the manner specified in claim 1.

[0017] Other components and auxiliary blocks of the memory module, such as a PLL (PLL phase-locked loop) or registers, can be placed between the rotated memory chips, which extend

parallel to the longitudinal direction of the circuit board with their longitudinal direction, and/or between the memory chips arranged in the usual manner. In this case, the PLL and/or register can be arranged in such a manner that they are either on both sides or only on one side of the circuit board. It is likewise possible to include the register and PLL in the central region between the individual memory chips.

[0018] The invention is explained in detail below with reference to the drawings. In the drawings:

[0019] Fig. 1 show a plan view of a first embodiment of the memory module according to the invention,

[0020] Fig. 2 shows a plan view of a second embodiment of the memory module according to the invention,

[0021] Fig. 3 shows a block diagram to explain the stub resistors in the memory module according to the invention, and

[0022] Fig. 4 shows the connection of the memory chip to a memory controller in the prior art.

[0023] Fig. 1 shows a PCB **1**, which accommodates memory chips **2** to **19** with DQ terminals **0** to **63** and CB terminals **0** to **7**. The assignment of the DQ terminals to the memory chips is only given by way of example. Of course, an entirely different assignment can be used. In addition, a PLL **20** and a register **21** are included approximately in the middle of the PCB **1**.

[0024] The memory chips **2** to **19** have a width b of about 8 mm, and a length l of about 14 to 16 mm. The distance between the individual chips is about 0.5 mm. The top edge in the drawing, between the memory chips **2**, **3**, **6** to **9** and **10** to **17** and the "top" edge of the PCB **1**, measures approximately 0.5 mm, while a lower edge between the memory chips **4**, **5**, **14**, **15**, **18** and **19** and the lower edge and/or connector edge **24** of the PCB **1** is only 4 mm. This results in a width or height h of the PCB **1** of about 27 mm, and a length and/or width w of about 133 mm. In this case, a space requirement of 17 mm is assumed for the PLL **20** and/or the register **21**, while for the capacitor rows C, a space requirement of about 8 mm is assumed. Resistor elements R are arranged between the memory chips **4**, **5**, **14**, **15**, **18** and **19** in the vicinity of pins **22**, which extend along the connector edge **24**.

[0025] The memory chips **2**, **3**, **6** to **9**, **10** to **13**, **16** and **17** lie in the conventional manner in the longitudinal direction of the PCB **1** in a row, wherein the longitudinal direction of the individual memory chips is perpendicular to the longitudinal direction of the PCB **1**. According to the invention, the memory chip **4**, **5**, **14**, **15**, **18** and **19** are then perpendicular to the memory chips of the "conventional" row, such that these rotated memory chips extend with their longitudinal direction in the longitudinal direction of the PCB **1**. In this case, the rotated memory chips **4**, **5**, **14**, **15**, **18** and **19** lie between the row of the "conventional" memory chips and the pins **22**. In this way, the longest distance between the DQ terminals of the memory chips **2**, **3**, **6** to **13**, **16** and **17** and the connector edge **24** does not exceed a value of about 850 mils (2.16 cm).

[0026] Fig. 2 shows a plan view of a further embodiment of the invention, wherein the register **21**, in contrast to the embodiment of **Fig.** 1, lies with its longitudinal direction in the longitudinal direction of the PCB **1**, and wherein furthermore the resistor elements R are still positioned in the lower region, and wherein the upper edge between the memory chips **2**, **3**, **6** to **13**, **16** and **17** and the upper edge of PCB **1** is only about 0.05 mm. The height h in this case is 28.5 mm, while the width w is 132.8 mm.

[0027] In the two embodiments in Figs. 1 and 2, further memory chips can be mounted in the same or a similar arrangement on the underside of the PCB **1** as well. Moreover, it is possible to stack a plurality of PCBs corresponding to the PCB **1** in Figs. 1 and 2. In this case as well, the PCB can be equipped on both sides or only on one surface with memory chips, etc.

[0028] Fig. 3 shows a block diagram for two adjacent memory chips - by way of example the memory chips **4** and **5**. In this case, it is essential that a dedicated resistor r is assigned to each DQ terminal of each memory chip **4** and **5**. Heretofore, a resistor has specifically only been positioned between a node **23**, at which the DQ terminals of the two memory chips **4**, **5** are brought together, and the pin **22**, as is shown in **Fig.** 4. However, it has been shown that the use of two resistors r - that is, the connection of a separate resistor r to each DQ terminal - achieves an improvement in the decoupling between the respective terminals DQ and the associated bus.

List of reference numbers

1 PCB
2 to 19, B0, B1. . . Memory chips
20 PLL
21 Register
22 Pins
23 Nodes
24 Connector edge
C1 to **C4** Capacitors
R Resistor elements
r resistor
MC Memory controller

Claims

1. A memory module made of a plurality of memory chips (**2** to **19**) which are arranged on at least one first surface of a substantially rectangular circuit board (**1**), which has pins (**22**) along at least one side which forms a connector edge (**24**), connected via a resistor to DQ terminals of the memory chip (**2** to **19**), wherein the likewise substantially rectangular memory chips (**2**, **3**, **6** to **13**, **16**, **17**) are arranged with their shorter sides in a row in the longitudinal direction of the circuit board (**1**) in such a manner that the longer sides of the memory chips (**2**, **3**, **6** to **13**, **16**, **17**) run parallel to each other and perpendicular to the longitudinal direction of the circuit board (**1**), characterized in that at least one additional memory chip (**4**, **5**, **14**, **15**, **18**, **19**) is mounted on the circuit board (**1**) between the row of memory chips (**2**, **3**, **6** to **13**, **16**, **17**) and the connector edge (**24**), the longer side therefore being parallel to the longitudinal direction of the circuit board (**1**).

2. A memory module, in particular according to claim 1, characterized in that, where there are two coupled DQ terminals of two different memory chips (**4**, **5**), each of the DQ terminals is connected via a separate resistor (R) to a pin (**22**) of the connector edge (**24**) (see **Fig**. 3).

3. The memory module according to claim 1 or 2, characterized in that at least one auxiliary block is disposed in the central region of the circuit board.

4. The memory module according to claim 3, characterized in that the auxiliary block is a PLL (**20**) and/or at least one register (**21**).

5. The memory module according to claim 4, characterized in that the longitudinal directions of the PLL (**20**) and the at least one register (**21**) run parallel and/or perpendicular to the longitudinal direction of the circuit board (**1**).

6. The memory module according to one of claims 1 to 5, characterized in that the longest distance between DQ terminals of the memory chip (**2** to **19**) and the connector edge (**24**) does not exceed 2.16 cm (850 mil).

(3 pages of drawings)

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