SDR SDRAM

MT48LC2M32B2 – 512K x 32 x 4 Banks

Features

- PC100-compliant
- Fully synchronous; all signals registered on positive edge of system clock
- Internal pipelined operation; column address can be changed every clock cycle
- Internal banks for hiding row access/precharge
- Programmable burst lengths: 1, 2, 4, 8, or full page
- Auto precharge, includes concurrent auto precharge and auto refresh modes
- Self refresh mode (not available on AT devices)
- Auto refresh
  - 64ms, 4096-cycle refresh (commercial and industrial)
  - 16ms, 4096-cycle refresh (automotive)
- LVTTL-compatible inputs and outputs
- Single 3.3V ±0.3V power supply
- Supports CAS latency (CL) of 1, 2, and 3

Options — Marking

- Configuration
  - 2 Meg x 32 (512K x 32 x 4 banks) — 2M32B2
- Plastic package – OCPL[1]
  - 86-pin TSOP II (400 mil) standard — TG
  - 86-pin TSOP II (400 mil) Pb-free — P
  - 90-ball VFBGA (8mm x 13mm) Pb-free — B5
- Timing – cycle time
  - 5ns (200 MHz) — -5
  - 5.5ns (183 MHz) — -55[2]
  - 6ns (167 MHz) — -6A[3]
  - 6ns (167 MHz) — -6[2]
  - 7ns (143 MHz) — -7[2]
- Operating temperature range
  - Commercial (0°C to +70°C) — None
  - Industrial (–40°C to +85°C) — IT
  - Automotive (–40°C to +105°C) — AT[4]
- Revision — :G/:J

Notes:
1. Off-center parting line.
2. Available only on revision G.
3. Available only on revision J.
4. Contact Micron for availability.

Table 1: Key Timing Parameters

CL = CAS (READ) latency

Speed Grade	Clock Frequency (MHz)	Target tRCD-tRP-CL	tRCD (ns)	tRP (ns)	CL (ns)
-5	200	3-3-3	15	15	15
-55	183	3-3-3	16.5	16.5	16.5
-6A	167	3-3-3	18	18	18
-6	167	3-3-3	18	18	18
-7	143	3-3-3	20	20	21

Table 2: Address Table

Parameter	2 Meg x 32
Configuration	512K x 32 x 4 banks
Refresh count	4K
Row addressing	2K A[10:0]
Bank addressing	4 BA[1:0]
Column addressing	256 A[7:0]

Table 3: 64Mb (x32) SDR Part Numbering

Part Numbers	Architecture	Package
MT48LC2M32B2TG	2 Meg x 32	86-pin TSOP II
MT48LC2M32B2P	2 Meg x 32	86-pin TSOP II
MT48LC2M32B2B5[1]	2 Meg x 32	90-ball VFBGA

Note: 1. FBGA Device Decoder: www.micron.com/decoder.

Contents

General Description 7
Automotive Temperature 7
Functional Block Diagrams 8
Pin and Ball Assignments and Descriptions 9
Package Dimensions 12
Temperature and Thermal Impedance 14
Electrical Specifications 17
Electrical Specifications – I_{DD} Parameters 19
Electrical Specifications – AC Operating Conditions 21
Functional Description 24
Commands 25
COMMAND INHIBIT 25
NO OPERATION (NOP) 26
LOAD MODE REGISTER (LMR) 26
ACTIVE 26
READ 27
WRITE 28
PRECHARGE 29
BURST TERMINATE 29
REFRESH 30
AUTO REFRESH 30
SELF REFRESH 30
Truth Tables 31
Initialization 36
Mode Register 38
Burst Length 40
Burst Type 40
CAS Latency 42
Operating Mode 42
Write Burst Mode 42
Bank/Row Activation 43
READ Operation 44
WRITE Operation 53
Burst Read/Single Write 60
PRECHARGE Operation 61
Auto Precharge 61
AUTO REFRESH Operation 73
SELF REFRESH Operation 75
Power-Down 77
Clock Suspend 78

List of Figures

Figure 1: 2 Meg x 32 Functional Block Diagram 8
Figure 2: 86-Pin TSOP (Top View) 9
Figure 3: 90-Ball VFBGA (Top View) 10
Figure 4: 86-Pin Plastic TSOP II (400 mil) – Package Codes TG/P 12
Figure 5: 90-Ball VFBGA (8mm x 13mm) – Package Codes B5 13
Figure 6: Example: Temperature Test Point Location, 86-Pin TSOP (Top View) 15
Figure 7: Example: Temperature Test Point Location, 90-Ball FBGA (Top View) 16
Figure 8: ACTIVE Command 26
Figure 9: READ Command 27
Figure 10: WRITE Command 28
Figure 11: PRECHARGE Command 29
Figure 12: Initialize and Load Mode Register 37
Figure 13: Mode Register Definition 39
Figure 14: CAS Latency 42
Figure 15: Example: Meeting ^{t}RCD (MIN) When 2 < ^{t}RCD (MIN)/^{t}CK ≤ 3 43
Figure 16: Consecutive READ Bursts 45
Figure 17: Random READ Accesses 46
Figure 18: READ-to-WRITE 47
Figure 19: READ-to-WRITE With Extra Clock Cycle 48
Figure 20: READ-to-PRECHARGE 48
Figure 21: Terminating a READ Burst 49
Figure 22: Alternating Bank Read Accesses 50
Figure 23: READ Continuous Page Burst 51
Figure 24: READ – DQM Operation 52
Figure 25: WRITE Burst 53
Figure 26: WRITE-to-WRITE 54
Figure 27: Random WRITE Cycles 55
Figure 28: WRITE-to-READ 55
Figure 29: WRITE-to-PRECHARGE 56
Figure 30: Terminating a WRITE Burst 57
Figure 31: Alternating Bank Write Accesses 58
Figure 32: WRITE – Continuous Page Burst 59
Figure 33: WRITE – DQM Operation 60
Figure 34: READ With Auto Precharge Interrupted by a READ 62
Figure 35: READ With Auto Precharge Interrupted by a WRITE 63
Figure 36: READ With Auto Precharge 64
Figure 37: READ Without Auto Precharge 65
Figure 38: Single READ With Auto Precharge 66
Figure 39: Single READ Without Auto Precharge 67
Figure 40: WRITE With Auto Precharge Interrupted by a READ 68
Figure 41: WRITE With Auto Precharge Interrupted by a WRITE 68
Figure 42: WRITE With Auto Precharge 69
Figure 43: WRITE Without Auto Precharge 70
Figure 44: Single WRITE With Auto Precharge 71
Figure 45: Single WRITE Without Auto Precharge 72
Figure 46: Auto Refresh Mode 74
Figure 47: Self Refresh Mode 76
Figure 48: Power-Down Mode 77
Figure 49: Clock Suspend During WRITE Burst 78
Figure 50: Clock Suspend During READ Burst 79

Figure 51: Clock Suspend Mode 80

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