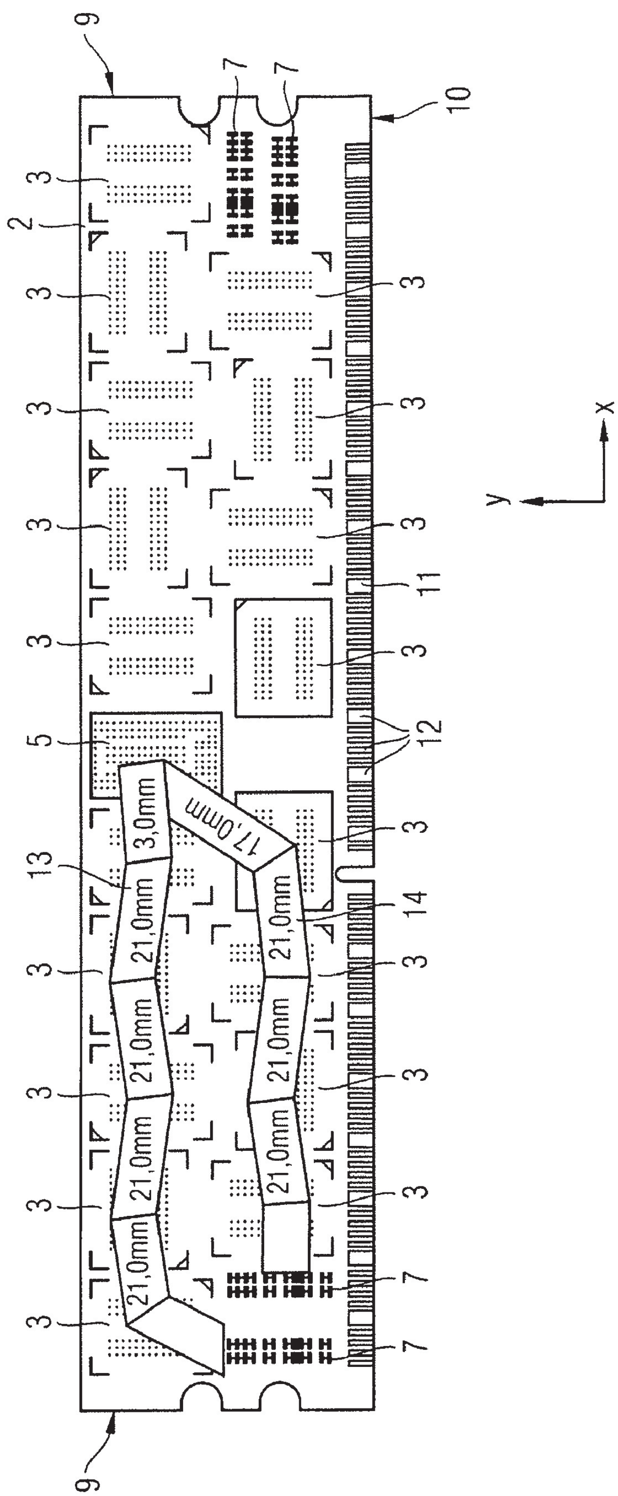
FIG 5


9
7
7
10
2
3
5
12
11
13
14
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21,0mm
21,0mm
x
y

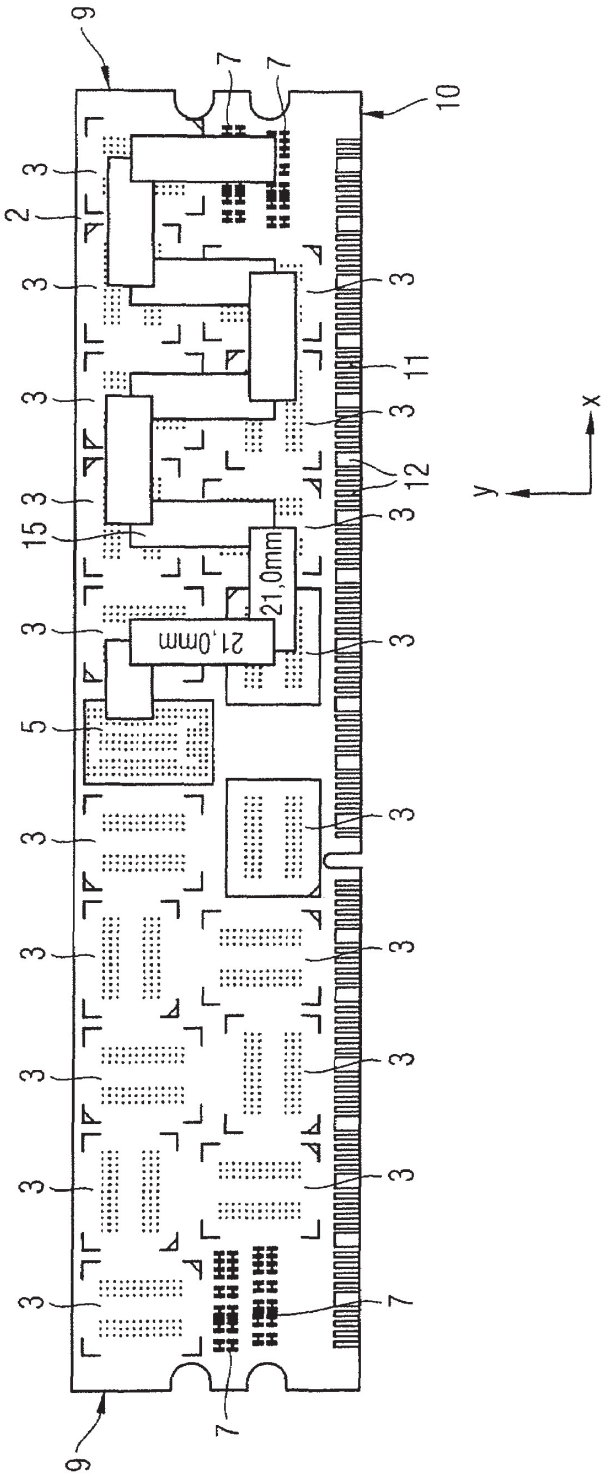


FIG 6

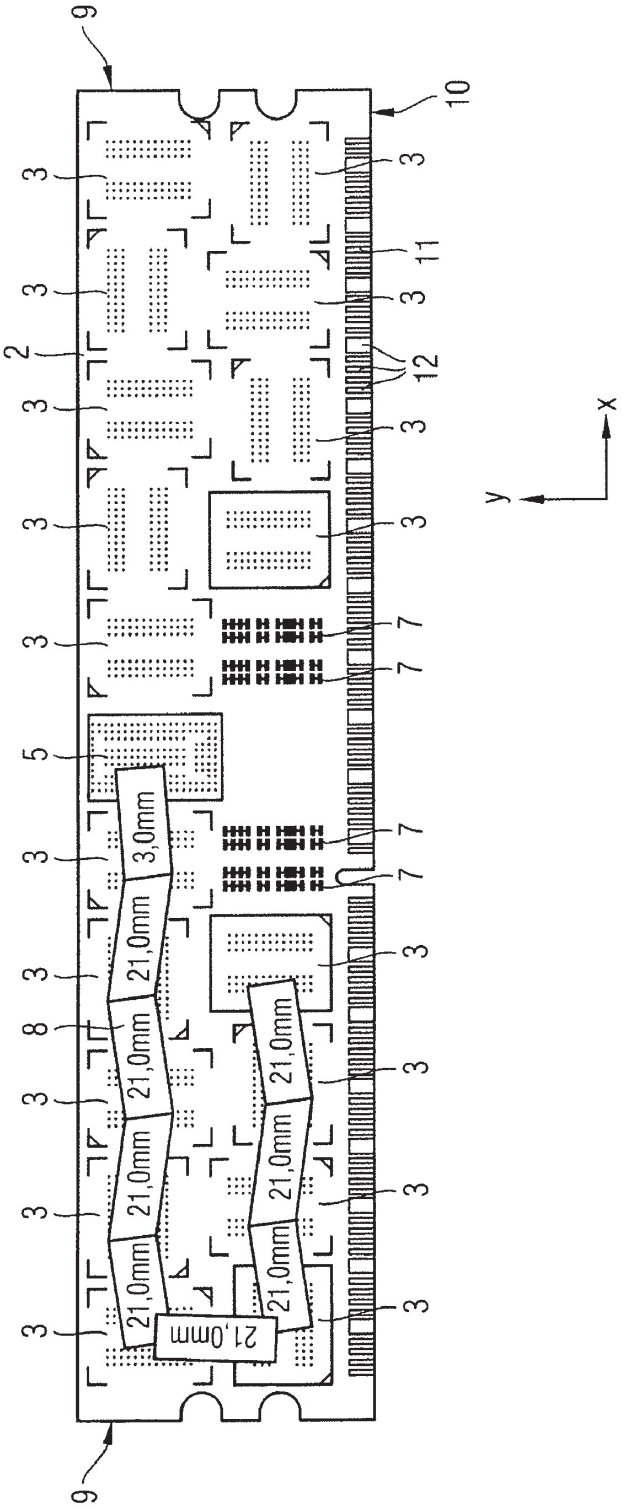


FIG 7

SEMICONDUCTOR MEMORY MODULE

CROSS REFERENCE TO RELATED APPLICATIONS

This application claims priority under 35 USC §119 to German Application No. DE 10 2005 051 998.9, filed on Oct. 31, 2005, and titled "Semiconductor Memory Module," the entire contents of which is hereby incorporated by reference.

FIELD OF THE INVENTION

The present invention relates to production of semiconductor components and more particularly to a semiconductor memory module having an electronic printed circuit board and a plurality of semiconductor memory chips of identical type that are mounted on the printed circuit board.

BACKGROUND

In modern semiconductor memory modules, a plurality of semiconductor memory chips, for example Dynamic Random Access Memories (DRAMs), are mounted on an electronic printed circuit board, which semiconductor memory chips can be operated in parallel and can simultaneously receive electrical signals. In this case, the electronic printed circuit board serves for distributing the electronic signals and may itself be connected to a superordinate electronic unit via a contact strip provided with contact terminals. To distribute the electronic signals and to read out data, the printed circuit board is provided with conductor tracks which may run in a plurality of planes within the printed circuit board.

Due to the rising demand for memory performance, it is desired to mount an increasing number of semiconductor memory chips on an individual semiconductor memory module without increasing the area of the module or of the electronic printed circuit board in the process. Moreover, the line tracks are desired to be as short as possible to keep the signal propagation times as short as possible.

Semiconductor memory modules are typically equipped such that the semiconductor memory chips are arranged symmetrically with respect to the center of the semiconductor memory module. By way of example, between the center and an edge of the semiconductor memory module that runs perpendicularly to the contact strip, at least eight semiconductor memory chips of identical type are mounted next to one another in two rows. In this case, only eight of the semiconductor memory chips serve for storing data, while one semiconductor memory chip serves as an error correction memory chip which compares the signals of the other eight semiconductor memory chips to avoid errors during storage and read-out.

Modern semiconductor memory chips have a square or rectangular form. It generally holds true that the dimensions of the semiconductor memory chips scale with the storage capacity. In particular, modern semiconductor memory chips with a particularly large storage capacity have comparatively large dimensions.

The problem arises that the electronic printed circuit boards for semiconductor memory modules in industrial series production have a standard size, in the case of rectangular memory chips with a large storage capacity, e.g., DDR3-DRAM memory chips, can no longer be arranged in two rows, lying one above another.

Moreover, when arranging the memory chips, care must be taken to ensure that an arrangement is found which exhibits the occurrence of signal propagation times that are as uniform as possible to all of the semiconductor memory chips in conjunction with conductor track lengths that are, to the greatest extent possible, identical in length. Meanwhile, the conductor track lengths are also desired to be as short as possible to keep the signal propagation times as short as possible.

Accordingly, it would be desirable to have a semiconductor memory module that can be equipped with comparatively large rectangular semiconductor memory chips, e.g., DDR3-DRAM memory chips, in two rows lying one above another, with the conductor tracks to the respective semiconductor memory chips being identical in length and as short as possible.

SUMMARY

A semiconductor memory module having an electronic printed circuit board and a plurality of semiconductor memory chips of identical type which are mounted on at least one external area of the printed circuit board is shown and described according to the invention. The printed circuit board has a contact strip that runs at a first edge of the printed circuit board along a first lateral direction (x) and is provided with a plurality of electrical contacts lined up along the first lateral direction (x). The electrical printed circuit board extends along the first lateral direction (x) between two second edges, which usually run in a second lateral direction (y), which is perpendicular to the first lateral direction (x).

Between the center of the printed circuit board and the two second edges of the printed circuit board, at least two adjacent rows of semiconductor chips of identical type are arranged in a manner lying one above another in the second lateral direction (y). In each of the two rows, the semiconductor memory chips of identical type are mounted next to one another along the first lateral direction (x) on the external area of the printed circuit board. The semiconductor memory chips of the two adjacent rows are respectively arranged in an opposite position.

The semiconductor memory chips of identical type have a rectangular form, which is composed of a smaller dimension and a larger dimension, the larger dimension extending in the direction perpendicular to the smaller dimension.

Furthermore, the semiconductor memory chips of identical type in one and the other of the at least two adjacent rows are oriented with their smaller or larger dimensions parallel to the contact strip, the semiconductor memory chips being arranged in an alternate sequence of different dimensions. In other words, within such an arrangement of rows of semiconductor memory chips, a smaller dimension is followed by a larger dimension and a larger dimension is followed by a smaller dimension. To put it in yet another way, successive semiconductor memory chips in a row are in each case rotated by 90° relative to one another.

Furthermore, the semiconductor memory chips are arranged such that one semiconductor memory chip of two semiconductor memory chips of identical type that are arranged in an opposite position in the second lateral direction (y) in the two rows is oriented with its shorter dimension parallel to the contact strip, while the other semiconductor memory chip of these two semiconductor memory chips is oriented with its longer dimension parallel to the contact strip. In this respect, the dimensions of the semiconductor

memory chips that are parallel to the second lateral direction (y) alternate in terms of their magnitude in the second lateral direction (y).

According to an exemplary embodiment of the invention, the arrangement chosen for the semiconductor memory chips makes it possible to achieve an optimum space utilization of the entire usable area of the electronic printed circuit board, so that rectangular semiconductor memory chips having larger dimensioning than in the case of a symmetrical arrangement (in which all the semiconductor memory chips have the same orientation) of rectangular semiconductor memory chips can be mounted onto the electronic printed circuit board. In particular, it is possible to mount rectangular semiconductor memory chips onto the electronic printed circuit board whose larger dimension would not permit a symmetrical two-row arrangement of the semiconductor memory chips, in the case of which the semiconductor memory chips are rotated by 0° or 180° relative to one another, between the center and a respective second edge of the electronic printed circuit board.

In an advantageous manner, at least four semiconductor memory chips of identical type are mounted in a row on the external area of the electrical printed circuit board. In particular, here at least eight semiconductor memory chips of identical type, distributed between two rows arranged in a manner lying one above another in the second lateral direction (y), are mounted on the external area of the electronic printed circuit board.

In one advantageous refinement of the semiconductor memory module according to the invention, the semiconductor memory chips of identical type that are mounted on the external area of the electrical printed circuit board between the center of the printed circuit board and the respective second edge of the printed circuit board are connected by a line bus branching once. In this case, the semiconductor memory chips of one row of the at least two adjacent rows of semiconductor memory chips of identical type are connected one after another to the line tracks of one branch of the line bus, while the semiconductor memory chips of the other row of the at least two adjacent rows of semiconductor memory chips of identical type are connected one after another to the line tracks of the other branch of the line bus.

In a further advantageous refinement of the semiconductor memory module according to the invention, the semiconductor memory chips of identical type that are mounted on the external area of the electrical printed circuit board between the center of the printed circuit board and the respective second edge of the printed circuit board are connected by a line bus, the semiconductor memory chips of one row of the at least two adjacent rows of semiconductor memory chips of identical type being connected one after another to the line tracks of the line bus and the semiconductor memory chips of the other row of the at least two adjacent rows of semiconductor memory chips of identical type being connected one after another to the line tracks of the line bus.

In a further advantageous refinement of the semiconductor memory module according to the invention, the semiconductor memory chips of identical type that are mounted on the external area of the electrical printed circuit board between the center of the printed circuit board and the respective second edge of the printed circuit board are connected by a line bus, on the one hand semiconductor memory chips that are situated oppositely in the second lateral direction (y) and on the other hand semiconductor memory chips that are adjacent in a row being connected alternately to the line tracks of the line bus.

The semiconductor memory module according to the invention is advantageously a DIMM module standardized according to the JEDEC (Joint Electron Device Engineering Council) Standard (JEDEC Solid State Technology Association).

BRIEF DESCRIPTION OF THE DRAWINGS

The invention will now be explained in more detail on the basis of exemplary embodiments, reference being made to the accompanying drawings, in which:

FIGS. **1**A and **1**B show a schematic plan view of a front side (FIG. **1**A) and a rear side (FIG. **1**B) of a conventional memory module;

FIG. **2** shows a schematic plan view of one embodiment of the memory module according to an exemplary embodiment of the invention;

FIG. **3** shows a schematic plan view of a further embodiment of the memory module according to the invention;

FIG. **4** shows a schematic plan view of a further embodiment of the memory module according to the invention;

FIG. **5** shows a schematic plan view of the embodiment of the memory module according to the invention that is shown in FIG. **2**, with schematic illustration of one configuration of the line bus;

FIG. **6** shows a schematic plan view of the embodiment of the memory module according to the invention that is shown in FIG. **2**, with schematic illustration of a further configuration of the line bus; and

FIG. **7** shows a schematic plan view of the embodiment of the memory Module according to the invention that is shown in FIG. **3**, with schematic illustration of a further configuration of the line bus.

DETAILED DESCRIPTION

Identical elements are designated by identical reference numerals in the figures.

First, reference is made to FIGS. **1**A and **1**B which illustrate a schematic plan view of a front side (FIG. **1**A) and a rear side (FIG. **1**B) of a conventional memory module. Such a memory module, which is designated in its entirety by the reference numeral **1**, comprises an electronic printed circuit board **2** with semiconductor memory chips **3** of identical type, e.g., DRAM memory chips, mounted on the front and back external areas of the printed circuit board. The electrical printed circuit board **2** extends along a first lateral direction (x) between two second edges **9** which run in a second lateral direction (y) which is perpendicular to the first lateral direction (x). The square-shaped semiconductor memory chips **3** are arranged in a manner lying one above another in the second lateral direction (y) in two adjacent rows in each case between the center (relative to the first lateral direction (x)) of the printed circuit board and the two second edges **9** of the printed circuit board. In each of the two rows, the semiconductor memory chips **3** of identical type are mounted next to one another along the first lateral direction (x) on the external area of the printed circuit board, wherein the semiconductor memory chips **3** of the two adjacent rows are respectively arranged in an opposite position. A register component **5** which is different from the semiconductor memory chips **3** is arranged in the center of the electronic printed circuit board **2**. A line bus **6**, i.e., control and address bus, enters into the register component **5** from outside, splits up and makes contact with each

individual of the semiconductor memory chips **3** in turn in a forward loop until it leads into a termination **7**, which serves for avoiding undesirable signal reflections. From each semiconductor memory chip **3** proceeds a data line **4**, for reading out the stored data that joins a contact strip that is not specifically illustrated in FIG. **1**. The contact strip is arranged at a first edge **10** of the electronic printed circuit board **2**, wherein the first edge is parallel to the first lateral direction (x) and is provided with a plurality of electrical contacts disposed along the first lateral direction (x). The contact strip may be plugged into a superordinate electronic unit, e.g., a motherboard.

FIGS. **2** to **4** illustrate schematic plan views of embodiments of the memory module according to the invention. A common aspect of the respective embodiments is that a memory module according to the invention comprises an electronic printed circuit board **2** with semiconductor memory chips **3** of identical type, e.g., DDR3-DRAM memory chips, mounted on the front and back external areas of the printed circuit board. The electrical printed circuit board **2** extends along a first lateral direction (x) between two second edges **9** that run in a second lateral direction (y) that is perpendicular to the first lateral direction (x). The rectangular shaped semiconductor memory chips **3** are arranged in a manner lying one above another in the second lateral direction (y) in two adjacent rows in each case between the center, relative to the first lateral direction (x) of the printed circuit board and the two second edges **9** of the printed circuit board. In each of the two rows, the semiconductor memory chips **3** of identical type are mounted next to one another along the first lateral direction (x) on the external area of the printed circuit board, wherein the semiconductor memory chips **3** of the two adjacent rows are respectively arranged in an opposite position. A register component **5** which is different from the semiconductor memory chips **3** is arranged in the center of the electronic printed circuit board **2**. From each semiconductor memory chip proceeds a data line **4**, for reading out the stored data, which joins a contact strip **11**. The contact strip **11**, which is arranged at a first edge **10** of the electronic printed circuit board **2** and wherein the first edge is parallel to the first lateral direction (x), is provided with a multiplicity of electrical contacts **12** disposed along the first lateral direction (x). The contact strip may be plugged into a superordinate electronic unit, e.g., a motherboard.

The semiconductor memory chips **3** of identical type have a rectangular shape comprising a smaller (shorter) dimension a and a larger (longer) dimension b, the larger dimension b extending in the direction perpendicular to the smaller dimension a. The semiconductor memory chips of identical type, in the two adjacent rows on an external area of the electronic printed circuit board **2**, are oriented with their smaller or larger dimensions parallel to the contact strip **11**. In particular, within such an arrangement of rows of semiconductor memory chips, a smaller dimension a is followed by a larger dimension b and a larger dimension b is followed by a smaller dimension a. Consequently, successive semiconductor memory chips **3** of a row are rotated in each case by 90° relative to one another. Furthermore, the semiconductor memory chips **3** are arranged such that one semiconductor memory chip of two semiconductor memory chips of identical type that are arranged in an opposite position in the second lateral direction (y) in the two rows is oriented with its shorter dimension a parallel to the contact strip **11**, while the other semiconductor memory chip of these two semiconductor memory chips is oriented with its longer dimension b parallel to the contact strip **11**. Therefore, maximizing the utilization of the space available on the electronic printed circuit board **2** can be achieved.

In the exemplary embodiments shown, the larger dimension b of the semiconductor memory chips of identical type is dimensioned with a magnitude such that a symmetrical arrangement of semiconductor memory chips **3** situated oppositely in the second lateral direction (y), in the case of which the shorter dimension of the semiconductor memory chips **3** is in each case parallel to the contact strip **11**, is not possible. In this respect, the arrangement of the rectangular semiconductor memory chips according to the invention only enables an arrangement of the semiconductor memory chips in two rows situated opposite one another in the second lateral direction (y).

In other words, the semiconductor memory chips of identical type each have a larger dimension b and a shorter dimension a. In order to maintain a symmetrical arrangement of the memory chips and to minimize the size of the PC board required, the memory chips are arranged in two rows and are situated such that the longer dimensions b of each memory chip are placed facing a shorter dimension a of each adjacent memory chip.

In FIGS. **2** and **3**, in each case five semiconductor memory chips are arranged next to one another in the upper rows between the center of the electronic printed circuit board **2** and the respective second edge **9**, while four semiconductor memory chips are arranged next to one another in the lower rows between the center of the electronic printed circuit board **2** and the respective second edge **9**. Viewed between the center of the electronic printed circuit board **2** and a second edge **9** thereof, only eight semiconductor memory chips of the upper and lower rows serve for data storage, while one semiconductor chip to the left and right of the center of the electronic printed circuit board serves as an error correction chip (ECC). In FIGS. **2** and **3**, the semiconductor memory chips **3** are arranged symmetrically with respect to the center of the electronic printed circuit board **2**.

In the plan view of FIG. **4**, ten semiconductor memory chips **3** of identical type are arranged on an external area to the left of the center of the electronic printed circuit board **2**, while eight semiconductor memory chips **3** of identical type are arranged on an external area to the right of the center. The semiconductor memory chips identified by "ECC" on the left-hand side each serve as an error correction chip. Consequently, the embodiment of the memory module according to the invention in FIG. **4** is not constructed symmetrically with respect to its center.

Altogether, thirty six semiconductor memory chips are mounted on the external areas of the front and rear sides of the memory modules illustrated in FIGS. **2** to **4**. In the embodiments of FIGS. **2** and **3**, respective terminations **7** for the line bus, in particular control and address bus, are arranged adjacent to the semiconductor memory chips of the lower rows.

The embodiments of the memory module according to the invention as shown in FIGS. **2** and **3** differ in that the terminations **7** for the line bus in the embodiment shown in FIG. **2** are arranged in the lower row in each case near to the second edges **9** of the electronic printed circuit board **2**. Meanwhile, the terminations **7** for the line bus in the embodiment shown in FIG. **3** are arranged in the lower row near to the center of the electronic printed circuit board **2**. The embodiment of the memory module according to the invention that is shown in FIG. **4** differs from the embodiments of FIGS. **2** and **3** by virtue of the asymmetrical arrangement of the semiconductor memory chips, set forth above, and the positioning of the terminations **7**, which are

arranged next to the semiconductor memory chips of the upper rows and above the register component **5**.

A line bus, in particular a control and address bus, which is not illustrated in FIGS. **2** to **4** enters into the register component **5** from outside and makes contact with each semiconductor memory chip **3** until it leads into the terminations **7**. The embodiments shown enable various possibilities for the wiring (line bus) of the semiconductor memory chips of identical type that are mounted thereon and is explained in more detail with reference to FIGS. **5** to **7**.

FIGS. **5** and **6** illustrate a schematic plan view of the embodiment of the memory module according to the invention that is shown in FIG. **2**, with a schematic illustration of one configuration of the line bus. Meanwhile, FIG. **7** illustrates a schematic plan view of the embodiment of the memory module according to the invention that is shown in FIG. **3**, with a schematic illustration of one configuration of the line bus.

In order to avoid unnecessary repetition, only the line buses are described in the forthcoming details. With regard to the other features of the memory modules, reference is made to the explanations given regarding the respective FIGS. **2** and **3**.

The line bus, in particular control and address bus, shown in FIG. **5** enters into the register component **5** from outside and makes contact with each semiconductor memory chip **3** until it leads into the terminations **7**. With regard to the semiconductor memory chips arranged between the center of the electronic printed circuit board **2** and the respective second edges **9**, the line bus branches into a branch **13**, the upper branch in FIG. **5**, and a branch **14**, the lower branch in FIG. **5**. In this case, the semiconductor memory chips of the upper row are connected to the upper branch **13** and the semiconductor memory chips of the lower row are connected to the lower branch **14**. Each branch **13**, **14** leads independently into a termination **7**. Such a wiring has the advantage that conductor track lengths that are identical in length and comparatively short can be obtained between the semiconductor memory chips **3**. In the example shown, the conductor track length between adjacent semiconductor memory chips is 21.0 mm. Moreover, the conductor track length between the register component **5** and the adjacent semiconductor memory chips is comparatively short, e.g., 3.0 mm to the semiconductor memory chip of the upper row and, e.g., 17.0 mm to the semiconductor memory chip of the lower row.

The line bus **15**, in particular a control and address bus, shown in FIG. **6** enters into the register component **5** from outside and makes contact with each semiconductor memory chip **3** until it leads into the terminations **7**. In this case, the semiconductor memory chips of identical type that are mounted on the external area of the electrical printed circuit board **2** between the center of the printed circuit board **2** and the respective second edge **9** are connected such that the semiconductor memory chips that are situated oppositely in the second lateral direction (y) and the semiconductor memory chips that are adjacent in a row are connected alternately to the line tracks of the line bus. Conductor track lengths which run parallel to the first lateral direction (x) and those which run parallel to the second lateral direction (y) in this case, advantageously, have an identical and comparatively short length, e.g., 21.0 mm in the exemplary embodiment shown.

The line bus **8**, in particular a control and address bus, shown in FIG. **7** enters into the register component **5** from outside and makes contact with each semiconductor memory chip **3** until it leads into the terminations **7**. In this case, the semiconductor memory chips of the upper row, viewed in the second lateral direction (y), of the two adjacent rows of semiconductor memory chips **3** of identical type are connected one after another to the line tracks of the line bus **8** and then the semiconductor memory chips of the lower row of the two adjacent rows are connected one after another to the line tracks of the line bus. Such a wiring has the advantage that conductor track lengths that are identical in length and comparatively short can be obtained between the semiconductor memory chips **3**. In the example shown, the conductor track length between adjacent semiconductor memory chips is, e.g., 21.0 mm. Moreover, the conductor track length between the register component **5** and the adjacent semiconductor memory chip may be comparatively short, e.g., 3.0 mm as shown in FIG. **7**.

A line bus, such as that illustrated in FIG. **7**, may be used for the embodiment of the memory module according to the invention that is shown in FIG. **4**. In this case, in contrast to the line bus of FIG. **7**, the semiconductor memory chips of the lower row viewed in the second lateral direction (y) of the two adjacent rows of semiconductor memory chips **3** of identical type, are connected one after another to the line tracks of the line bus **8** and then the semiconductor memory chips of the upper row of the two adjacent rows are connected one after another to the line tracks of the line bus.

While the invention has been described in detail and with reference to specific embodiments thereof, it will be apparent to one skilled in the art that various changes and modifications can be made therein without departing from the spirit and scope thereof. Accordingly, it is intended that the present invention covers the modifications and variations of this invention provided they come within the scope of the appended claims and their equivalents.

LIST OF REFERENCE SYMBOLS

1 Semiconductor memory module
2 Electronic printed circuit board
3 Memory chip
4 Data line
5 Register component
6 Line bus
7 Termination
8 Line bus
9 Second edge
10 First edge
11 Contact strip
12 Contact
13 Upper line bus branch
14 Lower line bus branch
15 Line bus

What is claimed is:

1. A semiconductor memory module, comprising:

an electronic printed circuit board including a contact strip that extends at a first edge of the printed circuit board along a first lateral direction and a plurality of electrical contacts disposed along the first lateral direction between two second edges that extend in a second lateral direction that is perpendicular to the first lateral direction; and

a plurality of semiconductor memory chips of substantially identical type mounted on at least one external area of the printed circuit board and having a rectangular form with a shorter dimension and a longer dimension in a direction perpendicular to the shorter dimension, the memory chips being arranged in at least two rows, each row extending, in the first lateral

direction, between a center of the printed circuit board and a respective second edge, wherein the memory chips in each row are arranged in an alternating sequence of opposite orientations with the longer dimension of each memory chip being parallel with the shorter dimension of adjacent memory chips in the same row, and wherein memory chips aligned in the second lateral direction and lying in respective adjacent rows have opposite orientations.

2. The semiconductor memory module according to claim **1**, wherein the semiconductor memory chips include at least four semiconductor memory chips that are mounted in a row on the external area of the electrical printed circuit board.

3. The semiconductor memory module according to claim **1**, wherein the semiconductor memory chips include nine semiconductor memory chips that are distributed between two rows arranged in a manner lying one adjacent to another in the second lateral direction.

4. The semiconductor memory module according to claim **1**, further comprising:

a branching separate line bus comprising a first branch and a second branch;

wherein the memory chips mounted on the external area between the center and the respective second edge of the printed circuit board are connected by the branching separate line bus, such that the memory chips of a first row are connected in a series via line tracks of the first branch of the branching separate line bus, and the memory chips of a second row are connected in a series via line tracks of the second branch of the branch separate line bus.

5. The semiconductor memory module according to claim **1**, further comprising:

a separate line bus comprising line tracks;

wherein the memory chips mounted on the external area between the center and the respective second edge of the printed circuit board are connected by the separate line bus, such that the memory chips of a first row are connected in series via the line tracks of the separate line bus and the semiconductor memory chips of an adjacent second row are connected in series via the line tracks of the separate line bus.

6. The semiconductor memory module according to claim **1**, further comprising:

a separate line bus comprising line tracks;

wherein the memory chips mounted on the external area between the center and the respective second edge of the printed circuit board are connected by the separate line bus, such that the line tracks of the separate line bus extend in a serpentine path between the center and the respective second edge of the printed circuit board and connect the memory chips of first and second rows in series, with the line tracks alternately connecting adjacent memory chips in the same row and adjacent memory chips in different rows.

7. The semiconductor memory module as claimed in claim **1**, wherein the semiconductor memory module is standardized in accordance with a Joint Electron Device Engineering Council (JEDEC) Solid State Technology Association Standard.

* * * * *

EXHIBIT 6

US007334150B2

(12) **United States Patent**
Ruckerbauer et al.

(10) **Patent No.: US 7,334,150 B2**
(45) **Date of Patent: Feb. 19, 2008**

(54) **MEMORY MODULE WITH A CLOCK SIGNAL REGENERATION CIRCUIT AND A REGISTER CIRCUIT FOR TEMPORARILY STORING THE INCOMING COMMAND AND ADDRESS SIGNALS**

(75) Inventors: **Hermann Ruckerbauer**, Moos (DE); **Abdallah Bacha**, Munich (DE); **Christian Sichert**, Munich (DE); **Dominique Savignac**, Ismaning (DE); **Peter Gregorius**, Munich (DE); **Paul Wallner**, Prien (DE)

(73) Assignee: **Infineon Technologies AG**, Neubiberg (DE)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 439 days.

(21) Appl. No.: **11/002,148**

(22) Filed: **Dec. 3, 2004**

(65) **Prior Publication Data**

US 2006/0123265 A1 Jun. 8, 2006

(51) **Int. Cl.**
G06F 1/04 (2006.01)

(52) **U.S. Cl.** **713/500**; 713/600

(58) **Field of Classification Search** 713/500, 713/600; 365/223

See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

7,155,627	B2 *	12/2006	Matsui	713/401
2002/0129215	A1	9/2002	Yoo et al.	
2003/0221044	A1	11/2003	Nishio	
2004/0100812	A1	5/2004	Wu	

* cited by examiner

Primary Examiner—Chun Cao
(74) *Attorney, Agent, or Firm*—Edell, Shapiro & Finnan, LLC

(57) **ABSTRACT**

A semiconductor memory module includes a plurality of semiconductor memory chips and bus signal lines that supply an incoming clock signal and incoming command and address signals to the semiconductor memory chips. A clock signal regeneration circuit and a register circuit are arranged on the semiconductor memory module in a common chip packing connected to the bus signal lines. The clock signal regeneration circuit and the register circuit respectively condition the incoming clock signal and temporarily store the incoming command and address signals, respectively multiply the conditioned clock signal and the temporarily stored command and address signals by a factor of 1:X, and respectively supply to the semiconductor memory chips the conditioned clock signal and the temporarily stored command and address signals.

17 Claims, 5 Drawing Sheets

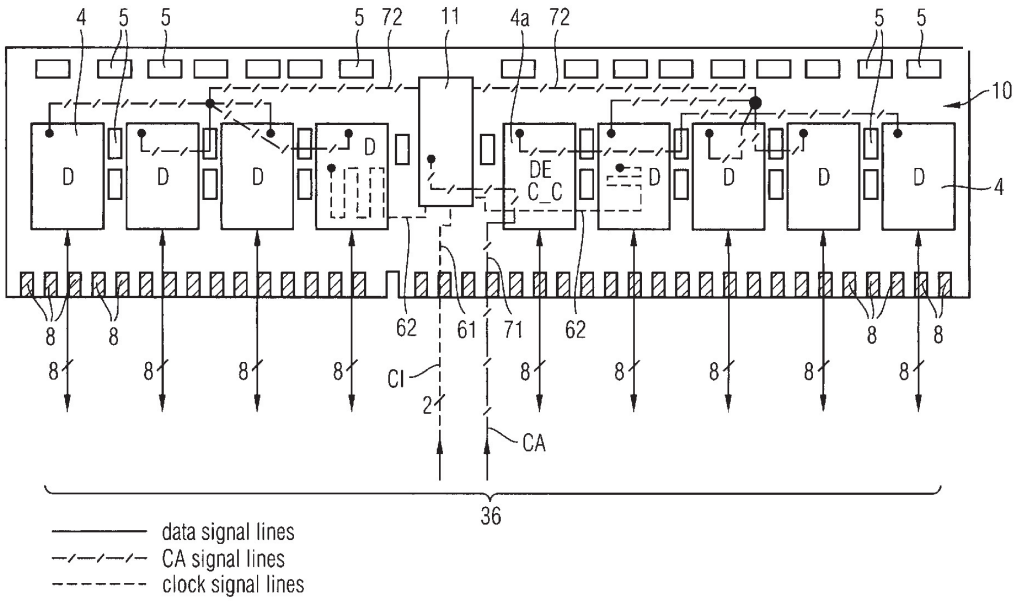
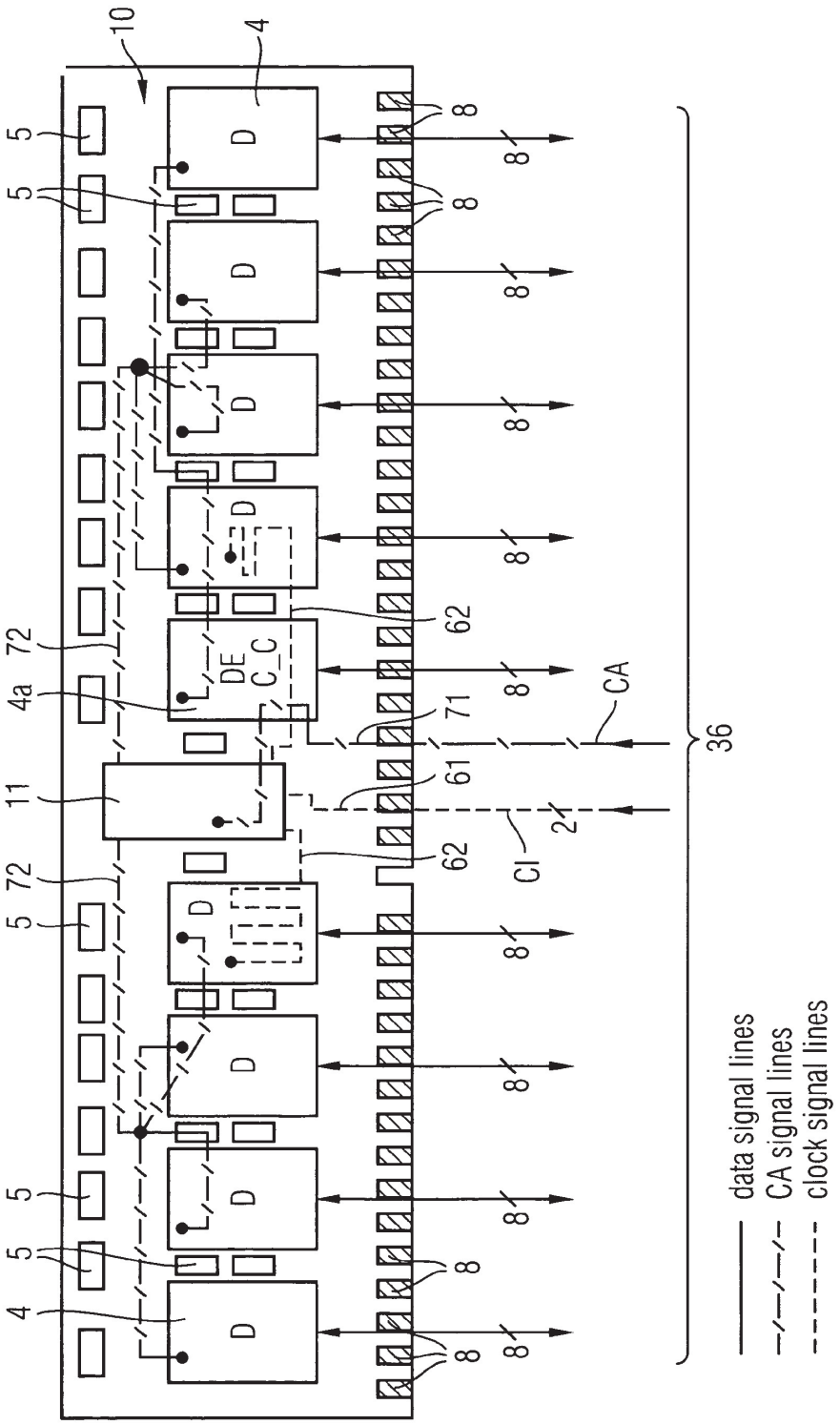


FIG 1


10
4
5
5
D
8
72
4a
DE
C_C
62
71
61
CA
36
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21
CI
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data signal lines
CA signal lines
clock signal lines

FIG 2

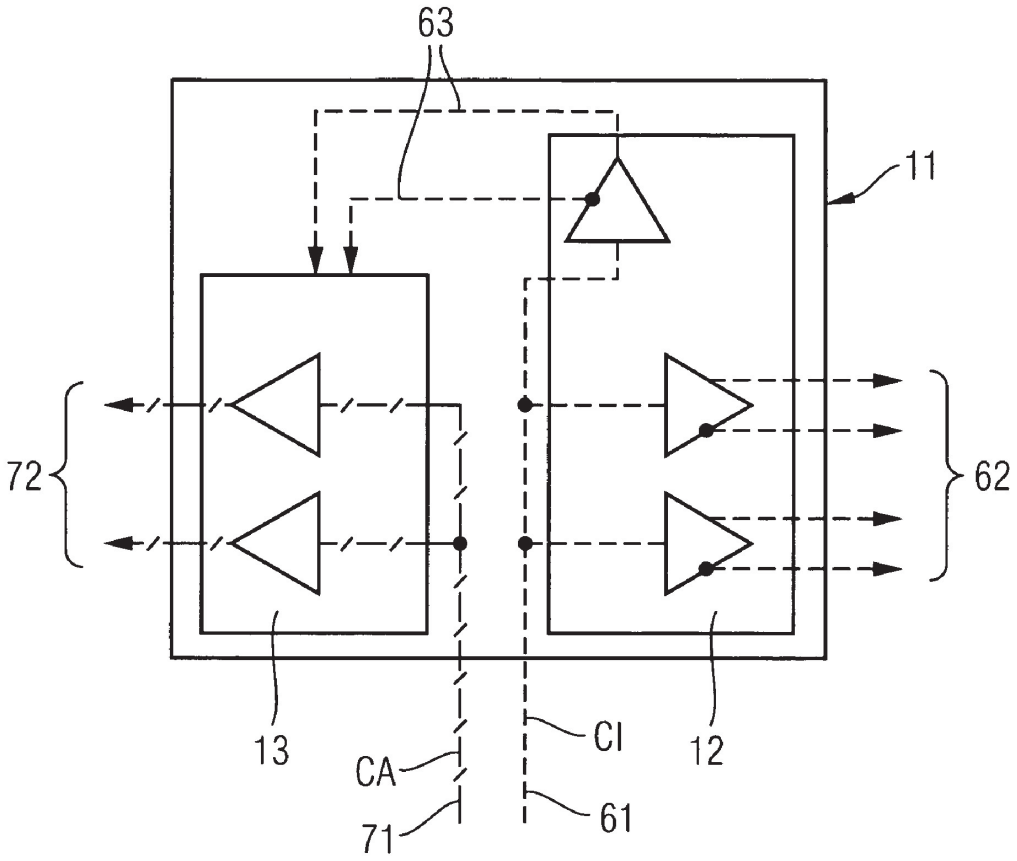
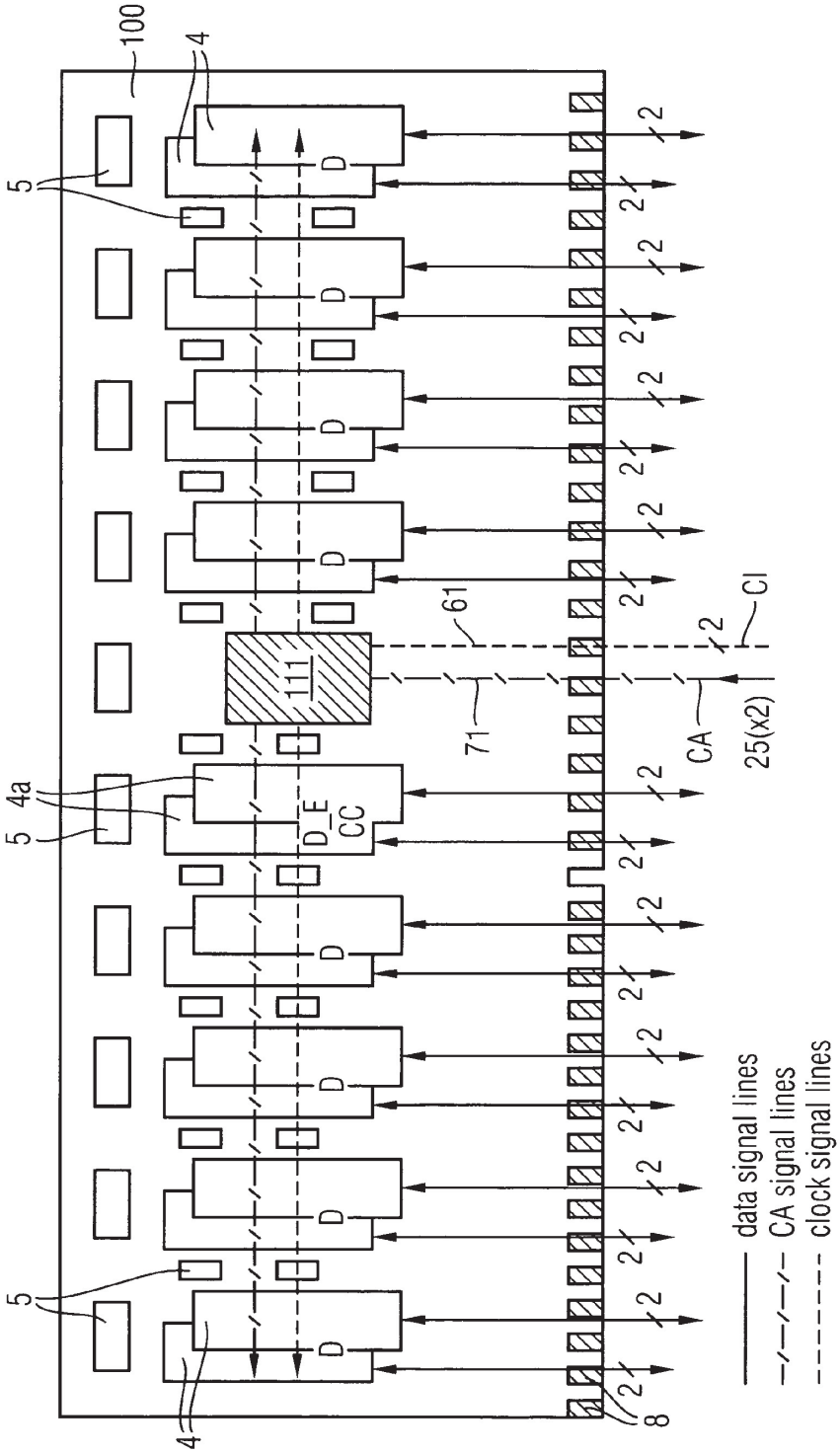


FIG 3


100
4
5
D
2
61
CI
111
71
CA
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4a
D_E
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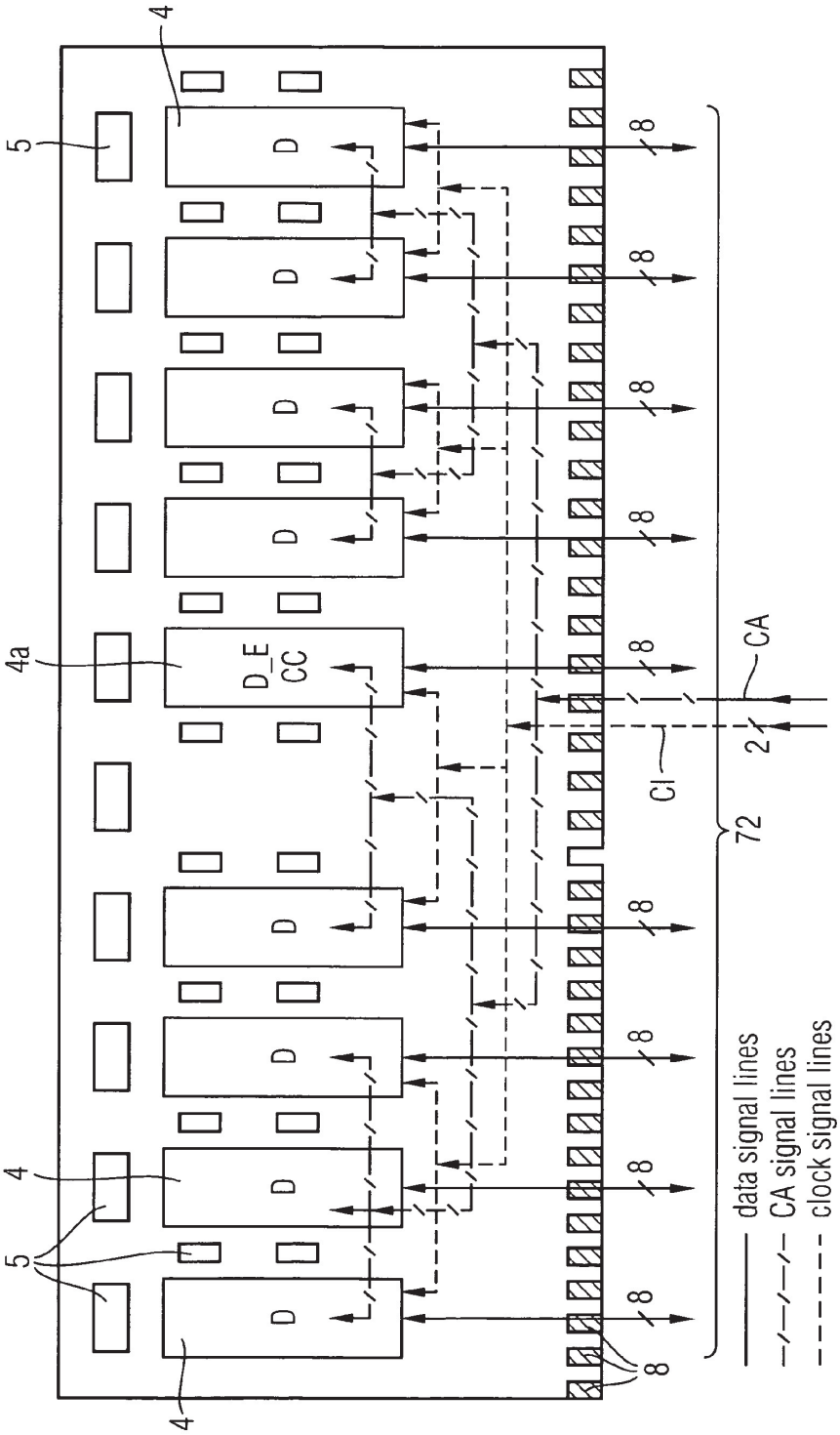
data signal lines
CA signal lines
clock signal lines

FIG 4


4
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CI
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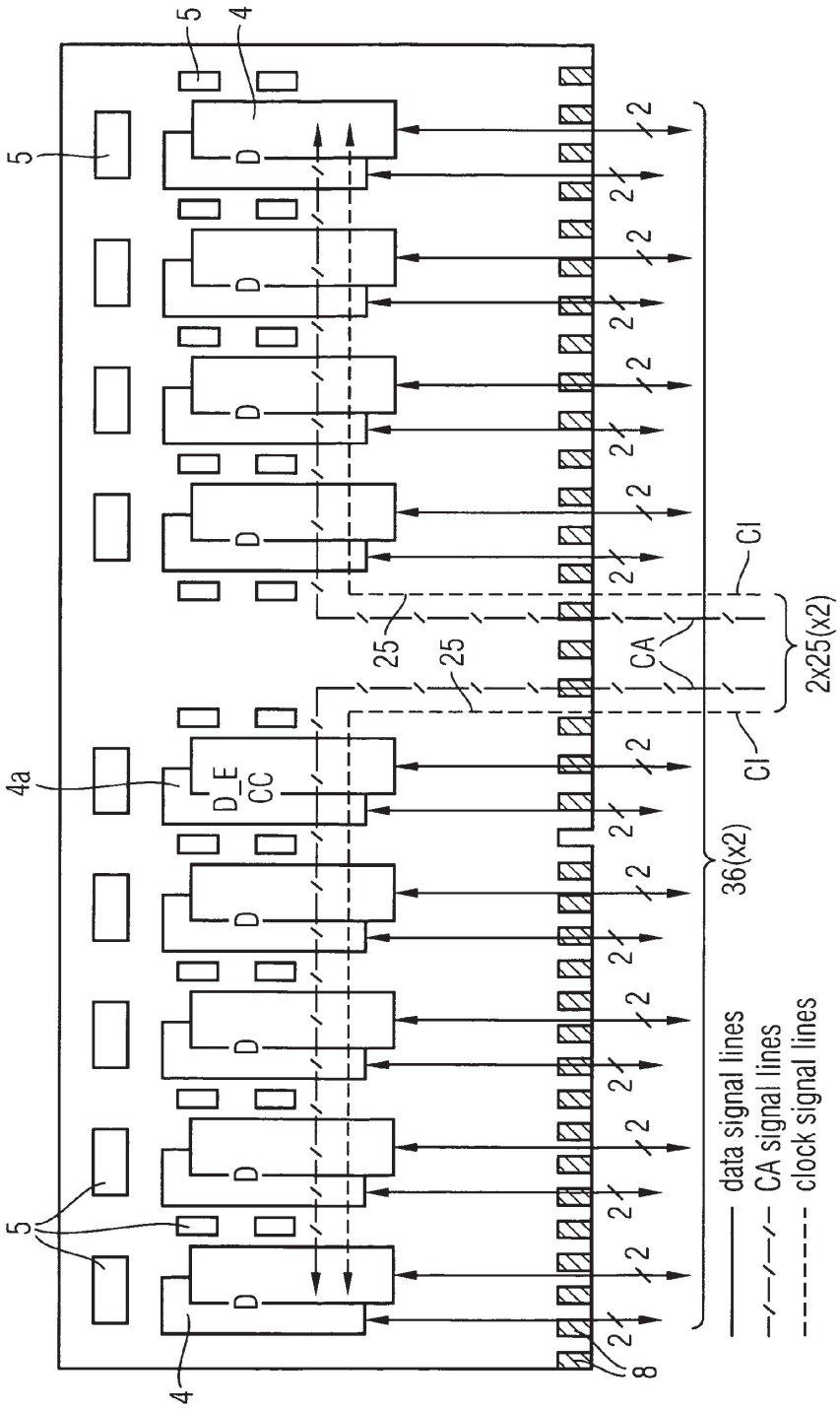
72
data signal lines
CA signal lines
clock signal lines

FIG 5


5
4
D
2
21
25
CA
CI
2x25(x2)
4a
D_E
CC
36(x2)
8
data signal lines
CA signal lines
clock signal lines

MEMORY MODULE WITH A CLOCK SIGNAL REGENERATION CIRCUIT AND A REGISTER CIRCUIT FOR TEMPORARILY STORING THE INCOMING COMMAND AND ADDRESS SIGNALS

FIELD OF THE INVENTION

The present invention relates to a semiconductor memory module, wherein several semiconductor memory chips and bus signal lines, each of which supplies an incoming clock signal as well as incoming command and address signals to at least the semiconductor memory chips, and a semiconductor circuit which comprises a buffer register circuit and a clock signal regeneration circuit are arranged on the semiconductor memory module.

BACKGROUND

Present memory systems (DDR1; DDR2; DDR3) provide the possibility of supplying the DIMM command/address bus transferring the command and address signals (CA) with only one version (copy) of the CA bus, for example via a hybrid-T or fly-by bus. With further increasing speeds and considering the high parallelism at the CA bus (for example up to 36 memory chips per CA bus), the conventional transfer of command and address signals is no longer possible.

A potential solution to the above-mentioned problem lies in using two copies of the CA bus. This, however, increases the pin number per memory channel (for example by 25 CA signals and the pins required for the necessary shielding). Because of the high bit rate on the data lines, a differential signal transfer is considered for successor technologies of the DDR3 system, for example for DDR4. For differential signal transfer, however, the number of pins required is distinctly higher, the implementation thereof being very difficult from a technical point of view (or causing high cost). This involves the pin number at the connector of the semiconductor memory module, the pin number at the memory controller and the routing on the motherboard.

Since, owing to the high bit rates of the successor technologies of the DDR system, only fly-by busses or point-to-point (P2P) busses will be possible, any clock signal required for synchronization must also be transferred differentially together with the CA signals.

The exemplary arrangement of DDR2 systems according to the state-of-the-art shown in the accompanying FIG. **4** is a schematic layout view of a DDR2 DIMM semiconductor memory module, wherein the CA signals CA coming from an external CA bus and the assigned clock signals Cl on the semiconductor circuit module are transferred to the DDR2 DIMM semiconductor memory module via a hybrid-T bus structure (the lines transferring the differential clock signals Cl are presented by broken lines and the lines transferring the differential CA signals are presented by dash-dotted lines). In the example, semiconductor memory chips **4** each storing eight data items D and an additional error correction chip (D-E-CC) **4***a* and additional passive components **5** are arranged on the DIMM semiconductor memory module. The data pertaining to the individual memory chips **4** and to the D-E-CC chip **4***a* is each transferred with a width of eight bits, thus being assigned to 72 connector locations or pin contacts **8** in case of this semiconductor module.

The accompanying FIG. **5** is an exemplary schematic view of a potential semiconductor memory module for the DDR4 system, wherein use is being made of two copies of the CA bus in accordance with the above-mentioned theoretical solution. In the example, the differentially supplied CA signals CA including the clock signals Cl require 25×2 (×2) connector locations or pin contacts **8** for a 2N timing. The lines required for shielding are also necessary. In the example shown in FIG. **5**, the write and read data is supplied to each memory chip **4**, **4***a* of the memory channel arranged to the left of the semiconductor memory module and of the memory channel arranged to the right of the semiconductor memory module with a width of two bits and differentially; this results in an X2-based DDR4 DIMM with 2N timing of the CA signals. In case of such a semiconductor memory module which comprises several memory channels or memory banks, the wide routing of the twice as many CA and Cl lines on the semiconductor memory module would limit the installation space for installing the passive components **5**, such as decoupling capacitors, and the space for routing the data signal lines to the semiconductor memory chips to an excessive degree, not to mention the increased number of pins.

SUMMARY

Therefore, the present invention aims at specifying a semiconductor memory module suitable for high-speed semiconductor memory systems such that the above-mentioned drawbacks of the state-of-the-art can be obviated and that the CA and Cl signals are supplied to the semiconductor memory chips arranged on the semiconductor memory module in a space-saving and pin-contact-saving manner and that, at the same time, it is possible to reach the speeds required for transferring the CA and Cl signals. Furthermore, the invention aims at specifying a semiconductor circuit that comprises a clock signal regeneration circuit and a register circuit that are designed to match such a semiconductor memory module.

According to a first aspect of the invention, there is provided a semiconductor memory module comprising a clock signal regeneration circuit and a register circuit arranged on the semiconductor memory module in a common chip packing and connected to bus signal lines, in order to condition the incoming clock signal and to temporarily store the incoming command and address signals and to supply the conditioned clock signal and the temporarily stored command and address signals to semiconductor memory chips after being multiplied by a factor of 1:X.

By using a clock signal regeneration circuit and a register circuit that are commonly accommodated in one chip packing in the manner described above to achieve a multiplication of CA and synchronizing clock signals by a factor of 1:X, it is possible to reach the speeds required for future memory technologies and, at the same time, save installation space and pin contacts on the semiconductor memory module. The combination of register circuit and clock signal regeneration circuit in a common chip packing allows supplying a complete semiconductor memory module (DIMM) with one CA copy from the memory controller. Since the CA signals are multiplied by a factor of 1:X, several CA copies can be provided to several DRAM branches or channels by local generation in the combined clock signal regeneration and register circuit (since, owing to the high bit rates, the higher-speed DDR memory systems succeeding the DDR3 system will facilitate only a fly-by bus structure or a point-to-point bus structure, it is also necessary that an associated clock signal required for synchronization be also conditioned on the semiconductor memory module and transmitted together with the CA signals).

By combining the register circuit with the clock signal regeneration circuit in a common chip packing, as is proposed according to the invention, the operating temperature of the clock signal regeneration circuit is, in addition, lowered. Should the clock signal regeneration circuit be provided as a single chip packing (separated from the register circuit), the operating temperature would significantly exceed the temperature of the memory chips and would increase with the number of loads the clock signal regeneration circuit has to drive. Thus, the combination of the clock signal regeneration circuit with the register circuit proposed by the invention allows an improved distribution of the heat generated by the clock signal regeneration circuit. The combination according to the invention of the clock signal regeneration circuit and the register circuit in a common chip packing causes the operating temperature of the common chip packing to drop to the temperature level of the semiconductor memory chip. Hence, the semiconductor memory module according to the invention, comprising the clock signal regeneration circuit that is accommodated in a common chip packing together with the register circuit, is of particular advantage when used in very densely packed semiconductor memory modules, for example in DIMM semiconductor memory modules that are fitted with several DDR-DRAM chips of the DDR systems succeeding the DDR3 system, because the module space saved through the routing of the CA signals can be used for the passive and active components in case of semiconductor modules that are fitted with such a high component density.

Preferably, the clock signal regeneration circuit comprises a phase locked loop (PLL) circuit. As previously mentioned, the clock signal and the clock signal conditioned by the clock signal regeneration circuit are each supplied via differential clock signal lines in case of the planned high-speed memory systems.

In one embodiment of the semiconductor memory module according to the invention, the clock signal regeneration circuit and the register circuit are arranged as separate partial chips (dies) in the common packing. These partial chips may, for example, be stacked in the chip packing.

By supplying the clock signal conditioned by the clock signal regeneration circuit to the register circuit inside the chip packing, the space required for these differential clock signal lines on the semiconductor memory module is advantageously reduced.

According to another embodiment of the semiconductor memory module of the invention, the clock signal regeneration circuit and the register circuit are integrated on one common chip (die) in the packing. This second embodiment is advantageous in that the chip area of the common clock signal regeneration and register circuit is reduced.

Preferably, the chip packing containing the clock signal regeneration circuit and the register circuit is essentially arranged at a central position on the semiconductor circuit module.

In the semiconductor circuit module according to the invention, the bus lines of the command and address signals including the signal lines for the clock signal that is also transferred, preferably (but not necessarily) form a fly-by bus structure.

The register and clock signal regeneration circuits are, preferably, designed such that they each multiply the clock signal and the command and address signal by a factor of 1:2.

In one embodiment, the semiconductor memory module can be an RDIMM module and can be fitted with DDR-DRAM semiconductor memory chips.

BRIEF DESCRIPTION OF THE DRAWINGS

The above and further advantageous elements of a semiconductor memory module according to the invention as well as of an appropriate semiconductor circuit comprising a clock signal regeneration circuit and a register circuit are illustrated in more detail in the following description, with reference being made to the accompanying drawing, wherein:

FIG. **1** is a schematic layout view of a first embodiment of a semiconductor memory module according to the invention;

FIG. **2** is a schematic top view of the clock signal regeneration circuit and register circuit in a common chip packing according to a first executive example;

FIG. **3** is a schematic layout view of a second embodiment of a semiconductor memory module according to the invention;

FIG. **4** is a schematic layout view of the afore described semiconductor memory module with hybrid-T bus structure for the clock signal and command and address signal lines; and

FIG. **5** is a schematic layout view of the afore described semiconductor memory module with fly-by bus structure with two copies of the clock signal and command and address signal bus.

DETAILED DESCRIPTION

In the first embodiment of the invention which is schematically shown in FIG. **1**, a chip packing **11** (shown in detail in FIG. **2**) that contains a clock signal regeneration circuit **12** together with a register circuit **13** is arranged on the semiconductor memory module **10**, an RDIMM module in this example, which is fitted with DDR-DRAM chips **4** each storing eight data items D and a further DDR-DRAM chip **4***a* for error correction (DE_CC), at an approximately central position on the semiconductor memory module **10**. External to the semiconductor memory module **10**, 8-bit-wide data line sections supply write and read data to the DDR-DRAM chips **4** and **4***a*. From pin contacts **8**, differential clock signal input lines **61** supply a clock signal Cl to the common chip packing **11**, and a line section **71** with a specific bit width supplies the command and address input signals CA, also from pin contacts **8** to the common chip packing **11**. It can be seen in FIG. **2** that, in this example, the clock signal regeneration circuit **12** and the register circuit **13** multiply the clock signals **61** and the CA signals **71** by a factor of 1:2 for the command and address signals. Starting at the clock signal regeneration circuit **12** which is, for example, a phase locked loop (PLL) circuit, differential clock signal lines **62** supply the conditioned clock signal to all of the memory chips **4**, **4***a*, each to the left and the right of the module **10**. In addition, differential clock signal lines **63** in the common chip packing **11** supply the conditioned clock signal to the register circuit **13**, as shown in FIG. **2**. From the register circuit **13**, temporarily stored (buffered) command and address signals run via differential command and address signal lines **72** on the semiconductor memory module to the semiconductor memory chips **4**, **4***a*, each to the left and the right of the semiconductor memory module **10**.

The solution proposed according to the invention and comprising the operation of accommodating the clock signal regeneration circuit and the register circuit **13** in a common chip packing **11** is advantageous in that space is saved on the semiconductor memory module **10**, this space saving being

increasingly important the more semiconductor memory chips **4** are arranged on the semiconductor memory module **10**.

By accommodating the clock signal regeneration circuit **12** and the register circuit **13** in a common chip packing **11**, the temperature of the clock signal regeneration circuit **12** will, during operation, assume approximately the same value as the temperature of the semiconductor memory chips **4**, **4***a*.

A comparison of the bus structure with that of the semiconductor memory module already described above in connection with FIG. **4** shows that the first embodiment of the semiconductor memory module **10** according to the invention also implements a hybrid-T bus structure for the clock signal lines and the CA signal lines.

In a first executive example, the clock signal regeneration circuit **12** and the register circuit **13** can be arranged in the common chip packing **11** according to FIG. **2**, i.e., either next to each other as separate partial chips (dies) or stacked one above the other as separate partial chips (dies) in a space-saving manner (not shown in FIG. **2**).

The accompanying FIG. **3** shows a schematic layout view of a second embodiment of a semiconductor memory module **100** according to the invention. In case of this second embodiment, the semiconductor memory chips **4**, **4***a* that are arranged on the semiconductor memory module **100** form a DDR4-DIMM module based on a x2 data structure (as shown) or a x4 data structure (not shown). A common chip packing **111** which is arranged at an approximately central position on the semiconductor memory module **100**, as was the case in the first embodiment according to FIG. **1**, accommodates a clock signal regeneration circuit **12** and an address and command signal register circuit **13**, each for multiplying a clock signal Cl supplied via differential clock signal input lines **61** by a factor of 1:2 as well as for temporarily storing/buffering and multiplying command and address signals CA that are supplied to the module **100** via CA lines **71** by a factor of 1:2. In the second embodiment of the semiconductor memory module **100** shown in FIG. **3**, the differential command and address signals CA are supplied via the input CA lines **71** and the differential clock signal Cl and via the differential clock signal input lines **61** by means of a fly-by or point-to-point bus structure, because a fly-by bus or point-to-point (P2P) bus is the only bus structure that is possible with the high bit rates of the DDR systems succeeding the DDR3 system. In the second embodiment of the semiconductor memory module **100** shown in FIG. **3**, the timing of the CA signals CA through the clock signals Cl is achieved by means of 1N timing, this, however, not limiting the scope of the present invention.

In the second embodiment shown in FIG. **3**, the clock signal conditioning and command and address signal register circuits accommodated in the common chip packing **111** each multiply the CA signals CA and the clock signals Cl by a factor of 1:2 by supplying, via differential clock signal lines, the clock signals Cl conditioned by the clock signal conditioning circuit in the common chip packing **111** to the semiconductor memory chips **4**, **4***a* that are each arranged to the left and the right of the semiconductor memory module **100**. The same applies to the temporarily stored/buffered CA signals.

In general, the invention proposes to arrange on the semiconductor memory module a clock signal regeneration circuit and a register circuit in a common chip packing and to connect them to the bus signal lines **61**, **71** supplying the command address signals CA and the clock signal Cl such that the incoming clock signal Cl is conditioned and the incoming command and address signals CA are temporarily stored, in order to multiply these signals by a factor of 1:X and to supply the conditioned clock signal Cl and the temporarily stored command and address signals CA to X semiconductor memory chip groups that are arranged on the semiconductor memory module. Although only two semiconductor memory chip groups are provided in the two embodiments of the semiconductor memory module **10** and **100** shown as examples in FIGS. **1** and **3**, those skilled in the art will immediately see that it is also possible to arrange more than two semiconductor memory chip groups or DRAM branches on the semiconductor memory module, which can then be activated by means of the clock signals and command and address signals that are multiplied by a factor of 1:X by the clock signal conditioning circuit and the command and address signal register circuit. This allows supplying a complete DIMM with only one CA copy from a memory controller (not shown). By the CA and Cl signals being multiplied by a factor of 1:X, several DRAM groups can be supplied by means of the local generation of several CA and Cl copies. The drawback of the double pin number of the pin contacts **8**, an element that is characteristic of the semiconductor memory module shown in FIG. **5** where two copies of the CA bus signals and the Cl bus signals must be supplied, has been obviated in the embodiments of the invention that have been described above in connection with FIGS. **1**-**3**. Furthermore, the high speeds required for future memory technologies can be reached by using a combined clock signal conditioning and register circuit **11**, **111** for multiplying the CA signals and clock signals by a factor of 1:X, as is proposed according to the invention.

The clock signal conditioning circuit and the register circuit can be arranged either next to each other as separate partial chips, as is shown in FIG. **2**, or stacked one above the other as separate partial chips. An alternative proposed by the invention provides that the two functionalities of the clock signal conditioning circuit and the register circuit are integrated on a common chip (combined die).

Having described preferred embodiments of a new and improved semiconductor memory module, it is believed that other modifications, variations and changes will be suggested to those skilled in the art in view of the teachings set forth herein. It is therefore to be understood that all such variations, modifications and changes are believed to fall within the scope of the present invention as defined by the appended claims. Although specific terms are employed herein, they are used in a generic and descriptive sense only and not for purposes of limitation.

LIST OF REFERENCE SYMBOLS

4, **4***a* Semiconductor memory chips
5 Passive components
8 Pin contacts
10, **100** Semiconductor memory module
11, **111** Common chip packing
12 Clock signal regeneration circuit
13 Register circuit
61, **62**, **63** Differential clock signal lines
71, **72** Command and address signal lines
CA Command and address signals
Cl Clock signal
D Data memory chips
DE_C_C Error correction data memory

What is claimed is:

1. A memory module, comprising:

a plurality of memory chips arranged on the memory module;

a plurality of bus signal lines operable to supply an incoming clock signal and incoming command and address signals to at least the memory chips;

a clock signal regeneration circuit configured to generate a plurality of copies of the incoming clock signal and to supply the copies of the incoming clock signal to the memory chips, the copies of the incoming clock signal having a same frequency as the incoming clock signal; and

a register circuit arrange on the memory module in a common chip packing with the clock regeneration circuit and configured to receive one of the copies of the incoming clock signal from the clock regeneration circuit, the register circuit being further configured to temporarily store the incoming command and address signals and to generate a plurality of copies of the incoming command and address signals and supply the copies of the incoming command and address signals to the memory chips, the copies of the incoming command and address signals having a same frequency as the incoming command and address signals.

2. The memory module according to claim 1, wherein the clock signal regeneration circuit comprises a phase locked loop (PLL) circuit.

3. The memory module according to claim 1, wherein the incoming clock signal and the copies of the incoming clock signal are each supplied via differential clock signal lines.

4. The memory module according to claim 1, wherein the clock signal regeneration circuit and the register circuit are arranged as separate partial chips in the common chip packing.

5. The memory module according to claim 1, wherein the clock signal regeneration circuit and the register circuit are integrated on a common chip in the common chip packing.

6. The memory module according to claim 1, wherein the common chip packing is arranged essentially at a central position on the memory module.

7. The memory module according to claim 1, wherein the bus signal lines of the command and address signals comprise a hybrid-T bus structure.

8. The memory module according to claim 1, wherein the bus signal lines of the command and address signals comprise a fly-by bus structure.

9. The memory module according to claim 1, wherein the clock signal regeneration circuit and the register circuit respectively generate two copies of the clock signal and the command and address signals for distribution to the memory chips.

10. The memory module according to claim 1, wherein the memory module comprises an RDIMM module.

11. The memory module according to claim 1, wherein the memory chips comprise DDR-DRAM memories.

12. An integrated circuit, comprising:

a clock signal regeneration circuit configured to generate a plurality of copies of a clock signal, wherein the copies of the clock signal have a same frequency as the clock signal; and

a register circuit arranged in a common chip packing with the clock signal regeneration circuit and configured to temporarily store incoming command and address signals and to generate a plurality of copies of the incoming command and address signals, wherein the copies of the incoming command and address signals have a same frequency as the incoming command and address signals, and

wherein the clock signal regeneration circuit supplies one of the copies of the clock signal to the register circuit.

13. The integrated circuit according to claim 12, wherein the clock signal regeneration circuit comprises a phase locked loop (PLL) circuit.

14. The integrated circuit according to claim 13, wherein the clock signal regeneration circuit supplies the clock signal as a differential clock signals on differential clock signal lines.

15. The integrated circuit according to claim 14, wherein the clock signal regeneration circuit and the register circuit are arranged as separate partial chips in the common chip packing.

16. The integrated circuit according to claim 14, wherein the clock signal regeneration circuit and the register circuit are integrated on a common chip in the common chip packing.

17. The integrated circuit according to claim 12, wherein the clock signal regeneration circuit and the register circuit respectively generate two copies of the clock signal and the command and address signals for distribution external to the common chip packing.

* * * * *

EXHIBIT 7

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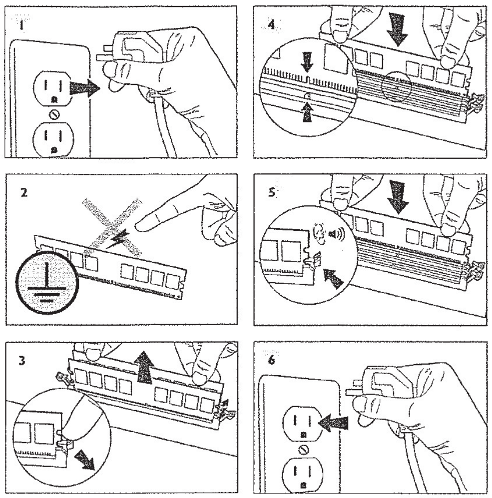

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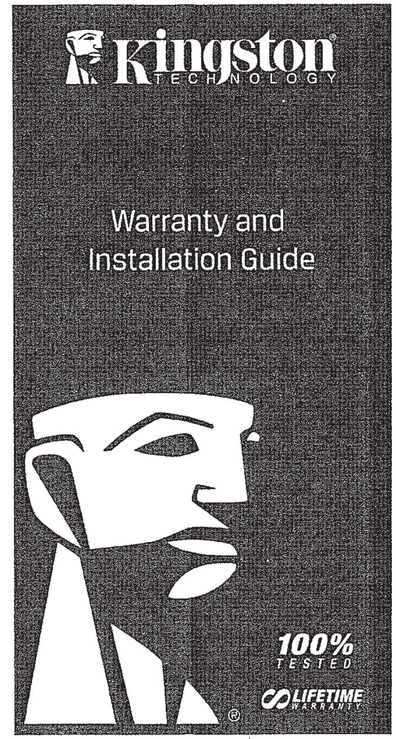

dimm

105

Exhibit 7
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TURKISH

ÖMÜR BOYU GARANTİ ÖZETİ: Garanti, arızalı ürün değişimi veya kanunların izin vermiş olduğu kapsamda ürün bedelinin (ödenen ücretle sınırlı olmak üzere) geri ödenmesiyle sınırlıdır ve devredilemez. Garantinin tamamını Kingston.com/wa adresinden veya e-mail yoluyla alabilirsiniz.

Kurulum öncesinde lütfen Kingston.com/installmemory adresini ziyaret ediniz.

RUSSIAN

ПОЖИЗНЕННАЯ ГАРАНТИЯ: гарантия распространяется на бракованную продукцию, которая подлежит замене или возмещению ее денежной стоимости (по текущей цене), согласно действующему законодательству. Гарантия на продукцию не может быть передана другому лицу. Полная информация о гарантийном обслуживании приведена на сайте Kingston.com/wa.

До начала установки посетите Kingston.com/installmemory

HINDI

अजीवन वारण्टी संक्षेप : वारण्टी दोषपूर्ण प्रोडक्ट के बदले जाने या मौजूदा मूल्य के लौटाए जाने (भाव भी गए भरेगा) तक सीमित है, जो कि कानून द्वारा स्वीकृत सीमा तक है एवं हस्तांतरणीय नहीं है. पूर्ण वारण्टी उपलब्धी Kingston.com/wa पर या मेल के जरिए प्राप्त कर सकते हैं।

Installation से पहले कृपया Kingston.com/installmemory पर जाएं।

THAI

การรับประกันตลอดอายุการใช้งาน : การรับประกันนี้เฉพาะการเปลี่ยนสินค้าที่เกิดข้อบกพร่องหรือชดเชยเป็นมูลค่า ณ ปัจจุบัน (ไม่สามารถชดเชยตามมูลค่าที่ซื้อ) การรับประกันนี้อยู่ภายใต้กฎหมายและไม่สามารถเปลี่ยนแปลงได้ ข้อมูลการรับประกันฉบับเต็มได้ที่ Kingston.com/wa

ก่อนทำการติดตั้ง ค้นหาข้อมูลได้ที่ Kingston.com/installmemory

SIMPLIFIED CHINESE

终身保固条款概要：保固只限于缺陷产品的维修、更换或者退还当前价款（只针对已付款产品），本保固在法律允许的范围内实施，且不可转移。完整保固内容请浏览 Kingston.com/wa，或者通过电子邮件联系我们。

安装之前，请浏览 Kingston.com/installmemory

TRADITIONAL CHINESE

終身保固摘錄概要：保固只限於有瑕疵的產品維修、更換或者退還購買款項（只針對已付款產品），本保固在法律允許的範圍內實施，且不可轉讓。完整保固內容請瀏覽 Kingston.com/wa，或者透過電子郵件與我們聯繫。

安裝之前，請先瀏覽 Kingston.com/installmemory

JAPANESE

生涯保証の概要：保証は法で認められている範囲内で、不具合品の交換、または現行価値の返金（購入金額に限定）に限られ、譲渡することはできません。完全な保証はKingston.com/waでまたは電子メールによって行われます。

インストールの前に、Kingston.com/installmemoryにアクセスしてください

ARABIC

مختصر الضمان لمدى الحياة: يقتصر الضمان على استبدال المنتج التالف أو سداد قيمته الحالية (بمقتصر على السعر الذي تم سداده). وذلك بالقدر المسموح به قانونيًا. ولا يجوز تحويله إلى طرف آخر. يمكن الحصول على الضمان الكامل من الموقع Kingston.com/wa أو عبر البريد.

يُرجى -قبل التثبيت- زيارة الموقع Kingston.com/installmemory