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12 *Attorneys for Plaintiff,*  
 13 *Polaris Innovations Limited*

14 UNITED STATES DISTRICT COURT  
 15 CENTRAL DISTRICT OF CALIFORNIA  
 16 SOUTHERN DIVISION

17 POLARIS INNOVATIONS LIMITED, )	Case No. 8:16-cv-300
18 an Irish limited company, )	
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COMPLAINT FOR PATENT INFRINGEMENT

1 Plaintiff Polaris Innovations Limited (“Polaris” or “Plaintiff”) hereby alleges  
2 for its Complaint against Defendant Kingston Technology Company, Inc.  
3 (“Kingston” or “Defendant”) as follows:

4 **JURISDICTION**

5 1. This is an action for patent infringement arising under the patent laws  
6 of the United States, Title 35 of the United States Code. This Court has subject  
7 matter jurisdiction of this action pursuant to 28 U.S.C. §§ 1331 and 1338(a).

8 2. This Court has personal jurisdiction over Kingston. Kingston is  
9 headquartered in the Central District of California, has systematic and continuous  
10 contacts with the forum, and conducts substantial business within this district.  
11 Upon information and belief, Kingston has committed and continues to commit  
12 acts of patent infringement, including making, selling, offering to sell, directly or  
13 through intermediaries, subsidiaries and/or agents, infringing products within this  
14 district, including to customers in this district.

15 **VENUE**

16 3. Venue is proper in this Court pursuant to 28 U.S.C. §§ 1391 and  
17 1400(b) because Kingston is subject to personal jurisdiction in this district, and  
18 because a substantial part of the events giving rise to Polaris’s claims occurred in  
19 this district, and Kingston, which is headquartered in Fountain Valley, California,  
20 has a regular and established place of business within this district.

21 **THE PARTIES**

22 4. Polaris Innovations Limited is a corporation organized and existing  
23 under the laws of Ireland, with its principal place of business at Polaris Innovations  
24 Limited, 29 Earlsfort Terrace, Dublin 2, Republic of Ireland.

25 5. On information and belief, Kingston Technology Company, Inc. is a  
26 corporation organized and existing under the laws of Delaware with its principal  
27 place of business at 17600 Newhope Street, Fountain Valley, California, 92708.  
28

1 **NATURE OF THE ACTION**

2 6. This is a patent infringement action by Polaris to end Kingston’s  
3 unauthorized, willful, and infringing manufacture, use, sale, offering for sale,  
4 and/or importation of products and methods incorporating Polaris’s patented  
5 inventions.

6 7. Polaris holds all substantial rights and interest in the Asserted Patents  
7 described below, including the exclusive right to sue Kingston for infringement  
8 and recover damages.

9 8. Kingston makes, uses, sells, offers for sale, and imports products and  
10 methods that infringe the Asserted Patents. Polaris seeks monetary damages and  
11 prejudgment interest for Kingston’s past and ongoing infringement of the Asserted  
12 Patents.

13 **THE ASSERTED PATENTS**

14 9. On December 5, 2000, the United States Patent and Trademark Office  
15 duly and legally issued U.S. Patent No. 6,157,589 (“the 589 Patent”), entitled  
16 “Dynamic semiconductor memory device and method for initializing a dynamic  
17 semiconductor memory device.” A copy of the 589 Patent is attached hereto as  
18 Ex. 1.

19 10. Polaris owns all substantial right, title, and interest in the 589 Patent,  
20 and holds the right to sue and recover damages for infringement thereof, including  
21 past infringement.

22 11. On August 20, 2002, the United States Patent and Trademark Office  
23 duly and legally issued U.S. Patent No. 6,438,057 B1 (“the 057 Patent”), entitled  
24 “DRAM refresh timing adjustment device, system and method.” A copy of the 057  
25 Patent is attached hereto as Ex. 2.

26 12. Polaris owns all substantial right, title, and interest in the 057 Patent,  
27 and holds the right to sue and recover damages for infringement thereof, including  
28 past infringement.

1           13. On February 1, 2005, the United States Patent and Trademark Office  
2 duly and legally issued U.S. Patent No. 6,850,414 B2 (“the 414 Patent”), entitled  
3 “Electronic printed circuit board having a plurality of identically designed,  
4 housing-encapsulated semiconductor memories.” A copy of the 414 Patent is  
5 attached hereto as Ex. 3.

6           14. Polaris owns all substantial right, title, and interest in the 414 Patent,  
7 and holds the right to sue and recover damages for infringement thereof, including  
8 past infringement.

9           15. On April 17, 2007, the United States Patent and Trademark Office  
10 duly and legally issued U.S. Patent No. 7,206,978 B2 (“the 978 Patent”), entitled  
11 “Error detection in a circuit module.” A copy of the 978 Patent is attached hereto  
12 as Ex. 4.

13           16. Polaris owns all substantial right, title, and interest in the 978 Patent,  
14 and holds the right to sue and recover damages for infringement thereof, including  
15 past infringement.

16           17. On January 1, 2008, the United States Patent and Trademark Office  
17 duly and legally issued U.S. Patent No. 7,315,454 B2 (“the 454 Patent”), entitled  
18 “Semiconductor memory module.” A copy of the 454 Patent is attached hereto as  
19 Ex. 5.

20           18. Polaris owns all substantial right, title, and interest in the 454 Patent,  
21 and holds the right to sue and recover damages for infringement thereof, including  
22 past infringement.

23           19. On February 19, 2008, the United States Patent and Trademark Office  
24 duly and legally issued U.S. Patent No. 7,334,150 B2 (“the 150 Patent”), entitled  
25 “Memory module with a clock signal regeneration circuit and a register circuit for  
26 temporarily storing the incoming command and address signals.” A copy of the  
27 150 Patent is attached hereto as Ex. 6.

28           20. Polaris owns all substantial right, title, and interest in the 150 Patent,

1 and holds the right to sue and recover damages for infringement thereof, including  
2 past infringement.

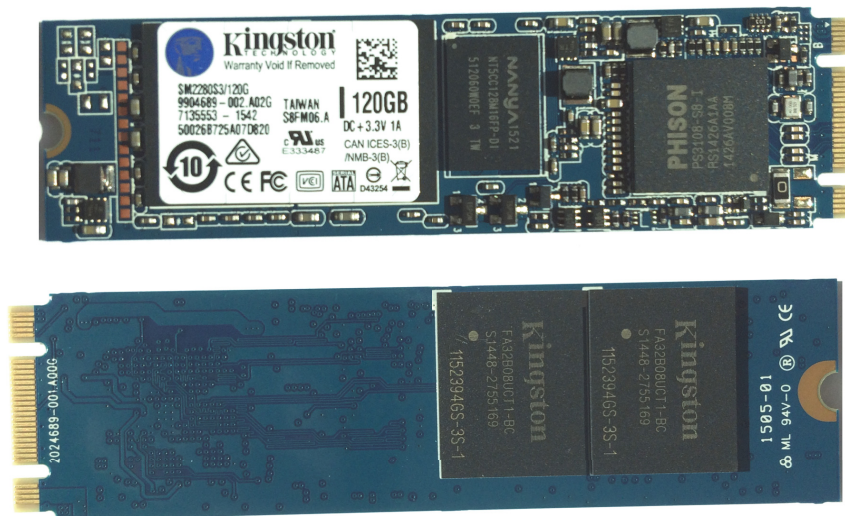
3 **COUNT I:**

4 **INFRINGEMENT OF U.S. PATENT NO. 6,157,589**

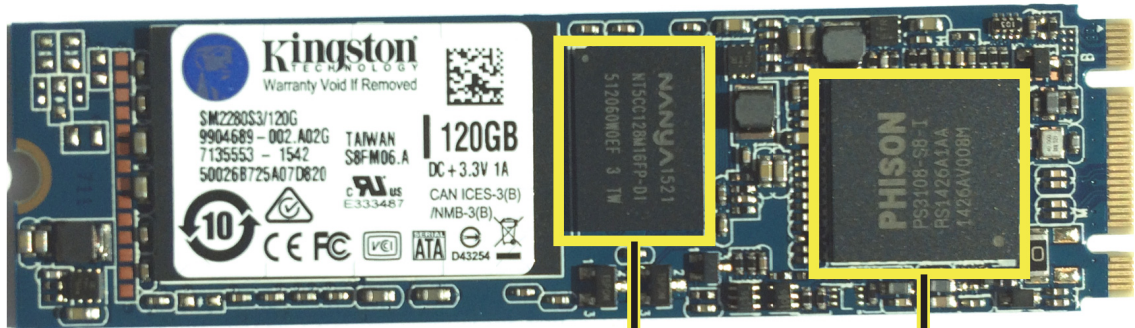
5 21. Polaris incorporates and realleges paragraphs 1-20 above as if fully set  
6 forth herein.

7 22. On information and belief, Kingston has willfully infringed and  
8 continues to willfully infringe one or more claims of the 589 Patent, including, but  
9 not limited to, Claims 11 and 12, pursuant to 35 U.S.C. § 271(a), literally or under  
10 the doctrine of equivalents, by making, using, selling, offering to sell in the United  
11 States without authority, and/or importing into the United States without authority,  
12 solid-state drives (SSDs) performing the claimed methods for initializing a  
13 dynamic semiconductor memory device. These products, the “589 Patent  
14 Infringing Products,” including by way of a non-limiting example only, Kingston’s  
15 SSDs with model number SM2280S3/120G, perform the methods for initializing a  
16 dynamic semiconductor memory device as required by the claims of the 589 Patent.

17 23. By way of example, the front and back views of a representative 589  
18 Patent Infringing Product (SM2280S3/120G) that performs the claimed methods  
19 are shown in the image below.



1 24. The front image of this representative 589 Infringing Product  
2 (SM2280S3/120G) is annotated below for illustration.



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10 DRAM chip (Nanya NT5CC128M16FP-D1)

11 Controller chip (Phison PS3108)

12  
13 Specifically, the 589 Patent Infringing Products, such as SM2280S3/120G, include  
14 a dynamic random access memory (DRAM) chip (labeled Nanya  
15 NT5CC128M16FP in the photo above) and a controller chip (labeled Phison  
16 PS3108 in the photo above). *See generally* 2Gb DDR3 SDRAM H-Die datasheet,  
17 Nanya Technology (“Nanya Datasheet”), *available at*  
18 <http://www.nanya.com/NanyaAdmin/GetFiles.ashx?ID=1199> (last visited February  
19 3, 2016). On information and belief, when Kingston, its customers, and other third  
20 parties turn on the 589 Patent Infringing Products, the controller chip supplies, via  
21 an initialization circuit, a supply voltage stable signal (for example, the Active  
22 Low Asynchronous Reset signal,  $\overline{RESET}$ , *see* Nanya Datasheet at 8) once a supply  
23 voltage has been stabilized (for example, at the time labeled Tb, *see* Nanya  
24 Datasheet, Fig. 3 at 13, and as described in Step 1 of the initialization sequence,  
25 Nanya Datasheet at 11) after the switching-on operation of the dynamic  
26 semiconductor memory device (for example, in the “Reset Procedure” state which  
27 follows the “Power ON” state, Nanya Datasheet, Fig. 2 at 10). The controller chip  
28 also supplies, via an enable circuit of the initialization circuit, an enable signal (for

1 example, the Clock Enable signal, CKE, Nanya Datasheet, Table 3 at 7, which the  
2 DRAM waits for as described in Step 2 of the initialization sequence, Nanya  
3 Datasheet at 11), the initialization circuit receiving the supply voltage stable signal  
4 (for example, as described in Step 2 of the Reset and Initialization Procedure,  
5 Nanya Datasheet at 11) and further command signals (for example, the “Command”  
6 signals, Nanya Datasheet, Fig. 3 at 13) externally applied to the dynamic  
7 semiconductor memory device, after an identification of a predetermined proper  
8 initialization sequence of the further command signals (for example, the Mode  
9 Register Set (“MRS”) and/or ZQ Calibration (“ZQCL”) commands issued in Steps  
10 6-10 of the initialization sequence, Nanya Datasheet at 12-14) the enable signal  
11 being generated (for example, as shown on the CKE line, Nanya Datasheet, Fig. 3  
12 at 13, and as described in Step 3 of the initialization sequence, Nanya Datasheet at  
13 11) and effecting an unlatching of a control circuit (for example, the control  
14 circuits contained in the DRAM chip which prepare the SDRAM for receiving  
15 valid commands during normal operation as described in Steps 10 and 12 of the  
16 initialization sequence, Nanya Datasheet at 12) provided for a proper operation of  
17 the dynamic semiconductor memory device. *See id.*

18 25. On information and belief, the controller provides at least one of a  
19 preparation command signal for word line activation, a refresh command signal,  
20 and a loading configuration register command signal as the further command  
21 signals (for example, the MRS command, which acts both as a preparation  
22 command signal and as a loading configuration register command signal, *see*  
23 Nanya Datasheet at 12-14).

24 26. On information and belief, Kingston has induced and continues to  
25 induce infringement of one or more claims of the 589 Patent, including, but not  
26 limited to, Claims 11 and 12, pursuant to 35 U.S.C. § 271(b), by encouraging its  
27 customers and other third parties to perform the claimed method for initializing a  
28 dynamic semiconductor memory device. This performance of the claimed method

1 for initializing a dynamic semiconductor memory device, constitutes infringement,  
2 literally or under the doctrine of equivalents, of one or more claims of the 589  
3 Patent by such customers or third parties. Kingston's acts of inducement include:  
4 providing its customers with the 589 Patent Infringing Products and intending its  
5 customers to use the 589 Infringing Products with hardware, software, and other  
6 infrastructure that enable and/or make use of these products; advertising these  
7 products through its own and third-party websites (for example,  
8 <http://www.kingston.com/ssd>); encouraging customers and other third parties to  
9 communicate directly with Kingston representatives about these products (for  
10 example, through the "Ask an Expert" feature on its website); and providing  
11 instructions on how to use these products. For example, Kingston's documentation  
12 supplied with the representative 589 Patent Infringing Product instructs users to  
13 install the product in a computer system and restart the computer system, and thus  
14 to perform the claimed methods. *See* Kingston Technology SSDNow Series Solid  
15 State Drive Getting Started, No. 4402105-001.B00, *available at*  
16 [http://media.kingston.com/support/downloads/SSD\\_mSATA\\_Installguide.pdf](http://media.kingston.com/support/downloads/SSD_mSATA_Installguide.pdf) (last  
17 visited on February 3, 2016).

18 27. Kingston proceeded in this manner despite its actual knowledge of the  
19 589 Patent and its knowledge that the specific actions it actively induced on the  
20 part of its customers and other third parties constitute infringement of the 589  
21 Patent at least as of February 1, 2016 when Polaris placed Kingston on notice of  
22 infringement of the 589 Patent and identified Kingston's infringing products. At  
23 the very least, because Kingston has been and remains on notice of the 589 Patent  
24 and the accused infringement, it has been and remains willfully blind regarding the  
25 infringement it has induced and continues to induce.

26 28. On information and belief, Kingston has contributed to and continues  
27 to contribute to infringement of one or more claims of the 589 Patent, including,  
28 but not limited to, Claims 11 and 12, pursuant to 35 U.S.C. § 271(c) by, without



1 authority, selling and/or offering to sell within the United States, importing, and/or  
2 supplying components of systems that perform the claimed methods for initializing  
3 a dynamic semiconductor memory device, including without limitation the 589  
4 Patent Infringing Products. These components supplied by Kingston are key  
5 components to building computer systems such as laptops or desktop computers.  
6 When, for example, these products are installed on a computing device and used  
7 for storage, the claimed dynamic semiconductor memory device is used, and/or the  
8 claimed methods performed, thereby infringing, literally or under the doctrine of  
9 equivalents, one or more claims of the 589 Patent. Kingston supplied and continues  
10 to supply these components, including without limitation the 589 Patent Infringing  
11 Products, with the knowledge of the 589 Patent and with the knowledge that these  
12 components constitute material parts of the claimed inventions of the 589 Patent.  
13 Kingston knows that these components are especially made and/or especially  
14 adapted for use as claimed in the 589 Patent. Further, Kingston knows that there is  
15 no substantial non-infringing use of these components.

16 29. Polaris has suffered damages as a result of Kingston's infringement of  
17 the 589 Patent.

18 30. Kingston's infringement of the 589 Patent has been and continues to  
19 be willful, deliberate, and in disregard of Polaris's patent rights. At least as of  
20 February 1, 2016, when Polaris placed Kingston on notice of infringement of the  
21 589 Patent and identified Kingston's infringing products, Kingston has had actual  
22 knowledge of infringement of the 589 Patent and has proceeded to infringe the 589  
23 Patent with full and complete knowledge of that patent and its applicability to  
24 Kingston's products without taking a license under the 589 Patent. Despite  
25 knowledge of the 589 Patent, Kingston has acted and is acting despite an  
26 objectively high likelihood that its actions constitute patent infringement. This  
27 objective risk was and is known to Kingston, and is also so obvious that it should  
28 have been known to Kingston. Such willful and deliberate conduct entitles Polaris

1 to increased damages under 35 U.S.C. § 284 and to attorneys’ fees and costs  
2 incurred in prosecuting this action under 35 U.S.C. § 285.

3 **COUNT II:**

4 **INFRINGEMENT OF U.S. PATENT NO. 6,438,057**

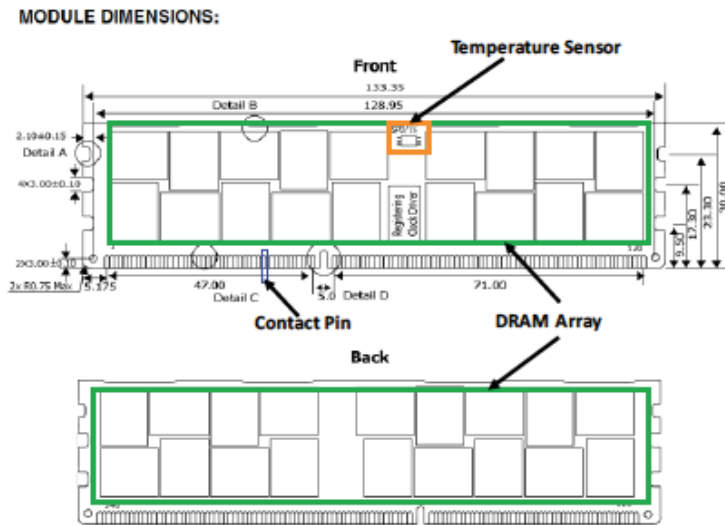
5 31. Polaris incorporates and realleges paragraphs 1-20 above as if fully set  
6 forth herein.

7 32. On information and belief, Kingston has willfully infringed and  
8 continues to willfully infringe one or more claims of the 057 Patent, including, but  
9 not limited to, Claims 1 and 2, pursuant to 35 U.S.C. § 271(a), literally or under the  
10 doctrine of equivalents, by making, using, selling, and/or offering to sell in the  
11 United States without authority and/or importing into the United States without  
12 authority, Double Data Rate 3 (DDR3) Dual In-line Memory Module (DIMM)  
13 products, devices, systems, and/or components of systems that support the  
14 Extended Temperature Range (85°C to 95°C). These products, the “057 Patent  
15 Infringing Products,” including by way of a non-limiting example only, Kingston’s  
16 memory module product with model number KVR16R11D4/16, include the  
17 temperature-based refresh rate adjustment required by the claims of the 057 Patent.

18 33. By way of example, the front and back views of a representative 057  
19 Patent Infringing Product (KVR16R11D4/16) that uses the claimed temperature-  
20 based refresh rate adjustment are shown in the image below.



34. The schematic diagram of this representative 057 Infringing Product (KVR16R11D4/16) is reproduced from publicly available Kingston documentation and annotated below for illustration.



Kingston Value RAM Memory Module Specifications, Doc. No. VALUERAM1123-001.A00 (Apr. 25, 2012) (“KVR16R11D4/16 Datasheet”) at 2, available at [http://www.kingston.com/dataSheets/KVR16R11D4\\_16.pdf](http://www.kingston.com/dataSheets/KVR16R11D4_16.pdf) (last visited February 3, 2016) (annotations added). Specifically, the 057 Patent Infringing Products, such as KVR16R11D4/16, are apparatuses comprising a

1 semiconductor package of the memory module including at least one contact pin  
2 (one example shown in the blue box in the diagram above) and at least one  
3 dynamic random access memory (DRAM) array comprising one or more DRAM  
4 chips (shown in the green box in the diagram above), such as “DDR3-1600 CL11  
5 SDRAM” in KVR16R11D4/16, *see* KVR16R11D4/16 Datasheet at 1. On  
6 information and belief, all 057 Patent Infringing Products that support the  
7 Extended Temperature Range comprise at least one temperature sensor (an  
8 example shown in the orange box above) in thermal communication with the  
9 DRAM array, operable to produce a signal indicative of a temperature of the  
10 DRAM array or the equivalent, and coupled to at least one connection pin such that  
11 the signal may be provided to external circuitry. For example, the representative  
12 057 Patent Infringing Product (KVR16R11D4/16) comprises an Atmel  
13 AT30TSE002B integrated temperature sensor with SEEPROM (annotated in the  
14 product image above). *See* AT30TSE002B Integrated Temperature Sensor with  
15 SEEPROM datasheet (“Atmel Datasheet”) at 1, *available at*  
16 <http://www.atmel.com/images/doc8711.pdf> (last visited February 3, 2016). This  
17 AT30TSE002B temperature sensor is in thermal communication with the DRAM  
18 array, operable to produce a signal indicative of a temperature of the DRAM array  
19 (for example, the Temperature Alert signal output by the EVENT pin) or the  
20 equivalent, and coupled to at least one connection pin (for example, the EVENT  
21 pin), such that the signal may be provided to external circuitry (for example, the  
22 controller). *See* Atmel Datasheet at 1-4, 11, 16-18. Further, the DRAM array on the  
23 057 Infringing Products is refreshed at a rate that decreases as the temperature of  
24 the DRAM array decreases and that increases as the temperature of the DRAM  
25 array increases. *See, e.g.*, KVR16R11D4/16 Datasheet at 1 (“Average Refresh  
26 Period 7.8 $\mu$ s at lower than TCASE 85°C, 3.9 $\mu$ s at 85°C < TCASE  $\leq$  95°C”).

27 35. On information and belief, at least one temperature sensor of one or  
28 more of the 057 Infringing Products includes at least one diode having a forward

1 voltage drop that varies as a function of the temperature of the DRAM array, and  
2 the signal corresponds to the forward voltage drop of the at least one diode. *See,*  
3 *e.g.*, Atmel Datasheet at 3 (“Band Gap Temperature Sensor”) and 11 (“a band gap  
4 type temperature sensor”).

5 36. On information and belief, Kingston has induced and continues to  
6 induce infringement of one or more claims of the 057 Patent, including, but not  
7 limited to, Claims 1, 2, 6, 7, 8, 9, 10, 11, 13, 14, 15, 16, and 17, pursuant to 35  
8 U.S.C. § 271(b) by inducing its customers and other third parties to make, use, sell,  
9 offer to sell, import into the United States without authorization infringing  
10 products that comprise an 057 Infringing Product as described above and a refresh  
11 unit and/or chip performing the temperature-based refresh rate adjustment (the  
12 “057 Infringing Systems”), and by inducing its customers and other third parties to  
13 perform the claimed method of the temperature-based refresh rate adjustment. This  
14 making, using, selling, offering to sell, importing into the United States without  
15 authorization one or more of the 057 Infringing Systems, and performance of the  
16 claimed method constitute infringement, literally or under the doctrine of  
17 equivalents, of one or more claims of the 057 Patent by such customers or third  
18 parties as further explained below.

19 37. Specifically, on information and belief, the 057 Infringing Systems  
20 comprise one of the 057 Infringing Products, as described in the paragraph 34  
21 *supra*, and a refresh unit (for example, a unit performing the temperature-based  
22 refresh rate adjustment in the controller, not shown in the images above) operable  
23 to refresh the DRAM array at a rate that varies in response to the signal (such as  
24 the Temperature Alert signal output by the EVENT pin). *See, e.g.*,  
25 KVR16R11D4/16 Datasheet at 1 (“Average Refresh Period 7.8 $\mu$ s at lower than  
26 TCASE 85°C, 3.9 $\mu$ s at 85°C < TCASE  $\leq$  95°C”).

27 38. On information and belief, such refresh unit of the 057 Infringing  
28 Systems further includes a refresh timing unit operable to establish the rate at

1 which the DRAM array is refreshed in response to the signal (such as the  
2 Temperature Alert signal output by the EVENT pin). *Id.*

3 39. On information and belief, such refresh timing unit of one or more of  
4 the 057 Infringing Systems further includes a refresh timing unit operable to  
5 decrease the rate at which the DRAM array is refreshed as the signal (such as the  
6 Temperature Alert signal output by the EVENT pin) indicates that the temperature  
7 of the DRAM array decreases. *Id.*

8 40. On information and belief, such refresh timing unit of one or more of  
9 the 057 Infringing Systems further includes a refresh timing unit operable to  
10 increase the rate at which the DRAM array is refreshed as the signal (such as the  
11 Temperature Alert signal output by the EVENT pin) indicates that the temperature  
12 of the DRAM array increases. *Id.*

13 41. On information and belief, at least one temperature sensor of one or  
14 more of the 057 Infringing Systems further includes at least one diode having a  
15 forward voltage drop that varies as a function of the temperature of the DRAM  
16 array, and the signal corresponds to the forward voltage drop of the at least one  
17 diode. *See, e.g.,* Atmel Datasheet at 3 (“Band Gap Temperature Sensor”) and 11  
18 (“a band gap type temperature sensor”).

19 42. On information and belief, the refresh unit of one or more of the 057  
20 Infringing Systems is operable to sense the forward voltage drop of the diode to  
21 determine the temperature of the DRAM array. *Id.*

22 43. On information and belief, one or more of the 057 Infringing Systems  
23 comprise at least one DRAM chip including a DRAM array and at least one  
24 temperature sensor in thermal communication with the DRAM array, at least one  
25 temperature sensor being operable to produce a signal indicative of a temperature  
26 of the DRAM array; the DRAM chip further includes at least one connection pin  
27 operable to provide the signal to external circuitry. *See* paragraph 34 *supra*. Such  
28 057 Infringing Systems further comprise at least one refresh chip (such as a chip in

1 the controller performing the temperature-based refresh rate adjustment, not shown  
2 in the images above) operable to refresh the DRAM array at a rate that varies in  
3 response to the signal, wherein the refresh chip is operable to (i) decrease the rate  
4 at which the DRAM array is refreshed as the signal indicates that the temperature  
5 of the DRAM array decreases; and (ii) increase the rate at which the DRAM array  
6 is refreshed as the signal indicates that the temperature of the DRAM array  
7 increases. *Id.*

8 44. On information and belief, at least one temperature sensor of the 057  
9 Infringing Systems as described in paragraph 43 further includes at least one diode  
10 having a forward voltage drop that varies as a function of the temperature of the  
11 DRAM array, and the signal corresponds to the forward voltage drop of the at least  
12 one diode. *See, e.g.,* Atmel Datasheet at 3 (“Band Gap Temperature Sensor”) and  
13 11 (“a band gap type temperature sensor”).

14 45. On information and belief, the refresh chip in the 057 Infringing  
15 Systems is operable to sense the forward voltage drop of the diode to determine the  
16 temperature of the DRAM array. *Id.*

17 46. On information and belief, Kingston’s customers and other third  
18 parties perform the claimed method of temperature-based refresh rate adjustment  
19 by using the 057 Infringing System. Such method comprises sensing a temperature  
20 of a dynamic random access memory (DRAM) array; outputting a signal indicative  
21 of the temperature of the DRAM array to external circuitry; and refreshing  
22 contents of the DRAM array at a rate that (i) decreases as the temperature of the  
23 DRAM array decreases; and (ii) increases as the temperature of the DRAM array  
24 increases. *See* paragraphs 34 and 37 *supra*.

25 47. On information and belief, the steps of the claimed method performed  
26 by Kingston’s customers and other third parties for sensing the temperature of the  
27 DRAM array also comprises sensing a forward voltage drop of a diode that is in  
28 thermal communication with the DRAM array. *See* paragraphs 35, 41, 42, 44 *supra*.

1           48. Kingston’s acts of active inducement of direct infringement by its  
2 customers and other third parties include: providing its customers with the 057  
3 Infringing Products and intending its customers to use these infringing memory  
4 module products with hardware and software and other infrastructure, including a  
5 controller that comprises a refresh unit and/or chip to make and use the 057  
6 Infringing Systems; advertising its infringing memory module products through its  
7 own and third-party websites (for example,  
8 [http://www.kingston.com/us/memory/search/MemoryType/Default.aspx?Memory](http://www.kingston.com/us/memory/search/MemoryType/Default.aspx?MemoryType=DIMM,3,,)  
9 [Type=DIMM,3,,](http://www.kingston.com/us/memory/search/MemoryType/Default.aspx?MemoryType=DIMM,3,,)); encouraging customers and other third parties to communicate  
10 regarding these products directly with Kingston representatives (for example,  
11 through the “Ask an Expert” feature on its website); and providing its customers  
12 and other third parties with instructions on how to combine these infringing  
13 memory module products with hardware and software and other infrastructure to  
14 make and use the 057 Infringing System, and to perform the claimed method. For  
15 example, Kingston’s user manual, supplied with the representative 057 Patent  
16 Infringing Product, instructs the users to install and use the product in a computer  
17 system, thus instructing the users to make and use the 057 Infringing System and  
18 enable the users to perform the claimed method. *See* Ex. 7, Kingston Technology  
19 Warranty and Installation Guide, Doc. 4402092-001.D00; *see also*,  
20 KVR16R11D4/16 Datasheet.

21           49. Kingston proceeded in this manner despite its actual knowledge of the  
22 057 Patent and its knowledge that the specific actions it actively induced on the  
23 part of its customers and other third parties constitute infringement of the 057  
24 Patent at least as of February 1, 2016, when Polaris placed Kingston on notice of  
25 infringement of the 057 Patent and identified Kingston’s infringing products. At  
26 the very least, because Kingston has been and remains on notice of the 057 Patent  
27 and the accused infringement, it has been and remains willfully blind regarding the  
28 infringement it has induced and continues to induce.



1           50. On information and belief, Kingston has contributed to and continues  
2 to contribute to infringement of one or more claims of the 057 Patent, including,  
3 but not limited to, Claims 1, 2, 6, 7, 8, 9, 10, 11, 13, 14, 15, 16, and 17, pursuant to  
4 35 U.S.C. § 271(c) by, without authority, selling, offering to sell within the United  
5 States, importing, and/or supplying components of the 057 Infringing Systems, and  
6 apparatuses for use in the claimed methods of the temperature-based refresh rate  
7 adjustment, including without limitation the 057 Patent Infringing Products. These  
8 components and apparatuses supplied by Kingston, including without limitation  
9 the 057 Patent Infringing Products, are key components for temperature-based  
10 refresh rate adjustment, thus constituting material parts of the claimed inventions  
11 of the 057 Patent. Kingston supplied and continues to supply these components and  
12 apparatuses, including without limitation the 057 Patent Infringing Products, with  
13 the knowledge of the 057 Patent and with the knowledge that these components  
14 constitute material parts of the claimed inventions of the 057 Patent. Kingston  
15 knows that these components and apparatuses are especially made and/or  
16 especially adapted for use as claimed in the 057 Patent to support the Extended  
17 Temperature Range (85°C to 95°C) of DDR3 memory module products. Further,  
18 Kingston knows that there is no substantial non-infringing use of these components  
19 for temperature-based refresh rate adjustment.

20           51. Polaris has suffered damages as a result of Kingston's infringement of  
21 the 057 Patent.

22           52. Kingston's infringement of the 057 Patent has been and continues to  
23 be willful, deliberate, and in disregard of Polaris's patent rights. At least as of  
24 February 1, 2016, when Polaris placed Kingston on notice of infringement of the  
25 057 Patent and identified Kingston's infringing products, Kingston has had actual  
26 knowledge of infringement of the 057 Patent and has proceeded to infringe the 057  
27 Patent with full and complete knowledge of that patent and its applicability to  
28 Kingston's products without taking a license under the 057 Patent. Despite

1 knowledge of the 057 Patent, Kingston has acted and is acting despite an  
2 objectively high likelihood that its actions constitute patent infringement. This  
3 objective risk was and is known to Kingston, and is also so obvious that it should  
4 have been known to Kingston. Such willful and deliberate conduct entitles Polaris  
5 to increased damages under 35 U.S.C. § 284 and to attorneys’ fees and costs  
6 incurred in prosecuting this action under 35 U.S.C. § 285.

7 **COUNT III:**

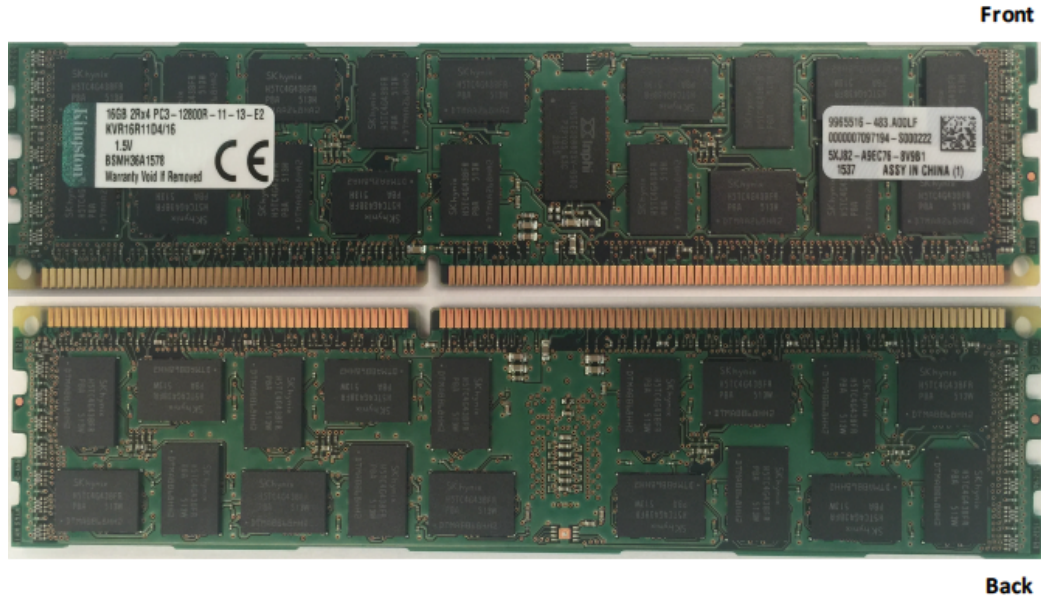
8 **INFRINGEMENT OF U.S. PATENT NO. 6,850,414**

9 53. Polaris incorporates and realleges paragraphs 1-20 above as if fully set  
10 forth herein.

11 54. On information and belief, Kingston has willfully infringed and  
12 continues to willfully infringe one or more claims of the 414 Patent, including, but  
13 not limited to, Claims 1, 4, and 8, pursuant to 35 U.S.C. § 271(a), literally or under  
14 the doctrine of equivalents, by making, using, selling, and/or offering to sell in the  
15 United States without authority and/or importing into the United States without  
16 authority, memory products, devices, systems, and/or components of systems that  
17 include the claimed arrangements and configurations of the memory chips (the  
18 “414 Patent Infringing Products”), including, for example, Kingston’s memory  
19 module products with model number KVR16R11D4/16.

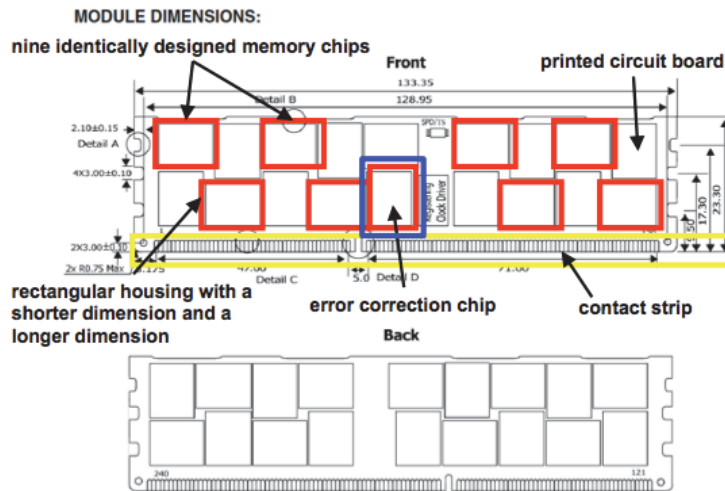
20 55. By way of example, the front and back views of a representative 414  
21 Patent Infringing Product (KVR16R11D4/16) that uses the claimed arrangement  
22 and configuration of the memory chips are shown in the image below.

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56. The schematic diagram of this representative 414 Infringing Product (KVR16R11D4/16) is reproduced from publicly available Kingston documentation and annotated below for illustration.



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See KVR16R11D4/16 Datasheet at 2 (annotations added).

57. Specifically, the 414 Patent Infringing Products, such as KVR16R11D4/16, are memory modules having at least nine identical semiconductor memories (shown in red in the diagram above) that are encapsulated in rectangular housing with a shorter dimension and a longer

1 dimension, each of which are individually connected to an electronic printed  
2 circuit board, the front and back sides of which are illustrated above. The  
3 electronic printed circuit board has a contact strip (one example shown in the  
4 yellow box in the diagram above) for insertion into another electronic unit. One of  
5 the semiconductor memories is connected as an error correction chip (shown in  
6 blue above in the diagram above) with its housing being oriented perpendicular to  
7 the contact strip, while the longer dimensions of eight other semiconductor  
8 memories are oriented parallel with the contact strip. *See* KVR16R11D4/16  
9 Datasheet at 2.

10 58. In addition, one or more of the 414 Patent Infringing Products has a  
11 height of 1 to 1.2 inches perpendicular to said contact strip. *See id.*

12 59. Further, one or more of the 414 Patent Infringing Products has a width  
13 of 5.25 inches. *See id.*

14 60. On information and belief, Kingston has induced and continues to  
15 induce infringement of one or more claims of the 414 Patent, including, but not  
16 limited to, Claims 1, 4, and 8, pursuant to 35 U.S.C. § 271(b) by inducing its  
17 customers and other third parties to use without authorization the infringing  
18 products that use the claimed arrangement and configuration of the memory chips,  
19 including but not limited to the 414 Patent Infringing Products. The use, without  
20 authorization, of the infringing products that comprise the claimed arrangement  
21 and configuration of the memory chips constitutes infringement, literally or under  
22 the doctrine of equivalents, of one or more claims of the 414 Patent by such  
23 customers or third parties. Kingston's acts of inducement include: providing its  
24 customers with the 414 Patent Infringing Products and intending its customers to  
25 use the 414 Infringing Products with hardware, software and other infrastructure  
26 that enable and/or make use of these products; advertising these products through  
27 its own and third-party websites (for example,  
28 <http://www.kingston.com/us/memory/search/MemoryType/Default.aspx?Memory>

1 [Type=DIMM,3,,](#)); encouraging customers and other third parties to communicate  
2 directly with Kingston representatives about these products (for example, through  
3 the “Ask an Expert” feature on its website); and providing instructions on how to  
4 use these products. For example, Kingston’s documentation accompanying the  
5 representative 414 Patent Infringing Product provides the users with instructions  
6 on how to install the product in a computer system and enables the users to use the  
7 product. *See* Ex. 7, Kingston Technology Warranty and Installation Guide, Doc.  
8 4402092-001.D00; *see also*, KVR16R11D4/16 Datasheet.

9         61. Kingston proceeded in this manner despite its actual knowledge of the  
10 414 Patent and its knowledge that the specific actions it actively induced on the  
11 part of its customers and other third parties constitute infringement of the 414  
12 Patent at least as of February 1, 2016 when Polaris placed Kingston on notice of  
13 infringement of the 414 Patent and identified Kingston’s infringing products. At  
14 the very least, because Kingston has been and remains on notice of the 414 Patent  
15 and the accused infringement, it has been and remains willfully blind regarding the  
16 infringement it has induced and continues to induce.

17         62. Polaris has suffered damages as a result of Kingston’s infringement of  
18 the 414 Patent.

19         63. Kingston’s infringement has been and continues to be willful,  
20 deliberate and in disregard of Polaris’s patent rights. At least as of February 1,  
21 2016, when Polaris placed Kingston on notice of infringement of the 414 Patent  
22 and identified Kingston’s infringing products, Kingston has had actual knowledge  
23 of infringement of the 414 Patent and has proceeded to infringe the 414 Patent with  
24 full and complete knowledge of that patent and its applicability to Kingston  
25 products without taking a license under the 414 Patent. Despite knowledge of the  
26 414 Patent, Kingston has acted and is acting despite an objectively high likelihood  
27 that its actions constitute patent infringement. This objective risk was and is known  
28 to Kingston, and is also so obvious that it should have been known to Kingston.

1 Such willful and deliberate conduct entitles Polaris to increased damages under 35  
2 U.S.C. § 284 and to attorneys’ fees and costs incurred in prosecuting this action  
3 under 35 U.S.C. § 285.

4 **COUNT IV:**

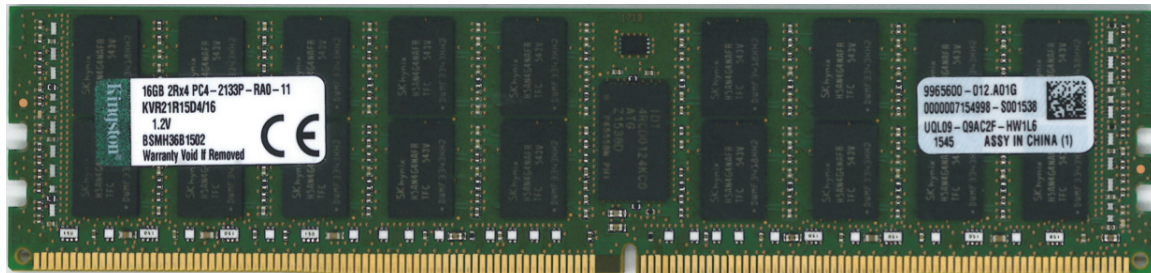
5 **INFRINGEMENT OF U.S. PATENT NO. 7,206,978**

6 64. Polaris incorporates and realleges paragraphs 1-20 above as if fully set  
7 forth herein.

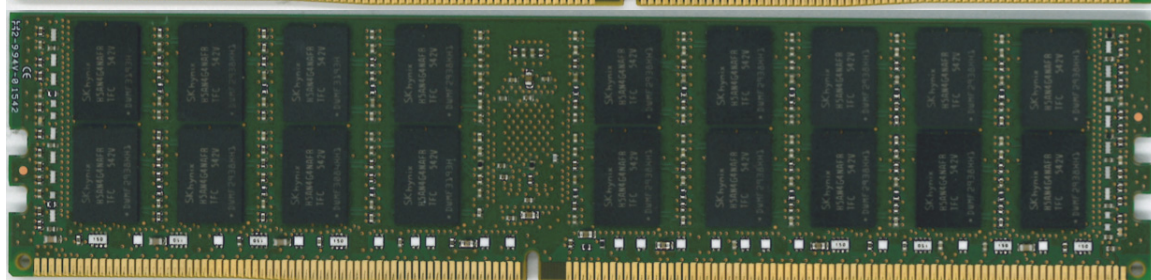
8 65. On information and belief, Kingston has willfully infringed and  
9 continues to willfully infringe one or more claims of the 978 Patent, including, but  
10 not limited to, Claims 1, 2, 3, 5, 10, 11, and 12, pursuant to 35 U.S.C. § 271(a),  
11 literally or under the doctrine of equivalents, by making, using, selling, and/or  
12 offering to sell in the United States and/or importing into the United States without  
13 authority, claimed memory module products, devices, systems, and/or components  
14 of systems (the “978 Patent Infringing Products”), including, for example,  
15 Kingston’s memory module products with model number KVR21R15D4/16.

16 66. By way of example, the front and back views of a representative 978  
17 Patent Infringing Product (KVR21R15D4/16) are shown in the image below.

18 **Front**



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28 **Back**



1           67. The 978 Patent Infringing Products, such as KVR21R15D4/16, are  
2 circuit modules comprising a module board, the front and back sides of which are  
3 shown above. A plurality of circuit units, each consisting of a single integrated  
4 circuit memory chip, is arranged on the module board (in the above example, 36  
5 integrated memory chips are arranged on the module board). *See, e.g.*, Kingston  
6 KVR21R15D4/16 16GB 2Rx4 2G x 72-Bit PC4-2133 CL15 Registered w/Parity  
7 288-Pin DIMM Specification, Doc. No. VALUERAM1447-001.C00 (Feb. 24,  
8 2015) (“KVR21R15D4/16 Datasheet”) at 1, *available at*  
9 [http://www.kingston.com/dataSheets/KVR21R15D4\\_16.pdf](http://www.kingston.com/dataSheets/KVR21R15D4_16.pdf) (last visited February  
10 3, 2016). Further, on information and belief, the 978 Patent Infringing Products  
11 comprise a main bus having a plurality of lines, branching into a plurality of sub-  
12 buses having a plurality of lines, each of the sub-buses being connected to one of  
13 the plurality of the circuit units. Further, upon information and belief, each circuit  
14 unit (in the example above, each dynamic random access memory, or “DRAM,”  
15 chip) in the 978 Patent Infringing Products comprises an indication signal  
16 generating unit for providing an indication signal based on a combination of the  
17 signals received on the plurality of lines of the sub-bus connected to the respective  
18 circuit unit (in the example above, each memory chip combines the PAR  
19 (command and address parity) input signal with the command and address input  
20 signals to determine whether there is an error and generate the appropriate  
21 indication signal). *See, e.g.*, KVR21R15D4/16 Datasheet at 1 (“CA parity  
22 (Command/Address Parity) mode is supported”). Each circuit unit also comprises  
23 an indication signal output for outputting the indication signal (in the example  
24 above, the ALERT\_n pin on each memory chip).

25           68. In addition, one or more 978 Patent Infringing Products comprise  
26 means for providing a check signal to each of the circuit units, the structure of  
27 which is the same as or equivalent to that disclosed in the patent specification (in  
28 the example above, the PAR (command and address parity) input on each dynamic

1 random access memory chip). *See, e.g.*, KVR21R15D4/16 Datasheet at 1 (“CA  
2 parity (Command/Address Parity) mode is supported”). Upon information and  
3 belief, this indication signal generating unit generates said indication signal based  
4 on a combination of the signals on the plurality of lines of the respective sub-bus  
5 and the check signal so that the indication signal represents an error signal (in the  
6 example above, each memory chip combines the PAR input signal with the  
7 command and address input signals to determine whether there is an error and  
8 generate the appropriate indication signal).

9         69. In addition, on information and belief, one or more 978 Patent  
10 Infringing Products comprise an error reporting means, the structure of which is  
11 the same as or equivalent to that disclosed in the patent specification, being  
12 connected to the indication signal outputs of the circuit units, and wherein each  
13 error reporting means is configured to drive a module error out signal (in the  
14 example above, the ALERT\_n outputs are connected to each other by traces on the  
15 printed circuit board, and buffered by a register, they drive the ALERT\_n signal  
16 for the entire module). *See, e.g.*, KVR21R15D4/16 Datasheet at 1 (“CA parity  
17 (Command/Address Parity) mode is supported”).

18         70. In addition, on information and belief, one or more 978 Patent  
19 Infringing Products comprise an indication reporting means, the structure of which  
20 is the same as or equivalent to that disclosed in the patent specification, being  
21 connected to the indication signal outputs of the circuit units and wherein each  
22 indication reporting means is configured to drive a module indication out signal (in  
23 the example above, the ALERT\_n outputs are connected to each other by traces on  
24 the printed circuit board, and buffered by a register, they drive the ALERT\_n  
25 signal for the entire module).

26         71. In addition, on information and belief, one or more 978 Patent  
27 Infringing Products comprise a DIMM, wherein the circuit units are memory units,  
28 wherein the main bus is a memory main bus, and the sub-busses are memory sub-



1 buses (in the example above, the module is a DIMM, the circuit units are DRAM  
2 memory chips and the traces providing address and command signals to the  
3 memory chips form a memory main bus and memory sub-buses). *See, e.g.,*  
4 KVR21R15D4/16 Datasheet at 1.

5 72. In addition, on information and belief, one or more 978 Patent  
6 Infringing Products comprise a main bus that is a command/address bus (in the  
7 example above, the traces providing address and command signals to the dynamic  
8 random access memory chips form a memory main bus and memory sub-buses).

9 73. In addition, on information and belief, one or more 978 Patent  
10 Infringing Products comprise means for providing a check signal that is a parity  
11 signal, the structure of which is the same as or equivalent to that disclosed in the  
12 patent specification (in the example above, the PAR input on each dynamic  
13 random access memory chip receives a parity signal from the module board).

14 74. On information and belief, Kingston has induced and continues to  
15 induce infringement of one or more claims of the 978 Patent, including, but not  
16 limited to, Claims 1, 2, 3, 5, 10, 11, and 12, pursuant to 35 U.S.C. § 271(b) by  
17 inducing its customers and other third parties to use without authorization the  
18 infringing products comprising the claimed arrangement of circuit units, including  
19 but not limited to the 978 Patent Infringing Products. This use, without  
20 authorization, of the infringing products comprising the claimed arrangement of  
21 circuit units constitutes infringement, literally or under the doctrine of equivalents,  
22 of one or more claims of the 978 Patent by such customers or third parties.  
23 Kingston's acts of inducement include: providing its customers with the 978 Patent  
24 Infringing Products and intending its customers to use the 978 Infringing Products  
25 with hardware, software, and other infrastructure that enable and/or make use of  
26 these products; advertising these products through its own and third-party websites  
27 (for example, [http://www.kingston.com/us/memory/search/MemoryType/De](http://www.kingston.com/us/memory/search/MemoryType/Default.aspx?MemoryType=DIMM,3,)  
28 [fault.aspx?MemoryType=DIMM,3,.](http://www.kingston.com/us/memory/search/MemoryType/Default.aspx?MemoryType=DIMM,3,)); encouraging customers and other third

1 parties to communicate directly with Kingston representatives about these products  
2 (for example, through the “Ask an Expert” feature on its website); and providing  
3 instructions on how to use these products. For example, Kingston’s documentation  
4 accompanying the representative 978 Patent Infringing Product provides the users  
5 with instructions on how to install the product in a computer system and enables  
6 the users to use the product. *See* Ex. 7, Kingston Technology Warranty and  
7 Installation Guide, Doc. 4402092-001.D00; *see also*, KVR21R15D4/16 Datasheet.

8         75. Kingston proceeded in this manner despite its actual knowledge of the  
9 978 Patent and its knowledge that the specific actions it actively induced on the  
10 part of its customers and other third parties constitute infringement of the 978  
11 Patent at least as of February 1, 2016, when Polaris placed Kingston on notice of  
12 infringement of the 978 Patent and identified Kingston’s infringing products. At  
13 the very least, because Kingston has been and remains on notice of the 978 Patent  
14 and the accused infringement, it has been and remains willfully blind regarding the  
15 infringement it has induced and continues to induce.

16         76. Polaris has suffered damages as a result of Kingston’s infringement of  
17 the 978 Patent.

18         77. Kingston’s infringement of the 978 Patent has been and continues to  
19 be willful, deliberate, and in disregard of Polaris’s patent rights. At least as of  
20 February 1, 2016, when Polaris placed Kingston on notice of infringement of the  
21 978 Patent and identified Kingston’s infringing products, Kingston has had actual  
22 knowledge of infringement of the 978 Patent and has proceeded to infringe the 978  
23 Patent with full and complete knowledge of that patent and its applicability to  
24 Kingston’s products without taking a license under the 978 Patent. Despite  
25 knowledge of the 978 Patent, Kingston has acted and is acting despite an  
26 objectively high likelihood that its actions constitute patent infringement. This  
27 objective risk was and is known to Kingston, and is also so obvious that it should  
28 have been known to Kingston. Such willful and deliberate conduct entitles Polaris

1 to increased damages under 35 U.S.C. § 284 and to attorneys’ fees and costs  
2 incurred in prosecuting this action under 35 U.S.C. § 285.

3 **COUNT V:**

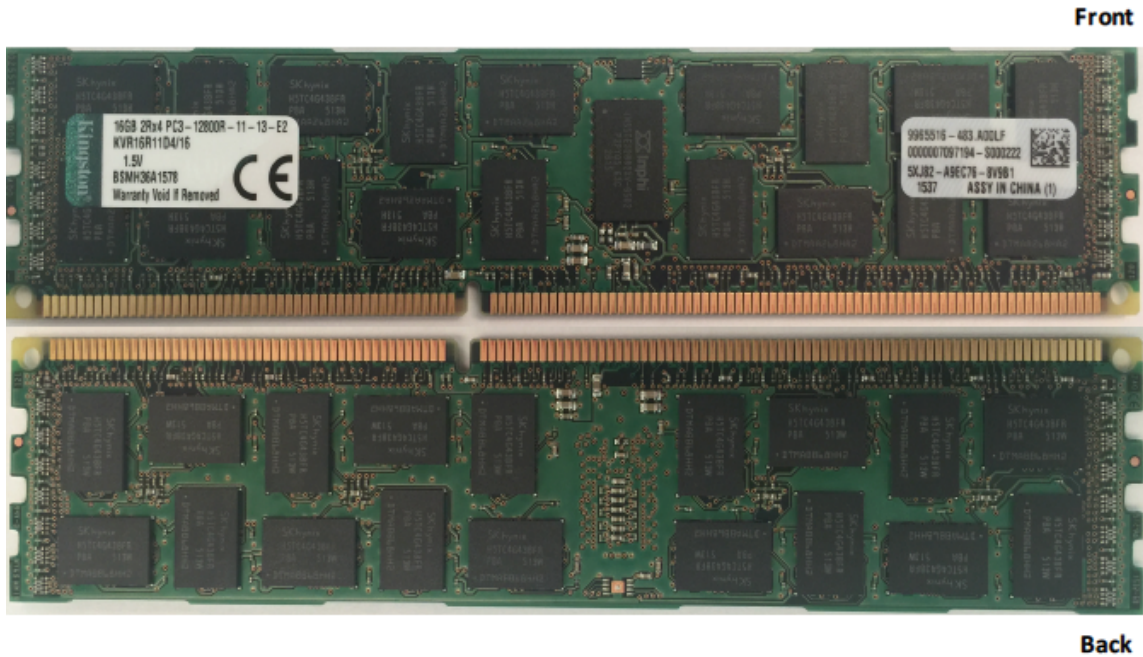
4 **INFRINGEMENT OF U.S. PATENT NO. 7,315,454**

5 78. Polaris incorporates and realleges paragraphs 1-20 above as if fully set  
6 forth herein.

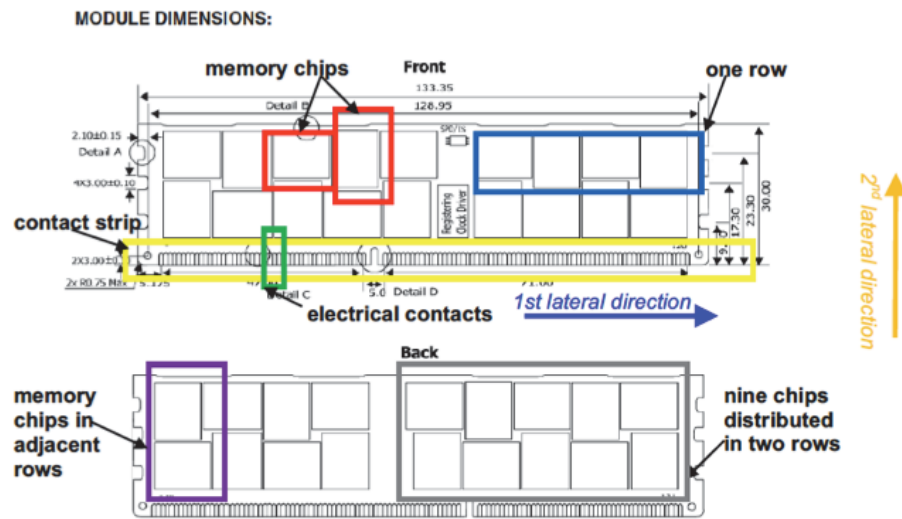
7 79. On information and belief, Kingston has willfully infringed and  
8 continues to willfully infringe one or more claims of the 454 Patent, including, but  
9 not limited to, Claims 1, 2, 3, 4, and 7, pursuant to 35 U.S.C. § 271(a), literally or  
10 under the doctrine of equivalents, by making, using, selling, and/or offering to sell  
11 in the United States and/or importing into the United States without authority,  
12 memory module products, devices, systems, and/or components of systems that  
13 include the claimed arrangements and configurations of the memory chips (the  
14 “454 Patent Infringing Products”), including, for example, Kingston’s memory  
15 module products with model number KVR16R11D4/16.

16 80. By way of example, the front and back views of a representative 454  
17 Patent Infringing Product (KVR16R11D4/16) that uses the claimed arrangement  
18 and configuration of the memory chips are shown in the image below.

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81. The schematic diagram of this representative 454 Patent Infringing Product (KVR16R11D4/16) is reproduced from publicly available Kingston documentation and annotated below for illustration.



See KVR16R11D4/16 Datasheet at 2 (annotations added). Specifically, the 454 Patent Infringing Products, such as KVR16R11D4/16, are semiconductor memory modules comprising an electronic printed circuit board, the front and back sides of

1 which are illustrated above. The electronic printed circuit board has a contact strip  
2 (one example shown in the yellow box) that extends at a first edge (for example,  
3 the bottom edge) of the printed circuit board along with a first lateral direction and  
4 a plurality of electrical contacts (a few shown in the green box as examples)  
5 disposed along the first lateral direction between two second edges (left and right  
6 edges) that extend in a second lateral direction that is perpendicular to the first  
7 lateral direction. The 454 Patent Infringing Products further comprise a plurality of  
8 semiconductor memory chips (two exemplary chips are shown in the red boxes) of  
9 substantially identical type, such as “DDR3-1600 CL11 SDRAM” in  
10 KVR16R11D4/16, *see* KVR16R11D4/16 Datasheet at 1, mounted on at least one  
11 external area (the front and/or back sides) of the printed circuit board and having a  
12 rectangular form with a shorter dimension and a longer dimension in a direction  
13 perpendicular to the shorter dimension. The memory chips are arranged in at least  
14 two rows, each row (one exemplary row shown in blue box) extending in the first  
15 lateral direction between a center of the printed circuit board and the left or right  
16 edge, wherein the memory chips in each row are arranged in an alternating  
17 sequence of opposite orientation with the longer dimension of each memory chip  
18 being parallel with the shorter dimension of adjacent memory chips in the same  
19 row. The memory chips aligned in the second lateral direction and lying in  
20 respective adjacent rows (one group of such chips shown in the purple box) have  
21 opposite orientations.

22 82. In addition, one or more 454 Patent Infringing Products include four  
23 semiconductor memory chips (one example shown in the blue box) that are  
24 mounted in a row on one external area (such as the front side) of the printed circuit  
25 board.

26 83. Further, one or more 454 Patent Infringing Products include nine  
27 chips (one example shown in the grey box) that are distributed between two rows  
28 arranged in a manner lying one adjacent to another in the second lateral direction.

1           84. Further, on information and belief, one or more 454 Patent Infringing  
2 Products comprise a branching separate line bus comprising a first branch and a  
3 second branch, wherein the memory chips mounted on the external area (the front  
4 and/or back sides) between the center and the respective second edge (left or right  
5 edge) of the printed circuit are connected by the branching separate line bus, such  
6 that the memory chips of a first row are connected in series via line tracks of the  
7 first branch and the memory chips of a second row are connected in a series via  
8 line tracks of the second branch of the branch separate line bus, or the 454 Patent  
9 Infringing Products comprise the equivalent.

10           85. Further, the 454 Patent Infringing Products are standardized memory  
11 modules in compliance with a JEDEC standard. *See, e.g.*, KVR16R11D4/16  
12 Datasheet at 1.

13           86. On information and belief, Kingston has induced and continues to  
14 induce infringement of one or more claims of the 454 Patent, including, but not  
15 limited to, Claims 1, 2, 3, 4, and 7, pursuant to 35 U.S.C. § 271(b) by inducing its  
16 customers and other third parties to use without authorization the infringing  
17 products comprising the claimed arrangements and configurations of the memory  
18 chips, including but not limited to the 454 Patent Infringing Products. This use,  
19 without authorization, of the infringing products comprising the claimed  
20 arrangements and configurations of the memory chips constitutes infringement,  
21 literally or under the doctrine of equivalents, of one or more claims of the 454  
22 Patent by such customers or third parties. Kingston's acts of inducement include:  
23 providing its customers with the 454 Patent Infringing Products and intending its  
24 customers to use the 454 Infringing Products with hardware, software, and other  
25 infrastructure that enable and/or make use of these products; advertising these  
26 products through its own and third-party websites (for example,  
27 [http://www.kingston.com/us/memory/search/MemoryType/Default.aspx?Memory](http://www.kingston.com/us/memory/search/MemoryType/Default.aspx?MemoryType=DIMM,3,)  
28 [Type=DIMM,3,.](http://www.kingston.com/us/memory/search/MemoryType/Default.aspx?MemoryType=DIMM,3,)); encouraging customers and other third parties to communicate

1 directly with Kingston representatives about these products (for example, through  
2 the “Ask an Expert” feature on its website); and providing instructions on how to  
3 use these products. For example, Kingston’s documentation accompanying the  
4 representative 454 Patent Infringing Product provides the users with instructions  
5 on how to install the product in a computer system and enables the users to use the  
6 product. *See* Ex. 7, Kingston Technology Warranty and Installation Guide, Doc.  
7 4402092-001.D00; *see also*, KVR16R11D4/16 Datasheet.

8 87. Kingston proceeded in this manner despite its actual knowledge of the  
9 454 Patent and its knowledge that the specific actions it actively induced on the  
10 part of its customers and other third parties constitute infringement of the 454  
11 Patent at least as of February 1, 2016, when Polaris placed Kingston on notice of  
12 infringement of the 454 Patent and identified infringing Kingston’s products. At  
13 the very least, because Kingston has been and remains on notice of the 454 Patent  
14 and the accused infringement, it has been and remains willfully blind regarding the  
15 infringement it has induced and continues to induce.

16 88. Polaris has suffered damages as a result of Kingston’s infringement of  
17 the 454 Patent.

18 89. Kingston’s infringement of the 454 Patent has been and continues to  
19 be willful, deliberate, and in disregard of Polaris’s patent rights. At least as of  
20 February 1, 2016, when Polaris placed Kingston on notice of infringement of the  
21 454 Patent and identified Kingston’s infringing products, Kingston has had actual  
22 knowledge of infringement of the 454 Patent and has proceeded to infringe the 454  
23 Patent with full and complete knowledge of that patent and its applicability to  
24 Kingston’s products without taking a license under the 454 Patent. Despite  
25 knowledge of the 454 Patent, Kingston has acted and is acting despite an  
26 objectively high likelihood that its actions constitute patent infringement. This  
27 objective risk was and is known to Kingston, and is also so obvious that it should  
28 have been known to Kingston. Such willful and deliberate conduct entitles Polaris

1 to increased damages under 35 U.S.C. § 284 and to attorneys’ fees and costs  
2 incurred in prosecuting this action under 35 U.S.C. § 285.

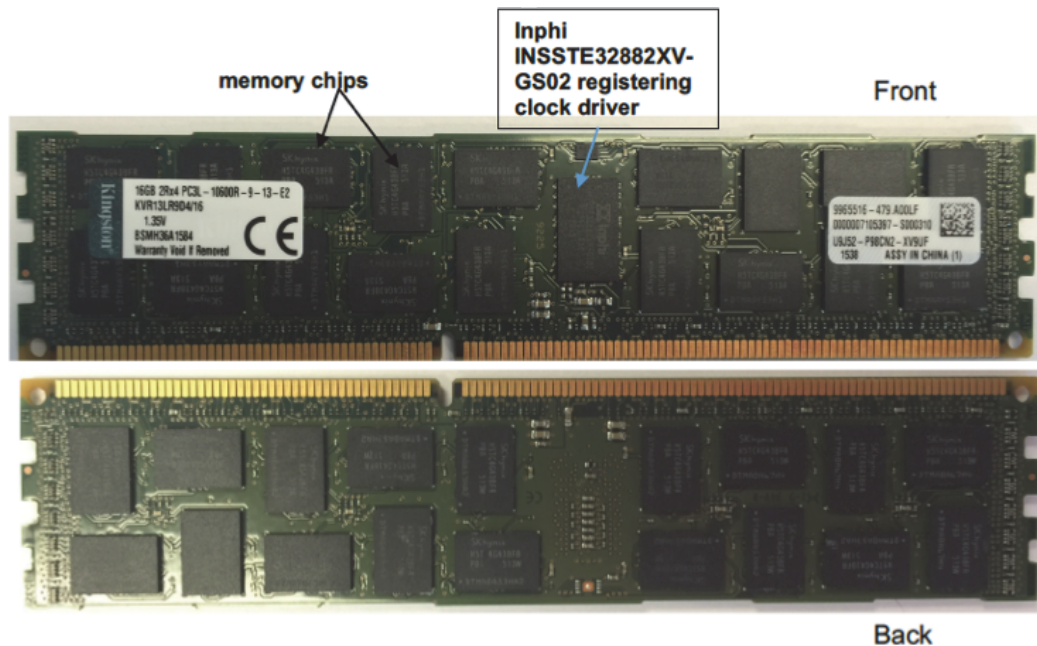
3 **COUNT VI:**

4 **INFRINGEMENT OF U.S. PATENT NO. 7,334,150**

5 90. Polaris incorporates and realleges paragraphs 1-20 above as if fully set  
6 forth herein.

7 91. On information and belief, Kingston has willfully infringed and  
8 continues to willfully infringe one or more claims of the 150 Patent, including, but  
9 not limited to, Claims 1, 2, 3, 5, 6, 8, 9, 10, and 11, pursuant to 35 U.S.C. § 271(a),  
10 literally or under the doctrine of equivalents, by making, using, selling, and/or  
11 offering to sell in the United States and/or importing into the United States without  
12 authority, memory module products, devices, systems, and/or components of  
13 systems that included the claimed clock signal regeneration circuit and register  
14 circuit (the “150 Patent Infringing Products”), including without limitation,  
15 Kingston’s memory module product with model number KVR13LR9D4/16.

16 92. By way of example, the front and back views of a representative 150  
17 Patent Infringing Product (KVR13LR9D4/16) are shown in the image below.





1           93. Specifically, the 150 Patent Infringing Products, such as  
2 KVR13LR9D4/16, comprise a plurality of memory chips arranged on the memory  
3 module. On information and belief, the 150 Patent Infringing Products, such as  
4 KVR13LR9D4/16, comprise a plurality of bus signal lines operable to supply an  
5 incoming clock signal (for example, clock signals CK0\_t, CK0\_c) and incoming  
6 command and address signal (for example, address signals A[N:0]) to at least the  
7 memory chips. On information and belief, the 150 Patent Infringing Products  
8 further comprise a clock signal regeneration circuit (for example, a standard SSTE  
9 32882 registering clock driver) configured to generate a plurality of copies of the  
10 incoming clock signal (for example, PCK0A\_t, PCK0B\_t, PCK\_0A\_c, PCK\_0B\_c)  
11 and to supply the copies of the incoming clock signal to the memory chip, where  
12 the copies of the incoming clock signal have the same frequency as the incoming  
13 clock signal. On information and belief, the 150 Patent Infringing Products further  
14 comprise a register circuit arranged on the memory module in a common chip  
15 packaging with the clock regeneration circuit. *See, e.g.*, Kingston Value RAM  
16 Memory Module Specifications, Doc. No. VALUERAM1223-001.B00 (Jan. 22,  
17 2013) (“KVR13LR9D4/16 Datasheet”) at 2 (the register and the clock driver are  
18 within the same chip), *available at*  
19 [http://www.kingston.com/dataSheets/KVR13LR9D4\\_16.pdf](http://www.kingston.com/dataSheets/KVR13LR9D4_16.pdf) (last visited February  
20 3, 2016) (annotations added). For example, the representative 150 Patent Infringing  
21 Product KVR13LR9D4/16, comprises an Inphi INSSTE32882XV-GS02  
22 registering clock driver chip (as annotated in the product image above), that  
23 includes both the clock regeneration circuit and the register circuit. *See*  
24 INSSTE32882XV datasheet (“Inphi Datasheet”), *available at*  
25 [http://www.inphi.com/product\\_pdf\\_generator.php?prod\\_link=960](http://www.inphi.com/product_pdf_generator.php?prod_link=960) (last visited  
26 December 21, 2015). On information and belief, the register circuit in the 150  
27 Infringing Products is configured to receive one of the copies of the incoming  
28 clock signal from the clock regeneration circuit. On information and belief, the

1 register circuit in the 150 Infringing Products is further configured to temporarily  
2 store the incoming command and address signals, and to generate a plurality of  
3 copies of the incoming command and address signals and to supply the copies of  
4 the incoming command and address signals to the memory chip, where the copies  
5 of the incoming command and address signals have the same frequency as the  
6 incoming command and address signals.

7 94. The clock signal regeneration circuit in the 150 Patent Infringing  
8 Product comprises a phase locked loop (PLL) circuit. *See, e.g.*, KVR13LR9D4/16  
9 Datasheet at 1 (“Register/PLL used”).

10 95. On information and belief, the incoming clock signal and the copies of  
11 incoming clock signals in the 150 Patent Infringing Products are each supplied via  
12 differential clock signal lines.

13 96. In addition, in the 150 Patent Infringing Products, the clock signal  
14 regeneration circuit and the register circuit are integrated on a common chip in the  
15 common chip packaging. *See, e.g.*, KVR13LR9D4/16 Datasheet at 2.

16 97. Further, the common chip packaging is arranged essentially at a  
17 central position on the exemplary 150 Patent Infringing Product  
18 (KVR13LR9D4/16) or is arranged equivalently. *See, e.g.*, KVR13LR9D4/16  
19 Datasheet at 2.

20 98. On information and belief, the 150 Patent Infringing Products  
21 comprise a fly-by bus structure for the bus signal lines of the command and  
22 address signals or the equivalent. *See* John Nieto, *The Evolution from DDR2 to*  
23 *DDR3 and its Impact on Signal Integrity*, available at  
24 [https://www.inphi.com/technology-overview/Evolution%20of%20DDR2%20](https://www.inphi.com/technology-overview/Evolution%20of%20DDR2%20to%20DDR3.pdf)  
25 [to%20DDR3.pdf](https://www.inphi.com/technology-overview/Evolution%20of%20DDR2%20to%20DDR3.pdf) (last visited December 21, 2015).

26 99. On information and belief, the clock signal regeneration circuit and  
27 the register circuit in the 150 Patent Infringing Products respectively generate two  
28 copies of the clock signal and the command signals for distribution to the memory

1 chips.

2 100. On information and belief, one or more of the 150 Patent Infringing  
3 Products further comprise an RDIMM module. *See, e.g.*, KVR13LR9D4/16  
4 Datasheet at 1 (“Registered w/Parity 240-Pin DIMM”).

5 101. The 150 Patent Infringing Products further comprise DDR-DRAM  
6 memories. *See, e.g.*, KVR13LR9D4/16 Datasheet at 1 (“DDR3L-1333 CL9  
7 SDRAM”).

8 102. On information and belief, Kingston has induced and continues to  
9 induce infringement of one or more claims of the 150 Patent, including, but not  
10 limited to, Claims 1, 2, 3, 5, 6, 8, 9, 10, and 11, pursuant to 35 U.S.C. § 271(b) by  
11 inducing its customers and other third parties to use without authorization the  
12 infringing products comprising the claimed clock signal regeneration circuit and  
13 register circuit, including but not limited to the 150 Patent Infringing Products.  
14 This use, without authorization, of the infringing products comprising the claimed  
15 arrangements and configurations of the memory chips constitutes infringement,  
16 literally or under the doctrine of equivalents, of one or more claims of the 150  
17 Patent by such customers or third parties. Kingston’s acts of inducement include:  
18 providing its customers with the 150 Patent Infringing Products and intending its  
19 customers to use the 150 Infringing Products with hardware, software and other  
20 infrastructure that enable and/or make use of these products; advertising these  
21 products through its own and third-party websites (for example,  
22 [http://www.kingston.com/us/memory/search/MemoryType/Default.aspx?Memory](http://www.kingston.com/us/memory/search/MemoryType/Default.aspx?MemoryType=DIMM,3,,)  
23 [Type=DIMM,3,,](http://www.kingston.com/us/memory/search/MemoryType/Default.aspx?MemoryType=DIMM,3,,)); encouraging customers and other third parties to communicate  
24 directly with Kingston representatives about these products (for example, through  
25 the “Ask an Expert” feature on its website); and providing instructions on how to  
26 use these products. For example, Kingston’s documentation accompanying the  
27 representative 150 Patent Infringing Product provides the users with instructions  
28 on how to install the product in a computer system and enables the users to use the

1 product. *See* Ex. 7, Kingston Technology Warranty and Installation Guide, Doc.  
2 4402092-001.D00; *see also*, KVR13LR9D4/16 Datasheet.

3 103. Kingston proceeded in this manner despite its actual knowledge of the  
4 150 Patent and its knowledge that the specific actions it actively induced on the  
5 part of its customers and other third parties constitute infringement of the 150  
6 Patent at least as of February 1, 2016, when Polaris placed Kingston on notice of  
7 infringement of the 150 Patent and identified infringing Kingston's products. At  
8 the very least, because Kingston has been and remains on notice of the 150 Patent  
9 and the accused infringement, it has been and remains willfully blind regarding the  
10 infringement it has induced and continues to induce.

11 104. Polaris has suffered damages as a result of Kingston's infringement of  
12 the 150 Patent.

13 105. Kingston's infringement of the 150 Patent has been and continues to  
14 be willful, deliberate and in disregard of Polaris's patent rights. At least as of  
15 February 1, 2016, when Polaris placed Kingston on notice of infringement of the  
16 150 Patent and identified Kingston's infringing products, Kingston has had actual  
17 knowledge of infringement of the 150 Patent and has proceeded to infringe the 150  
18 Patent with full and complete knowledge of that patent and its applicability to  
19 Kingston's products without taking a license under the 150 Patent. Despite  
20 knowledge of the 150 Patent, Kingston has acted and is acting despite an  
21 objectively high likelihood that its actions constitute patent infringement. This  
22 objective risk was and is known to Kingston, and is also so obvious that it should  
23 have been known to Kingston. Such willful and deliberate conduct entitles Polaris  
24 to increased damages under 35 U.S.C. § 284 and to attorneys' fees and costs  
25 incurred in prosecuting this action under 35 U.S.C. § 285.

26 **PRAYER FOR RELIEF**

27 106. Polaris respectfully prays for relief as follows:

28 107. A judgment that Kingston has infringed and continues to infringe one

1 or more claims of the Asserted Patents;

2 108. A judgment that Kingston has willfully infringed one or more claims  
3 of the Asserted Patents;

4 109. A judgment awarding Polaris all damages adequate to compensate for  
5 Kingston's infringement, and in no event less than a reasonable royalty for  
6 Kingston's acts of infringement, including all pre-judgment and post-judgment  
7 interest at the maximum rate allowed by law;

8 110. A judgment awarding Polaris treble damages pursuant to 35 U.S.C. §  
9 284 as a result of Kingston's willful conduct;

10 111. A judgment and order finding that this is an exceptional case within  
11 the meaning of 35 U.S.C. § 285 and awarding Polaris its reasonable attorneys fees  
12 and costs; and

13 112. A judgment awarding Polaris such other relief as the Court may deem  
14 just and equitable.

15 **DEMAND FOR JURY TRIAL**

16 113. Pursuant to Rule 38(b) of the Federal Rules of Civil Procedure,  
17 Polaris demands a trial by jury in this action.

18  
19 Dated: February 19, 2016

Respectfully submitted,

20 TENSEGRITY LAW GROUP LLP

21  
22 By: /s/ Matthew D. Powers

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Polaris Innovations Limited*

# EXHIBIT 1



US006157589A

**United States Patent** [19]  
**Krause**

[11] **Patent Number:** **6,157,589**  
 [45] **Date of Patent:** **Dec. 5, 2000**

[54] **DYNAMIC SEMICONDUCTOR MEMORY DEVICE AND METHOD FOR INITIALIZING A DYNAMIC SEMICONDUCTOR MEMORY DEVICE**

FOREIGN PATENT DOCUMENTS

0 797 207 A2 9/1997 European Pat. Off. .  
 9-106668 4/1997 Japan .

[75] Inventor: **Gunnar Krause**, Munich, Germany

*Primary Examiner*—Vu A. Le  
*Attorney, Agent, or Firm*—Herbert L. Lerner; Laurence A. Greenber; Werner H. Stemer

[73] Assignee: **Siemens Aktiengesellschaft**, Munich, Germany

[57] **ABSTRACT**

A dynamic semiconductor memory device of a random access type has an initialization circuit that controls the switching-on operation of the semiconductor memory device and of its circuit components. The initialization circuit supplies a supply voltage stable signal once the supply voltage has been stabilized after the switching-on of the semiconductor memory device. The initialization circuit has an enable circuit that receives the supply voltage stable signal and further command signals externally applied to the semiconductor memory device. The enable circuit supplies an enable signal after a predetermined proper initialization sequence of the command signals applied to the semiconductor memory device is identified. The enable signal effects the unlatching of a control circuit provided for the proper operation of the semiconductor memory device.

[21] Appl. No.: **09/343,431**

[22] Filed: **Jun. 30, 1999**

[30] **Foreign Application Priority Data**

Jun. 30, 1998 [DE] Germany ..... 198 29 287

[51] **Int. Cl.**<sup>7</sup> ..... **G11C 8/00**

[52] **U.S. Cl.** ..... **365/226; 365/228**

[58] **Field of Search** ..... **365/226, 227, 365/228**

[56] **References Cited**

U.S. PATENT DOCUMENTS

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 5,841,724 11/1998 Ebel et al. .... 365/226  
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**13 Claims, 3 Drawing Sheets**

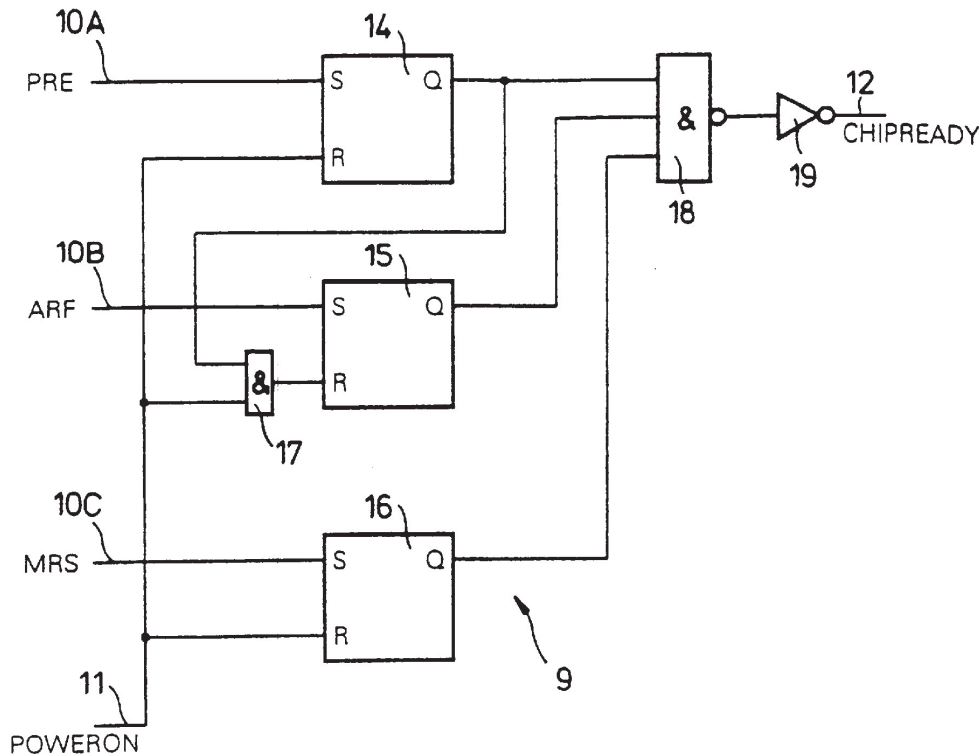
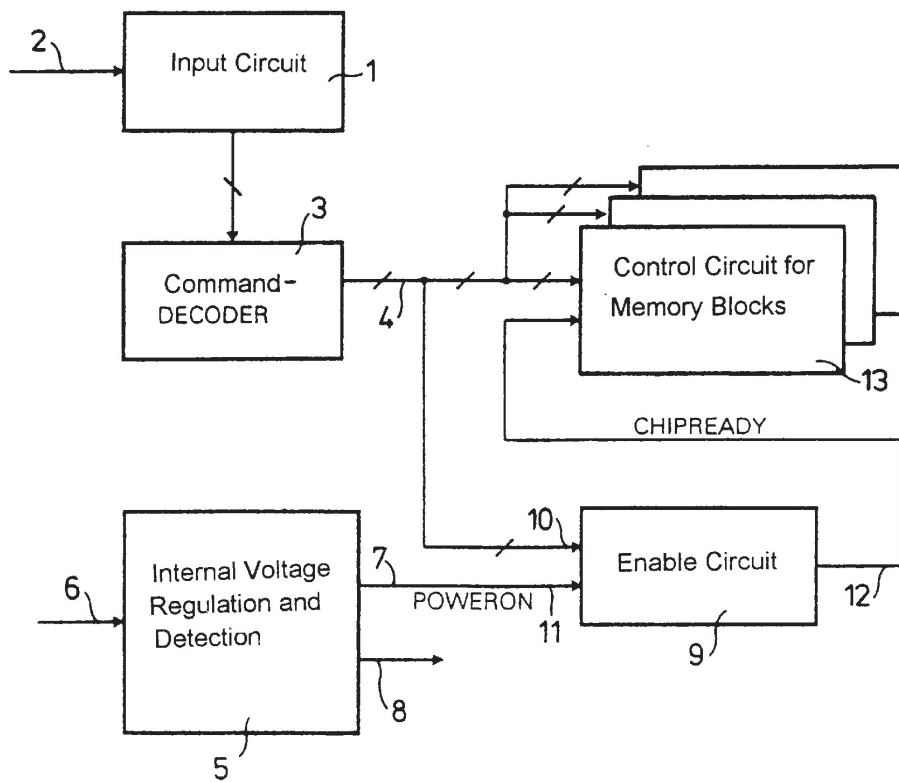




Fig 1



U.S. Patent

Dec. 5, 2000

Sheet 2 of 3

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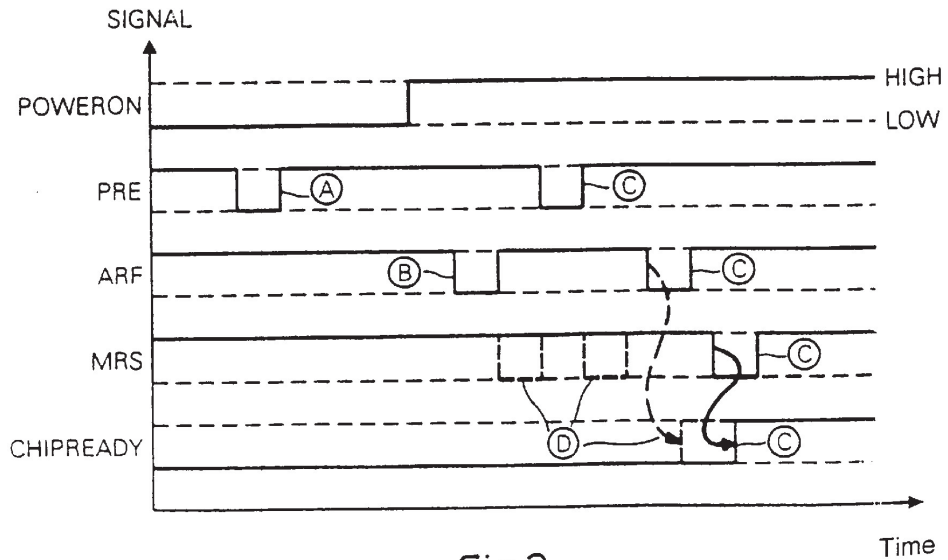
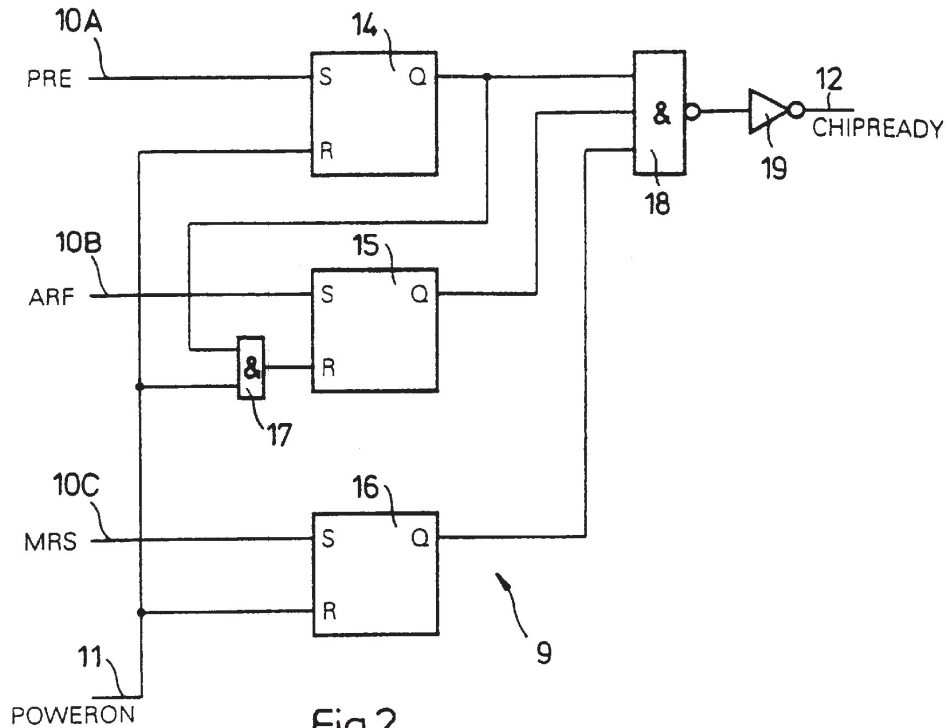


Fig 3

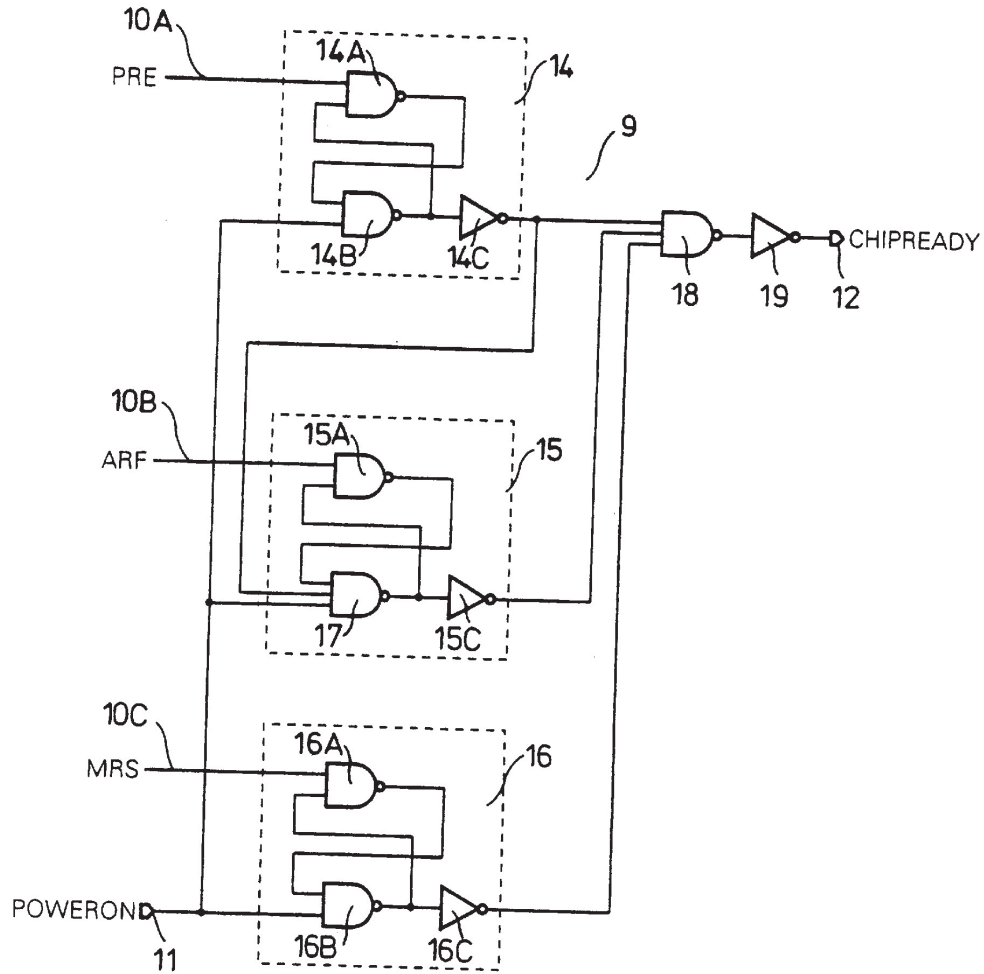


Fig 4

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**DYNAMIC SEMICONDUCTOR MEMORY  
DEVICE AND METHOD FOR INITIALIZING  
A DYNAMIC SEMICONDUCTOR MEMORY  
DEVICE**

**BACKGROUND OF THE INVENTION**

Field of the Invention

The invention relates to a dynamic semiconductor memory device of the random access type (DRAM/SDRAM) having an initialization circuit which controls a switching-on operation of the semiconductor memory device and of its circuit components. The initialization circuit supplies a supply voltage stable signal (POWERON) once a supply voltage has been stabilized after the switching-on of the semiconductor memory device. The invention also relates to a method for initializing such a dynamic semiconductor memory device, and also to the use of an enable circuit, that supplies an enable signal, for controlling the switching-on operation of the dynamic semiconductor memory device.

In the case of SDRAM semiconductor memories according to the JEDEC standard, it is necessary to ensure during the switch-on operation ("POWERUP") that the internal control circuits provided for the proper operation of the semiconductor memory device are reliably held in a defined desired state, in order to prevent undesirable activation of output transistors that would cause, on the data lines, a short circuit (so-called "bus contention" or "data contention") or uncontrolled activation of internal current loads. The solution to the problem turns out to be difficult on account of a fundamental unpredictability of the time characteristic of the supply voltage and of the voltage level or levels at the external control inputs during the switch-on operation of the semiconductor memory. According to the specifications of the manufacturer an SDRAM component should ignore all commands which are present chronologically before a defined initialization sequence. The sequence consists of predetermined commands that must be applied in a defined chronological order. However, a series of functions and commands which are allowed during proper operation of the component are desired or allowed chronologically only after the initialization sequence. According to the JEDEC standard for SDRAM semiconductor memories, a recommended initialization sequence (so-called "POWERON-SEQUENCE") is provided as follows:

- a. the application of a supply voltage and a start pulse in order to maintain an NOP condition at the inputs of the component;
- b. the maintenance of a stable supply voltage of a stable clock signal, and of stable NOP input conditions for a minimum time period of 200 us;
- c. the preparation command for word line activation (PRECHARGE) for all the memory banks of the device;
4. the activation of eight or more refresh commands (AUTOREFRESH); and
5. the activation of a loading configuration register command (MODE-REGISTER-SET) for initializing the mode register.

After the identification of such a defined initialization sequence, the memory module is normally in a so-called IDLE state, that is to say it is precharged and prepared for proper operation. In the case of the SDRAM semiconductor memory modules that have been disclosed to date, all the control circuits of the component have been unlatched only

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with the POWERON signal. The signal POWERON is active if the internal supply voltages have reached the necessary values that are necessary for the proper operation of the component. The module is then in a position to recognize and execute instructions.

**SUMMARY OF THE INVENTION**

It is accordingly an object of the invention to provide a dynamic semiconductor memory device and a method for initializing a dynamic semiconductor memory device which overcome the above-mentioned disadvantages of the prior art methods and devices of this general type, which is as simple as possible in structural terms and which effectively prevents the risk of a short circuit of the data lines and/or of uncontrolled activation of internal current loads.

With the foregoing and other objects in view there is provided, in accordance with the invention, a dynamic semiconductor memory device of a random access type, containing an initialization circuit controlling a switching-on operation and supplying a supply voltage stable signal once a supply voltage has been stabilized after the switching-on operation. The initialization circuit has a control circuit for controlling operations and an enable circuit receiving the supply voltage stable signal and externally applied further command signals. The enable circuit outputting an enable signal after a predetermined proper initialization sequence of the externally applied further command signals are identified and the enable signal effecting an unlatching of the control circuit.

The invention provides for the initialization circuit to have an enable circuit, which receives the supply voltage stable signal and the externally applied further command signals. The enable circuit generates the enable signal after the identification of the predetermined proper initialization sequence of the command signals is achieved. The enable signal effects the unlatching of the control circuit provided for the proper operation of the semiconductor memory device.

Following the principle of the invention, the enable signal (CHIPREADY) is generated and becomes active in dependence on further internal signals and the initialization sequence and then unlatches predetermined circuits. The predetermined circuits remain latched until the end of the predetermined initialization sequence. By way of example, commands are decoded but not executed and the output drivers are held at high impedance.

According to the preferred application in SDRAM memory devices according to the JEDEC standard, it is provided that the command signals, externally applied to the semiconductor memory device, of the initialization sequence are to be identified by the enable circuit. The command signals include a preparation command signal for word line activation (PRECHARGE), and/or a refresh command signal (AUTOREFRESH), and/or a loading configuration register command signal (MODE-REGISTER-SET).

According to an advantageous structural refinement of the initialization circuit according to the invention, it is provided that the enable circuit has at least one bistable multivibrator stage with a set input which receives the command signal (PRECHARGE, AUTOREFRESH, MODE-REGISTER-SET). The bistable multivibrator also has a reset input to which the supply voltage stable signal (POWERON), a signal derived therefrom, or a linked signal is applied. The bistable multivibrator further has an output at which the enable signal (CHIPREADY) is outputted.

In particular, the enable circuit has a plurality of bistable multivibrator stages respectively receiving the command signals.

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In an expedient refinement of the invention, it is provided that the output of at least one of the bistable multivibrator stages is passed to a reset input of a further multivibrator stage. In this case, it may furthermore be provided that, in one of the bistable multivibrator stages, the supply voltage stable signal (POWERON) and the signal output from the output of the further multivibrator stage are passed, after having been logically combined by a gate, to the reset input of the multivibrator stage.

Other features which are considered as characteristic for the invention are set forth in the appended claims.

Although the invention is illustrated and described herein as embodied in a dynamic semiconductor memory device and a method for initializing a dynamic semiconductor memory device, it is nevertheless not intended to be limited to the details shown, since various modifications and structural changes may be made therein without departing from the spirit of the invention and within the scope and range of equivalents of the claims.

The construction and method of operation of the invention, however, together with additional objects and advantages thereof will be best understood from the following description of specific embodiments when read in connection with the accompanying drawings.

#### BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a diagrammatic, block diagram of components of an initialization circuit which controls a switching-on operation of a semiconductor memory and its circuit components according to the invention;

FIG. 2 is circuit diagram of an enable circuit that supplies an enable signal (CHIPREADY);

FIG. 3 is a time sequence diagram for elucidating a method of operation of the circuit according to FIG. 2; and

FIG. 4 is a circuit diagram of the enable circuit according to an exemplary embodiment of the invention.

#### DESCRIPTION OF THE PREFERRED EMBODIMENTS

In all the figures of the drawing, sub-features and integral parts that correspond to one another bear the same reference symbol in each case. Referring now to the figures of the drawing in detail and first, particularly, to FIG. 1 thereof, there are shown circuit components, important for understanding the invention, of an SDRAM memory device operating according to the JEDEC standard. The circuit components include an initialization circuit controlling a switching-on operation of the SDRAM memory device and its circuit components. The initialization circuit has an input circuit 1, to whose input 2 command and clock signals that are externally applied in reference to the semiconductor memory are provided. The command and clock signals are amplified and conditioned before being received by a command decoder 3 connected downstream of the input circuit 1 and at whose output 4, inter alia, the command signals PRE or PRECHARGE (preparation command for word line activation), ARF or AUTOREFRESH (refresh command) and MRS or MODE-REGISTER-SET (loading configuration register command) are output. The initialization circuit further has a circuit 5 for internal voltage regulation and/or detection, at whose input 6 the external supply voltages that are externally applied to the semiconductor memory externally are fed in. The circuit 5 has a first output 7 outputting a POWERON signal and a second output 8 supplying stabilized internal supply voltages. The method of operation

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and the structure of the circuits 1, 3 and 5 are sufficiently known to the person skilled in the art and therefore do not need to be explained in any more detail. What is important for understanding the invention is the fact that the circuit 5 supplies an active POWERON signal if, after the POWERUP phase of the SDRAM memory, the internal supply voltages present at the output 8 have reached the values necessary for proper operation of the component.

According to the invention, the initialization circuit furthermore has an enable circuit 9 connected downstream of the circuits 3 and 5. The command signals PRE, ARF and MRS are applied to an input 10 of the enable circuit 9 and the POWERON signal is applied to an input 11 of the enable circuit 9. An enable signal CHIPREADY is supplied at an output 12 of the enable circuit 9 after the identification of a predetermined proper initialization sequence of the command signals applied to the semiconductor memory device is achieved. The enable signal effects unlatching of control circuits 13 provided for proper operation of the semiconductor memory device. The internal control circuits 13 serve inter alia for sequence control for one or more of the memory blocks of the SDRAM memory and are known as such.

FIG. 2 shows a preferred exemplary embodiment of the enable circuit 9 according to the invention. The enable circuit 9 contains three bistable multivibrator stages 14, 15 and 16 each having a set input S, a reset input R, and also an output Q. An AND gate 17 connected upstream of the reset input R of the multivibrator stage 15 and an AND gate 18 connected downstream of all the outputs Q of the multivibrator stages 14, 15, 16 are further provided. The enable circuit further has an inverter 19 connected downstream of the AND gate 18. The enable signal CHIPREADY being output at the output 12 of the inverter 19 and the enable signal CHIPREADY is active HIGH, that is to say activated when its voltage level is at logic HIGH. The command signals PRE, ARF, MRS applied to the respective set inputs S of the bistable multivibrator stages 14, 15, 16 are each active LOW, that is to say these signals are active when their voltage level is at logic LOW, while the POWERON signal is again active HIGH. The POWERON signal is applied directly to the reset inputs R in the case of the multivibrator stages 14 and 16 and is firstly applied to one input of the AND gate 17 in the case of the multivibrator stage 15, the signal output from the output Q of the multivibrator stage 14 is applied to the other input of the AND gate 17, the output of the AND gate 17 is connected to the reset input of the multivibrator stage 15.

The method of operation of the enable circuit 9 illustrated in FIG. 2 is such that activation of the enable signal CHIPREADY at is the output 12 to logic HIGH is generated only when a predetermined chronological initialization sequence of the command signals PRE, ARF and MRS and activation of the POWERON signal to the logic level HIGH are detected. Only then are the control circuits 13 unlatched on account of the activation of the enable signal CHIPREADY; the control circuits 13 remaining latched prior to this.

In the schematic time sequence diagram according to FIG. 3, exemplary command sequences during the switching-on operation of the semiconductor memory device are illustrated in order to elucidate the method of operation of the enable circuit 9. In the case situation A, the signal PRECHARGE is activated to active LOW too early relative to the activation of the POWERON signal, with the result that, the enable signal CHIPREADY is not yet activated to logic HIGH since the proper initialization sequence requires a

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waiting time before the first command. The signal swing of the command PRECHARGE according to case situation A is thus correctly ignored. In case situation B, the chronological order of the activation of the signal AUTOREFRESH to logic LOW is incorrect since the proper initialization sequence prescribes a previous PRECHARGE command before the AUTOREFRESH command. The signal swing of the AUTOREFRESH signal to logic LOW according to case situation B is therefore likewise ignored, and the enable signal does not go to logic HIGH. In case situation C, a correct chronological order of the commands PRECHARGE, AUTOREFRESH, MODE-REGISTER-SET is present conforming to the JEDEC standard, in a logically consistent manner, since the POWERON signal is also at logic HIGH, an enable signal CHIPREADY at logic HIGH is now supplied. Illustrated using dashed lines, another further conceivable initialization sequence that is allowed and therefore triggers an enable signal is represented by the symbol D; activation of the command MODE-REGISTER-SET to logic LOW is allowed at any time after the activation of the POWERON signal.

FIG. 4 shows further details of a preferred exemplary embodiment of the enable circuit 9 according to the invention. In this exemplary embodiment, each of the bistable multivibrators 14, 15, 16 is constructed from in each case two NAND gates 14A, 14B, 15A, 17, 16A, 16B and also an inverter 14C, 15C and 16C, which are connected to one another in the manner illustrated. The NAND gate 17 is provided with three inputs in the bistable multivibrator 15.

I claim:

1. A dynamic semiconductor memory device of a random access type, comprising:

an initialization circuit controlling a switching-on operation and supplying a supply voltage stable signal once a supply voltage has been stabilized after the switching-on operation, said initialization circuit having a control circuit for controlling operations and an enable circuit receiving the supply voltage stable signal and externally applied further command signals, said enable circuit outputting an enable signal after a predetermined proper initialization sequence of the externally applied further command signals being identified and the enable signal effecting an unlatching of said control circuit.

2. The semiconductor memory device according to claim 1, wherein the externally applied further command signals forming the predetermined proper initialization sequence to be identified by said enable circuit includes at least one of a preparation command signal for word line activation, a refresh command signal, and a loading configuration register command signal.

3. The semiconductor memory device according to claim 1, wherein said enable circuit has at least one bistable multivibrator stage having a set input receiving the externally applied further command signals, a reset input receiving one of the supply voltage stable signal, a signal derived from the supply voltage stable signal and a linked signal, and an output outputting said enable signal.

4. The semiconductor memory device according to claim 3, wherein said at least one bistable multivibrator stage is a plurality of bistable multivibrator stages respectively receiving one of the externally applied further command signals.

5. The semiconductor memory device according to claim 4, wherein said output of one of said plurality of bistable multivibrator stages is passed to said reset input of another of said plurality of bistable multivibrator stages.

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6. The semiconductor memory device according to claim 4, including an AND gate receiving the supply voltage stable signal and a signal output from said output of one of said plurality of bistable multivibrator stages, said AND gate outputting an output signal received at said reset input of another of said plurality of bistable multivibrator stages.

7. The semiconductor memory device according to claim 4, wherein said plurality of bistable multivibrator stages are each formed of an RS flip-flop constructed from one of at least two NOR and at least two NAND gates.

8. The semiconductor memory device according to claim 1, wherein the identification of an initialization sequence that is identified as the predetermined proper initialization sequence by said enable circuit and generates the enable signal constitutes a command sequence conforming to a JEDEC standard.

9. The semiconductor memory device according to claim 1, wherein said control circuit has output drivers remaining latched during the switching-on operation until said enable signal is generated by said enable circuit.

10. The semiconductor memory device according to claim 1, wherein the predetermined proper initialization sequence includes one of the following chronologically successive command sequences:

- a) firstly PRE, secondly ARF, thirdly MRS;
- b) firstly PRE, secondly MRS, thirdly ARF; and
- c) firstly MRS, secondly PRE, or thirdly ARF;

where,

PRE=the preparation command signal for word line activation,

ARF=the refresh command signal, and

MRS=the loading configuration register command signal.

11. An improved method for initializing a dynamic semiconductor memory device of a random access type via an initialization circuit controlling a switching-on operation of the dynamic semiconductor memory device and of its circuit components, the improvement which comprises:

supplying, via the initialization circuit, a supply voltage stable signal once a supply voltage has been stabilized after the switching-on operation of the dynamic semiconductor memory device; and

supplying, via an enable circuit of the initialization circuit, an enable signal, the initialization circuit receiving the supply voltage stable signal and further command signals externally applied to the dynamic semiconductor memory device, after an identification of a predetermined proper initialization sequence of the further command signals the enable signal being generated and effecting an unlatching of a control circuit provided for a proper operation of the dynamic semiconductor memory device.

12. The method according to claim 11, which comprises providing at least one of a preparation command signal for word line activation, a refresh command signal, and a loading configuration register command signal as the further command signals.

13. The method according to claim 11, which comprises maintaining a latched condition of output drivers of the dynamic semiconductor memory device during the switching-on operation until the enable signal is generated by the enable circuit.

\* \* \* \* \*

# EXHIBIT 2



US006438057B1

(12) **United States Patent**  
**Ruckerbauer**

(10) **Patent No.: US 6,438,057 B1**  
 (45) **Date of Patent: Aug. 20, 2002**

- (54) **DRAM REFRESH TIMING ADJUSTMENT DEVICE, SYSTEM AND METHOD**
- (75) Inventor: **Hermann Ruckerbauer, Moos (DE)**
- (73) Assignee: **Infineon Technologies AG (DE)**
- (\* ) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.
- (21) Appl. No.: **09/900,626**
- (22) Filed: **Jul. 6, 2001**
- (51) **Int. Cl.<sup>7</sup> ..... G11C 7/00**
- (52) **U.S. Cl. .... 365/222; 365/211**
- (58) **Field of Search ..... 365/222, 211, 365/228**

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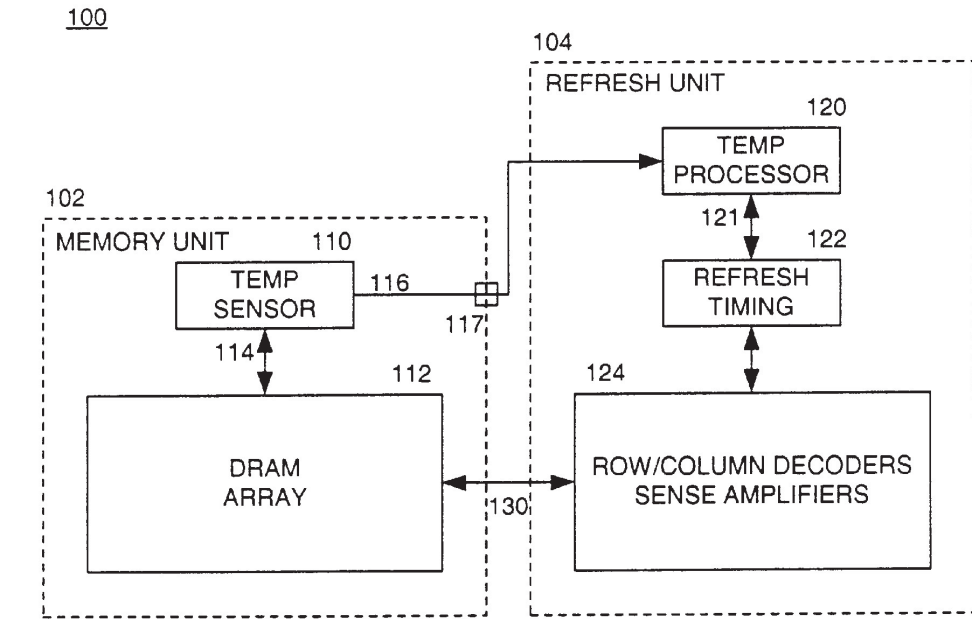
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*Primary Examiner*—Vu A. Le  
 (74) *Attorney, Agent, or Firm*—Lerner, David, Littenberg, Krumholz & Mentlik, LLP

(57) **ABSTRACT**

An apparatus includes at least one dynamic random access memory (DRAM) array; and at least one temperature sensor in thermal communication with the DRAM array and operable to produce a signal indicative of a temperature of the DRAM array.

**17 Claims, 5 Drawing Sheets**





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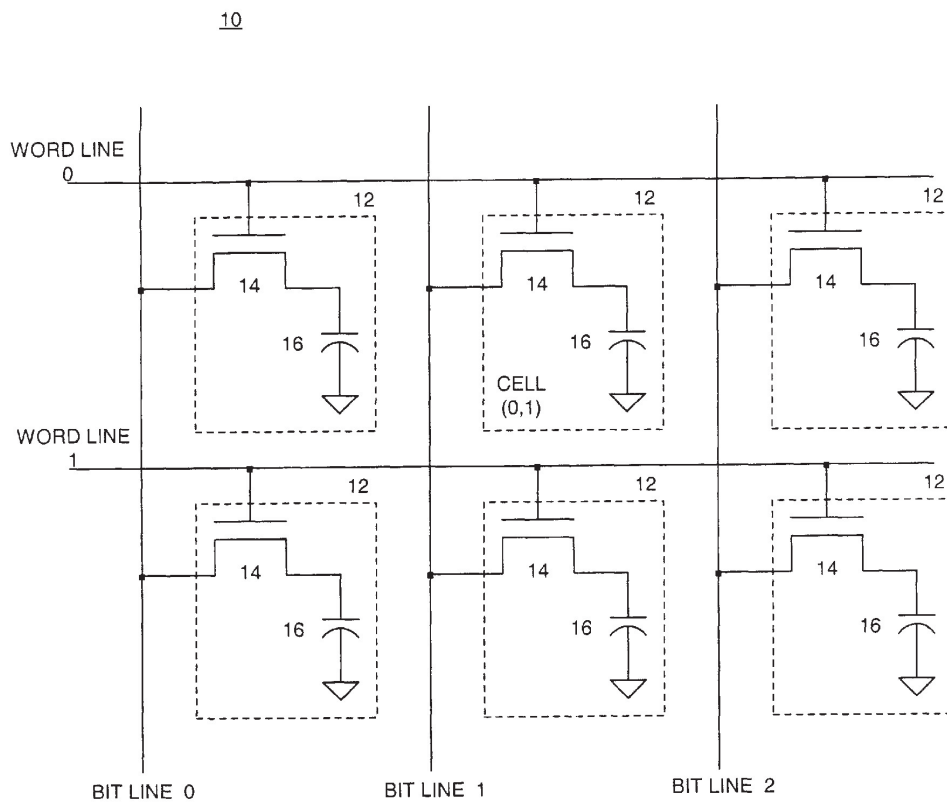


FIG. 1

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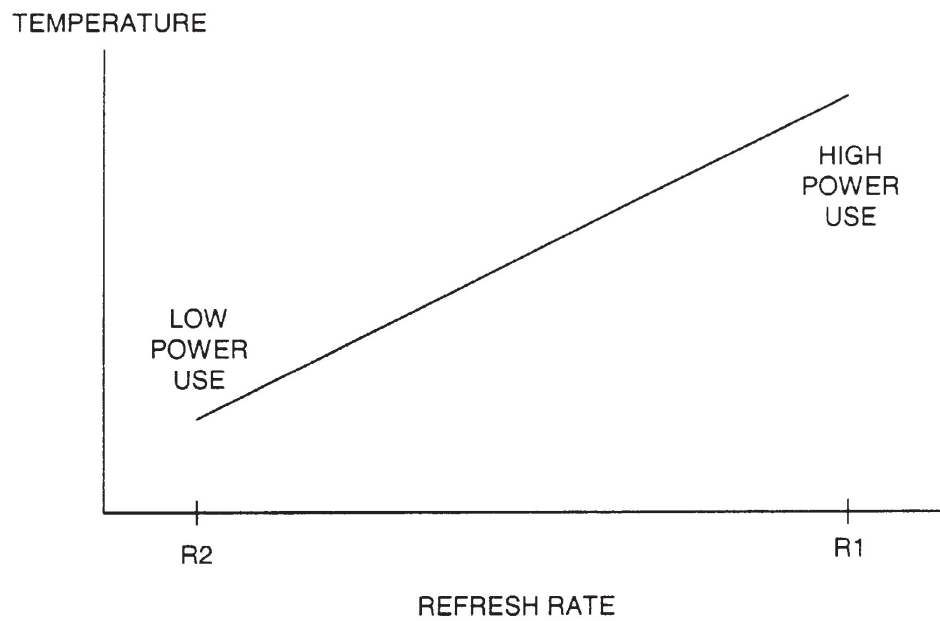


FIG. 2

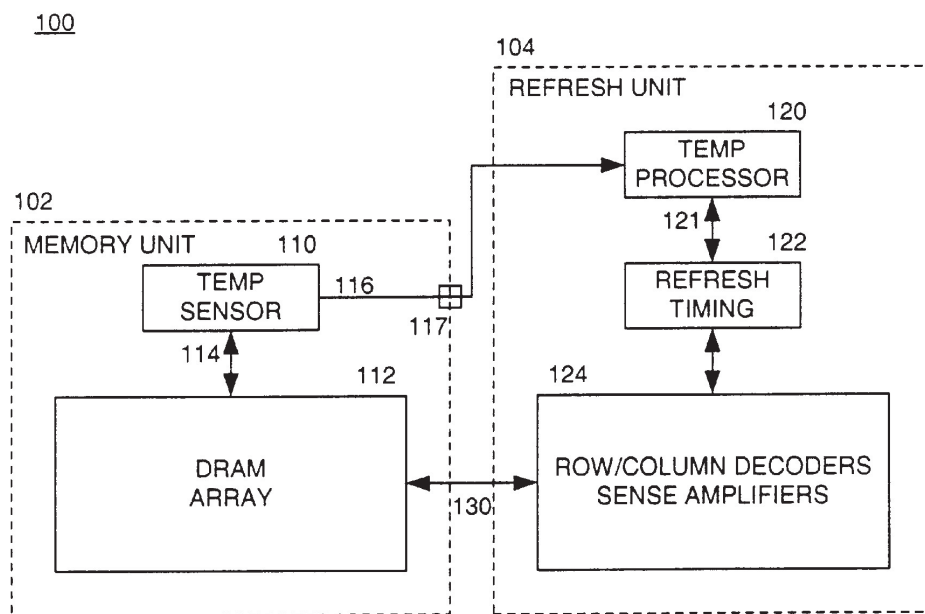


FIG. 3

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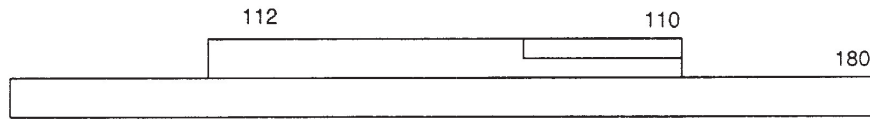


FIG. 4A

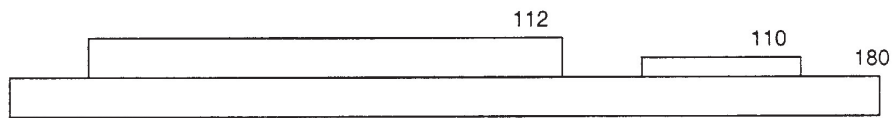


FIG. 4B

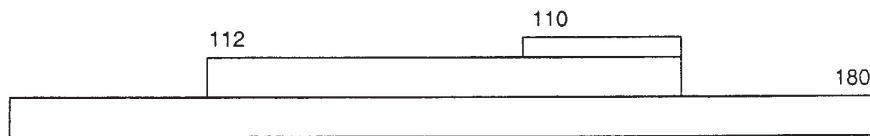


FIG. 4C

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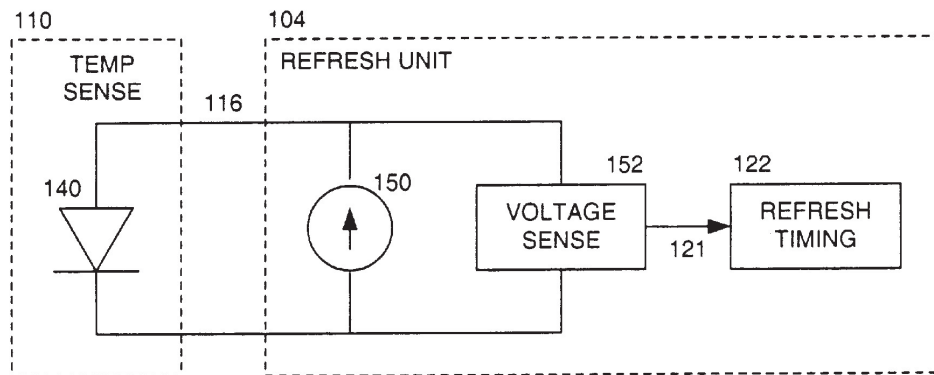


FIG. 5

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**DRAM REFRESH TIMING ADJUSTMENT  
DEVICE, SYSTEM AND METHOD****BACKGROUND OF THE INVENTION**

The present invention relates to devices, systems, and/or methods for refreshing the contents of a dynamic random access memory (DRAM) array and, more particularly, to devices, systems, and/or methods for utilizing a temperature of the DRAM array to adjust a refresh rate at which the contents of the DRAM array are updated.

A common form of random access memory (RAM) is dynamic random access memory (DRAM). With reference to the equivalent circuit shown in FIG. 1, DRAMs employ a semiconductor technology called complementary metal-oxide-semiconductor CMOS to implement a memory array 10 including a plurality of memory cells 12, each cell 12 consisting of a single transistor 14 and a single capacitor 16. A given cell 12 of the DRAM array 10 may be accessed by activating a particular bit line and word line. As the cells 12 of the DRAM array are arranged in a grid, only one cell 12 will be accessed for each combination of word line and bit line.

For example, in order to write a data bit into cell (0,1), word line 0 is activated by applying an appropriate voltage to that line, e.g., a logic high (such as 3.3V, 5V, 15V, etc.) or a logic low (such as 0V). The appropriate voltage on word line 0 will turn on each of the transistors 14 connected to that line including the transistor 14 of cell (0,1). A voltage may then be presented on bit line 1, which will charge the capacitor 16 of cell (0,1) to a desired level, e.g., a logic high or logic low consistent with the data bit. The voltage may be presented on bit line 1 (and/or any of the other bit lines) by way of a suitably connected data bus. When the voltage on word line 0 is removed, the transistor 14 of cell (0,1) is biased off and the charge on the capacitor 16 of cell (0,1) is stored.

Reading a data bit from a particular cell 12, such as cell (0,1), is substantially similar to writing a data bit except that the voltage on bit line 1 is imposed by the capacitor 16 of the cell 12 rather than by the data bus. Typically, a single cell 12 is not written to or read from; rather, an entire word (series of data bits) is written into the DRAM array 10 or read from the DRAM array 10 by applying the appropriate voltage on a particular word line and either imposing or sensing voltage on each of the bit lines 0,1,2, etc.

Once data bits (i.e., voltages) have been stored on the capacitors 16 of the DRAM array 10, the data are not permanent. Indeed, various leakage paths exist around the capacitors 16 and, therefore, failure to read the data may corrupt the stored voltages. In order to avoid the loss of data stored in the DRAM array 10, the data are refreshed on a periodic basis. In particular, an external sense amplifier is employed to sense the data stored in the DRAM array 10 and rewrite (i.e., refresh) the data onto the capacitors 16. Typically, the data associated with a particular word line (i.e., one data word) are refreshed every 7.8 microseconds (e.g., for 256 Mbit DRAM arrays) or every 15.6 microseconds (e.g., for 64 Mbit DRAM arrays). The refresh rate for a particular DRAM array 10 is established by the manufacturer and is based on a worst-case high temperature condition.

The refresh process may be implemented in either of two ways, namely, internally (self refresh) or externally (CBR or Ras only refresh). The internal refresh process requires that the DRAM itself set the refresh timing. The external refresh process requires an external chip (chipset) that issues a

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refresh command. The DRAM receives the refresh command from the external chip through a dedicated pin.

Unfortunately, the refresh process has a deleterious effect on overall system performance. Among these deleterious effects are: (i) an increase in power consumed by the DRAM array 10 and any external circuitry involved in the refresh process; and (ii) a decrease in overall system bandwidth. As to the former, the external sense amplifiers and other associated circuitry (e.g., row decoders, column decoders, etc.) involved in the refresh process, not to mention the DRAM array 10 itself, draw power in order to rewrite the data into the DRAM array 10. In certain applications, such as in the automotive industry, power efficiency is desirable and increases in power consumption due to DRAM array 10 refresh cycles may be problematic. As to the latter, the refresh cycles of the DRAM array 10 take priority over routine reading and writing cycles and, therefore, the rate at which the DRAM array 10 is refreshed has a corresponding impact on the bandwidth (e.g., data throughput) of the overall system in which the DRAM array 10 is utilized.

Accordingly, there is a need in the art for a new device, system, and/or method for refreshing the data of a DRAM array such that power consumption is reduced and system bandwidth is increased.

**SUMMARY OF THE INVENTION**

In accordance with at least one aspect of the present invention, an apparatus includes: at least one DRAM array; and at least one temperature sensor in thermal communication with the DRAM array and operable to produce a signal indicative of a temperature of the DRAM array.

Preferably, the DRAM array is refreshed at a rate that varies in response to the signal. For example, the rate at which the DRAM array is refreshed may decrease as the temperature of the DRAM array decreases. Further, the rate at which the DRAM array is refreshed may increase as the temperature of the DRAM array increases.

Preferably, the at least one temperature sensor includes at least one diode having a forward voltage drop that varies as a function of the temperature of the DRAM array, and the signal corresponds to the forward voltage drop of the at least one diode. Alternatively, the at least one temperature sensor may be taken from the group consisting of thermocouples, thermistors, or any other device that provides an output signal that varies as a function of temperature.

In accordance with one or more further aspects of the invention, the apparatus may further include a refresh unit operable to refresh the DRAM array at a rate that varies in response to the signal. Preferably, the refresh unit includes a refresh timing unit operable to establish the rate at which the DRAM array is refreshed in response to the signal. It is preferred that the refresh timing unit is operable to decrease the rate at which the DRAM array is refreshed as the signal indicates that the temperature of the DRAM array decreases. It is also preferable that the refresh timing unit is operable to increase the rate at which the DRAM array is refreshed as the signal indicates that the temperature of the DRAM array increases.

When the at least one temperature sensor is a diode, it is preferable that the refresh unit is operable to sense the forward voltage drop of the diode to determine the temperature of the DRAM array.

In accordance with one or more further aspects of the present invention, the DRAM array and the at least one temperature sensor are disposed in a semiconductor package, the package including at least one connection pin operable to provide the signal to external circuitry.

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In accordance with one or more further aspects of the invention, the DRAM array, the at least one temperature sensor, and the refresh unit are integrated in a semiconductor package.

In accordance with at least one further aspect of the present invention, the apparatus includes: at least one DRAM chip including the DRAM array and the at least one temperature sensor; at least one refresh chip operable to refresh the DRAM array at a rate that varies in response to the signal. Preferably, the refresh chip includes the refresh timing unit.

In accordance with one or more further aspects of the present invention, a method includes: sensing a temperature of a DRAM array; and refreshing contents of the DRAM array at a rate that varies in response to the temperature thereof.

The method preferably further includes decreasing the rate at which the DRAM array is refreshed as the temperature of the DRAM array decreases. The method may also include increasing the rate at which the DRAM array is refreshed as the temperature of the DRAM array increases. It is most preferred that the step of sensing the temperature of the DRAM array includes sensing a forward voltage drop of a diode that is in thermal communication with the DRAM array.

Other aspects, features, advantages, etc. will become apparent to one skilled in the art in view of the description herein taken in combination with the accompanying drawings.

#### BRIEF DESCRIPTION OF THE DRAWINGS

For the purposes of illustrating the invention, there are shown in the drawings forms which are presently preferred, it being understood, however, that the invention is not limited to the precise arrangements and/or instrumentalities shown.

FIG. 1 is a DRAM array in accordance with the prior art;

FIG. 2 is a graph illustrating the relationship between a temperature of the DRAM array and a desirable refresh rate of the DRAM array;

FIG. 3 is a block diagram of a DRAM apparatus in accordance with one or more aspects of the present invention; and

FIGS. 4A–4C are structural views of alternative DRAM configurations in accordance with the present invention; and

FIG. 5 is a block diagram showing additional details of certain components of FIG. 3.

#### DETAILED DESCRIPTION

With reference to FIG. 2, it has been found that the refresh rate established by DRAM array manufacturers may be altered when the temperature of the DRAM array is lower than a worst-case value. For example, when the temperature of the DRAM array is relatively high, a correspondingly high refresh rate R1 may be required to ensure integrity of the data stored in the DRAM array. The relatively high refresh rate R1 unfortunately results in a correspondingly high power use and a low system bandwidth. Conversely, when the temperature of the DRAM array is relatively low, it has been found that a correspondingly lower refresh rate R2 may be utilized to ensure the integrity of the data stored in the DRAM array. Advantageously, the relatively lower refresh rate R2 results in a lower power usage and higher overall system bandwidth. Although the relationship between the temperature and the refresh rate of the DRAM

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array is illustrated as being a linear function in FIG. 2, it is noted that the relationship may not be linear and may vary depending on the specific implementation of the DRAM array. It is believed, however, that the overall relationship between temperature and refresh rate for DRAM arrays will exhibit a positive slope. In accordance with one or more aspects of the present invention, this relationship is exploited to reduce power consumption of the DRAM array (and any associated circuitry) and improve overall system bandwidth.

FIG. 3, is a block diagram of a system 100 for storing data in a DRAM array. The system 100 includes a memory unit 102 and a refresh unit 104. The memory unit 102 preferably includes at least one temperature sensor 110 and at least one DRAM array 112. The DRAM array 112 may be configured in a substantially similar way as shown in FIG. 1 and/or may be configured in accordance with any of the known technologies. Preferably, the temperature sensor 110 is in thermal communication with the DRAM array 112 (schematically illustrated by way of line 114) and is operable to produce a signal on line 116 that is indicative of a temperature of the DRAM array 112. By way of example, the DRAM array 112 may be implemented on a semiconductor chip and the temperature sensor 110 may be thermally coupled to the same semiconductor chip or to an intermediate member that is in thermal communication with the semiconductor chip.

The refresh unit 104 preferably includes a temperature processor 120, a refresh timing unit 122, and a decoder/amplifier unit 124. The refresh unit 104 is preferably operable to refresh the DRAM array 112 (by way of connection 130) at a rate that varies in response to the signal on line 116. More particularly, the DRAM array 112 is preferably refreshed at a rate that decreases as the temperature of the DRAM array 112 decreases and/or refreshed at a rate that increases as the temperature of the DRAM array 112 increases. The temperature processor 120 is preferably operable to detect a level of the signal on line 116 and to provide an indication of the temperature (by way of line 121) of the DRAM array 112 to the refresh timing unit 122. The refresh timing unit 122 is preferably operable to establish the rate at which the DRAM array 112 is refreshed in response to the temperature indication from the temperature processor 120. The row/column decoders and sense amplifiers 124 are preferably operable to perform the refresh function on the DRAM array 112 in accordance with known techniques at intervals dictated by the refresh timing unit 122.

In accordance with at least one aspect of the present invention, the temperature sensor 110 and the DRAM array 112 are preferably disposed in a semiconductor package where the package includes at least one connection pin 117 operable to provide the signal on line 116 to external circuitry, such as the refresh unit 104. In accordance with a further aspect of the present invention, the DRAM array 112, temperature sensor 110, and the refresh unit 104 are integrated in the same semiconductor package such that external circuitry is not required to perform the refresh function. In accordance with a further aspect of the present invention, the refresh unit 104 is implemented by way of one or more semiconductor packages so as to form a chipset with the package containing the temperature sensor 110 and the DRAM array 112.

Reference is now made to FIGS. 4A–4C, which are structural views of alternative configurations of the DRAM array 112 and temperature sensor 110. In FIG. 4A, the DRAM array 112 is disposed on an intermediate member 180, such as a substrate, a heatsink, etc. The temperature

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sensor 110 is integrated with the DRAM array structure 112, such as by implementing the temperature sensor 110 into the semiconductor material of the DRAM array 112. As shown in FIG. 4B, an alternative structural configuration is contemplated where the DRAM array 112 and the temperature sensor 110 are disposed on the intermediate member 180, where the intermediate member 180 exhibits desirable thermal conductivity properties. Indeed, in this configuration it is preferred that the intermediate member 180 exhibits a low thermal resistance between the DRAM array 112 and the temperature sensor 110 such that an accurate measurement of the temperature of the DRAM array 112 may be obtained. The structural configuration shown in FIG. 4C shows that the temperature sensor 110 may be coupled to the semiconductor device 112, such as by bonding it to the semiconductor material of the DRAM array 112.

With reference to FIG. 5, the temperature sensor 110 preferably includes at least one diode 140 having a forward voltage drop that varies as a function of the temperature of the DRAM array 112. The signal on line 116 preferably corresponds to the forward voltage drop of the diode 140. By way of example, the refresh unit 104 may include a current source 150 operatively coupled to the diode 140 such that the diode 140 is forward biased. The refresh unit 104 may also include a voltage sensor 152 operatively coupled across the diode 140 such that the forward voltage drop across the diode 140 may be measured. The voltage sensor 152 preferably produces a value on line 121 indicative of the temperature of the DRAM array 112 vis-a-vis the forward voltage drop of the diode 140.

Although the use of diode 140 is preferred, various other temperature sensing devices and techniques may be employed, such as the use of one or more thermocouples, thermistors, etc.

In accordance with at least one further aspect of the present invention, a method of refreshing the contents of a DRAM array may be achieved utilizing suitable hardware, such as that illustrated in FIGS. 3-5 and/or utilizing a manual or automatic process. An automatic process may be implemented using any of the known processors that are operable to execute instructions of a software program. In either case, the steps and/or actions of the method preferably correspond to the functions described hereinabove with respect to at least portions of the hardware shown in FIGS. 3-5.

Although the invention herein has been described with reference to particular embodiments, it is to be understood that these embodiments are merely illustrative of the principles and applications of the present invention. It is therefore to be understood that numerous modifications may be made to the illustrative embodiments and that other arrangements may be devised without departing from the spirit and scope of the present invention as defined by the appended claims.

What is claimed is:

1. An apparatus, comprising:

a semiconductor package including at least one connection pin;

at least one dynamic random access memory (DRAM) array disposed within the package; and

at least one temperature sensor in thermal communication with the DRAM array, operable to produce a signal

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indicative of a temperature of the DRAM array, and coupled to the at least one connection pin such that the signal may be provided to external circuitry,

wherein the DRAM array is refreshed at a rate that decreases as the temperature of the DRAM array decreases and that increases as the temperature of the DRAM array increases.

2. The apparatus of claim 1, wherein the at least one temperature sensor includes at least one diode having a forward voltage drop that varies as a function of the temperature of the DRAM array, and the signal corresponds to the forward voltage drop of the at least one diode.

3. The apparatus of claim 1, wherein the at least one temperature sensor is taken from the group consisting of thermocouples and thermistors.

4. The apparatus of claim 1, wherein the at least one temperature sensor includes a diode having a forward voltage drop that varies as a function of the temperature of the DRAM array; the at least one connection pin includes a first pin coupled to an anode of the diode and a second pin coupled to a cathode of the diode; and the signal corresponds to a potential voltage between the first and second pins.

5. The apparatus of claim 1, wherein the at least one temperature sensor is taken from the group consisting of thermocouples and thermistors.

6. The apparatus of claim 1, further comprising a refresh unit operable to refresh the DRAM array at a rate that varies in response to the signal.

7. The apparatus of claim 6, wherein the refresh unit includes a refresh timing unit operable to establish the rate at which the DRAM array is refreshed in response to the signal.

8. The apparatus of claim 7, wherein the refresh timing unit is operable to decrease the rate at which the DRAM array is refreshed as the signal indicates that the temperature of the DRAM array decreases.

9. The apparatus of claim 7, wherein the refresh timing unit is operable to increase the rate at which the DRAM array is refreshed as the signal indicates that the temperature of the DRAM array increases.

10. The apparatus of claim 7, wherein the at least one temperature sensor includes at least one diode having a forward voltage drop that varies as a function of the temperature of the DRAM array, and the signal corresponds to the forward voltage drop of the at least one diode.

11. The apparatus of claim 10, wherein the refresh unit is operable to sense the forward voltage drop of the diode to determine the temperature of the DRAM array.

12. The apparatus of claim 6, wherein the DRAM array, the at least one temperature sensor, and the refresh unit are integrated in a semiconductor package.

13. A dynamic random access memory (DRAM) chipset, comprising:

at least one DRAM chip including a DRAM array and at least one temperature sensor in thermal communication with the DRAM array, the at least one temperature sensor being operable to produce a signal indicative of a temperature of the DRAM array, the DRAM chip including at least one connection pin operable to provide the signal to external circuitry; and

at least one refresh chip operable to refresh the DRAM array at a rate that varies in response to the signal,



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wherein the refresh chip is operable to (i) decrease the rate at which the DRAM array is refreshed as the signal indicates that the temperature of the DRAM array decreases; and (ii) increase the rate at which the DRAM array is refreshed as the signal indicates that the temperature of the DRAM array increases.

14. The apparatus of claim 13, wherein the at least one temperature sensor includes at least one diode having a forward voltage drop that varies as a function of the temperature of the DRAM array, and the signal corresponds to the forward voltage drop of the at least one diode.

15. The apparatus of claim 14, wherein the refresh chip is operable to sense the forward voltage drop of the diode to determine the temperature of the DRAM array.

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16. A method, comprising:  
sensing a temperature of a dynamic random access memory (DRAM) array;  
outputting a signal indicative of the temperature of the DRAM array to external circuitry; and  
refreshing contents of the DRAM array at a rate that (i) decreases as the temperature of the DRAM array decreases; and (ii) increases as the temperature of the DRAM array increase.

17. The method of claim 16, wherein the step of sensing the temperature of the DRAM array includes sensing a forward voltage drop of a diode that is in thermal communication with the DRAM array.

\* \* \* \* \*

# EXHIBIT 3



US006850414B2

(12) **United States Patent**  
Benisek et al.

(10) **Patent No.:** US 6,850,414 B2  
(45) **Date of Patent:** Feb. 1, 2005

(54) **ELECTRONIC PRINTED CIRCUIT BOARD HAVING A PLURALITY OF IDENTICALLY DESIGNED, HOUSING-ENCAPSULATED SEMICONDUCTOR MEMORIES**

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(75) Inventors: **Martin Benisek**, München (DE);  
**Martin Schober**, Gröbenzell (DE)  
(73) Assignee: **Infineon Technologies AG**, Munich (DE)  
(\* ) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 374 days.

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(21) Appl. No.: **10/187,763**

(22) Filed: **Jul. 2, 2002**

(65) **Prior Publication Data**

US 2003/0002262 A1 Jan. 2, 2003

(30) **Foreign Application Priority Data**

Jul. 2, 2001 (DE) ..... 101 31 939

(51) **Int. Cl.**<sup>7</sup> ..... **H05K 1/00**; H05K 1/18;  
H05K 1/16; H05K 7/02; H05K 7/06

(52) **U.S. Cl.** ..... **361/748**; 361/760; 174/260

(58) **Field of Search** ..... 361/728-730,  
361/735, 736-737, 748, 749, 760, 763,  
767, 768, 807, 808, 785, 788, 790, 791,  
803; 257/693, 684, 679, 678; 711/301;  
714/773; 365/51-52, 63; 174/250, 253,  
255-256, 260

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*Primary Examiner*—Phuong T. Vu  
(74) *Attorney, Agent, or Firm*—Laurence A. Greenberg;  
Werner H. Stemer; Ralph E. Locher

(57) **ABSTRACT**

An electronic printed circuit board has a memory module and a contact strip for insertion into another electronic unit. The memory module has at least nine identically designed housing-encapsulated integrated semiconductor memories configured on the printed circuit board. The longer dimension of the housing of one of the semiconductor memories, which is connected as an error correction chip, is oriented perpendicular to the contact strip. The longer dimension of the housings of the other semiconductor memories are oriented parallel to the contact strip. The different orientation of the semiconductor memories makes it possible to reduce the height of the printed circuit board while enabling the rectangular housings to keep the same physical form.

**8 Claims, 3 Drawing Sheets**

