FIG. 7C

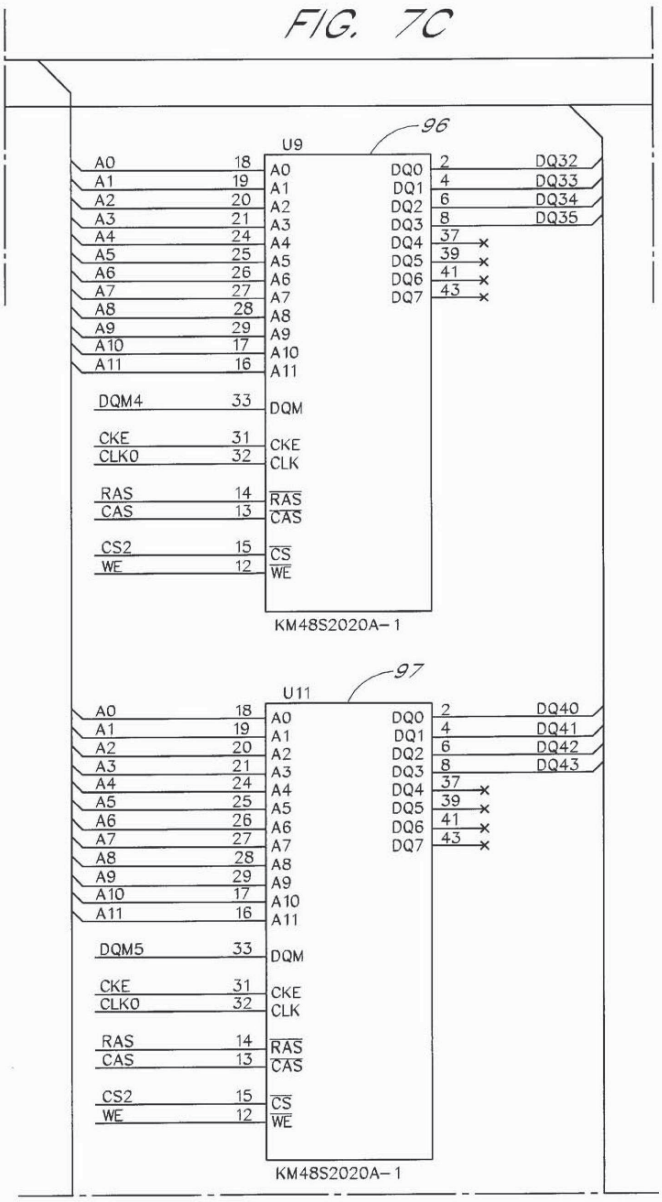

96
U9
A0 18
A1 19
A2 20
A3 21
A4 24
A5 25
A6 26
A7 27
A8 28
A9 29
A10 17
A11 16
DQM4 33
CKE 31
CLK0 32
RAS 14
CAS 13
CS2 15
WE 12
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
DQM
CKE
CLK
RAS
CAS
CS
WE
DQ0 2
DQ1 4
DQ2 6
DQ3 8
DQ4 37
DQ5 39
DQ6 41
DQ7 43
DQ32
DQ33
DQ34
DQ35
KM48S2020A-1
97
U11
A0 18
A1 19
A2 20
A3 21
A4 24
A5 25
A6 26
A7 27
A8 28
A9 29
A10 17
A11 16
DQM5 33
CKE 31
CLK0 32
RAS 14
CAS 13
CS2 15
WE 12
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
DQM
CKE
CLK
RAS
CAS
CS
WE
DQ0 2
DQ1 4
DQ2 6
DQ3 8
DQ4 37
DQ5 39
DQ6 41
DQ7 43
DQ40
DQ41
DQ42
DQ43
KM48S2020A-1

FIG. 7D

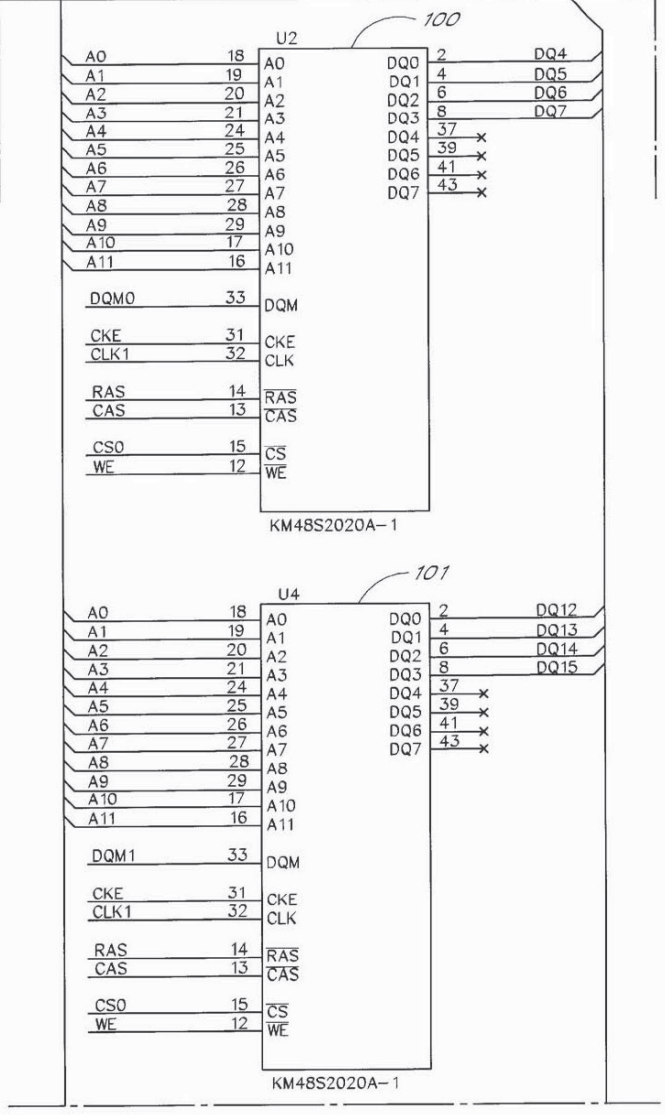
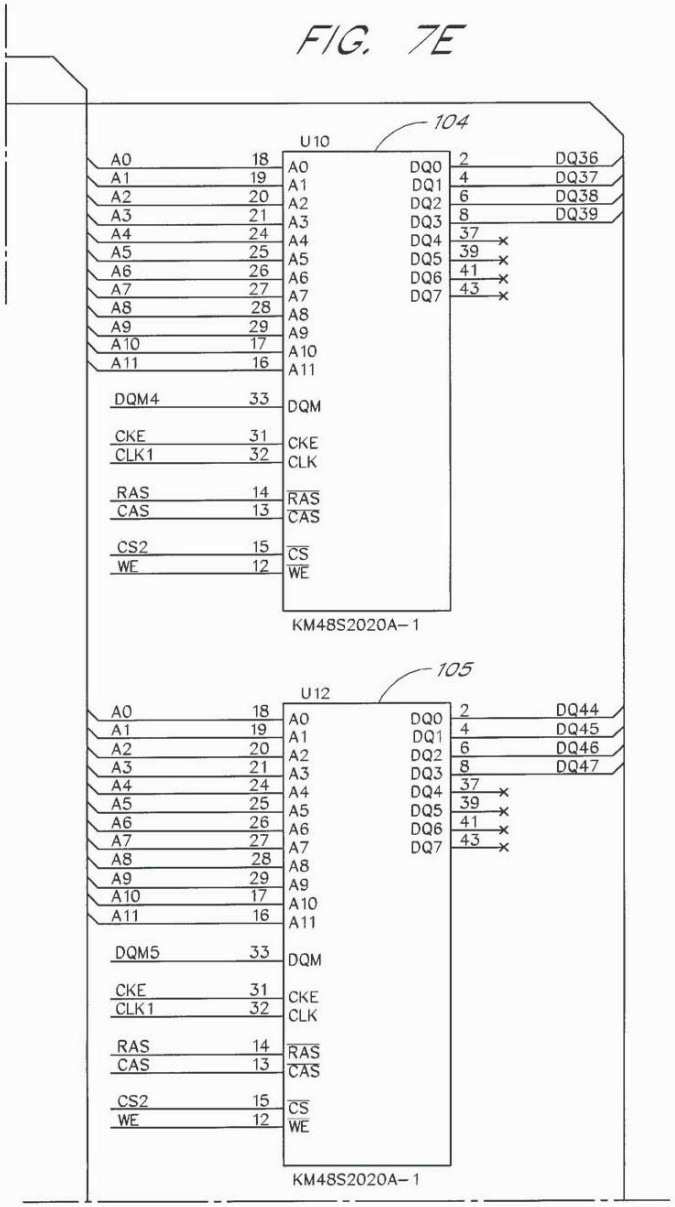

100
U2
A0 18
A1 19
A2 20
A3 21
A4 24
A5 25
A6 26
A7 27
A8 28
A9 29
A10 17
A11 16
DQM0 33
CKE 31
CLK1 32
RAS 14
CAS 13
CS0 15
WE 12
DQ0 2
DQ1 4
DQ2 6
DQ3 8
DQ4 37
DQ5 39
DQ6 41
DQ7 43
DQ4
DQ5
DQ6
DQ7
KM48S2020A-1
101
U4
A0 18
A1 19
A2 20
A3 21
A4 24
A5 25
A6 26
A7 27
A8 28
A9 29
A10 17
A11 16
DQM1 33
CKE 31
CLK1 32
RAS 14
CAS 13
CS0 15
WE 12
DQ0 2
DQ1 4
DQ2 6
DQ3 8
DQ4 37
DQ5 39
DQ6 41
DQ7 43
DQ12
DQ13
DQ14
DQ15
KM48S2020A-1

FIG. 7E


104
U10
A0 18
A1 19
A2 20
A3 21
A4 24
A5 25
A6 26
A7 27
A8 28
A9 29
A10 17
A11 16
DQM4 33
CKE 31
CLK1 32
RAS 14
CAS 13
CS2 15
WE 12
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
DQM
CKE
CLK
RAS
CAS
CS
WE
DQ0 2 DQ36
DQ1 4 DQ37
DQ2 6 DQ38
DQ3 8 DQ39
DQ4 37
DQ5 39
DQ6 41
DQ7 43
KM48S2020A-1
105
U12
A0 18
A1 19
A2 20
A3 21
A4 24
A5 25
A6 26
A7 27
A8 28
A9 29
A10 17
A11 16
DQM5 33
CKE 31
CLK1 32
RAS 14
CAS 13
CS2 15
WE 12
DQ0 2 DQ44
DQ1 4 DQ45
DQ2 6 DQ46
DQ3 8 DQ47
DQ4 37
DQ5 39
DQ6 41
DQ7 43
KM48S2020A-1

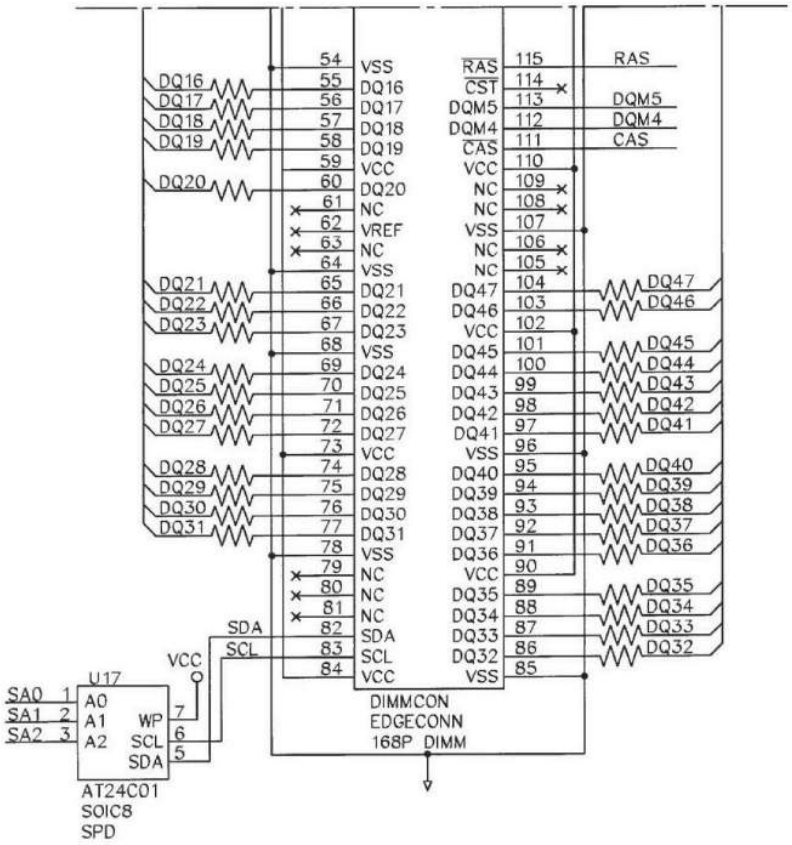

54 VSS
55 DQ16
56 DQ17
57 DQ18
58 DQ19
59 VCC
60 DQ20
61 NC
62 VREF
63 NC
64 VSS
65 DQ21
66 DQ22
67 DQ23
68 VSS
69 DQ24
70 DQ25
71 DQ26
72 DQ27
73 VCC
74 DQ28
75 DQ29
76 DQ30
77 DQ31
78 VSS
79 NC
80 NC
81 NC
82 SDA
83 SCL
84 VCC
115 RAS
114 CST
113 DQM5
112 DQM4
111 CAS
110 VCC
109 NC
108 NC
107 VSS
106 NC
105 NC
104 DQ47
103 DQ46
102 VCC
101 DQ45
100 DQ44
99 DQ43
98 DQ42
97 DQ41
96 VSS
95 DQ40
94 DQ39
93 DQ38
92 DQ37
91 DQ36
90 VCC
89 DQ35
88 DQ34
87 DQ33
86 DQ32
85 VSS
DIMMCON
EDGECONN
168P DIMM
SDA
SCL
VCC
U17
SA0 1
SA1 2
SA2 3
A0
A1
A2
WP 7
SCL 6
SDA 5
AT24C01
SOIC8
SPD

FIG. 7F

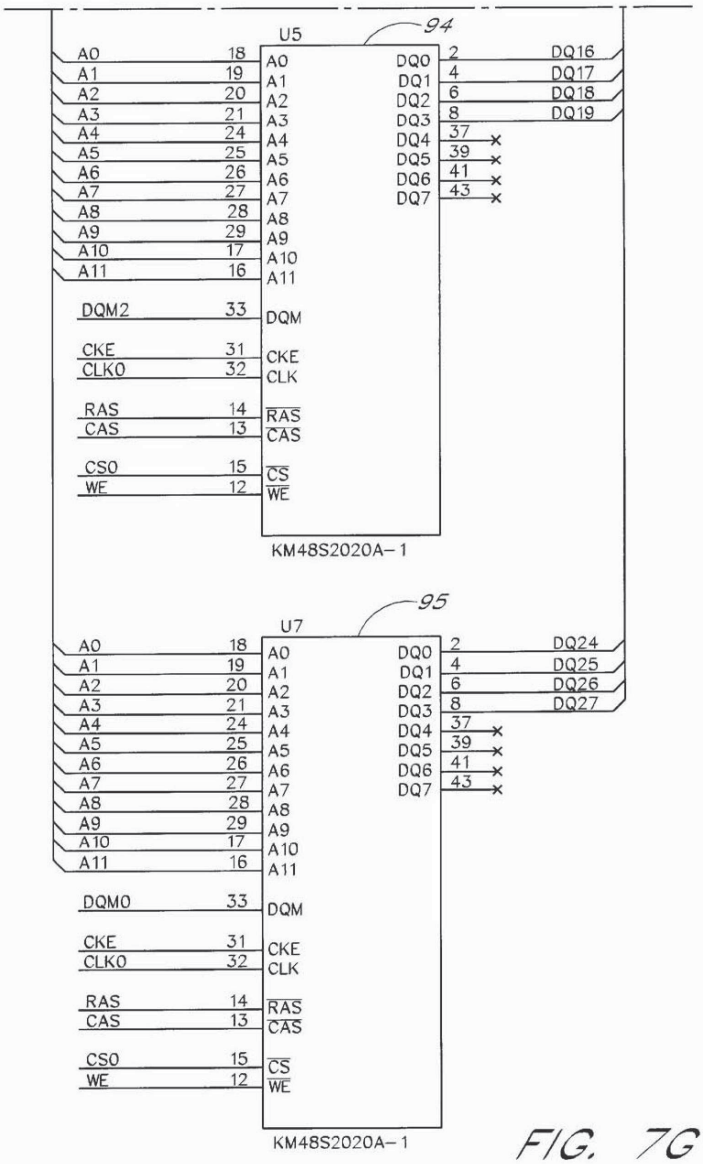

U5
94
A0 18
A1 19
A2 20
A3 21
A4 24
A5 25
A6 26
A7 27
A8 28
A9 29
A10 17
A11 16
DQM2 33
CKE 31
CLK0 32
RAS 14
CAS 13
CS0 15
WE 12
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
DQM
CKE
CLK
RAS
CAS
CS
WE
DQ0 2
DQ1 4
DQ2 6
DQ3 8
DQ4 37
DQ5 39
DQ6 41
DQ7 43
DQ16
DQ17
DQ18
DQ19
KM48S2020A-1
U7
95
A0 18
A1 19
A2 20
A3 21
A4 24
A5 25
A6 26
A7 27
A8 28
A9 29
A10 17
A11 16
DQM0 33
CKE 31
CLK0 32
RAS 14
CAS 13
CS0 15
WE 12
DQ0 2
DQ1 4
DQ2 6
DQ3 8
DQ4 37
DQ5 39
DQ6 41
DQ7 43
DQ24
DQ25
DQ26
DQ27
KM48S2020A-1

FIG. 7G

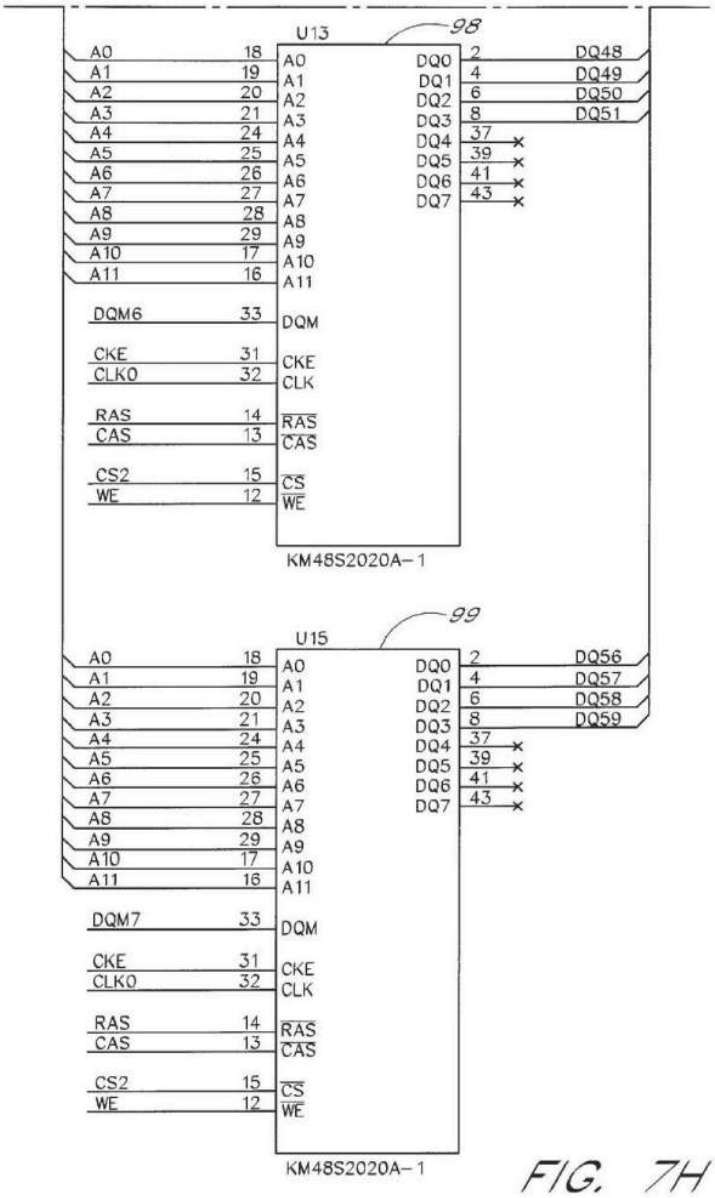

98
U13
A0 18
A1 19
A2 20
A3 21
A4 24
A5 25
A6 26
A7 27
A8 28
A9 29
A10 17
A11 16
DQM6 33
CKE 31
CLK0 32
RAS 14
CAS 13
CS2 15
WE 12
DQ0 2
DQ1 4
DQ2 6
DQ3 8
DQ4 37
DQ5 39
DQ6 41
DQ7 43
DQ48
DQ49
DQ50
DQ51
KM48S2020A-1
99
U15
DQM7 33
DQ56
DQ57
DQ58
DQ59
KM48S2020A-1

FIG. 7H

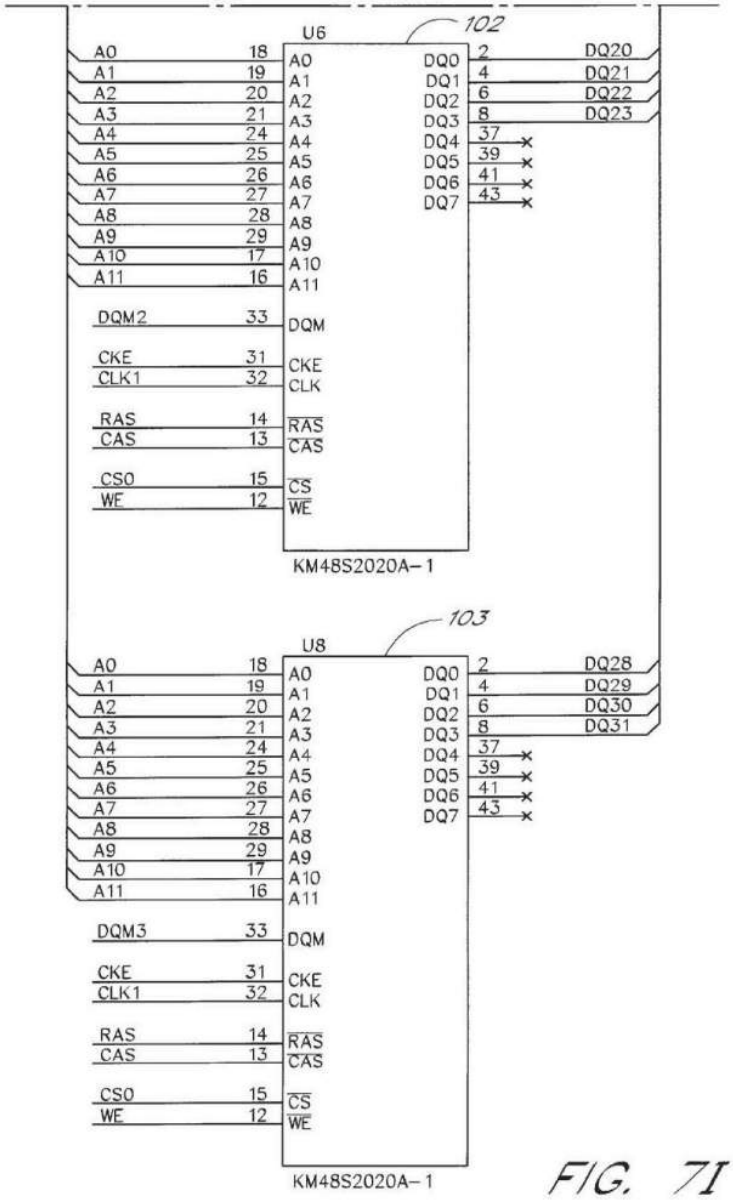

U6
102
A0 18
A1 19
A2 20
A3 21
A4 24
A5 25
A6 26
A7 27
A8 28
A9 29
A10 17
A11 16
DQM2 33
CKE 31
CLK1 32
RAS 14
CAS 13
CS0 15
WE 12
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
DQM
CKE
CLK
RAS
CAS
CS
WE
DQ0 2
DQ1 4
DQ2 6
DQ3 8
DQ4 37
DQ5 39
DQ6 41
DQ7 43
DQ20
DQ21
DQ22
DQ23
KM48S2020A-1
U8
103
A0 18
A1 19
A2 20
A3 21
A4 24
A5 25
A6 26
A7 27
A8 28
A9 29
A10 17
A11 16
DQM3 33
CKE 31
CLK1 32
RAS 14
CAS 13
CS0 15
WE 12
DQ0 2
DQ1 4
DQ2 6
DQ3 8
DQ4 37
DQ5 39
DQ6 41
DQ7 43
DQ28
DQ29
DQ30
DQ31
KM48S2020A-1

FIG. 7I

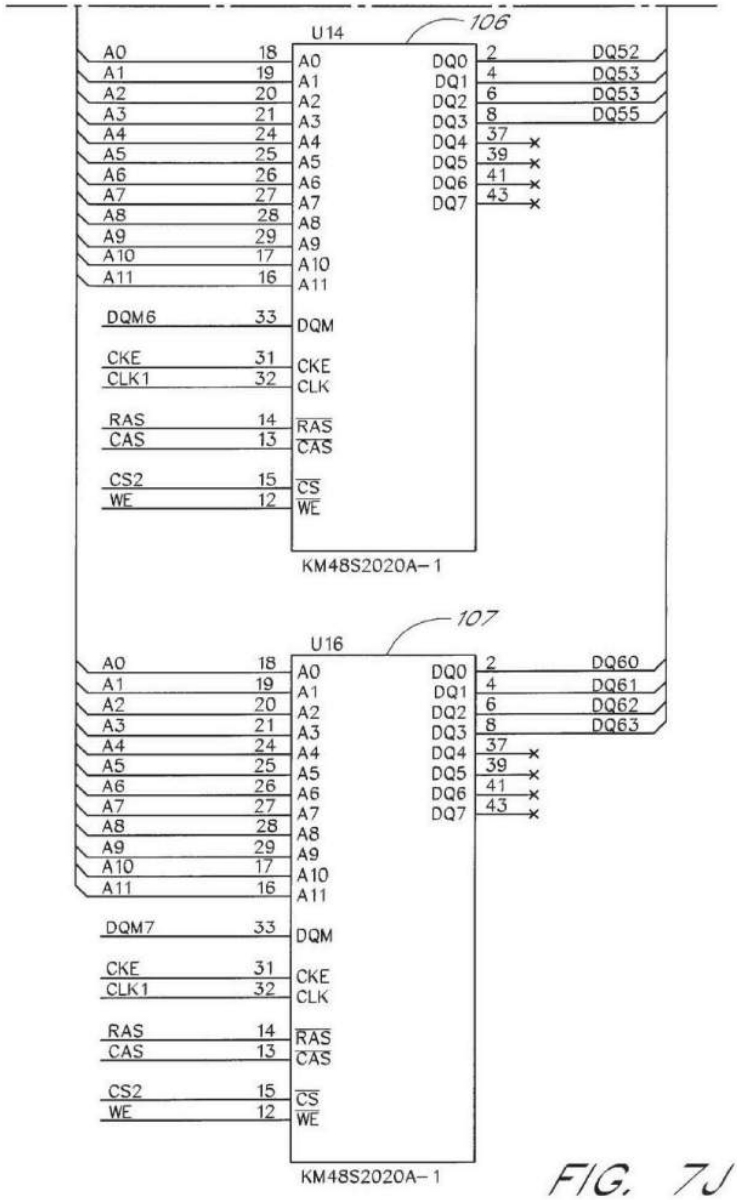

106
U14
A0 18
A1 19
A2 20
A3 21
A4 24
A5 25
A6 26
A7 27
A8 28
A9 29
A10 17
A11 16
DQM6 33
CKE 31
CLK1 32
RAS 14
CAS 13
CS2 15
WE 12
DQ0 2
DQ1 4
DQ2 6
DQ3 8
DQ4 37
DQ5 39
DQ6 41
DQ7 43
DQ52
DQ53
DQ53
DQ55
KM48S2020A-1
107
U16
DQM7 33
DQ60
DQ61
DQ62
DQ63
KM48S2020A-1

FIG. 7J

METHOD FOR RECOVERY OF USEFUL AREAS OF PARTIALLY DEFECTIVE SYNCHRONOUS MEMORY COMPONENTS

This application includes subject matter related to application Ser. No. 09/035,629, filed concurrently herewith on Mar. 5, 1998.

FIELD OF THE INVENTION

The present invention relates generally to the use partially defective synchronous memory chips. More particularly, the present invention relates to the configuration of defective SDRAM components to create a nondefective memory module or array.

BACKGROUND AND SUMMARY OF THE DISCLOSURE

As is well known in the art, during the production of monolithic memory devices from silicon wafers, some of the memory storage cells can become defective and unreliable. The defective cells can be the result of a number of causes, such as impurities introduced in the process of manufacturing the monolithic memory device from the silicon wafer, or localized imperfections in the silicon substrate itself.

Often, while some memory cells are defective, many other cells on the same memory chip are not defective, and will work reliably and accurately. In addition, it is often the case that the defective cells are localized and confined to particular outputs from the memory device. The remaining, nondefective outputs can be relied upon to provide a consistent and accurate representation of the information in the storage cell.

Techniques have been developed for salvaging the nondefective portions of defective asynchronous memory technologies (e.g., DRAM). Asynchronous memory technologies are relatively slow devices that operate in response to control signals generated by a memory controller, rather than in response to the system clock. The control signals allow the asynchronous memory device to operate at a speed that is much slower than the system clock, and that ensures reliable read and write memory operations.

Synchronous memory devices such as SDRAM, on the other hand, are much faster devices that operate on the system clock. SDRAM is an improvement over prior memory technologies principally because SDRAM is capable of synchronizing itself with the microprocessor's clock. This synchronization can eliminate the time delays and wait states often necessary with prior memory technologies (e.g., DRAM), and it also allows for fast consecutive read and write capability.

However, no attempts have been made to salvage nondefective portions of synchronous memory. Some people skilled in the art may believe that the use of techniques for salvaging defective memory devices would not work with higher-speed synchronous memory devices such as SDRAM because they operate at much higher speeds than previous memory devices, such as asynchronous DRAM. For SDRAM, it may be believed that the rate at which the clock input cycles and the load on the device driving the inputs (e.g., the clock and the address) to the SDRAM devices would make reliable input transitions unattainable.

The present invention addresses the problem of salvaging partially defective synchronous memory devices. In one embodiment of the present invention, multiple partially defective SDRAM components are configured to provide a reliable and nondefective memory module. Such an embodiment takes advantage of the manner in which defective cells are localized on each memory chip, and combines multiple memory chips to provide a memory bus that is of the desired width and granularity. In addition, it is possible with such an embodiment to provide a computer system in which the main memory is synchronized with the system clock, and is constructed, at least in part, from partially defective memory chips.

The nature of the present invention as well as other embodiments of the present invention may be more clearly understood by reference to the following detailed description of the invention, to the appended claims, and to the several drawings herein.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a block diagram of a prior art computer system using a wait state control device with DRAM memory chips.

FIG. **2** is a block diagram of a computer system employing SDRAM memory chips.

FIG. **3** is a block diagram of a partially defective SDRAM component.

FIG. **4** is a memory map showing the localized nature of defective memory cells in one embodiment of the present invention.

FIG. **4**A is a memory map showing defective memory cells corresponding to a defect that differs from that of FIG. **4**.

FIG. **5** is an embodiment of the present invention using six partially defective SDRAM components to make a 64-bit memory module.

FIGS. **6** and **7** are embodiments of the present invention using sixteen defective SDRAM components where four bits in each of the eight bit memory cells are defective.

DETAILED DESCRIPTION

FIG. **1** is a block diagram of a prior art computer system comprising a microprocessor **16**, a memory controller **14**, and main memory **12**. In the system shown, main memory **12** is made up of dynamic random access memory (DRAM). Also shown in FIG. **1** is a wait state control device **18** and a system clock **20**. As is well known in the art, due to differences in speed between the processor **16** and the DRAM **12**, it is often necessary to insert "wait states" when the processor carries out a memory operation involving the DRAM **12**. Typically, the DRAM **12** is slower than the processor **16**, so one or more additional states are added to the microprocessor's memory access cycle to ensure that the memory **12** is given a sufficient amount of time to carry out the memory (read/write) operation.

In addition, the clock **20** in the system of FIG. **1** is not a direct input to the DRAM **12**. Instead, as is well known in the art, control signals are derived from the clock, and the DRAM **12** is operated through the use of these control signals. The signals presented to the DRAM device **12** change relatively slowly compared to the rate at which the clock changes.

FIG. **2** shows a block diagram of a computer system in one embodiment of the present invention, where the computer system comprises a clock **20**, a processor **16**, a memory controller **22**, and main memory **24**. Often, the clock **20** operates at 66 MHz or 100 MHz, but it may operate at any speed. Unlike FIG. **1**, the main memory in FIG. **2** is made up of one or more SDRAM chips, and the SDRAM memory is synchronized with the clock **20**, which means

that it operates synchronously with the clock **20**. This synchronization can eliminate some or all of the wait states normally necessary with DRAM devices, and it also allows for fast consecutive read and write capability. Unlike FIG. **1**, in FIG. **2** the clock **20** is provided as an input to the memory **24**. Thus, in FIG. **2**, at least some of the inputs to the memory **24** may change at a rate approaching or equal to the rate of the clock **20**.

FIG. **3** is a block diagram of a partially defective SDRAM component **26** having twelve address inputs A0 to A11, and eight data outputs DQ**0** to DQ**7**. The component **26** is a 1024 K×83×2 SDRAM. The "8" in this description represents the eight output lines, meaning the data width is 8 bits wide (the granularity may also be eight bits). The "1024K" is the addressable space in each bank of memory within the SDRAM, and the "2" indicates that there are two such 1024K banks of memory within this component. Generally, components such as that described in FIG. **3** are mounted on SIMMs (Single In-line Memory Modules) or DIMMs (Dual Inline Memory Modules), but any other appropriate packaging technology could be used to practice one or more of the inventions described herein.

In operation, the SDRAM component **26** is addressed by using a multiplexed row and column address, as is well known in the art. The twelve address inputs on the memory component are first presented with an eleven bit row address on A0 to A10. After the row address has been presented to the SDRAM **26**, an nine bit column address is presented to the SDRAM **26** on address inputs A0 to A8. Thus, the full address is twenty bits wide, thereby making a 1024K address space based on the row and column addresses. The SDRAM **26** has two of these 1024K banks of memory addressable with the row and column addresses. The particular 1024K bank within the SDRAM component is selected by an additional row address bit, which is presented to the SDRAM with the row address on address input A11.

The SDRAM component shown in FIG. **3** is partially defective in the sense that some of the DQ outputs do not consistently present valid or accurate data. In the particular SDRAM shown in FIG. **3**, data outputs DQ**2** to DQ**5** are defective, whereas data outputs DQ**0**, DQ**1**, DQ**6**, and DQ**7** are not defective. Thus, these latter DQ outputs can be relied upon for accurate and consistent data, whereas the data outputs DQ**2** to DQ**5** cannot.

FIG. **4** is a memory map of the SDRAM component of FIG. **3**, showing the portions of memory that are defective. As can be seen from FIG. **4**, in the particular SDRAM component of FIG. **3**, the defects are such that every addressable eight bit memory location has both reliable and unreliable (or unused) DQ outputs, and they are consistently arranged within each addressable octet.

This result may follow from the nature of the defect, where certain DQ outputs always present valid data, whereas other DQ outputs may not be reliable, and may occasionally present bad data. Defects in the silicon or impurities introduced in the manufacturing process will often result in defects like those illustrated in FIG. **4**.

FIG. **5** is a schematic diagram of a memory module in one embodiment of the present invention where multiple partially defective SDRAM components are combined to create a nondefective 512K×64×2 memory module. The edge connector **52** is connected to each of the partially defective 512k×16×2 SDRAM components **54** to **59**. Each of the SDRAM components are defective in a manner similar to that shown in FIG. **4**. The SDRAM components **54**, **55**, **57**, and **58** each have four defective or unused DQ outputs (i.e., DQ**0** to DQ**3**), and the remaining twelve DQ outputs are not defective. The SDRAM components **56** and **59** have eight unreliable or unused DQ outputs (DQ**0** to DQ**7**), and eight reliable and nondefective DQ outputs. By using the twelve nondefective DQ outputs from SDRAM components **54**, **55**, **57**, and **58** and by using the eight nondefective DQ outputs from SDRAM components **56** and **59**, a 512K×64×2 memory module can be constructed from the six partially defective SDRAM components as shown in FIG. **5**.

In a manner similar to that described in connection with FIG. **3**, the SDRAM components in FIG. **5** are addressed by first presenting an eleven bit row address followed by an eight bit column address. Thus, the memory address is nineteen bits wide. An additional bit is presented at address input A11 with the eleven bit row address to select one of the two 512K memory banks within each SDRAM component.

FIG. **6** is a schematic of another embodiment of the present invention, where sixteen partially defective 1024K×8×2 SDRAM components **72** to **87** are used to create a 1024K×64×2 memory module. Each of the partially defective SDRAM components in FIG. **6** has four unreliable or unused outputs (DQ**0** to DQ**3**) and four nondefective outputs (DQ**4** to DQ**7**). Using the four nondefective outputs from each of the sixteen SDRAM components provides a 64 bit quad word data path.

The SDRAM components of FIG. **6** are addressed by first presenting an eleven bit row address followed by a nine bit column address. Thus, the memory address is twenty bits wide. An additional bit is presented at address input A11 with the eleven-bit row address to select one of the two 1024K memory banks within each SDRAM component.

It should be understood that the present invention does not necessarily require any particular arrangement for the defective DQ outputs. For example, in FIG. **6**, the defective DQ outputs need not be the same for each component **72**–**87**, and the defective outputs may not be consecutive or symmetric. As can be seen from FIG. **6**, the components **72** and **80** make up the low order byte of data in the 64-bit quad word. It is possible that component **72** may have only three defective outputs, thereby allowing five bits in the low order byte to be taken from component **72**, and only three bits from component **80**. Any other combination would also be appropriate. Similarly, the defective outputs in component **80** could come in any combination, and need not be DQ**0**, DQ**1**, DQ**2**, DQ**3**. Rather, the defective outputs could be DQ**1**, DQ**4**, DQ**6**, and DQ**7**, or any other combination.

FIG. **7** is a schematic of another embodiment of the present invention, where sixteen partially defective 1M×8×2 SDRAM components **92** to **107** are used to create a 1M×64×2 memory module. Each of the partially defective SDRAM components in FIG. **7** have four unreliable or unused outputs and four nondefective outputs. This embodiment differs from that in FIG. **6** in that the outputs DQ**0** to DQ**3** are nondefective, whereas outputs DQ**4** to DQ**7** are defective. The four nondefective outputs from each of the sixteen SDRAM components provides a 64 bit quad word data path.

Although the SDRAM components in FIG. **7** are 1M×8×2 components having two banks of 1M×8 bit memory, it is possible that they could be 2M×8 bit components having only a single bank of memory. In such an embodiment, the components are addressed by first presenting a twelve bit row address to the address inputs A0 to A11, followed by a nine bit column address, which is presented at address inputs A0 to A8. Thus, the full address is 21 bits wide, thereby providing a 2M address space, and the SDRAM components have (or are treated as having) only a single bank of memory.

It is also possible that the memory components have more than two banks of memory. In some more modem devices, two bank select lines (e.g., BA**0** and BA**1**) are used to select one of four banks of memory in a particular component or module. (Often, but not necessarily, such select signals are presented to the component with the row address.) As one skilled in the art would recognize, the present invention is applicable to memory components of this nature, and is applicable generally to memory components having any number of banks of memory.

Although the present invention has been shown and described with respect to preferred embodiments, various changes and modifications that are obvious to a person skilled in the art to which the invention pertains, even if not shown or specifically described herein, are deemed to lie within the spirit and scope of the invention and the following claims.

What is claimed is:

1. A method of accessing a memory module comprising the acts of:

presenting a row address to the address inputs of each of a plurality of partially defective SDRAM components that have at least one unreliable data output, and that also have a plurality of valid data outputs, wherein the valid data outputs are data outputs that provide reliable and accurate data; and

presenting a column address to the address inputs of each SDRAM component;

aggregating the valid data outputs of each of the SDRAM components to provide a data path; and

communicating the data from the valid data outputs to a microprocessor.

2. The method of claim **1**, wherein the act of presenting a row address includes the act of presenting a row address to the address inputs of partially defective SDRAM components, where for each of these SDRAM components, the plurality of valid data outputs are the same for each addressable memory location within that component so that the same portion of each addressable memory location within any given SDRAM component consistently provides valid and accurate data.

3. The method of claim **2**, wherein the act of presenting a row address to the address inputs of each of a plurality of partially defective SDRAM components includes the act of presenting a row address to SDRAM components mounted on SIMMs.

4. The method of claim **3**, wherein the act of presenting a row address to the address inputs of each of a plurality of partially defective SDRAM components includes the act of presenting a row address to SDRAM components mounted on DIMMs.

5. A method of accessing memory cells in a memory module having a plurality of SDRAM components, each of the SDRAM components having a plurality of address inputs, and wherein each of the SDRAM components further comprises a plurality of banks of memory that are addressable by the address inputs, the method comprising the acts of:

presenting a row address to the address inputs of each SDRAM component;

presenting a column address to the address inputs of each SDRAM component;

selecting one of the plurality of banks within each SDRAM component by presenting at least one selection bit at the address inputs when the row address is presented to the address inputs, wherein each of the SDRAM components is partially defective such that each SDRAM components has at least one unreliable data output, and also a plurality of valid data outputs that provide reliable and accurate data;

aggregating the valid data outputs of each of the SDRAM components to provide a data path; and

communicating the data from the valid data outputs from each of the SDRAM components to a microprocessor.

6. The method of claim **5**, wherein the act of presenting a row address includes the act of presenting a row address to the address inputs of partially defective SDRAM components, where for each of these SDRAM components, the plurality of valid data outputs are the same for each addressable memory location within that component so that the same portion of each addressable memory location within any given SDRAM component consistently provides valid and accurate data.

7. The method of claim **6**, wherein the act of presenting a row address to the address inputs of each of a plurality of partially defective SDRAM components includes the act of presenting a row address to SDRAM components mounted on SIMMs.

8. The method of claim **7**, wherein the act of presenting a row address to the address inputs of each of a plurality of partially defective SDRAM components includes the act of presenting a row address to SDRAM components mounted on DIMMs.

9. A method of enabling data access between a memory module having data outputs and a microprocessor comprising the acts of:

determining which SDRAM data outputs of a group of SDRAM components are defective;

assembling a set of SDRAM components from the group of SDRAM components, wherein at least one of the SDRAM components has defective SDRAM data outputs, such that each memory module data output is connected to an operative SDRAM data output; and

applying a clock signal that is processed to synchronously apply operating signals to the memory module and the microprocessor to effect data access between the memory module and the microprocessor.

10. The method of claim **9** firther comprising sorting SDRAM components based on which of the data outputs of the respective SDRAM components are defective.

11. The method of claim **10** further comprising providing sorted SDRAM components with predetermined numbers and arrangements of defective SDRAM data outputs for assemble on predetermined, complementary memory modules.

12. The method of claim **9** wherein determining which data outputs are defective includes testing SDRAM components prior to assembling the SDRAM components on a memory module.

* * * * *

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NUMBER	FILING DATE	CLASS	GROUP ART UNIT	...TORNEY DOCKET NO.
9/035,739	03/05/98	711	2751	6325

HARD WEBER, BOISE, ID; COREY LARSEN, MARSING, ID.

CONTINUING DOMESTIC DATA********
VERIFIED none
MR

371 (NAT'L STAGE) DATA********
VERIFIED none
MK

FOREIGN APPLICATIONS********
VERIFIED none
MR

FOREIGN FILING LICENSE GRANTED 05/19/98

Foreign Priority claimed 35 USC 119 (a-d) conditions met	STATE OR COUNTRY	SHEETS DRAWING	TOTAL CLAIMS	INDEPENDENT CLAIMS
☐yes ☒no ☐yes ☒no ☐Met after Allowance Verified and Acknowledged MR (Examiner's Initials) (Initials)	ID	6	8	2

ADDRESS
DORSEY & WHITNEY
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MINNEAPOLIS MN 55402

TITLE
METHOD FOR RECOVERY OF USEFUL AREAS OF PARTIALLY DEFECTIVE SYNCHRONOUS MEMORY COMPONENTS

FILING FEE RECEIVED	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT NO. _____ for the following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit
$920		

PATENT APPLICATION SERIAL NO. _____

U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE
FEE RECORD SHEET

03/12/1998 MGORDON 00000039 09035739
01 FC:101 790.00 DP

PTO-1556
(5/87)

A

03/05/98 JC135 U.S. PTO

Form PTO-1082
ASSISTANT COMMISSIONER FOR PATENTS
Box Application
Washington D.C. 20231

Case Docket No. 6325

Dear Sir:

Transmitted herewith for filing is the patent application of:
Inventor: Richard Weber and Corey Larsen
For: Method for Recovery of Useful Areas of Partially Defective Synchronous Memory Components

Enclosed are: 8 sheets of Specification, 2 sheets of Claims, 1 sheet of Abstract
6 sheets of informal drawings

- ☐ An assignment of the invention to _____.
- ☐ A certified copy of application.
- ☐ A combined Declaration and Power of Attorney.
- ☐ A Verified Statement to establish small entity status under 37 CRR 1.9 and 37 CFR 1.27.

The filing fee has been calculated as shown:

				☐ Small Entity		☒ Other than Small Entity	
Basic Filing Fee					$395.00		$790.00
Additional Fees:				(rate)		(rate)	
Total Claims	1	No. Extra	0	$11.00		$22.00	$790.00
Indep. Claims	1	No. Extra	0	$41.00		$82.00	
Multiple dependent claim presented.				$130.00		$260.00	
TOTAL							$790.00

☐ Please Charge my Deposit Account No. 04-1420 in the amount of _____. A duplicate copy of this sheet is enclosed.

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- ☐ The issue fee set in 37 CFR 1.18 at or before the mailing of the Notice of Allowance, pursuant to 37 CFR 1.311(b).
- ☐ Any filing fees under 37 CFR 1.16 for presentation of extra claims.

Date: 3/5/98

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Form PTO-1082
ASSISTANT COMMISSIONER FOR PATENTS
Box Application
Washington D.C. 20231

Case Docket No. 6325

JC557 U.S. PTO
09/035739
03/05/98

Dear Sir:

Transmitted herewith for filing is the patent application of:
Inventor: Richard Weber and Corey Larsen
For: Method for Recovery of Useful Areas of Partially Defective Synchronous Memory Components

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Total Claims	8	No. Extra 0	$11.00		$22.00	$790.00
Indep. Claims	2	No. Extra 0	$41.00		$82.00	
Multiple dependent claim presented.			$130.00		$260.00	
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  - ☐ Any filing fees under 37 CFR 1.16 for presentation of extra claims.

Date: 3/5/98

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Express Mail mailing label number EH359935298US

Date of Deposit 5 March 1998

I hereby certify that this paper or fee is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10 on the date indicated above and is addressed to the Assistant Commissioner for Patents, Washington D.C. 20231

Elvina Smith
Name

Elvina Smith
Signature

SPECIFICATION

TO WHOM IT MAY CONCERN:

BE IT KNOWN THAT WE, Richard Weber, a Citizen of the United States and a resident of Boise, Ada County, Idaho, and Corey Larsen, a Citizen of the United States and a resident of Marsing, Owyhee County, Idaho, have invented certain new and useful improvements in

METHOD FOR RECOVERY OF USEFUL AREAS OF PARTIALLY DEFECTIVE SYNCHRONOUS MEMORY COMPONENTS

of which the following is a specification.

TITLE: METHOD FOR RECOVERY OF USEFUL AREAS OF PARTIALLY DEFECTIVE SYNCHRONOUS MEMORY COMPONENTS

FIELD OF THE INVENTION

The present invention relates generally to the use partially defective synchronous memory chips. More particularly, the present invention relates to the configuration of defective SDRAM components to create a nondefective memory module or array.

BACKGROUND AND SUMMARY OF THE DISCLOSURE

As is well known in the art, during the production of monolithic memory devices from silicon wafers, some of the memory storage cells can become defective and unreliable. The defective cells can be the result of a number of causes, such as impurities introduced in the process of manufacturing the monolithic memory device from the silicon wafer, or localized imperfections in the silicon substrate itself.

Often, while some memory cells are defective, many other cells on the same memory chip are not defective, and will work reliably and accurately. In addition, it is often the case that the defective cells are localized and confined to particular outputs from the memory device. The remaining, nondefective outputs can be relied upon to provide a consistent and accurate representation of the information in the storage cell.

Techniques have been developed for salvaging the non-defective portions of defective *asynchronous* memory technologies (e.g., DRAM). Asynchronous memory technologies are relatively slow devices that operate in response to control signals generated by a memory controller, rather than in response to the system clock. The control signals allow the asynchronous memory device to operate at a speed that is much slower than the system clock, and that ensures reliable read and write memory operations.

Synchronous memory devices such as SDRAM, on the other hand, are much faster devices that operate on the system clock. SDRAM is an improvement over prior memory technologies principally because SDRAM is capable of synchronizing itself with the microprocessor's clock. This synchronization can eliminate the time delays and wait states often necessary with prior memory

technologies (e.g., DRAM), and it also allows for fast consecutive read and write capability.

However, no attempts have been made to salvage non-defective portions of synchronous memory. Some people skilled in the art may believe that the use of techniques for salvaging defective memory devices would not work with higher-speed synchronous memory devices such as SDRAM because they operate at much higher speeds than previous memory devices, such as asynchronous DRAM. For SDRAM, it may be believed that the rate at which the clock input cycles and the load on the device driving the inputs (e.g., the clock and the address) to the SDRAM devices would make reliable input transitions unattainable.

The present invention addresses the problem of salvaging partially defective synchronous memory devices. In one embodiment of the present invention, multiple partially defective SDRAM components are configured to provide a reliable and nondefective memory module. Such an embodiment takes advantage of the manner in which defective cells are localized on each memory chip, and combines multiple memory chips to provide a memory bus that is of the desired width and granularity. In addition, it is possible with such an embodiment to provide a computer system in which the main memory is synchronized with the system clock, and is constructed, at least in part, from partially defective memory chips.

The nature of the present invention as well as other embodiments of the present invention may be more clearly understood by reference to the following detailed description of the invention, to the appended claims, and to the several drawings herein.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a block diagram of a prior art computer system using a wait state control device with DRAM memory chips.

Figure 2 is a block diagram of a computer system employing SDRAM memory chips.

Figure 3 is a block diagram of a partially defective SDRAM component.

Figure 4 is a memory map showing the localized nature of defective memory cells in one embodiment of the present invention.

~~Figure 4A is a memory map showing defective memory cells corresponding to a defect that differs from that of Figure 4.~~

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Figure 5 is an embodiment of the present invention using six partially defective SDRAM components to make a 64-bit memory module.

Figures 6 and 7 are embodiments of the present invention using sixteen defective SDRAM components where four bits in each of the eight bit memory cells are defective.

DETAILED DESCRIPTION

Figure 1 is a block diagram of a prior art computer system comprising a microprocessor 16, a memory controller 14, and main memory 12. In the system shown, main memory 12 is made up of dynamic random access memory (DRAM). Also shown in Figure 1 is a wait state control device 18 and a system clock 20. As is well known in the art, due to differences in speed between the processor 16 and the DRAM 12, it is often necessary to insert "wait states" when the processor carries out a memory operation involving the DRAM 12. Typically, the DRAM 12 is slower than the processor 16, so one or more additional states are added to the microprocessor's memory access cycle to ensure that the memory 12 is given a sufficient amount of time to carry out the memory (read/write) operation.

In addition, the clock 20 in the system of Figure 1 is not a direct input to the DRAM 12. Instead, as is well known in the art, control signals are derived from the clock, and the DRAM 12 is operated through the use of these control signals. The signals presented to the DRAM device 12 change relatively slowly compared to the rate at which the clock changes.

Figure 2 shows a block diagram of a computer system in one embodiment of the present invention, where the computer system comprises a clock 20, a processor 16, a memory controller 22, and main memory 24. Often, the clock 20 operates at 66 MHz or 100 MHz, but it may operate at any speed. Unlike Figure 1, the main memory in Figure 2 is made up of one or more SDRAM chips, and the SDRAM memory is synchronized with the clock 20, which means that it operates synchronously with the clock 20. This synchronization can eliminate some or all of the wait states normally necessary with DRAM devices, and it also allows for fast consecutive read and write capability. Unlike Figure 1, in Figure 2 the clock 20 is provided as an input to the memory 24. Thus, in Figure 2, at least some of the inputs to the memory 24 may change at a rate approaching or equal to the rate of the clock 20.

Figure 3 is a block diagram of a partially defective SDRAM component 26 having twelve address inputs A0 to A11, and eight data outputs DQ0 to DQ7. The component 26 is a 1024K x 8 x 2 SDRAM. The "8" in this description represents the eight output lines, meaning the data width is 8 bits wide (the granularity may also be eight bits). The "1024K" is the addressable space in each bank of memory within the SDRAM, and the "2" indicates that there are two such 1024K banks of memory within this component. Generally, components such as that described in Figure 3 are mounted on SIMMs (Single In-line Memory Modules) or DIMMs (Dual In-line Memory Modules), but any other appropriate packaging technology could be used to practice one or more of the inventions described herein.

In operation, the SDRAM component 26 is addressed by using a multiplexed row and column address, as is well known in the art. The twelve address inputs on the memory component are first presented with an eleven bit row address on A0 to A10. After the row address has been presented to the SDRAM 26, an nine bit column address is presented to the SDRAM 26 on address inputs A0 to A8. Thus, the full address is twenty bits wide, thereby making a 1024K address space based on the row and column addresses. The SDRAM 26 has two of these 1024K banks of memory addressable with the row and column addresses. The particular 1024K bank within the SDRAM component is selected by an additional row address bit, which is presented to the SDRAM with the row address on address input A11.

The SDRAM component shown in Figure 3 is partially defective in the sense that some of the DQ outputs do not consistently present valid or accurate data. In the particular SDRAM shown in Figure 3, data outputs DQ2 to DQ5 are defective, whereas data outputs DQ0, DQ1, DQ6, and DQ7 are not defective. Thus, these latter DQ outputs can be relied upon for accurate and consistent data, whereas the data outputs DQ2 to DQ5 cannot.

Figure 4 is a memory map of the SDRAM component of Figure 3, showing the portions of memory that are defective. As can be seen from Figure 4, in the particular SDRAM component of Figure 3, the defects are such that every addressable eight bit memory location has both reliable and unreliable (or unused) DQ outputs, and they are consistently arranged within each addressable octet. This result may follow from the nature of the defect, where certain DQ outputs always present valid data, whereas other DQ outputs may not be reliable, and may occasionally present bad data. Defects

in the silicon or impurities introduced in the manufacturing process will often result in defects like those illustrated in Figure 4.

Figure 5 is a schematic diagram of a memory module in one embodiment of the present invention where multiple partially defective SDRAM components are combined to create a nondefective 512K x 64 x 2 memory module. The edge connector 52 is connected to each of the partially defective 512k x 16 x 2 SDRAM components 54 to 59. Each of the SDRAM components are defective in a manner similar to that shown in Figure 4. The SDRAM components 54, 55, 57, and 58 each have four defective or unused DQ outputs (i.e., DQ0 to DQ3), and the remaining twelve DQ outputs are not defective. The SDRAM components 56 and 59 have eight unreliable or unused DQ outputs (DQ0 to DQ7), and eight reliable and nondefective DQ outputs. By using the twelve nondefective DQ outputs from SDRAM components 54, 55, 57, and 58 and by using the eight nondefective DQ outputs from SDRAM components 56 and 59, a 512K x 64 x 2 memory module can be constructed from the six partially defective SDRAM components as shown in Figure 5.

In a manner similar to that described in connection with Figure 3, the SDRAM components in Figure 5 are addressed by first presenting an eleven bit row address followed by an eight bit column address. Thus, the memory address is nineteen bits wide. An additional bit is presented at address input A11 with the eleven bit row address to select one of the two 512K memory banks within each SDRAM component.

Figure 6 is a schematic of another embodiment of the present invention, where sixteen partially defective 1024K x 8 x 2 SDRAM components 72 to 87 are used to create a 1024K x 64 x 2 memory module. Each of the partially defective SDRAM components in Figure 6 has four unreliable or unused outputs (DQ0 to DQ3) and four nondefective outputs (DQ4 to DQ7). Using the four nondefective outputs from each of the sixteen SDRAM components provides a 64 bit quad word data path.

The SDRAM components of Figure 6 are addressed by first presenting an eleven bit row address followed by a nine bit column address. Thus, the memory address is twenty bits wide. An additional bit is presented at address input A11 with the eleven-bit row address to select one of the two 1024K memory banks within each SDRAM component.

It should be understood that the present invention does not necessarily require any particular

arrangement for the defective DQ outputs. For example, in Figure 6, the defective DQ outputs need not be the same for each component 72-87, and the defective outputs may not be consecutive or symmetric. As can be seen from Figure 6, the components 72 and 80 make up the low order byte of data in the 64-bit quad word. It is possible that component 72 may have only three defective outputs, thereby allowing five bits in the low order byte to be taken from component 72, and only three bits from component 80 . Any other combination would also be appropriate. Similarly, the defective outputs in component 80 could come in any combination, and need not be DQ0, DQ1, DQ2, DQ3. Rather, the defective outputs could be DQ1, DQ4, DQ6, and DQ7, or any other combination.

Figure 7 is a schematic of another embodiment of the present invention, where sixteen partially defective 1M x 8 x 2 SDRAM components 92 to 107 are used to create a 1M x 64 x 2 memory module. Each of the partially defective SDRAM components in Figure 7 have four unreliable or unused outputs and four nondefective outputs. This embodiment differs from that in Figure 6 in that the outputs DQ0 to DQ3 are nondefective, whereas outputs DQ4 to DQ7 are defective. The four nondefective outputs from each of the sixteen SDRAM components provides a 64 bit quad word data path.

Although the SDRAM components in Figure 7 are 1M x 8 x 2 components having two banks of 1M x 8 bit memory, it is possible that they could be 2M x 8 bit components having only a single bank of memory. In such an embodiment, the components are addressed by first presenting a twelve bit row address to the address inputs A0 to A11, followed by a nine bit column address, which is presented at address inputs A0 to A8. Thus, the full address is 21 bits wide, thereby providing a 2M address space, and the SDRAM components have (or are treated as having) only a single bank of memory.

It is also possible that the memory components have more than two banks of memory. In some more modern devices, two bank select lines (e.g., BA0 and BA1) are used to select one of four banks of memory in a particular component or module. (Often, but not necessarily, such select signals are presented to the component with the row address.) As one skilled in the art would recognize, the present invention is applicable to memory components of this nature, and is applicable generally to memory components having any number of banks of memory.

Although the present invention has been shown and described with respect to preferred embodiments, various changes and modifications that are obvious to a person skilled in the art to which the invention pertains, even if not shown or specifically described herein, are deemed to lie within the spirit and scope of the invention and the following claims.

What is claimed is:

1. A method of accessing a memory module comprising the acts of:

presenting a row address to the address inputs of each of a plurality of partially defective SDRAM components that have at least one unreliable data output, and that also have a plurality of valid data outputs, wherein the valid data outputs are data outputs that provide reliable and accurate data; and

presenting a column address to the address inputs of each SDRAM component;

aggregating the valid data outputs of each of the SDRAM components to provide a data path; and

communicating the data from the valid data outputs to the microprocessor.

2. The method of claim 1, wherein the act of presenting a row address includes the act of presenting a row address to the address inputs of partially defective SDRAM components, where for each of these SDRAM components, the plurality of valid data outputs are the same for each addressable memory location within that component so that the same portion of each addressable memory location within any given SDRAM component consistently provides valid and accurate data.

3. The method of claim 2, wherein the act of presenting a row address to the address inputs of each of a plurality of partially defective SDRAM components includes the act of presenting a row address to SDRAM components mounted on SIMMs.

4. The method of claim 3, wherein the act of presenting a row address to the address inputs of each of a plurality of partially defective SDRAM components includes the act of presenting a row address to SDRAM components mounted on DIMMs.

5. A method of accessing memory cells in a memory module having a plurality of SDRAM components, each of the SDRAM components having a plurality of address inputs, and wherein each of the SDRAM components further comprises a plurality of banks of memory that are addressable by the address inputs, the method comprising the acts of:

presenting a row address to the address inputs of each SDRAM component;

presenting a column address to the address inputs of each SDRAM component;

selecting one of the plurality of banks within each SDRAM component by presenting at least one selection bit at the address inputs when the row address is presented to the address inputs, wherein each of the SDRAM components is partially defective such that each SDRAM components has at least one unreliable data output, and also a plurality of valid data outputs that provide reliable and accurate data;

aggregating the valid data outputs of each of the SDRAM components to provide a data path; and

communicating the data from the valid data outputs from each of the SDRAM components to the microprocessor.

6. The method of claim 5, wherein the act of presenting a row address includes the act of presenting a row address to the address inputs of partially defective SDRAM components, where for each of these SDRAM components, the plurality of valid data outputs are the same for each addressable memory location within that component so that the same portion of each addressable memory location within any given SDRAM component consistently provides valid and accurate data.

7. The method of claim 6, wherein the act of presenting a row address to the address inputs of each of a plurality of partially defective SDRAM components includes the act of presenting a row address to SDRAM components mounted on SIMMs.

8. The method of claim 7, wherein the act of presenting a row address to the address inputs of each of a plurality of partially defective SDRAM components includes the act of presenting a row address to SDRAM components mounted on DIMMs.

09/035739

ABSTRACT

Memory module using partially defective synchronous memory devices, such as SDRAM components. Multiple partially defective SDRAM components are configured to provide a reliable and nondefective memory module that takes advantage of the manner in which defective cells are localized on each SDRAM component.

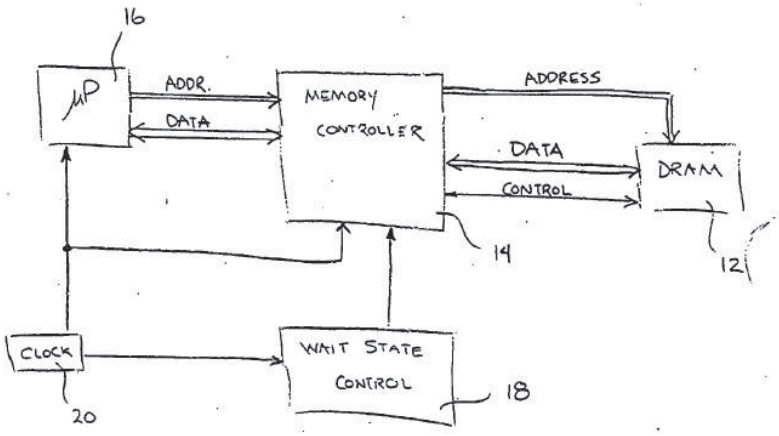

FIGURE 1 (PRIOR ART)

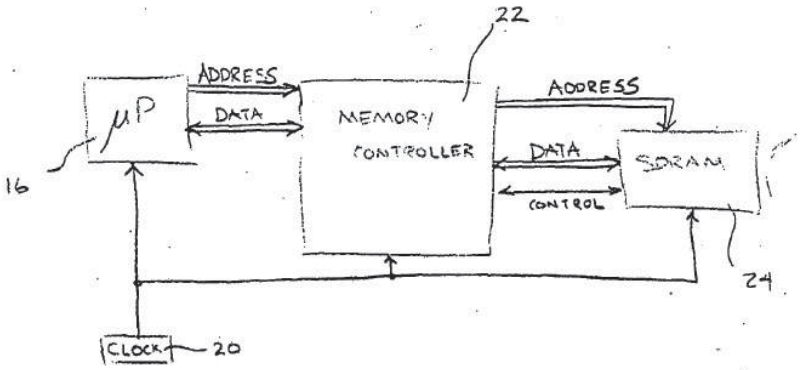
22
ADDRESS
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FIGURE 2

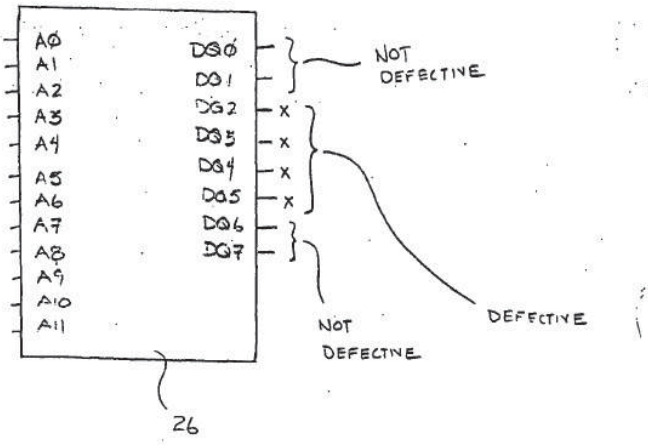


FIGURE 3

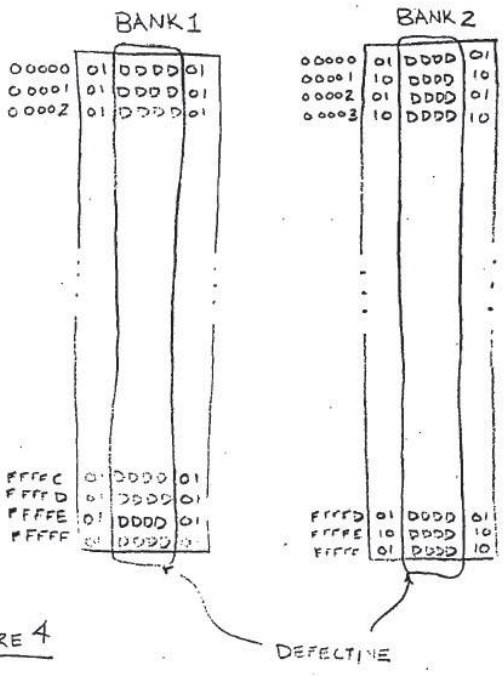
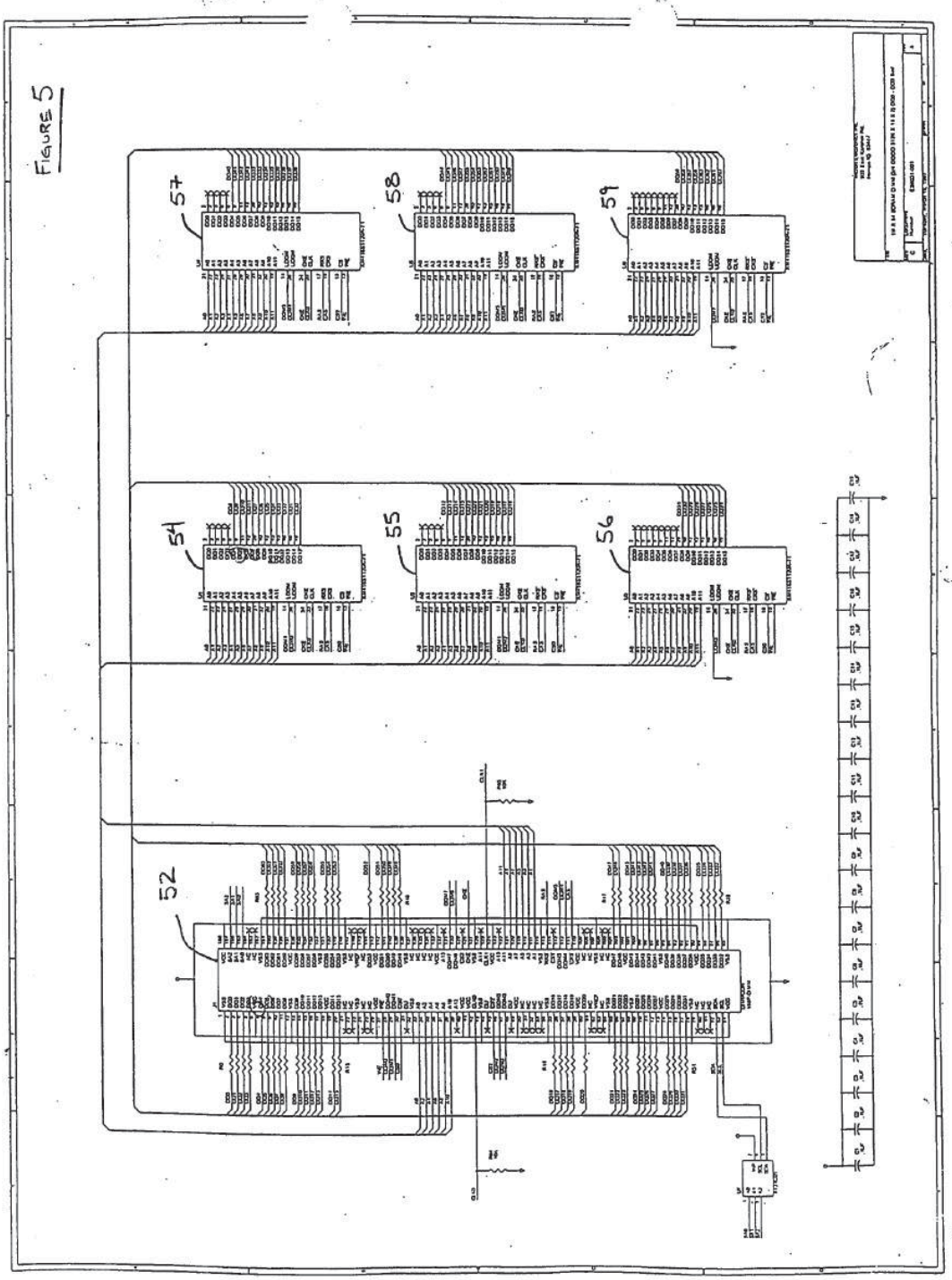


FIGURE 4

FIGURE 5



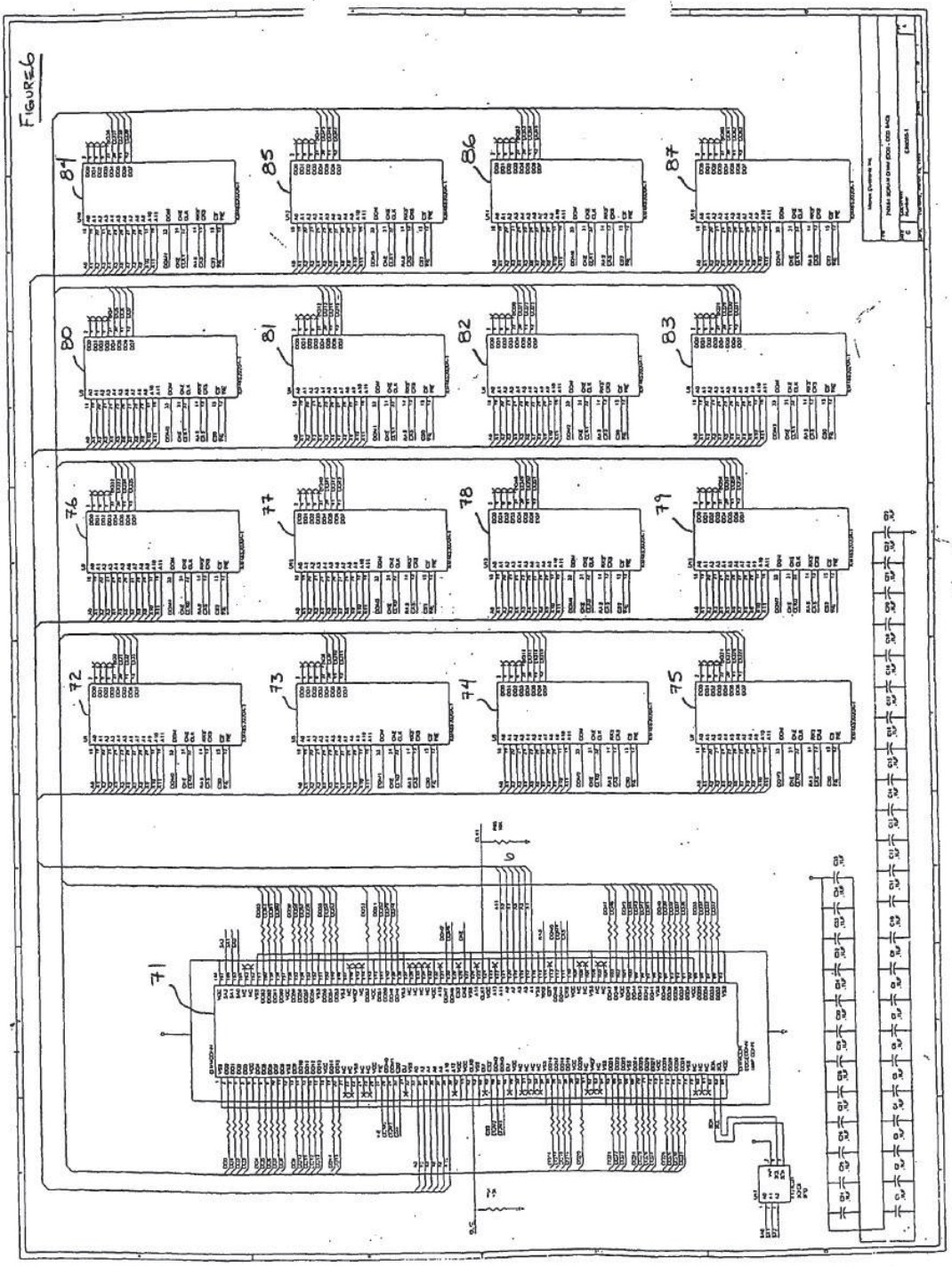


FIGURE 6
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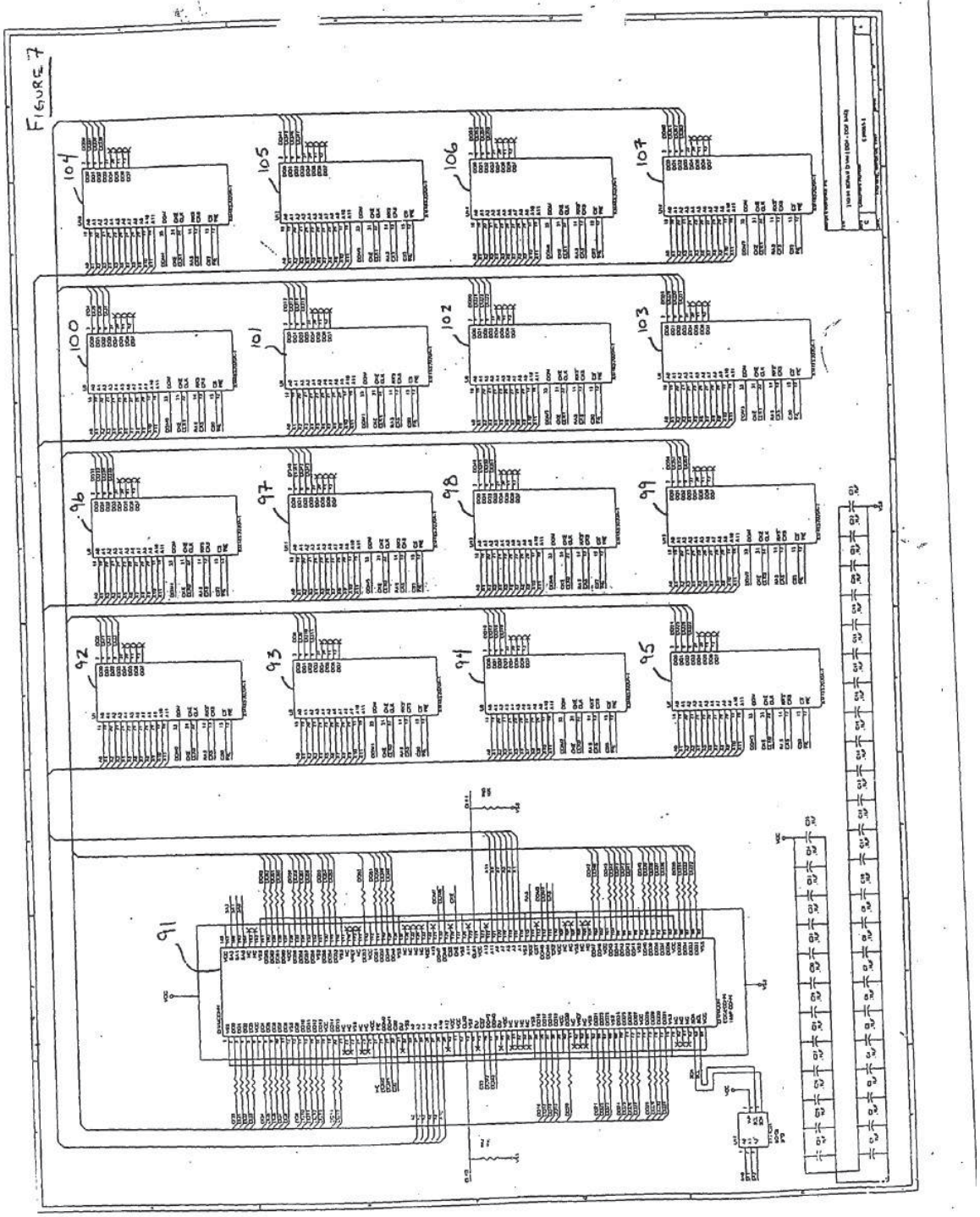
FIGURE 7



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APPLICATION NUMBER	FILING/RECEIPT DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NO./TITLE
09/035,739	03/05/98	WEBER M	R 6325

#2

0372/0612

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MINNEAPOLIS MN 55402

NOT ASSIGNED

2751

DATE MAILED: 06/12/98

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Filing Date Granted

An Application Number and Filing Date have been assigned to this application. The items indicated below, however, are missing. Applicant is given TWO MONTHS FROM THE DATE OF THIS NOTICE within which to file all required items and pay fees required below to avoid abandonment. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1:136(a). **If any of items 1 or 3 through 5 are indicated as missing, the SURCHARGE set forth in 37 CFR 1.16(e) of ☐ $65.00 for a small entity in compliance with 37 CFR 1.27, or ☒ $130.00 for a non-small entity, must also be timely submitted in reply to this NOTICE to avoid abandonment.**

If all required items on this form are filed within the period set above, the total amount owed by applicant as a ☐ small entity (statement filed) ☒ non-small entity is $ 130.00 .

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- ☐ insufficient.

Applicant must submit $ _____ to complete the basic filing fee and/or file a small entity statement claiming such status (37 CFR 1.27).

☐ 2. Additional claim fees of $_____, including any multiple dependent claim fees, are required.

$_____ for _____ independent claims over 3.

$_____ for _____ dependent claims over 20.

$_____ for multiple dependent claim surcharge.

Applicant must either submit the additional claim fees or cancel additional claims for which fees are due.

☒ 3. The oath or declaration:
- ☒ is missing or unexecuted.
- ☐ does not cover the newly submitted items.
- ☐ does not identify the application to which it applies.
- ☐ does not include the city and state or foreign country of applicant's residence.

An oath or declaration in compliance with 37 CFR 1. 63, including residence information and identifying the application by the above Application Number and Filing Date is required.

☐ 4. The signature(s) to the oath or declaration is/are by a person other than inventor or person qualified under 37 CFR 1.42, 1.43 or 1.47.
A properly signed oath or declaration in compliance with 37 CFR 1.63, identifying the application by the above Application Number and Filing Date, is required.

☐ 5. The signature of the following joint inventor(s) is missing from the oath or declaration:

An oath or declaration in compliance with 37 CFR 1.63 listing the names of all inventors and signed by the omitted inventor(s), identifying this application by the above Application Number and Filing Date, is required.

☐ 6. A $50.00 processing fee is required since your check was returned without payment (37 CFR 1.21(m)).

☐ 7. Your filing receipt was mailed in error because your check was returned without payment.

☐ 8. The application does not comply with the Sequence Rules.
See attached "Notice to Comply with Sequence Rules 37 CFR 1.821-1.825."

☐ 9. OTHER: _____

Direct the reply and any questions about this notice to "Attention: Box Missing Parts."

A copy of this notice MUST be returned with the reply.

Customer Service Center
Initial Patent Examination Division (703) 308-1202

PART 3 - OFFICE COPY

FORM PTO-1533 (REV 9-97)

Section 8

Docket: 6235

0300

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Richard Weber and Corey Larsen

Serial No.: 09/035,739

Filing Date: March 5, 1998

Title: Method for Recovery of Partially Defective Synchronous Memory Components

FILING OF MISSING PARTS OF APPLICATION UNDER 37 CFR §1.53(f)

Assistant Commissioner for Patents
Attention: Box Missing Parts
Washington, D.C. 20231

Dear Sir:

In response to the Notice To File Missing Parts of Application--Filing Date Granted, mailed June 12, 1998, pursuant to 37 CFR § 1.53(f) enclosed are the following:

1. Required copy of the Notice to File Missing Parts of Application;
2. Signed Declaration; and
3. A check in the amount of $130.00 for the surcharge under 37 CFR 1.16(e)).

8/19/1998 MPEOPLES 00000040 09035739

1 FC:105 130.00 OP

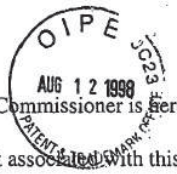
I hereby certify that the document is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231 on

August 10, 1998
(Date of Deposit)

Cathy Bombard
(Name)

Cathy Bombard
Signature

August 10, 1998
Date of Signature



The Commissioner is hereby authorized to charge any underpayment or credit any overpayment associated with this communication to Deposit Account No. 04-1420. A copy of this letter is enclosed for that purpose.

Respectfully submitted,

Date: Aug. 7, 1998

Stuart R. Hemphill (Reg. No. 28,084)
Dorsey & Whitney LLP
Pillsbury Center South
220 South Sixth Street
Minneapolis, Minnesota 55402-1498
Telephone: 612-340-2734

Attorney for Applicant

Docket: 6235

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Richard Weber and Corey Larsen

Serial No.: 09/035,739

Filing Date: March 5, 1998

Title: Method for Recovery of Partially Defective Synchronous Memory Components

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August 10, 1998
(Date of Deposit)

Cheryl Thompson
(Name)

Cheryl Thompson
Signature

August 10, 1998
Date of Signature

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Dorsey & Whitney LLP
Pillsbury Center South
220 South Sixth Street
Minneapolis, Minnesota 55402-1498
Telephone: 612-340-2734

Attorney for Applicant

UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

APPLICATION NUMBER	FILING/RECEIPT DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NO./TITLE
09/035,939	03/05/98	WEBER	R 6128

FB

0372/0612

DORSEY & WHITNEY
PILLSBURY CENTER SOUTH
220 SOUTH SIXTH STREET
MINNEAPOLIS MN 55402

NOT ASSIGNED

2751

DATE MAILED: 06/12/98

NOTICE TO FILE MISSING PARTS OF APPLICATION

Filing Date Granted

An Application Number and Filing Date have been assigned to this application. The items indicated below, however, are missing. Applicant is given TWO MONTHS FROM THE DATE OF THIS NOTICE within which to file all required items and pay fees required below to avoid abandonment. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a). **If any of items 1 or 3 through 5 are indicated as missing, the SURCHARGE set forth in 37 CFR 1.16(e) of ☐ $65.00 for a small entity in compliance with 37 CFR 1.27, or ☒ $130.00 for a non-small entity, must also be timely submitted in reply to this NOTICE to avoid abandonment.**

If all required items on this form are filed within the period set above, the total amount owed by applicant as a ☐ small entity (statement filed) ☒ non-small entity is $ 130.00.

☐ 1. The statutory basic filing fee is:
- ☒ missing.
- ☐ insufficient.

Applicant must submit $_____ to complete the basic filing fee and/or file a small entity statement claiming such status (37 CFR 1.27).

☐ 2. Additional claim fees of $_____, including any multiple dependent claim fees, are required.

$_____ for _____ independent claims over 3.

$_____ for _____ dependent claims over 20.

$_____ for multiple dependent claim surcharge.

Applicant must either submit the additional claim fees or cancel additional claims for which fees are due.

☒ 3. The oath or declaration:
- ☒ is missing or unexecuted.
- ☐ does not cover the newly submitted items.
- ☐ does not identify the application to which it applies.
- ☐ does not include the city and state or foreign country of applicant's residence.

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See attached "Notice to Comply with Sequence Rules 37 CFR 1.821-1.825."

☐ 9. OTHER:

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A copy of this notice MUST be returned with the reply.

D Jones MAE

Customer Service Center
Initial Patent Examination Division (703) 308-1202

PART 2 - COPY TO BE RETURNED WITH RESPONSE

FORM PTO-1533 (REV 9-97)

Dkt No. 6325

DECLARATION FOR PATENT APPLICATION

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled **"Method for Recovery of Partially Defective Synchronous Memory Components"**, the specification of which

- ☐ is attached hereto.
- ☒ was filed on March 5, 1998 as United States application number 09/035,739 and amended on (NA).

I do not know and do not believe that the invention was ever known or used in the United States before my or our invention thereof;

I do not know and do not believe that the invention was ever patented or described in any printed publication in any country before my or our invention thereof or more than one year prior to this application;

I do not know and do not believe that the invention was in public use or on sale in the United States more than one year prior to this application.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose to the United States Patent and Trademark Office information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, Section 119(a)-(d) or Section 365(b) of any foreign application(s) for patent or inventor's certificate, or Section 365(a) of any PCT international application which designated at least one country other than the United States, listed below, and I have also identified and listed below any foreign application(s) for patent or inventor's certificate, or PCT international application, having a filing date before that of the application(s) on which priority is claimed:

FOREIGN APPLICATION(S)

Number	Country	day/month/year filed	Priority Claimed
NA			

I hereby claim the benefit under Title 35, United States Code, Section 119(e) of any U.S. provisional application(s) listed below:

U.S. PROVISIONAL APPLICATION(S)

Application Serial No.	Filing Date
NA	

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s), or under Section 365(c) of any PCT international application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT international application in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose to the United States Patent and Trademark Office information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application:

PRIORITY U.S. APPLICATION(S)

Application Serial No.	Filing Date	Status
NA		

I hereby appoint the following attorneys and/or agents to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith: Ronald J. Brown (29,016), David E. Bruhn (36,762), David N. Fronek (25,678), Joseph F. Haag (P 42,612); Stuart R. Hemphill (28,084), Eugene L. Johnson (21,028), Kenneth E. Levitt (39,747), Niall A. MacLeod (P41,963), Erik Nordstrom (39,792), Devan Padmanabhan (38,262), Gerald H. Sullivan (37,243), Jon F. Tuttle (25,713) and Mark A. Wolfe (36,311).