Address all telephone calls to: Mark A. Wolfe at (612) 340-5659.

Address all correspondence to: Mark A. Wolfe at Dorsey & Whitney LLP, Pillsbury Center South, 220 South Sixth Street, Minneapolis, Minnesota 55402.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Richard Weber
Name of Sole or First Inventor


Inventor's Signature

May 15, 1998
Date

2972 North Woodcreek Lane
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USA
Citizenship

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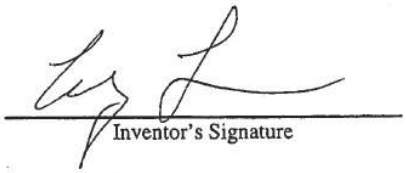
Residence Address

Corey Larsen
Name of Second Inventor


Inventor's Signature

May 21, 1998
Date

P.O. Box 383
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Citizenship

225 Canal Street
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GP. 2751
#4
11-20-98
aw

Docket: 6325

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Richard Weber and Corey Larsen

Serial No.: 09/035,739

Filing Date: March 5, 1998

Title: Method for Recovery of Useful Areas of Partially Defective Synchronous Memory Components

Information Disclosure Statement

Assistant Commissioner for Patents
Washington D.C. 20231

Dear Sir:

Pursuant to 37 CFR §1.56, the references listed on the attached Form PTO-1449 (1 sheet, submitted in duplicate) are being brought to the attention of the Examiner for consideration in connection with the examination of the above identified patent application. Copies of the identified references are enclosed.

Applicant reserves the right to show, pursuant to 37 CFR §1.131 or otherwise, that any of the identified publications, and any referenced in the present application and its parent applications, is not prior art with respect to the present inventions.

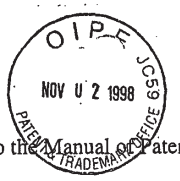
I hereby certify that the document is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231 on

October 26, 1998
(Date of Deposit)

Carl Bombolli
(Name)

Carl Bombolli
Signature

October 26, 1998
Date of Signature



Pursuant to the Manual of Patent Examining Procedure, Chapter 609, applicant requests that the Examiner consider each of the listed documents and initial and return to the undersigned a copy of the enclosed Form PTO-1449.

Respectfully submitted,

Date: 10/25/98

By _____

Niall A. MacLeod, Esq.
Registration No. 41,963
Dorsey & Whitney LLP
Pillsbury Center South
220 South Sixth Street
Minneapolis, Minnesota 55402
Telephone: (612) 343-2193
Attorney for Applicant

Form PTO-1449 (Rev. 2-32) U.S DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY DOCKET NO. 6325	SERIAL NO. 09/035,739
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use several sheets if necessary)	APPLICANT Richard Weber and Corey Larsen	
	FILING DATE March 5, 1998	GROUP ART UNIT 2751

U.S. PATENT DOCUMENTS

Examiner Initial		Document Number	Date	Inventor Name	Class	Sub-class	Filing Date (if appropriate)
KR		3 7 1 4 6 3 7	1/30/73	Beausoleil	365	200	
KR		3 7 3 5 3 6 8	5/22/73	Beausoleil	365	200	
KE		3 7 7 2 6 5 2	11/13/73	Hilberg	711	151	
KE		3 7 8 1 8 2 6	12/25/73	Beausoleil	365	200	
KE		4 3 5 5 3 7 6	10/19/82	Gould	365	200	
KE		4 4 7 5 1 9 4	10/2/84	LaVallee et al.	714	710	
KR		4 4 9 3 0 7 5	1/8/85	Anderson et al.	714	711	
KE		4 5 2 7 2 5 1	7/2/85	Nibby, Jr. et al.	714	8	
KR		4 8 3 7 7 4 7	6/6/89	Dosaka et al.	714	711	
KE		4 9 9 2 9 8 4	2/12/91	Busch et al.	365	200	
KE		5 1 2 6 9 7 3	6/30/92	Gallia et al.	365	200	

FOREIGN PATENT DOCUMENTS

Examiner Initial		Document Number	Date	Country	Class	Sub-class	Translation	

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

Examiner Initial		Document Description

EXAMINER	DATE CONSIDERED
Kevin L. Ellis	10/22/99

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Form PTO-1449 (Rev. 2-32) U.S DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY DOCKET NO. 6325	SERIAL NO. 09/035,739
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use several sheets if necessary)	APPLICANT Richard Weber and Corey Larsen	
	FILING DATE March 5, 1998	GROUP ART UNIT 2751

U.S. PATENT DOCUMENTS

Examiner Initial		Document Number	Date	Inventor Name	Class	Sub-class	Filing Date (if appropriate)
KE		5 2 0 8 7 7 5	5/4/93	Lee	365	200	
KE		5 2 4 3 5 7 0	9/7/93	Saruwatari	365	200	
KE		5 2 6 8 8 6 6	12/7/93	Feng et al.	365	200	
KE		5 2 7 0 9 7 4	12/14/93	Reddy	365	200	
KE		5 2 7 0 9 7 6	12/14/93	Tran	365	200	
KE		5 3 3 2 9 2 2	7/26/94	Oguchi et al.	257	723	
KE		5 3 4 9 5 5 6	9/20/94	Lee	365	200	
KE		5 3 9 2 2 4 7	2/21/95	Fujita	365	200	
KE		5 4 0 6 5 6 5	4/11/95	MacDonald	714	711	
KE		5 4 6 5 2 3 4	11/7/95	Hannai	365	200	
KE		5 4 7 5 6 4 8	12/12/95	Fujiwara	365	230.06	

FOREIGN PATENT DOCUMENTS

Examiner Initial		Document Number	Date	Country	Class	Sub-class	Translation	

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Kevin L. Ellis	10/22/99

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use several sheets if necessary)	APPLICANT Richard Weber and Corey Larsen	
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U.S. PATENT DOCUMENTS

Examiner Initial		Document Number	Date	Inventor Name	Class	Sub-class	Filing Date (if appropriate)
KE		5 5 2 8 5 5 3	6/18/96	Saxena	365	230.01	
KE		5 5 7 6 9 9 9	11/19/96	Kim et al.	345	200	
KE		5 6 6 8 7 6 3	9/16/97	Fujioka et al.	365	200	

FOREIGN PATENT DOCUMENTS

Examiner Initial		Document Number	Date	Country	Class	Sub-class	Translation	

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Examiner Initial		Document Description

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Kevin L. Ellis	10/22/99

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Form PTO-1449 (Rev. 2-32) U.S DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY DOCKET NO. 6325	SERIAL NO. 09/035,739
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use several sheets if necessary)	APPLICANT Richard Weber and Corey Larsen	
	FILING DATE March 5, 1998	GROUP ART UNIT 2755

U.S. PATENT DOCUMENTS

Examiner Initial		Document Number	Date	Inventor Name	Class	Sub-class	Filing Date (if appropriate)
		3 7 1 4 6 3 7	1/30/73	Beausoleil			
		3 7 3 5 3 6 8	5/22/73	Beausoleil			
		3 7 7 2 6 5 2	11/13/73	Hilberg			
		3 7 8 1 8 2 6	12/25/73	Beausoleil			
		4 3 5 5 3 7 6	10/19/82	Gould			
		4 4 7 5 1 9 4	10/2/84	LaVallee et al.			
		4 4 9 3 0 7 5	1/8/85	Anderson et al.			
		4 5 2 7 2 5 1	7/2/85	Nibby, Jr. et al.			
		4 8 3 7 7 4 7	6/6/89	Dosaka et al.			
		4 9 9 2 9 8 4	2/12/91	Busch et al.			
		5 1 2 6 9 7 3	6/30/92	Gallia et al.			

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Form PTO-1449 U.S DEPARTMENT OF COMMERCE (Rev. 2-32) PATENT AND TRADEMARK OFFICE	ATTY DOCKET NO. 6325	SERIAL NO. 09/035,739
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use several sheets if necessary)	APPLICANT Richard Weber and Corey Larsen	
	FILING DATE March 5, 1998	GROUP ART UNIT 2751

U.S. PATENT DOCUMENTS

Examiner Initial		Document Number	Date	Inventor Name	Class	Sub-class	Filing Date (if appropriate)
		5,208,735	5/4/93	Lee			
		5,243,507	9/7/93	Saruwatari			
		5,268,866	12/7/93	Feng et al.			
		5,270,964	12/14/93	Reddy			
		5,270,967	12/14/93	Tran			
		5,332,922	7/26/94	Oguchi et al.			
		5,349,549	9/20/94	Lee			
		5,392,224	2/21/95	Fujita			
		5,404,306	4/11/95	MacDonald			
		5,463,564	10/31/95	Hannai			
		5,475,615	12/12/95	Fujiwara			

FOREIGN PATENT DOCUMENTS

Examiner Initial		Document Number	Date	Country	Class	Sub-class	Translation	

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

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Form PTO-1449 (Rev. 2-32) U.S DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY DOCKET NO. 6325	SERIAL NO. 09/035,739
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U.S. PATENT DOCUMENTS

Examiner Initial		Document Number	Date	Inventor Name	Class	Sub-class	Filing Date (if appropriate)
		5 5 2 8 5 5 3	6/18/96	Saxena			
		5 5 7 6 9 9 9	11/19/96	Kim et al.			
		5 6 6 8 7 6 3	9/16/97	Fujioka et al.			

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UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/035,739	03/05/98	WEBER	R 6325

LMC1/1026

DORSEY & WHITNEY
PILLSBURY CENTER SOUTH
220 SOUTH SIXTH STREET
MINNEAPOLIS MN 55402

EXAMINER	
ELLIS,K	
ART UNIT	**PAPER NUMBER**
2751	5

DATE MAILED: 10/26/99

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

PTO-90C (Rev. 2/95)

1- File Copy

Office Action Summary

Application No.	Applicant(s)
09/035,739	Weber et al.
Examiner	**Group Art Unit**
Kevin L. Ellis	2751

---The MAILING DATE of this communication appears on the cover sheet beneath the correspondence address---

Period for Response

A SHORTENED STATUTORY PERIOD FOR RESPONSE IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a response be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for response specified above is less than thirty (30) days, a response within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for response is specified above, such period shall, by default, expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to respond within the set or extended period for response will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).

Status

☐ Responsive to communication(s) filed on _____.

☐ This action is **FINAL.**

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 1 1; 453 O.G. 213.

Disposition of Claims

☒ Claim(s) 1-8 is/are pending in the application.

Of the above claim(s) _____ is/are withdrawn from consideration.

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) 1-8 is/are rejected.

☐ Claim(s) _____ is/are objected to.

☐ Claim(s) _____ are subject to restriction or election requirement.

Application Papers

☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The proposed drawing correction, filed on _____ is ☐ approved ☐ disapproved.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119 (a)-(d)

☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 11 9(a)-(d).

☐ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number) _____.

☐ received in this national stage application from the International Bureau (PCT Rule 1 7.2(a)).

*Certified copies not received: _____.

Attachment(s)

☒ Information Disclosure Statement(s), PTO-1449, Paper No(s). 4

☐ Interview Summary, PTO-413

☒ Notice of References Cited, PTO-892

☐ Notice of Informal Patent Application, PTO-152

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Other _____

Office Action Summary

U. S. Patent and Trademark Office
PTO-326 (Rev. 3-97)

*U.S. GPO: 1997-417-381/62710

Part of Paper No. 5

Detailed Action

1. Claims 1-8 are presented for examination.

2. Information disclosed and listed on PTO 1449 was considered.

Drawings

3. This application has been filed with informal drawings which are acceptable for examination purposes only. Formal drawings will be required when the application is allowed.

Claim Objections

4. Claims 1-8 are objected to because of the following informalities:

Claims 1 and 5 recites:

A) "to the microprocessor" (Lines 9 and 15 respectively) It is suggested that the word 'the' be changed to 'a' since the 'microprocessor' as not been set forth it the claim.

Claims 2-4 and 6-8 are objected to as fully incorporating the defects of an objected base claim.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 USC § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

6. Claims 1 and 2 are rejected under 35 USC 102(e) as being anticipated by Jacobson, U.S. Patent 5,920,513.

A) As to claim 1, Jacobson discloses the invention as claimed. There is a method of accessing a memory module (Fig 4) comprising the acts of presenting a row address to the address inputs (see Col 3 Lines 2-12) of each of a plurality of partially defective SDRAM components (see Fig 4 & 5, Col 3 Lines 35-41, Col 4 Lines 25-42, and Col 5 Lines 4-45) that have at least one unreliable data output (Col 3 Lines 12-27, Col 5 Lines 4-7 & 33-45) and that also have a plurality of valid data outputs, wherein the valid data outputs are data outputs that provide reliable and accurate data (Col 3 Lines 12-27, Col 5 Lines 4-7 & 33-45), and presenting a column address to the address inputs of each SDRAM component (Col 3 Lines 2-12), aggregating the valid data outputs of each of the SDRAM components to provide a data path (see Fig 5 and Col 4 Lines 26-67), and communicating the data from the valid data outputs to a microprocessor (Col 4 Lines 7-8; one of ordinary skill in the art would recognize that a computer would include some sort of processing device, i.e. a microprocessor).

B) As to claim 2, the act of presenting a row address does include the act of presenting a row address to the address inputs of partially defective SDRAM components (see Col 4 Line 67 to Col 5 Line 3), where for each of these SDRAM components, the plurality of valid data outputs are the same for each addressable memory location within that component so that the same portion of each addressable memory location within any given SDRAM component consistently provides valid and accurate data (see Col 3 Lines 13-27).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 USC § 103 which forms the basis for all obviousness rejections set forth in this Office action:

A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Subject matter developed by another person, which qualifies as prior art only under subsection (f) or (g) of section 102 of this title, shall not preclude patentability under this section where the subject matter and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person.

8. Claims 3 and 4 are rejected under 35 USC § 103 as being unpatentable over Jacobson, U.S. Patent 5,920,513, in view of Dell et al., U.S. Patent 5,896,346.

A) As to claims 3 and 4, Jacobson discloses the invention substantially as claimed. However, Jacobson does not disclose that the SDRAM components are mounted on SIMMs or DIMMs.

Dell et al. teaches that it was common for SDRAM components to come mounted on SIMMs or DIMMs (see Col 1 Lines 38-47). SIMMs and DIMMs were common memory modules in the art at the time of the invention. They provide a convenient and standardized packaging of the SDRAM components which could be easily inserted into and removed from a computer system motherboard.

Accordingly, it would have been obvious to one having ordinary skill in the art at the time of the invention to package the SDRAM components of Jacobson in a SIMM or DIMM module as these were common memory module designs in the industry.

9. Claims 5 and 6 are rejected under 35 USC § 103 as being unpatentable over Jacobson, U.S. Patent 5,920,513, in view of Schaefer, U.S. Patent 5,636,173.

A) As to claim 5, Jacobson discloses the invention substantially as claimed. There is a method of accessing memory cells in a memory module (Fig 4) having a plurality of SDRAM components (see Col 3 Lines 35-42), each of the SDRAM components having a plurality of address inputs (see Fig 5 and Col 4 Line 67 to Col 5 Line 3), the

method comprising the acts of presenting a row address to the address inputs of each SDRAM component (see Col 3 Lines 2-12), presenting a column address to the address inputs of each SDRAM component (Col 3 Lines 2-12), wherein each of the SDRAM components is partially defective (see Fig 4 & 5, Col 3 Lines 35-41, Col 4 Lines 25-42, and Col 5 Lines 4-45) such that each SDRAM components has at least one unreliable data output (Col 3 Lines 12-27, Col 5 Lines 4-7 & 33-45) and also a plurality of valid data outputs that provide reliable and accurate data (Col 3 Lines 12-27, Col 5 Lines 4-7 & 33-45), aggregating the valid data outputs of each of the SDRAM components to provide a data path (see Fig 5 and Col 4 Lines 26-67), and communicating the data from the valid data outputs from each of the SDRAM components to a microprocessor (Col 4 Lines 7-8; one of ordinary skill in the art would recognize that a computer would include some sort of processing device, i.e. a microprocessor). However, Jacobson does not disclose that each of the SDRAM components further comprises a plurality of banks of memory that are addressable by address inputs and that the method comprises selecting one of the plurality of banks within each SDRAM component by presenting at least one selection bit at the address inputs when the row address is presented to the address inputs.

Schaefer teaches SDRAM components that comprise a plurality of banks of memory that are addressable by address inputs and that the selecting of one of the plurality of banks within the SDRAM component is performed by presenting at least one selection bit at the address inputs when the row address is presented to the address inputs (see Col 1 Lines 23-42 and Col 4 Lines 22-36). The advantage to using SDRAM with banks is that it allows interleaving between the two or more banks to hide the precharging time.

Accordingly, it would have been obvious to one having ordinary skill in the art at the time the invention was made to utilize SDRAM components that include a

plurality of banks of memory that are addressable by address inputs and that the selecting of one of the plurality of banks within each SDRAM component is performed by presenting at least one selection bit at the address inputs when the row address is presented to the address inputs as taught by Schaefer for the advantage that using SDRAM components with multiple banks allows the precharging time to be hidden thus increasing the speed of the memory.

B) As to claim 6, the act of presenting a row address does include the act of presenting a row address to the address inputs of partially defective SDRAM components (see Col 4 Line 67 to Col 5 Line 3), where for each of these SDRAM components, the plurality of valid data outputs are the same for each addressable memory location within that component so that the same portion of each addressable memory location within any given SDRAM component consistently provides valid and accurate data (see Col 3 Lines 13-27).

10. Claims 7 and 8 are rejected under 35 USC § 103 as being unpatentable over Jacobson, U.S. Patent 5,920,513, and Schaefer, U.S. Patent 5,636,173, and in further view of Dell et al., U.S. Patent 5,896,346.

A) As to claims 7 and 8, Jacobson discloses the invention substantially as claimed. However, Jacobson does not disclose that the SDRAM components are mounted on SIMMs or DIMMs.

Dell et al. teaches that it was common for SDRAM components to come mounted on SIMMs or DIMMs (see Col 1 Lines 38-47). SIMMs and DIMMs were common memory modules in the art at the time of the invention. They provide a convenient and standardized packaging of the SDRAM components which could be easily inserted into and removed from a computer system motherboard.

Accordingly, it would have been obvious to one having ordinary skill in the art

at the time of the invention to package the SDRAM components of Jacobson in a SIMM or DIMM module as these were common memory module designs in the industry.

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

12. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) days from the mail date of this letter. Failure to respond within the period for response will result in **ABANDONMENT** of the application (see 35 USC 133, MPEP 710.02, 710.02(b)).

13. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Kevin Ellis whose telephone number is (703) 305-9659. The Examiner can normally be reached on the weekdays from 6:30am to 3:00pm.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Eddie Chan, can be reached on (703) 305-9712.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks
Washington, D.C. 20231

or faxed to:
(703)308-9051, (for formal communications intended for entry)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-3900.

Kevin L. Ellis
Patent Examiner
October 22, 1999

Kevin L. Ellis

TO SEPARATE, H[illegible]OP AND BOTTOM EDGES, SNAP–APART AND [illegible]ARD CARBON

FORM PTO-892 (REV. 2-92) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	SERIAL NO.	GROUP ART UNIT	ATTACHMENT TO PAPER NUMBER
NOTICE OF REFERENCES CITED	09/035,739	2751	5
	APPLICANT(S) Weber et al.		

U.S. PATENT DOCUMENTS

*		DOCUMENT NO.	DATE	NAME	CLASS	SUB-CLASS	FILING DATE IF APPROPRIATE
	A	5920513	7/6/99	Jacobson	365	200	
	B	5896346	4/20/99	Dell et al.	365	233	
	C	5636173	6/3/97	Schaefer	365	230.03	
	D	4355376	10/19/82	Gould	365	200	
	E	4992984	2/12/91	Busch et al.	365	200	
	F	5768173	6/16/98	Seo et al.	365	52	
	G	5970008	10/19/99	Zagar et al.	365	226	
	H	3845476	10/29/74	Boehm	365	200	
	I						
	J						
	K						

FOREIGN PATENT DOCUMENTS

*		DOCUMENT NO.	DATE	COUNTRY	NAME	CLASS	SUB-CLASS	PERTINENT SHTS. DWG	PERTINENT PP. SPEC.
	L								
	M								
	N								
	O								
	P								
	Q								

OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, Etc.)

R	
S	
T	
U	

EXAMINER	DATE
Kevin L. Ellis	10/22/99

* A copy of this reference is not being furnished with this office action.
(See Manual of Patent Examining Procedure, section 707.05 (a).)

GP 2751 RS

6

Docket: 6325

RECEIVED
JAN 5 - 2000
Group 2700

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

OIPE JC89 JAN 03 2000 PATENT & TRADEMARK OFFICE

Applicant:	Richard Weber and Corey Larsen		
Serial No.:	09/035,739		
Filing Date:	March 5, 1998	Examiner:	K. Ellis
Title:	Method for Recovery of Useful Areas of Partially Defective Synchronous Memory Components	Group Art Unit:	2751

COMBINED: (1) INFORMATION DISCLOSURE STATEMENT
(2) CERTIFICATION UNDER 37 C.F.R. §1.97(c) and (e)

Assistant Commissioner for Patents
Washington D.C. 20231

Dear Sir:

(1) Information Disclosure Statement

Pursuant to 37 C.F.R. §1.56, the references listed on the attached form PTO-1449 (1 sheet, submitted in duplicate) are being brought to the attention of the Examiner for consideration in connection with the examination of the above identified patent application. Copies of the identified references are enclosed. These references were cited in an Office Action mailed December 8, 1999, by Examiner P. Kormanyos in related application Serial No. 09/035,629.

I hereby certify that the document is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231 on

December 29, 1999
(Date of Deposit)

Marilyn Yahr
(Name)

Marilyn Yahr
Signature

12/29/99
Date of Signature

(2) Certification Under 37 C.F.R. §1.97(c) and (e)

The undersigned hereby certifies that no item of information contained in the above Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application or, to the knowledge of the undersigned, was known to any individual designated in §1.56(c) more than three months prior to the filing of this statement.

Pursuant to the Manual of Patent Examining Procedure, Chapter 609, Applicant requests that the Examiner consider each of the listed documents and initial and return to the undersigned a copy of the enclosed Form PTO-1449 (submitted in duplicate).

Respectfully submitted,

Date: 12/29/99

By _____
Niall A. MacLeod
Registration No. 41,963
Dorsey & Whitney LLP
220 South Sixth Street
Minneapolis, Minnesota 55402
Telephone: 612/340-2755

Attorney for Applicant

Form PTO-1449 (Rev. 2-32) U.S DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY DOCKET NO. 6325	SERIAL NO. 09/035,739
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use several sheets if necessary)	APPLICANT Richard Weber and Corey Larsen	RECEIVED
	FILING DATE March 5, 1998	GROUP ART UNIT 2751

JAN 5 - 2000

Group 2700

U.S. PATENT DOCUMENTS

Examiner Initial		Document Number	Date	Inventor Name	Class	Sub-class	Filing Date (if appropriate)
UR		3,717,535	2/6/73	Moss	365	94	
UR		3,846,756	10/29/74	Boehm	365	200	
UR		5,051,994	9/24/91	Bluethman, et al.	714	8	
UR		5,251,174	10/5/93	Hwang	365	200	
UR		5,511,033	4/30/96	Dell, et al.	365	52	
UR		5,539,697	7/23/96	Kim, et al.	365	200	
UR		5,796,652	8/25/98	Di Zenzo, et al.	365	52	
UR		5,953,276	9/21/99	Yew, et al.	361	760	
UR		5,963,462	10/12/99	Ryan	711	105	

FOREIGN PATENT DOCUMENTS

Examiner Initial		Document Number	Date	Country	Class	Sub-class	Translation	

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

Examiner Initial		Document Description
UR		INTEL, PC SDRAM UNBUFFERED DIMM SPECIFICATION, REVISION 1.0, February 1998, 47 pages
UR		INTEL, PC SDRAM SPECIFICATION, REVISION 1.63, October 1998

EXAMINER	DATE CONSIDERED
Kevin L. Ellis	3/30/00

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Form PTO-1449 U.S DEPARTMENT OF COMMERCE (Rev. 2-32) PATENT AND TRADEMARK OFFICE	ATTY DOCKET NO. 6325	SERIAL NO. 09/035,739
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use several sheets if necessary)	APPLICANT Richard Weber and Corey Larsen	
	FILING DATE March 5, 1998	GROUP ART UNIT 2754

U.S. PATENT DOCUMENTS

Examiner Initial		Document Number	Date	Inventor Name	Class	Sub-class	Filing Date (if appropriate)
		3 7 1 5 7 3 5	2/6/73	Moss			
		3 8 4 5 4 7 6	10/29/74	Boehm			
		5 0 5 1 9 9 4	9/24/91	Bluethman, et al.			
		5 2 5 1 1 7 4	10/5/93	Hwang			
		5 5 1 3 1 3 5	4/30/96	Dell, et al.			
		5 5 3 9 6 9 7	7/23/96	Kim, et al.			
		5 7 9 8 9 6 2	8/25/98	Di Zenzo, et al.			
		5 9 5 6 2 3 3	9/21/99	Yew, et al.			
		5 9 6 6 7 2 4	10/12/99	Ryan			

FOREIGN PATENT DOCUMENTS

Examiner Initial		Document Number	Date	Country	Class	Sub-class	Translation	

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

Examiner Initial		Document Description
		INTEL, PC SDRAM UNBUFFERED DIMM SPECIFICATION, REVISION 1.0, February 1998, 47 pages
		INTEL, PC SDRAM SPECIFICATION, REVISION 1.63, October 1998

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

98/2751

OIPE JC81 JAN 31 2000 PATENT & TRADEMARK OFFICE

Docket: 6325

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

RECEIVED FEB - 3 2000 TC 2700 MAIL ROOM

Applicant: Richard Weber and Corey Larsen

Serial No.: 09/035,739

Filing Date: March 5, 1998 Examiner: K. Ellis

Title: Method for Recovery of Useful Areas of Partially Defective Synchronous Memory Components Group Art Unit: 2751

Amendment and Request for Reconsideration

Assistant Commissioner for Patents
Washington D.C. 20231

Dear Sir:

The following amendments and remarks are submitted in response to the Office Action of October 26, 1999.

I. In the Claims

Please amend the claims as follows:

1. (Amended) A method of accessing a memory module comprising the acts of:

presenting a row address to the address inputs of each of a plurality of partially defective SDRAM components that have at least one unreliable data output, and that also have a plurality

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January 26, 2000
(Date of Deposit)
Catherine A. Lawrence
(Name)
Catherine A. Lawrence
Signature
January 26, 2000
Date of Signature

of valid data outputs, wherein the valid data outputs are data outputs that provide reliable and accurate data; and

presenting a column address to the address inputs of each SDRAM component;

aggregating the valid data outputs of each of the SDRAM components to provide a data path; and

communicating the data from the valid data outputs to a [the] microprocessor.

5. A method of accessing memory cells in a memory module having a plurality of SDRAM components, each of the SDRAM components having a plurality of address inputs, and wherein each of the SDRAM components further comprises a plurality of banks of memory that are addressable by the address inputs, the method comprising the acts of:

presenting a row address to the address inputs of each SDRAM component;

presenting a column address to the address inputs of each SDRAM component;

selecting one of the plurality of banks within each SDRAM component by presenting at least one selection bit at the address inputs when the row address is presented to the address inputs, wherein each of the SDRAM components is partially defective such that each SDRAM components has at least one unreliable data output, and also a plurality of valid data outputs that provide reliable and accurate data;

aggregating the valid data outputs of each of the SDRAM components to provide a data path; and

communicating the data from the valid data outputs from each of the SDRAM components to a [the] microprocessor.

II. Remarks

A. Office Action Dated October 26, 1999

In the Office Action dated October 26, 1999, the Examiner rejected all pending claims 1-8 in light of U.S. Patent Nos. 5,920,513 to Jacobson, 5,896,346 to Dell, and 5,636,173 to Schaefer. The primary reference cited by the Examiner (and the only one discussed further) is the Jacobson reference. While the Jacobson reference and the present invention are directed to solutions to the same problem -- how to avoid complete replacement of a memory device that is only partially defective -- they do so in patentably distinct manners.

In Jacobson, repair sites 54 and 56 are provided on a particular memory chip module 32 in anticipation that one or more of the memory device 38, etc. on the module 32 will be partially defective. See Figs. 3 and 4. In the event that a memory device 38, etc. is found to be defective, the data lines of the memory device 38, etc. that correspond to the defective portions of memory device 38, etc. are linked to the data lines of a memory device 66 (termed a "repair memory device") located in the repair sites 54 and 56. In this manner, according to the Jacobson reference, "[r]ather than replacing device 38 entirely, repair device 66 only replaces those sections of device 38 that are defective." Jacobson, col. 5, lines 7-9.

In the present invention, however, the problem is solved in a different manner. The present invention, unlike Jacobson, does not require the addition of repair memory devices to replace partially defective memory portions, rather the present invention aggregates existing SDRAM data outputs found to be reliable in order to form the desired bank of memory. See Application, p. 6, lines 10-13 ("By using the twelve nondefective DQ outputs from SDRAM components 54, 55, 57, and 58 and by using the eight nondefective DQ outputs from SDRAM

components 56 and 59, a 512K x 64 x 2 memory module can be constructed from the six partially defective SDRAM components.").

These two approaches are quite distinct. In Jacobson, the amount of memory planned for the module prior to the detection of defects is maintained, but it is maintained at a price -- space on the memory module must be reserved for one or more of the "memory repair devices." In contrast, in the present invention, several defective memory devices of capacity N are used to form an "aggregate" memory device of the same capacity N, but in the present invention, no additional components are required. Rather, the valid data outputs of the SDRAMS are aggregated to form the data outputs of an overall "non-defective" memory device of capacity N. The Applicant submits that this aspect of the present invention differentiates Jacobson and it is clearly embodied in each of the pending independent claims. See, e.g., claim 1 ("aggregating the valid data outputs of each of the SDRAM components to provide a data path") and claim 5 ("aggregating the valid data outputs of each of the SDRAM components to provide a data path"). These claims and, *a fortiori*, claims dependent therefrom are allowable over the cited references.

IV. Conclusion

In view of the above amendments and preceding remarks, it is urged respectfully that the rejection of the claims be reconsidered and withdrawn, and that the claims be allowed. However, if the Examiner believes that any issues remain unresolved, he is invited to telephone the undersigned to expedite allowance. Upon receiving the Notice of Allowance, the applicant will submit formal drawings.

Respectfully submitted,

Date: Jan. 26, 2000

By _____

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UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office
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Washington, D.C. 20231

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/035,739	03/05/98	WEBER	R 6325

LM02/0404

DORSEY & WHITNEY
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220 SOUTH SIXTH STREET
MINNEAPOLIS MN 55402

EXAMINER	
ELLIS,K	
ART UNIT	**PAPER NUMBER**
2751	

DATE MAILED: 04/04/00

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

PTO-90C (Rev. 2/95) U.S. G.P.O. 1999 460-693 1- File Copy

Office Action Summary

Application No.	Applicant(s)
09/035,739	Weber et al.
Examiner	**Group Art Unit**
Kevin L. Ellis	2751

---The MAILING DATE of this communication appears on the cover sheet beneath the correspondence address---

Period for Response

A SHORTENED STATUTORY PERIOD FOR RESPONSE IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a response be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for response specified above is less than thirty (30) days, a response within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for response is specified above, such period shall, by default, expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to respond within the set or extended period for response will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).

Status

☒ Responsive to communication(s) filed on 1/3/00.

☒ This action is **FINAL.**

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 1 1; 453 O.G. 213.

Disposition of Claims

☒ Claim(s) 1-8 is/are pending in the application.

Of the above claim(s)____ is/are withdrawn from consideration.

☐ Claim(s)____ is/are allowed.

☒ Claim(s) 1-8 is/are rejected.

☐ Claim(s)____ is/are objected to.

☐ Claim(s)____ are subject to restriction or election requirement.

Application Papers

☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The proposed drawing correction, filed on____ is ☐ approved ☐ disapproved.

☐ The drawing(s) filed on____ is/are objected to by the Examiner.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119 (a)-(d)

☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 11 9(a)-(d).

☐ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number)____.

☐ received in this national stage application from the International Bureau (PCT Rule 1 7.2(a)).

*Certified copies not received:____.

Attachment(s)

☒ Information Disclosure Statement(s), PTO-1449, Paper No(s). 6

☐ Interview Summary, PTO-413

☐ Notice of References Cited, PTO-892

☐ Notice of Informal Patent Application, PTO-152

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Other____

Office Action Summary

Detailed Action

1. Claims 1-8 are presented for examination. This Office Action is in response to the Amendment filed 1/3/00.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 USC § 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

3. Claims 1 and 2 are rejected under 35 USC 102(e) as being anticipated by Jacobson, U.S. Patent 5,920,513.

A) As to claim 1, Jacobson discloses the invention as claimed. There is a method of accessing a memory module (Fig 4) comprising the acts of presenting a row address to the address inputs (see Col 3 Lines 2-12) of each of a plurality of partially defective SDRAM components (see Fig 4 & 5, Col 3 Lines 35-41, Col 4 Lines 25-42, and Col 5 Lines 4-45) that have at least one unreliable data output (Col 3 Lines 12-27, Col 5 Lines 4-7 & 33-45) and that also have a plurality of valid data outputs, wherein the valid data outputs are data outputs that provide reliable and accurate data (Col 3 Lines 12-27, Col 5 Lines 4-7 & 33-45), and presenting a column address to the address inputs of each SDRAM component (Col 3 Lines 2-12), aggregating the valid data outputs of each of the SDRAM components to provide a data path (see Fig 5 and Col 4 Lines 26-67), and communicating the data from the valid data outputs to a microprocessor (Col 4 Lines 7-8; one of ordinary skill in the art would recognize that a computer would include some sort of processing device, i.e. a microprocessor).

B) As to claim 2, the act of presenting a row address does include the act of presenting a row address to the address inputs of partially defective SDRAM components (see Col 4 Line 67 to Col 5 Line 3), where for each of these SDRAM components, the plurality of valid data outputs are the same for each addressable memory location within that component so that the same portion of each addressable memory location within any given SDRAM component consistently provides valid and accurate data (see Col 3 Lines 13-27).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 USC § 103 which forms the basis for all obviousness rejections set forth in this Office action:

> A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
>
> Subject matter developed by another person, which qualifies as prior art only under subsection (f) or (g) of section 102 of this title, shall not preclude patentability under this section where the subject matter and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person.

5. Claims 3 and 4 are rejected under 35 USC § 103 as being unpatentable over Jacobson, U.S. Patent 5,920,513, in view of Dell et al., U.S. Patent 5,896,346.

A) As to claims 3 and 4, Jacobson discloses the invention substantially as claimed. However, Jacobson does not disclose that the SDRAM components are mounted on SIMMs or DIMMs.

Dell et al. teaches that it was common for SDRAM components to come mounted on SIMMs or DIMMs (see Col 1 Lines 38-47). SIMMs and DIMMs were common memory modules in the art at the time of the invention. They provide a convenient and standardized packaging of the SDRAM components which could be

easily inserted into and removed from a computer system motherboard.

Accordingly, it would have been obvious to one having ordinary skill in the art at the time of the invention to package the SDRAM components of Jacobson in a SIMM or DIMM module as these were common memory module designs in the industry.

6. Claims 5 and 6 are rejected under 35 USC § 103 as being unpatentable over Jacobson, U.S. Patent 5,920,513, in view of Schaefer, U.S. Patent 5,636,173.

A) As to claim 5, Jacobson discloses the invention substantially as claimed. There is a method of accessing memory cells in a memory module (Fig 4) having a plurality of SDRAM components (see Col 3 Lines 35-42), each of the SDRAM components having a plurality of address inputs (see Fig 5 and Col 4 Line 67 to Col 5 Line 3), the method comprising the acts of presenting a row address to the address inputs of each SDRAM component (see Col 3 Lines 2-12), presenting a column address to the address inputs of each SDRAM component (Col 3 Lines 2-12), wherein each of the SDRAM components is partially defective (see Fig 4 & 5, Col 3 Lines 35-41, Col 4 Lines 25-42, and Col 5 Lines 4-45) such that each SDRAM components has at least one unreliable data output (Col 3 Lines 12-27, Col 5 Lines 4-7 & 33-45) and also a plurality of valid data outputs that provide reliable and accurate data (Col 3 Lines 12-27, Col 5 Lines 4-7 & 33-45), aggregating the valid data outputs of each of the SDRAM components to provide a data path (see Fig 5 and Col 4 Lines 26-67), and communicating the data from the valid data outputs from each of the SDRAM components to a microprocessor (Col 4 Lines 7-8; one of ordinary skill in the art would recognize that a computer would include some sort of processing device, i.e. a microprocessor). However, Jacobson does not disclose that each of the SDRAM components further comprises a plurality of banks of memory that are addressable by address inputs and that the method comprises selecting one of the plurality of banks within each SDRAM component by

presenting at least one selection bit at the address inputs when the row address is presented to the address inputs.

Schaefer teaches SDRAM components that comprise a plurality of banks of memory that are addressable by address inputs and that the selecting of one of the plurality of banks within the SDRAM component is performed by presenting at least one selection bit at the address inputs when the row address is presented to the address inputs (see Col 1 Lines 23-42 and Col 4 Lines 22-36). The advantage to using SDRAM with banks is that it allows interleaving between the two or more banks to hide the precharging time.

Accordingly, it would have been obvious to one having ordinary skill in the art at the time the invention was made to utilize SDRAM components that include a plurality of banks of memory that are addressable by address inputs and that the selecting of one of the plurality of banks within each SDRAM component is performed by presenting at least one selection bit at the address inputs when the row address is presented to the address inputs as taught by Schaefer for the advantage that using SDRAM components with multiple banks allows the precharging time to be hidden thus increasing the speed of the memory.

B) As to claim 6, the act of presenting a row address does include the act of presenting a row address to the address inputs of partially defective SDRAM components (see Col 4 Line 67 to Col 5 Line 3), where for each of these SDRAM components, the plurality of valid data outputs are the same for each addressable memory location within that component so that the same portion of each addressable memory location within any given SDRAM component consistently provides valid and accurate data (see Col 3 Lines 13-27).

7. Claims 7 and 8 are rejected under 35 USC § 103 as being unpatentable over Jacobson,

U.S. Patent 5,920,513, and Schaefer, U.S. Patent 5,636,173, and in further view of Dell et al., U.S. Patent 5,896,346.

A) As to claims 7 and 8, Jacobson discloses the invention substantially as claimed. However, Jacobson does not disclose that the SDRAM components are mounted on SIMMs or DIMMs.

Dell et al. teaches that it was common for SDRAM components to come mounted on SIMMs or DIMMs (see Col 1 Lines 38-47). SIMMs and DIMMs were common memory modules in the art at the time of the invention. They provide a convenient and standardized packaging of the SDRAM components which could be easily inserted into and removed from a computer system motherboard.

Accordingly, it would have been obvious to one having ordinary skill in the art at the time of the invention to package the SDRAM components of Jacobson in a SIMM or DIMM module as these were common memory module designs in the industry.

Answers to Remarks

8. Applicant's arguments filed 1/3/00 have been fully considered but they are not deemed to be persuasive.

9. Applicant argues that Jacobson does not teach the same solution to the problem as taught by the present invention and cites the specification as teaching the difference (see P 3 of the Amendment). However, the broad recitation of the claim language allows Jacobson to be read upon the presently claimed invention.

Conclusion

10. **THIS ACTION IS MADE FINAL**. Applicant is reminded of the extension of time policy as set forth in 37 CFR § 1.136(a). The practice of automatically extending the shortened statutory period an additional month upon the filing of a timely first response to a

final rejection has been discontinued by the Office. See 1021 TMOG 35.

A SHORTENED STATUTORY PERIOD FOR RESPONSE TO THIS FINAL ACTION IS SET TO EXPIRE THREE MONTHS FROM THE DATE OF THIS ACTION. IN THE EVENT A FIRST RESPONSE IS FILED WITHIN TWO MONTHS OF THE MAILING DATE OF THIS FINAL ACTION AND THE ADVISORY ACTION IS NOT MAILED UNTIL AFTER THE END OF THE THREE-MONTH SHORTENED STATUTORY PERIOD, THEN THE SHORTENED STATUTORY PERIOD WILL EXPIRE ON THE DATE THE ADVISORY ACTION IS MAILED, AND ANY EXTENSION FEE PURSUANT TO 37 CFR § 1.136(a) WILL BE CALCULATED FROM THE MAILING DATE OF THE ADVISORY ACTION. IN NO EVENT WILL THE STATUTORY PERIOD FOR RESPONSE EXPIRE LATER THAN SIX MONTHS FROM THE DATE OF THIS FINAL ACTION.

11. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Kevin Ellis whose telephone number is (703) 305-9659. The Examiner can normally be reached on the weekdays from 6:30am to 3:00pm.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Eddie Chan, can be reached on (703) 305-9712.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks
Washington, D.C. 20231

or faxed to:
(703)308-9051, (for formal communications intended for entry)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-3900.

Kevin L. Ellis
Patent Examiner
March 29, 2000

EDDIE P. CHAN
SUPERVISORY PATENT EXAMINER

GB 2751
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8-11-00
OC

MPAT.179A

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	:	Weber et al.
App. No.	:	09/035,739
Filed	:	March 5, 1998
For	:	METHOD FOR RECOVERY OF USEFUL AREAS OF PARTIALLY DEFECTIVE SYNCHRONOUS MEMORY COMPONENTS
Examiner	:	K. Ellis

ESTABLISHMENT OF RIGHT OF ASSIGNEE TO TAKE ACTION
AND
REVOCATION AND POWER OF ATTORNEY

Assistant Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

The undersigned is empowered to act on behalf of the assignee below (the "Assignee"). The original assignment is recorded at Reel 9378 and Frame 0800. This Assignment represents the entire chain of title of this invention from the Inventor(s) to the Assignee.

I declare that all statements made herein are true, and that all statements made upon information and belief are believed to be true, and further, that these statements were made with the knowledge that willful, false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. § 1001, and that willful, false statements may jeopardize the validity of the application, or any patent issuing thereon.

The undersigned hereby revokes any previous powers of attorney in the subject application, and hereby appoints the registrants of Knobbe, Martens, Olson & Bear, LLP, 620 Newport Center Drive, Sixteenth Floor, Newport Beach, California 92660, Telephone

App. No. : 09/035,739
Filed : March 5, 1998

(949) 760-0404, **Customer No. 20,995**; also Steven P. Arnold, Registration No. 33,354, Hoyt A. Fleming, III, Registration No. 41,752, and Paul A. Revis, Registration No. 45,040, of Micron Electronics, Inc., 900 East Karcher Road, Nampa, Idaho 83687, Telephone (208) 898-3434, as its attorneys with full power of substitution and revocation to prosecute this application and to transact all business in the U.S. Patent and Trademark Office connected herewith. This appointment is to be to the exclusion of the inventor(s) and his attorney(s) in accordance with the provisions of 37 C.F.R. § 3.71.

Please use **Customer No. 20,995** for all communications.

Micron Electronics, Inc.

Dated: 5/2/10

By: _____
Paul A. Revis

Title: Intellectual Property Counsel

Address: 900 East Karcher Road
Nampa, Idaho 83687

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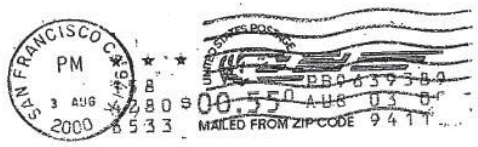

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AUG 10 2000
PATENT & TRADEMARK OFFICE

#ext①/request for CPA 1.53(d) 8/16/00 EW

PTO/SB/29 (8/98)
Approved for use through 09/30/2000. OMB 0651-0032
Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE
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CONTINUED PROSECUTION APPLICATION (CPA) REQUEST TRANSMITTAL

Submit an original, and a duplicate for fee processing.
(Only for Continuation or Divisional applications under 37 C.F.R. § 1.53(d))

CHECK BOX, if applicable: ☐ DUPLICATE

Address to:
Assistant Commissioner for Patents
Box CPA
Washington, DC 20231

Attorney Docket No. of Prior Application	97.00031.01
First Named Inventor	Richard Weber
Examiner Name	Kevin Ellis
Group / Art Unit	2751
Express Mail Label No.	

This is a request for a ☒ continuation or ☐ divisional application under 37 C.F.R. § 1.53(d), (continued prosecution application (CPA)) of prior application number 09 / 035,739, filed on 3/5/98, entitled Method For Recovery of Useful Area of Partially, etal

NOTES

FILING QUALIFICATIONS. The prior application identified above must be a nonprovisional application that is either (1) complete (as defined by 37 C.F.R. § 1.51(b)) or (2) the national stage of an international application in compliance with 35 U.S.C. 371. A Notice will be placed on a patent issuing from a CPA, except for reissues, and designs, to the effect that the patent issued on a CPA and is subject to the twenty year patent term provisions of 35 U.S.C. § 154(a)(2). Therefore, the prior application or a CPA may have been filed before, on or after June 8, 1995.

ICs IP NOT PERMITTED. A continuation-in-part application cannot be filed as a CPA under 37 C.F.R. § 1.53(d), but must be filed under 37 C.F.R. § 1.53(b).

EXPRESS ABANDONMENT OF PRIOR APPLICATION. The filing of this CPA is a request to expressly abandon the prior application as of the filing date of the request for a CPA. 37 C.F.R. § 1.53(b) must be used to file a continuation, divisional, or continuation-in-part of an application that is not to be abandoned.

ACCESS TO PRIOR APPLICATION. The filing of this CPA will be construed to include a waiver of confidentiality by the applicant under 35 U.S.C. 122 to the extent that any member of the public who is entitled under the provisions of 37 C.F.R. § 1.14 to access to, copies of, or information concerning, the prior applications may be given similar access to, copies of, or similar information concerning, the other application or applications in the file jacket.

35 U.S.C. 120 STATEMENT. In a CPA, no reference to the prior application is needed in the first sentence of the specification and none should be submitted. If a sentence referencing the prior application is submitted, it will not be entered. A request for a CPA is the specific reference required by 35 U.S.C. 120 and to every application assigned the application number identified in such request, 37 C.F.R. § 1.78(a).

1. ☐ Enter the unentered amendment previously filed on _____ under 37 C.F.R. § 1.116 in the prior nonprovisional application.
2. ☒ A preliminary amendment is enclosed.
3. This application is filed by fewer than all the inventors named in the prior application, 37 C.F.R. § 1.53 (d)(4).
   a. ☐ ***DELETE*** the following inventor(s) named in the prior nonprovisional application:
      .....
      .....
   b. ☐ The inventor(s) to be deleted are set forth on a separate sheet attached hereto.
4. ☐ A new power of attorney or authorization of agent (PTO/SB/81) is enclosed.
5. Information Disclosure Statement (IDS) is enclosed:
   a. ☐ PTO-1449
   b. ☐ Copies of IDS Citations

08/17/2000 TCOLE1 00000001 09035739
01 FC:131 690.00 CH
02 FC:115 110.00 CH

PTO/SB/29 (8/98)
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Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE
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CLAIMS	(1) FOR	(2) NUMBER FILED	(3) NUMBER EXTRA	(4) RATE	(5) CALCULATIONS
	TOTAL CLAIMS (37 C.F.R. § 1.16(c) or (j))	12 -20* =	0	x $_____ =	$ 0
	INDEPENDENT CLAIMS (37 C.F.R.§1.16(b) or (i))	3 -3** =	0	x $_____ =	0
	MULTIPLE DEPENDENT CLAIMS (if applicable) (37 C.F.R. § 1.16(d))			+ $_____ =	
				BASIC FEE (37 C.F.R. §1.16)	
				Total of above Calculations =	
	Reduction by 50% for filing by small entity (Note 37 C.F.R. §§ 1.9, 1.27 & 1.28).				
	* Reissue claims in excess of 20 and over original patent. ** Reissue independent claims over original patent.			TOTAL =	0

6. Small entity status:
   a. ☐ A small entity statement is enclosed, if (b) and (c) do not apply.
   b. ☐ A small entity statement was filed in the prior nonprovisional application and such status is still proper and desired.
   c. ☐ Is no longer claimed.
7. The Commissioner is hereby authorized to credit overpayments or charge the following fees to Deposit Account No. _____-_500659_____:
   a. ☒ Fees required under 37 C.F.R. § 1.16.
   b. ☒ Fees required under 37 C.F.R. § 1.17.
   c. ☒ Fees required under 37 C.F.R. § 1.18.
8. ☐ A check in the amount of $_____ is enclosed.
9. ☐ New Attorney Docket Number, if desired _____
   [Prior application Attorney Docket Number will carryover to this CPA unless a new Attorney Docket Number has been provided herein.]
10 a. ☐ Receipt For Facsimile Transmitted CPA (PTO/SB/29A)
   b. ☐ Return Receipt Postcard (Should be specifically itemized, See MPEP 503)
11. ☐ Other: .....

NOTE: The prior application's correspondence address will carry over to this CPA UNLESS a new correspondence address is provided below.

12. NEW CORRESPONDENCE ADDRESS

☐ Customer Number or Bar Code Label [redacted] (Insert Customer No. or Attach bar code label here) or ☐ New correspondence address below

Name					
Address					
City		State		Zip Code	
Country		Telephone		Fax	

RECEIVED
AUG 1 2000
TECH CENTER 2700 MAIL ROOM

13. SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED

Name (Print/Type)	Raul A. Reyes
Signature	[redacted]
Registration No. (Attorney/Agent)	45,040
Date	8/1/00

#12 pre amdt

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventors:	Richard Weber and Corey Larsen
Application No.:	09/035,739
Filed:	March 5, 1998
Title:	METHOD FOR RECOVERY OF USEFUL AREAS OF PARTIALLY DEFECTIVE SYNCHRONOUS MEMORY COMPONENTS
Examiner:	Kevin Ellis
Art Unit:	2751
Atty. Docket No.:	97.00031.01

Assistant Commissioner for Patents
Washington, DC 20231

PRELIMINARY AMENDMENT

Dear Assistant Commissioner:

This paper responds to the second Office action in this patent application mailed April 4, 2000 and presents amendments for further prosecution of the application in a continuing prosecution application. Please consider the application in light of the following amendments and remarks.

AMENDMENTS

In the Specification

On page 2, in the paragraph prior to "FIELD OF THE INVENTION," insert --

This application includes subject matter related to application No. 09/035,629, filed concurrently herewith on March 5, 1998.--

In the Claims

Please add claims 9-12 as follows:

9. A method of enabling data access between a memory module having data outputs and a microprocessor comprising the acts of:

determining which SDRAM data outputs of a group of SDRAM components are defective;

assembling a set of SDRAM components from the group of SDRAM components, wherein at least one of the SDRAM components has defective SDRAM data outputs, such that each memory module data output is connected to an operative SDRAM data output; and

applying a clock signal that is processed to synchronously apply operating signals to the memory module and the microprocessor to effect data access between the memory module and the microprocessor.

10. The method of claim 9 further comprising sorting SDRAM components based on which of the data outputs of the respective SDRAM components are defective.

11. The method of claim 10 further comprising providing sorted SDRAM components with predetermined numbers and arrangements of defective SDRAM data outputs for assemble on predetermined, complementary memory modules.

12. The method of claim 9 wherein determining which data outputs are defective includes testing SDRAM components prior to assembling the SDRAM components on a memory module.

REMARKS

Claims 1-12 are pending in the present application.

In the Office action mailed on April 4, 2000, the examiner rejected claims 1and 2 under 35 U.S.C. §102(e) as anticipated over U.S. Pat. No. 5,920,513 to Jacobson ("Jacobson"). Claims 3 and 4 were rejected under 35 U.S.C. §103 as being unpatentable

over Jacobson in view of U.S. Pat. No. 5,896,346 to Dell et al. ("Dell"). Claims 5 and 6 were rejected under 35 U.S.C. §103 as being unpatentable over Jacobson in view of U.S. Pat. No. 5,636,173 to Schaefer, ("Schaefer"). Claims 5 and 6 were rejected under 35 U.S.C. §103 as being unpatentable over Jacobson and Schaefer and further in view of Dell.

Reconsideration is respectfully requested.

The Jacobson Reference

The applicant has submitted herewith a declaration under 37 C.F.R. §1.131 removing Jacobson as a reference. Claims 2-4 and 6-8 depend from claims 1 and 5, directly or indirectly, and are patentable for at least the same reason.

New claims 9-12 have been added to more fully describe patentable aspects of the present invention. The claims are supported by the original specification as filed. Allowance of these claims is earnestly solicited.

CONCLUSION

In light of the foregoing remarks, applicant respectfully requests that the outstanding rejections be removed. If the examiner wishes to discuss the above remarks, the examiner is encouraged to contact the undersigned. Additionally, if the examiner notices any informalities in the claims, he is also encouraged to contact the undersigned to expediently correct any such informalities. The applicant has attempted to address all issues raised in the previous Office action. If the examiner believes that there are issues that have not been addressed, the examiner is invited to contact the undersigned.

Respectfully submitted,

Paul A. Revis
Attorney for Applicant
Registration No. 45,040

Enclosures:
Transmittal Letter (2 copies)
Declaration of Inventors with Exhibit A
Postcard

Micron Electronics, Inc.
Legal Department
900 East Karcher Road
Nampa, ID 83687
(208)898-1316 – Voice
(208)898-7211 – Fax

#13 Declaration

DATE OF DEPOSIT: 8-3-00

I hereby certify that this paper is being deposited with the United States Postal Service as first-class mail in an envelope addressed to the Assistant Commissioner for Patents, Washington, D.C. 20231

8/10/00

Nancy Hammond

Signature

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventors:	Richard Weber and Corey Larsen
Application No.:	09/035,739
Filed:	March 5, 1998
Title:	METHOD FOR RECOVERY OF USEFUL AREAS OF PARTIALLY DEFECTIVE SYNCHRONOUS MEMORY COMPONENTS

Examiner:	Kevin Ellis
Art Unit:	2751
Atty. Docket No.:	97.00031.01

Assistant Commissioner for Patents
2011 Jefferson Davis Highway
Washington, DC 20231

DECLARATION OF RICHARD WEBER AND COREY LARSEN UNDER 37 C.F.R. § 1.131

Dear Assistant Commissioner for Patents:

We, Richard Weber and Corey Larsen, declare and state that:

1. We are the inventors of the invention described and claimed in U.S. Patent Application No. 09/035,739, filed March 5, 1998. This declaration establishes invention in this country before August 22, 1997, and thus before the U.S. filing date of U.S. Patent No. 5,920,513 issued to Jacobson.

2. Before August 22, 1997, we conceived the invention currently presented in claims 1-12 of the above-captioned patent application. Our conception of the invention is corroborated by the Micron Electronics, Inc. drawing entitled "2MX64 SDRAM DIMM (DQ4 – DQ7 BAD)," dated March 6, 1997, attached hereto as Exhibit A.

3. As shown in Exhibit A, we did conceive a method of accessing a memory module, and particularly the memory cells of the memory module. Exhibit A illustrates a structure through which a row address may be presented to a plurality of partially defective SDRAM components that have unreliable and reliable data outputs, and a column address may be presented to the SDRAM address inputs. Further, a particular bank may be selected. Aggregation of the valid data outputs of each of the SDRAM component to provide a data path is also shown. Data may then be communicated from the valid data outputs to a microprocessor. In another embodiment, the invention includes a method of enabling data access between a memory module having data outputs and a microprocessor. The illustrated memory module may result from determining which SDRAM data outputs of a group of SDRAM components are defective, and assembling a set of SDRAM components from the group of SDRAM components, wherein at least one of the SDRAM components has defective SDRAM data outputs, such that each memory module data output is connected to an operative SDRAM data output. A clock signal may then be processed to synchronously apply operating signals to the memory module and the microprocessor to effect data access between the memory module and the microprocessor.

4. After conceiving this invention, we proceeded diligently by preparing schematic drawings, accomplishing testing, disclosing the invention to our employer, working through an initial invention review procedure, and participating in the preparation of the present patent application. On March 5, 1998, we constructively reduced this invention to practice with the filing of the present application.

5. We further declare that all statements herein made of our own knowledge are true, and that all statements made on information or belief are believed to be true; and further, that the statements are made with the knowledge that the making of willful or false statements or the like is punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and may jeopardize the validity of any patent issuing from this patent application.

Dated this 3rd day of August, 2000.

Richard Weber

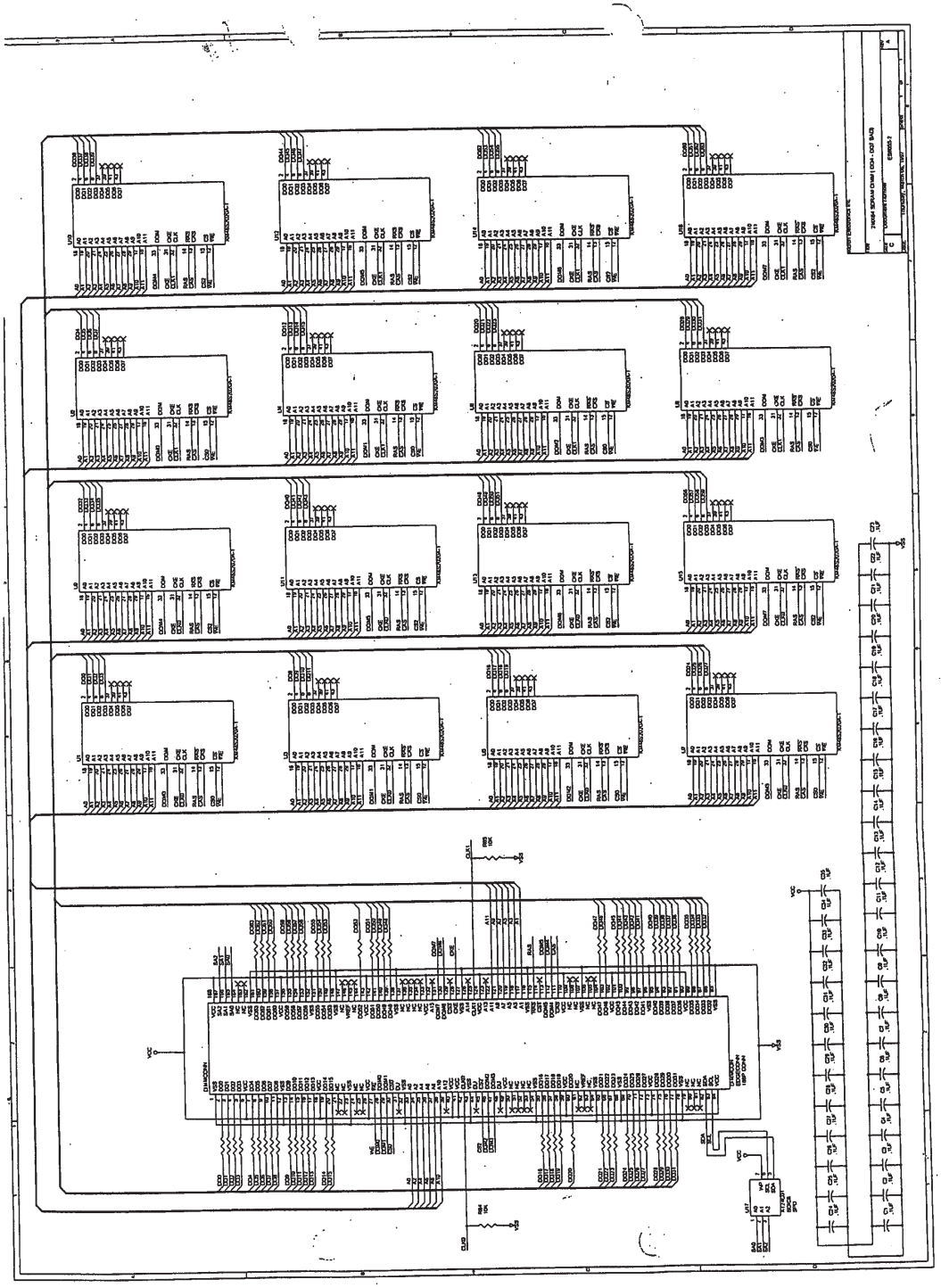
Residence	:	Boise, County of Ada State of Idaho
Citizenship	:	United States
P.O. Address	:	2972 N. Woodcreek Ln. Boise, Idaho 83704

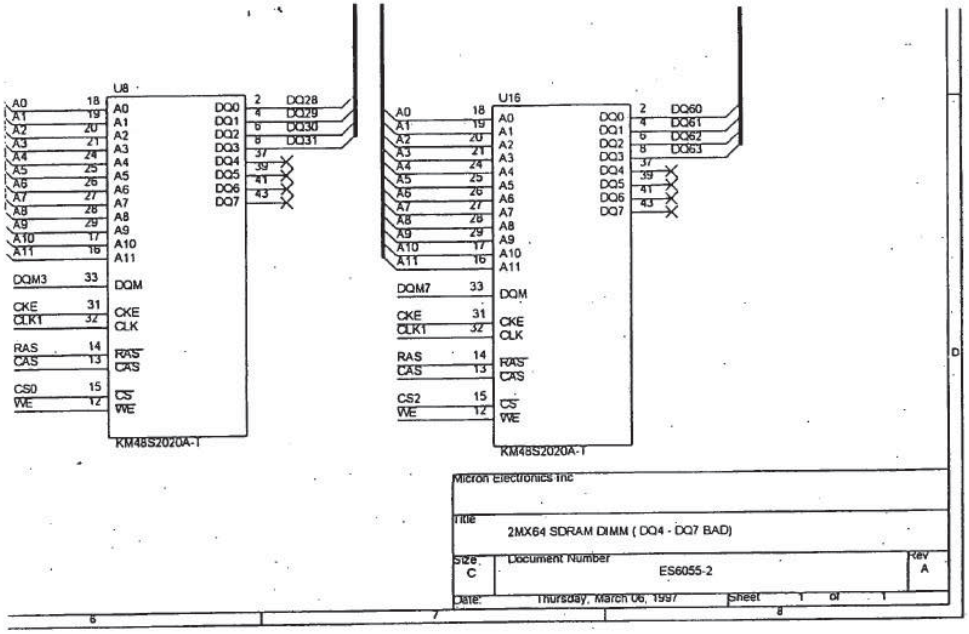
Dated this 3ed day of August, 2000.

Corey Larsen

Residence	:	Marsing, County of Owyhee State of Idaho
Citizenship	:	United States
P.O. Address	:	P.O. Box 383 Marsing, Idaho 83639

Exhibit A




U8
U16
KM48S2020A-T
KM48S2020A-T
Micron Electronics Inc
Title
2MX64 SDRAM DIMM (DQ4 - DQ7 BAD)
Size
C
Document Number
ES6055-2
Rev
A
Date:
Thursday, March 06, 1997
Sheet
1
of
1

#10

OC000000005316714

UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office
Address: COMMISSIONER OF PATENT AND TRADEMARKS
Washington, D.C. 20231

APPLICATION NUMBER	FILING DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
09/035,739	03/05/1998	RICHARD WEBER	6325

20995
KNOBBE MARTENS OLSON & BEAR LLP
620 NEWPORT CENTER DRIVE
SIXTEENTH FLOOR
NEWPORT BEACH, CA 92660

Date Mailed: 08/11/2000

NOTICE REGARDING POWER OF ATTORNEY

This is in response to the Power of Attorney filed 08/07/2000.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

Oteaba Coles

Customer Service Center
Initial Patent Examination Division (703) 308-1202

OFFICE COPY

#10

OC000000005316687

UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office
Address: COMMISSIONER OF PATENT AND TRADEMARKS
Washington, D.C. 20231

APPLICATION NUMBER	FILING DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
09/035,739	03/05/1998	RICHARD WEBER	6325

DORSEY & WHITNEY
PILLSBURY CENTER SOUTH
220 SOUTH SIXTH STREET
MINNEAPOLIS, MN 55402

Date Mailed: 08/11/2000

NOTICE REGARDING POWER OF ATTORNEY

This is in response to the Power of Attorney filed 08/07/2000.

The Power of Attorney to you in this application has been revoked by the assignee who has intervened as provided by 37 CFR 3.71. Future correspondence will be mailed to the new address of record(37 CFR 1.33).

Ofealia Coles
Customer Service Center
Initial Patent Examination Division (703) 308-1202
NEW ATTORNEY/AGENT COPY

UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/035,739	03/05/98	WEBER	R 6325

020995 LM02/0907
KNOBBE MARTENS OLSON & BEAR LLP
620 NEWPORT CENTER DRIVE
SIXTEENTH FLOOR
NEWPORT BEACH CA 92660

EXAMINER	
ELLIS,K	
ART UNIT	PAPER NUMBER
2751	14

DATE MAILED: 09/07/00

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

PTO-90C (Rev. 2/95) U.S. G.P.O. 1999 460-693 1- File Copy

Office Action Summary

Application No.	Applicant(s)
09/035,739	Weber et al.
Examiner	**Group Art Unit**
Kevin L. Ellis	2751

---The MAILING DATE of this communication appears on the cover sheet beneath the correspondence address---

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, such period shall, by default, expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).

Status

☒ Responsive to communication(s) filed on 8/10/00.

☐ This action is **FINAL.**

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

☒ Claim(s) 1-12 is/are pending in the application.

Of the above claim(s) _____ is/are withdrawn from consideration.

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) 1-12 is/are rejected.

☐ Claim(s) _____ is/are objected to.

☐ Claim(s) _____ are subject to restriction or election requirement.

Application Papers

☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The proposed drawing correction, filed on _____ is ☐ approved ☐ disapproved.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119 (a)-(d)

☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 11 9(a)-(d).

☐ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number) _____.

☐ received in this national stage application from the International Bureau (PCT Rule 1 7.2(a)).

*Certified copies not received: _____.

Attachment(s)

☐ Information Disclosure Statement(s), PTO-1449, Paper No(s). _____

☐ Interview Summary, PTO-413

☐ Notice of Reference(s) Cited, PTO-892

☐ Notice of Informal Patent Application, PTO-152

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Other _____

Office Action Summary

U. S. Patent and Trademark Office
PTO-326 (Rev. 9-97)

Part of Paper No. 14

*U.S. GPO: 1998-454-457/97505

Detailed Action

1. Claims 1-12 are presented for examination. New claims 9-12 have been added by Amendment. This Office Action is in response to the Amendment filed 8/10/00.

Declaration Under 37 CFR § 1.131

2. The declaration filed on 8/10/00 under 37 CFR § 1.131 has been considered but is ineffective to overcome the Jacobson reference.

3. The evidence submitted is insufficient to establish diligence from a date prior to the effective date of the Jacobson reference to a subsequent reduction to practice or to the filing of the application.

Applicant has not provided evidence of diligence as required. (see MPEP § 715.07(a)) As stated in MPEP § 715.07(a), "... it is not enough merely to allege that applicant or patent owner had been diligent. ... Rather, applicant must show evidence of facts establishing diligence." (1st Paragraph) Applicant's declaration on page 2, item 4, merely alleges diligence without providing evidence to support these allegations. Applicant should submit evidence showing diligence which will remove the Jacobson reference as prior art.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the first paragraph of 35 USC § 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

The specification is objected to under 35 USC § 112, first paragraph, as the specification as originally filed, does not provide support for the invention as is now claimed.

The specification does not teach sorting SDRAM components based upon which of the data outputs are defective (see Claim 10) or providing sorted SDRAM components with

predetermined numbers and arrangements of defective SDRAM data outputs for assembly (see Claim 11).

5. Claims 10 and 11 are rejected under 35 USC § 112, first paragraph, for the reasons set forth in the objection to the specification.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 USC § 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

7. Claims 1, 2, 9, and 12 are rejected under 35 USC 102(e) as being anticipated by Jacobson, U.S. Patent 5,920,513.

A) As to claims 1 and 9, Jacobson discloses the invention as claimed. There is a method of accessing a memory module (Fig 4) comprising the acts of presenting a row address to the address inputs (see Col 3 Lines 2-12) of each of a plurality of partially defective SDRAM components (see Fig 4 & 5, Col 3 Lines 35-41, Col 4 Lines 25-42, and Col 5 Lines 4-45) that have at least one unreliable data output (Col 3 Lines 12-27, Col 5 Lines 4-7 & 33-45) and that also have a plurality of valid data outputs, wherein the valid data outputs are data outputs that provide reliable and accurate data (Col 3 Lines 12-27, Col 5 Lines 4-7 & 33-45), and presenting a column address to the address inputs of each SDRAM component (Col 3 Lines 2-12), aggregating the valid data outputs of each of the SDRAM components to provide a data path (see Fig 5 and Col 4 Lines 26-67), and communicating the data from the valid data outputs to a microprocessor (Col 4 Lines 7-8; one of ordinary skill in the art would recognize that a

computer would include some sort of processing device, i.e. a microprocessor).

The memory taught by Jacobson would be connected to a microprocessor as claimed in claim 9.

B) As to claim 2, the act of presenting a row address does include the act of presenting a row address to the address inputs of partially defective SDRAM components (see Col 4 Line 67 to Col 5 Line 3), where for each of these SDRAM components, the plurality of valid data outputs are the same for each addressable memory location within that component so that the same portion of each addressable memory location within any given SDRAM component consistently provides valid and accurate data (see Col 3 Lines 13-27).

C) As to claim 12, Jacobson teaches testing the SDRAM components prior to "assembling" them on a memory module (see Fig 6).

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 USC § 103 which forms the basis for all obviousness rejections set forth in this Office action:

> A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
>
> Subject matter developed by another person, which qualifies as prior art only under subsection (f) or (g) of section 102 of this title, shall not preclude patentability under this section where the subject matter and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person.

9. Claims 3 and 4 are rejected under 35 USC § 103 as being unpatentable over Jacobson, U.S. Patent 5,920,513, in view of Dell et al., U.S. Patent 5,896,346.

A) As to claims 3 and 4, Jacobson discloses the invention substantially as claimed. However, Jacobson does not disclose that the SDRAM components are mounted on

SIMMs or DIMMs.

Dell et al. teaches that it was common for SDRAM components to come mounted on SIMMs or DIMMs (see Col 1 Lines 38-47). SIMMs and DIMMs were common memory modules in the art at the time of the invention. They provide a convenient and standardized packaging of the SDRAM components which could be easily inserted into and removed from a computer system motherboard.

Accordingly, it would have been obvious to one having ordinary skill in the art at the time of the invention to package the SDRAM components of Jacobson in a SIMM or DIMM module as these were common memory module designs in the industry.

10. Claims 5 and 6 are rejected under 35 USC § 103 as being unpatentable over Jacobson, U.S. Patent 5,920,513, in view of Schaefer, U.S. Patent 5,636,173.

A) As to claim 5, Jacobson discloses the invention substantially as claimed. There is a method of accessing memory cells in a memory module (Fig 4) having a plurality of SDRAM components (see Col 3 Lines 35-42), each of the SDRAM components having a plurality of address inputs (see Fig 5 and Col 4 Line 67 to Col 5 Line 3), the method comprising the acts of presenting a row address to the address inputs of each SDRAM component (see Col 3 Lines 2-12), presenting a column address to the address inputs of each SDRAM component (Col 3 Lines 2-12), wherein each of the SDRAM components is partially defective (see Fig 4 & 5, Col 3 Lines 35-41, Col 4 Lines 25-42, and Col 5 Lines 4-45) such that each SDRAM components has at least one unreliable data output (Col 3 Lines 12-27, Col 5 Lines 4-7 & 33-45) and also a plurality of valid data outputs that provide reliable and accurate data (Col 3 Lines 12-27, Col 5 Lines 4-7 & 33-45), aggregating the valid data outputs of each of the SDRAM components to provide a data path (see Fig 5 and Col 4 Lines 26-67), and communicating the data from the valid data outputs from each of the SDRAM components to a microprocessor

(Col 4 Lines 7-8; one of ordinary skill in the art would recognize that a computer would include some sort of processing device, i.e. a microprocessor). However, Jacobson does not disclose that each of the SDRAM components further comprises a plurality of banks of memory that are addressable by address inputs and that the method comprises selecting one of the plurality of banks within each SDRAM component by presenting at least one selection bit at the address inputs when the row address is presented to the address inputs.

Schaefer teaches SDRAM components that comprise a plurality of banks of memory that are addressable by address inputs and that the selecting of one of the plurality of banks within the SDRAM component is performed by presenting at least one selection bit at the address inputs when the row address is presented to the address inputs (see Col 1 Lines 23-42 and Col 4 Lines 22-36). The advantage to using SDRAM with banks is that it allows interleaving between the two or more banks to hide the precharging time.

Accordingly, it would have been obvious to one having ordinary skill in the art at the time the invention was made to utilize SDRAM components that include a plurality of banks of memory that are addressable by address inputs and that the selecting of one of the plurality of banks within each SDRAM component is performed by presenting at least one selection bit at the address inputs when the row address is presented to the address inputs as taught by Schaefer for the advantage that using SDRAM components with multiple banks allows the precharging time to be hidden thus increasing the speed of the memory.

B) As to claim 6, the act of presenting a row address does include the act of presenting a row address to the address inputs of partially defective SDRAM components (see Col 4 Line 67 to Col 5 Line 3), where for each of these SDRAM components, the plurality of valid data outputs are the same for each addressable

memory location within that component so that the same portion of each addressable memory location within any given SDRAM component consistently provides valid and accurate data (see Col 3 Lines 13-27).

11. Claims 7 and 8 are rejected under 35 USC § 103 as being unpatentable over Jacobson, U.S. Patent 5,920,513, and Schaefer, U.S. Patent 5,636,173, and in further view of Dell et al., U.S. Patent 5,896,346.

A) As to claims 7 and 8, Jacobson discloses the invention substantially as claimed. However, Jacobson does not disclose that the SDRAM components are mounted on SIMMs or DIMMs.

Dell et al. teaches that it was common for SDRAM components to come mounted on SIMMs or DIMMs (see Col 1 Lines 38-47). SIMMs and DIMMs were common memory modules in the art at the time of the invention. They provide a convenient and standardized packaging of the SDRAM components which could be easily inserted into and removed from a computer system motherboard.

Accordingly, it would have been obvious to one having ordinary skill in the art at the time of the invention to package the SDRAM components of Jacobson in a SIMM or DIMM module as these were common memory module designs in the industry.

Conclusion

12. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) days from the mail date of this letter. Failure to respond within the period for response will result in **ABANDONMENT** of the application (see 35 USC 133, MPEP 710.02, 710.02(b)).

13. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Kevin Ellis whose telephone number is (703) 305-9659. The

Examiner can normally be reached on the weekdays from 6:00am to 2:30pm.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Eddie Chan, can be reached on (703) 305-9712.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks
Washington, D.C. 20231

or faxed to:
(703)308-9051, (for formal communications intended for entry)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-3900.

Kevin L. Ellis
Patent Examiner
September 1, 2000

Kevin L. Ellis

GAU: 2751
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SEP 13 2000
TC 2700 MAIL ROOM

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:
RICHARD WEBER and COREY LARSEN

Serial No.: 09/035,739

Filed: March 5, 1998

For:

METHOD FOR RECOVERY OF USEFUL AREAS OF PARTIALLY DEFECTIVE SYNCHRONOUS MEMORY COMPONENTS

§ Group Art Unit: 2751
§ Examiner: Kevin Ellis
§ Atty. Docket: 97.0003101

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TC 2700 MAIL ROOM
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2751
9-15-00

TRANSMITTAL LETTER

Assistant Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

Certificate of Mailing (37 C.F.R. 1.8)
I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail, postage prepaid, in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231 on the date below.
9-6-00 Signature
Date

Enclosed for filing in the referenced case, please find the following document(s):

Supplemental Information Disclosure Statement
Form PTO-1449

Should the submission of the above referenced document(s) require any fees which are not otherwise provided for, the Commissioner is authorized to charge such fees, to Micron Electronics, Deposit Account 500659. This transmittal is being submitted in duplicate.

Respectfully submitted,

Paul A. Revis
Registration No. 45,040
Micron Electronics, Inc.
900 East Karcher Road
Nampa, ID 83687

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:
RICHARD WEBER and COREY LARSEN

Serial No.: 09/035,739

Filed: March 5, 1998

For:

METHOD FOR RECOVERY OF USEFUL AREAS OF PARTIALLY DEFECTIVE SYNCHRONOUS MEMORY COMPONENTS

§ Group Art Unit: 2751

§ Examiner: Kevin Ellis

§ Atty. Docket: 97.00031.01

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Washington, D.C. 20231

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METHOD FOR RECOVERY OF USEFUL AREAS OF PARTIALLY DEFECTIVE SYNCHRONOUS MEMORY COMPONENTS

§ Group Art Unit: 2751
§ Examiner: *Kevin Ellis*
§ Atty. Docket: 97.00031.01
§ Paper No.

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

In compliance with the duty of disclosure under 37 C.F.R. § 1.56, Applicant[s] respectfully request[s] that this Supplemental Information Disclosure Statement be entered and that the references listed on the attached Form PTO-1449 be considered by the Examiner and made of record. Copies of the listed references are enclosed for the convenience of the Examiner.

In accordance with 37 C.F.R. § 1.97(b), this Supplemental Information Disclosure Statement is not to be construed as a representation that a search has been made or that no other possible material information as defined in 37 C.F.R. § 1.56(a) exists.

The following references are submitted for the Examiner's review:

U.S. Patents

U.S. Patent No.	Issue Date	Inventor
3,800,294	3/26/74	Lawlor
4,376,300	3/8/83	Tsang
4,450,560	5/22/84	Conner

4,479,214	10/23/84	Ryan
4,646,299	2/24/87	Schinabeck
4,807,191	2/21/89	Flannagan
4,876,685	10/24/89	Rich
4,881,200	11/14/89	Urai
4,908,798	3/13/90	Urai
4,918,662	4/17/90	Kondo
4,935,899	6/19/90	Morigami
5,060,197	10/22/91	Park & Kim
5,124,948	6/23/92	Takizawa
5,134,584	7/28/92	Boler & Lukanc
5,200,959	4/6/93	Gross & Norman
5,233,614	8/3/93	Singh
5,315,552	5/24/94	Yoneda
5,327,380	7/5/94	Kersh, et al.
5,331,188	7/19/94	Acovic, et al.
5,337,277	8/9/94	Jang
5,371,866	12/6/94	Cady
5,379,415	1/3/95	Papenberg, et al.
5,390,129	2/14/95	Rhodes
5,400,263	3/21/95	Rohrbaugh, et al.
5,400,342	3/21/95	Matsumura, et al.
5,410,545	4/25/95	Porter & Myers
5,424,989	6/13/95	Hagiwara & Sakihama
5,434,792	7/18/95	Saka, et al.
5,469,390	11/21/95	Sasaki & Tanaka
5,475,695	12/12/95	Caywood, et al.
5,491,664	2/13/96	Phelan
5,497,381	3/5/96	O'Donoghue & Cheek
5,502,333	3/26/96	Bertin, et al.
5,535,328	7/9/96	Harari, et al.
5,538,115	7/23/96	Koch
5,544,106	8/6/96	Koike
5,548,553	8/20/96	Cooper & Leary
5,553,231	9/3/96	Papenberg, et al.
5,588,115	12/24/96	Augarten
5,600,258	2/4/97	Graham, et al.
5,602,987	2/11/97	Harari
5,631,868	5/20/97	Termullo, et al.
5,633,826	5/27/97	Tsukada
5,654,204	8/5/97	Anderson
5,717,694	2/10/98	Ohsawa
5,734,621	3/31/98	Ito
5,745,673	4/28/98	Di Zenzo & Grimani
5,754,753	5/19/98	Smelser
5,758,056	5/26/98	Barr
5,841,710	11/24/98	Larsen
5,862,314	1/19/99	Jeddeloh
5,913,020	6/15/99	Rohwer
5,920,512	7/6/99	Larsen
5,963,463	10/5/99	Rondeau & Magee
5,966,724	10/12/99	Ryan
5,974,564	10/26/99	Jeddeloh
5,991,215	11/23/99	Brunelle

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5,995,409	11/30/99	Holland
6,009,536	12/28/99	Rohwer

Other References:

"MindShare, Inc., Anderson and Shanley," Pentium ™ Processor System Architecture, Second Edition, PC System Architecture Series: 126-132, 221-234, 1995.
09/035,629 – "Recovery of Partially Defective Synchronous Memory Components" filed 3/5/98
08/903,819 – "System For Remapping Defective Memory Bit Sets" filed 7/31/97
09/217,781 – "Use of Partially Dysfunctional Memory Devices" filed 12/21/98
09/067,347 – "A System For Decoding Addresses For A Defective Memory Array" filed 4/28/98
09/067,467 – "A Method For Decoding Addresses For A Defective Memory Array" filed 4/28/98
09/519,641 – "Method and Apparatus For Recovery of Useful Areas of Partially Defective Direct Rambus Rimm Components" filed 3/6/00
09/548,826 – "Method and Apparatus For Storing Failing Part Locations In A Module" – filed 4/13/00

Applicant understands that no fee or certification is required for the submission and consideration of this information at this time. If the fee of 37 C.F.R. § 1.17(p) is required at this time, the Commissioner is authorized to charge such fee to Deposit Account No. 500659

****

A Form PTO-1449 is enclosed herewith.

Respectfully submitted,

Date: 9/6/10

Paul A. Revis
Reg. No. 45,040
Micron Electronics, Inc.
900 East Karcher Road
Nampa, ID 83687
(208) 898-1316
AGENT FOR APPLICANT

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SEP 11

PATENT & TRADEMARK OFFICE

Sheet: 1 of: 3

PTO-1449 (Rev. 7-80) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	Atty Docket No: 97.00031.01	Serial No: 09/035,739
INFORMATION DISCLOSURE STATEMENT BY APPLICANT	Applicant: Richard Weber and Corey Larsen	
(37 CFR 1.98(b)) *(use several sheets if necessary)*	Filing Date: March 5, 1998	Group: 2751

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U.S. PATENT DOCUMENTS

Examiner Initial		Document Number	Date	Name	Class	Subclass	
KR	AA	3,800,294	3/26/74	Lawlor	340	172.5	
KR	AB	4,376,300	3/8/83	Tsang	365	200	
KR	AC	4,450,560	5/22/84	Conner	371	25	
KR	AD	4,479,214	10/23/84	Ryan	371	11	
KR	AE	4,646,299	2/24/87	Schinabeck & Murdock	371	20	
KR	AF	4,807,191	2/21/89	Flannagan	365	189	
KR	AG	4,876,685	10/24/89	Rich	371	21.6	
KR	AH	4,881,200	11/14/89	Urai	365	189.04	
KR	AI	4,908,798	3/13/90	Urai	365	230.03	
KR	AJ	4,918,662	4/17/90	Kondo	365	210	
KR	AK	4,935,899	6/19/90	Morigami	365	200	
KR	AL	5,060,197	10/22/91	Park & Kim	365	200	
KR	AM	5,124,948	6/23/92	Takizawa, et al.	365	200	
KR	AN	5,134,584	7/28/92	Boler & Lukanc	365	200	
KR	AO	5,200,959	4/6/93	Gross & Norman	371	21.6	
KR	AP	5,233,614	8/3/93	Singh	371	21.6	
KR	AQ	5,315,552	5/24/94	Yoneda	365	200	
KR	AR	5,327,380	7/5/94	Kersh & Norwood	365	195	
KR	AS	5,331,188	7/19/94	Acovic, et al.	257	298	
KR	AT	5,337,277	8/9/94	Jang	365	200	
KR	AU	5,371,866	12/6/94	Cady	395	400	
KR	AV	5,379,415	1/3/95	Papenberg, et al.	395	575	
KR	AW	5,390,129	2/14/95	Rhodes	364	480	

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FOREIGN PATENT DOCUMENTS

Examiner Initial		Document Number	Date	Country	Class	Subclass	Translation Yes	Translation No
	AX						☐	☐

OTHER ART (including author, title, date, pertinent pages, etc.)

Initial			
KR	AY		"MindShare, Inc., Anderson and Shanley," Pentium™ Processor System Architecture, Second Edition, PC System Architecture Series: 126-132, 221-234, 1995.
	~~AZ~~		~~09/035,629 – "Recovery of Partially Defective Synchronous Memory Components" filed 3/5/98~~
	~~BA~~		~~08/903,819 – "System For Remapping Defective Memory Bit Sets" filed 7/31/97~~
	~~BB~~		~~09/217,781 – "Use of Partially Dysfunctional Memory Devices" filed 12/21/98~~
	~~BC~~		~~09/067,347 – "A System For Decoding Addresses For A Defective Memory Array" filed 4/28/98~~

Examiner: Kevin L. Ellis	Date Considered: 4/20/01

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication with applicant.

SEP 11 2000 U.S. PATENT & TRADEMARK OFFICE

FORM: PTO-1449 (REV: 7-80)	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	Atty Docket No: 97.00031.01	Serial No: 09/035,739
		Applicant: Richard Weber and Corey Larsen	
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U.S. PATENT DOCUMENTS

Examiner Initial		Document Number	Date	Name	Class	Subclass	
KR	BD	5,400,263	3/21/95	Rohrbaugh, et al.	364	490	
KR	BE	5,400,342	3/21/95	Matsumura, et al.	371	21.2	
KR	BF	5,410,545	4/25/95	Porter & Myers	371	21.6	
KR	BG	5,424,989	6/13/95	Hagiwara & Sakihama	365	201	
KR	BH	5,434,792	7/18/95	Saka, et al.	364	468	
KR	BI	5,469,390	11/21/95	Sasaki & Tanaka	365	200	
KR	BJ	5,475,695	12/12/95	Caywood, et al.	371	27	
KR	BK	5,491,664	2/13/96	Phelan	365	200	
KR	BL	5,497,381	3/5/96	O'Donoghue & Cheek	371	28	
KR	BM	5,502,333	3/26/96	Bertin, et al.	257	685	
KR	BN	5,535,328	7/9/96	Harari, et al.	395	182.05	
KR	BO	5,538,115	7/23/96	Koch	188	299	
KR	BP	5,544,106	8/6/96	Koike	365	200	
KR	BQ	5,548,553	8/20/96	Cooper & Leary	365	200	
KR	BR	5,553,231	9/3/96	Papenberg, et al.	395	182.03	
KR	BS	5,588,115	12/24/96	Augarten	395	183.05	
KR	BT	5,600,258	2/4/97	Graham, et al.	324	758	
KR	BU	5,602,987	2/11/97	Harari, et al.	395	182.06	
KR	BV	5,631,868	5/20/97	Termullo, et al.	365	200	
KR	BW	5,633,826	5/27/97	Tsukada	365	200	
KR	BX	5,654,204	8/5/97	Anderson	438	15	
KE	BY	5,717,694	2/10/98	Ohsawa	371	5.1	
KE	BZ	5,734,621	3/21/98	Ito	365	230.03	

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FOREIGN PATENT DOCUMENTS

Examiner Initial		Document Number	Date	Country	Class	Subclass	Translation Yes	Translation No
	CA						☐	☐

Initial			OTHER ART (including author, title, date, pertinent pages, etc.)
	~~CB~~		~~09/067,467 – "A Method For Decoding Addresses For A Defective Memory Array" filed 4/28/98~~
	~~CC~~		~~09/519,641 – "Method And Apparatus For Recovery of Useful Areas of Partially Defective Direct Rambus RIMM Components" filed 3/6/00~~
	~~CD~~		~~09/548,826 – "Method and Apparatus For Storing Failing Part Locations In a Module" filed 4/13/00~~

Examiner: Kevin L. Ellis	Date Considered: 4/20/01

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PATENT & TRADEMARK OFFICE

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		Applicant: Richard Weber and Corey Larsen	
		Filing Date: March 5, 1998	Group: 2751

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(37 CFR 1.98(b)) *(use several sheets if necessary)*

U.S. PATENT DOCUMENTS

Examiner Initial		Document Number	Date	Name	Class	Subclass	
UK	CE	5,745,673	4/28/98	Di Zenzo & Grimani	395	182.05	
UK	CF	5,754,753	5/19/98	Smelser	395	182.06	
UK	CG	5,758,056	5/26/98	Barr	395	182.05	
UK	CH	5,841,710	11/24/98	Larsen	365	200	
UK	CI	5,862,314	1/19/99	Jeddeloh	395	182.06	
UK	CJ	5,913,020	6/15/99	Rohwer	395	182.06	
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UK	CL	5,963,463	10/5/99	Rondeau & Magee	365	52	
UK	CM	5,966,724	10/12/99	Ryan	711	105	
UK	CN	5,974,564	10/26/99	Jeddeloh	714	8	
UK	CO	5,991,215	11/23/99	Brunelle	365	201	
UK	CP	5,995,409	11/30/99	Holland	365	149	
UK	CQ	6,009,536	12/28/99	Rohwer	714	8	

FOREIGN PATENT DOCUMENTS

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	CC		
	CD		

Examiner: Kevin L. Ellis	Date Considered: 4/20/01

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Examiner: Kevin L. Ellis	Date Considered: 4/20/01

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication with applicant.

FORM: PTO-1449 (REV: 7-80) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	Atty Docket No: 97.00031.01	Serial No: 09/035,739
INFORMATION DISCLOSURE STATEMENT BY APPLICANT	Applicant: **Richard Weber and Corey Larsen**	
(37 CFR 1.98(b)) *(use several sheets if necessary)*	Filing Date: **March 5, 1998**	Group: **2751**

U.S. PATENT DOCUMENTS

Examiner Initial		Document Number	Date	Name	Class	Subclass	
NR	BD	5,400,263	3/21/95	Rohrbaugh, et al.	364	490	
NR	BE	5,400,342	3/21/95	Matsumura, et al.	371	21.2	
NR	BF	5,410,545	4/25/95	Porter & Myers	371	21.6	
NR	BG	5,424,989	6/13/95	Hagiwara & Sakihama	365	201	
NR	BH	5,434,792	7/18/95	Saka, et al.	364	468	
NR	BI	5,469,390	11/21/95	Sasaki & Tanaka	365	200	
NR	BJ	5,475,695	12/12/95	Caywood, et al.	371	27	
NR	BK	5,491,664	2/13/96	Phelan	365	200	
NR	BL	5,497,381	3/5/96	O'Donoghue & Cheek	371	28	
NR	BM	5,502,333	3/26/96	Bertin, et al.	257	685	
NR	BN	5,535,328	7/9/96	Harari, et al.	395	182.05	
NR	BO	5,538,115	7/23/96	Koch	188	299	
NR	BP	5,544,106	8/6/96	Koike	365	200	
NR	BQ	5,548,553	8/20/96	Cooper & Leary	365	200	
NR	BR	5,553,231	9/3/96	Papenberg, et al.	395	182.03	
NR	BS	5,588,115	12/24/96	Augarten	395	183.05	
NR	BT	5,600,258	2/4/97	Graham, et al.	324	758	
NR	BU	5,602,987	2/11/97	Harari, et al.	395	182.06	
NR	BV	5,631,868	5/20/97	Termullo, et al.	365	200	
NR	BW	5,633,826	5/27/97	Tsukada	365	200	
NR	BX	5,654,204	8/5/97	Anderson	438	15	
KE	BY	5,717,694	2/10/98	Ohsawa	371	5.1	
KE	BZ	5,734,621	3/21/98	Ito	365	230.03	

FOREIGN PATENT DOCUMENTS

Examiner Initial		Document Number	Date	Country	Class	Subclass	Translation Yes	Translation No
	CA						☐	☐

Initial			**OTHER ART** (including author, title, date, pertinent pages, etc.)
	CB		~~09/067,467 – "A Method For Decoding Addresses For A Defective Memory Array" filed 4/28/98~~
	CC		~~09/519,641 – "Method And Apparatus For Recovery of Useful Areas of Partially Defective Direct Rambus RIMM Components" filed 3/6/00~~
	CD		~~09/548,826 – "Method and Apparatus For Storing Failing Part Locations In a Module" filed 4/13/00~~

Examiner: Kevin L. Bill	Date Considered: 4/20/01

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication with applicant.

FORM: PTO-1449 (REV: 7-80)	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	Atty Docket No: 97.00031.01	Serial No: 09/035,739
		Applicant: Richard Weber and Corey Larsen	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (37 CFR 1.98(b))	*(use several sheets if necessary)*	Filing Date: March 5, 1998	Group: 2751

U.S. PATENT DOCUMENTS

Examiner Initial		Document Number	Date	Name	Class	Subclass	
NK	CE	5,745,673	4/28/98	Di Zenzo & Grimani	395	182.05	
NK	CF	5,754,753	5/19/98	Smelser	395	182.06	
NK	CG	5,758,056	5/26/98	Barr	395	182.05	
NK	CH	5,841,710	11/24/98	Larsen	365	200	
NK	CI	5,862,314	1/19/99	Jeddeloh	395	182.06	
NK	CJ	5,913,020	6/15/99	Rohwer	395	182.06	
NK	CK	5,920,512	7/6/99	Larsen	365	200	
NK	CL	5,963,463	10/5/99	Rondeau & Magee	365	52	
NK	CM	5,966,724	10/12/99	Ryan	711	105	
NK	CN	5,974,564	10/26/99	Jeddeloh	714	8	
NK	CO	5,991,215	11/23/99	Brunelle	365	201	
NK	CP	5,995,409	11/30/99	Holland	365	149	
NK	CQ	6,009,536	12/28/99	Rohwer	714	8	

FOREIGN PATENT DOCUMENTS

Examiner Initial		Document Number	Date	Country	Class	Subclass	Translation Yes	Translation No
	CA						☐	☐

Initial			**OTHER ART** (including author, title, date, pertinent pages, etc.)
	CB		
	CC		
	CD		

Examiner: Nevin L. Ellis	Date Considered: 4/20/01

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication with applicant.

~~2751~~ 2185

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:
Richard Weber and Corey Larsen

Serial No.: 09/035,739

Filed: March 5, 1998

For:

METHOD FOR RECOVERY OF USEFUL AREAS OF PARTIALLY DEFECTIVE SYNCHRONOUS MEMORY COMPONENTS

§ Group Art Unit: 2751

§ Examiner: Kevin Ellis

§ Atty. Docket: 97.00031.01

RECEIVED
FEB 1 4 2001
Technology Center 2100

TRANSMITTAL LETTER

"Certificate of Mailing (37 C.F.R. § 1.8)"
I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail, postage prepaid, in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231 on the date below.
2-5-01 Signature

Assistant Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

Enclosed for filing in the referenced case, please find the following document(s):

Response to Third Office Action
Declaration of Richard Weber and Corey Larsen under 37 C.F.R. §1.131
Petition For Extension of Time

Should the submission of the above referenced document(s) require any fees which are not otherwise provided for, the Commissioner is authorized to charge such fees, to Micron Electronics, Deposit Account #500659. This transmittal is being submitted in duplicate.

Respectfully submitted,

Paul A. Revis
Reg #45,040
Micron Electronics, Inc.
900 East Karcher Road
Nampa, ID 83687

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventors:	Richard Weber and Corey Larsen
Application No.:	09/035,739
Filed:	March 5, 1998
Title:	METHOD FOR RECOVERY OF USEFUL AREAS OF PARTIALLY DEFECTIVE SYNCHRONOUS MEMORY COMPONENTS

Examiner:	Kevin Ellis
Art Unit:	2751
Atty. Docket No.:	97.00031.01

Assistant Commissioner for Patents
Washington, DC 20231

RESPONSE TO THIRD OFFICE ACTION

Dear Assistant Commissioner:

This paper responds to the third Office action in this patent application mailed September 7, 2000. Please consider the application in light of the following remarks.

REMARKS

Claims 1 – 12 are pending in the present application.

In the Office action mailed on September 7, 2000, the examiner rejected claims 1, 9, and 12 under 35 U.S.C. §102(e) as anticipated over U.S. Pat. No. 5,920,513 to Jacobson ("Jacobson"). Claims 3 and 4 were rejected under 35 U.S.C. §103 as being unpatentable over Jacobson in view of U.S. Pat. No. 5,896,346 to Dell et al. ("Dell"). Claims 5 and 6 were rejected under 35 U.S.C. §103 as being unpatentable over Jacobson in view of U.S. Pat. No. 5,636,173 to Schaefer, ("Schaefer"). Claims 7 and 8 were rejected under 35 U.S.C. §103 as being unpatentable over Jacobson and Schaefer and

further in view of Dell. Claims 10 and 11 were rejected under 35 U.S.C. §112, first paragraph.

Reconsideration is respectfully requested.

The Jacobson Reference

In the prior amendment and response by the applicant, a declaration under 37 C.F.R. §1.131 swearing back of Jacobson was submitted. The effectiveness of the declaration was found lacking to establish diligence from a date prior to the effective date of the Jacobson reference to a subsequent reduction to practice or to the filing of the application. A substitute declaration with further evidence establishing diligence from a date prior to the effective date of the Jacobson reference to the filing of the application has been provided herewith. Consequently, applicant respectfully submits that claims 1 – 9 and 12 are patentable over the art cited.

Claims 10 and 11 were rejected under 35 U.S.C. §112, first paragraph. Specifically, the reason cited for rejecting claim 10 was that "[t]he specification does not teach sorting SDRAM components based upon which of the data outputs are defective." However, the applicant respectfully points out that the specification does point to at least three embodiments of the invention where multiple partially defective SDRAM components are combined in predetermined arrangements. See Specification, each of the three respective embodiments sections beginning at p. 6, ln. 3; p. 6, ln. 19; and p. 7, ln. 10. For each of these embodiments, the specification teaches sorting out select components based on which of the data outputs of the respective SDRAM components are defective. For example, in the first embodiment listed, it is stated that "[t]he SDRAM components 54, 55, 57, and 58 each have four defective or unused DQ outputs … components 56 and 59 have eight unreliable or unused DQ outputs…." p. 6, lns. 7 – 10. Therefore, based on which of the data outputs are defective, SDRAM components are sorted and combined to form operative memory modules. Alternative sortings and combinations are illustrated in the other embodiments listed. Absent sorting, no memory module could be logically assembled, much less the variety of memory modules described in the specification. The application teaches, by numerous examples, sorting based on which of the data outputs are defective. Based on the prior teaching in the art of record, and if not for the teaching and examples of the application, a memory module

attempting to provide the utility of the modules of the present invention would merely be a combination of randomly arranged components. Such a random combination simply would not consistently work with partially defective components. The specification clearly illustrates and teaches sorting based on which of the data outputs are defective. Consequently, the applicant respectfully requests that the §112, paragraph 1 rejection of claim 10 be removed.

The reason cited for rejecting claim 11 was that "providing sorted SDRAM components with predetermined numbers and arrangements of defective SDRAM data outputs for assembly" is not taught in the specification. Again, the applicant respectfully points to the example embodiments provided in the specification. Each of the embodiments clearly shows a predetermined number and arrangement of defective SDRAM components that may be assembled into complementary memory modules. Absent providing components with predetermined numbers and arrangement of defective SDRAM data output for assembly into modules, the embodiments clearly presented in the specification could not be made. The fact that general, as well as specific, example embodiments of effective memory modules have been provided proves that the specification clearly teaches providing sorted SDRAM components with predetermined numbers and arrangements of defective SDRAM data outputs for assembly. Therefore, the applicant respectfully requests that the §112, paragraph 1 rejection of claim 11 be removed.

CONCLUSION

In light of the foregoing remarks, applicant respectfully requests that the outstanding rejections be removed. If the examiner wishes to discuss the above remarks, the examiner is encouraged to contact the undersigned. Additionally, if the examiner notices any informalities in the application, he is also encouraged to contact the undersigned to expediently correct any such informalities. The applicant has attempted to address all issues raised in the previous Office action. If the examiner believes that there are issues that have not been addressed, the examiner is invited to contact the undersigned.

Respectfully submitted,

Paul A. Revis
Attorney for Applicant
Registration No. 45,040

Enclosures:
Transmittal Letter (2 copies)
Declaration of Inventors
Postcard

Micron Electronics, Inc.
Legal Department
900 East Karcher Road
Nampa, ID 83687
(208)898-1316 – Voice
(208)898-7211 – Fax

#19

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventors:	Richard Weber and Corey Larsen
Application No.:	09/035,739
Filed:	March 5, 1998
Title:	METHOD FOR RECOVERY OF USEFUL AREAS OF PARTIALLY DEFECTIVE SYNCHRONOUS MEMORY COMPONENTS

Examiner:	Kevin Ellis
Art Unit:	2751
Atty. Docket No.:	97.00031.01

Assistant Commissioner for Patents
2011 Jefferson Davis Highway
Washington, DC 20231

DECLARATION OF RICHARD WEBER AND COREY LARSEN UNDER 37 C.F.R. § 1.131

Dear Assistant Commissioner for Patents:

We, Richard Weber and Corey Larsen, declare and state that:

1. We are the inventors of the invention described and claimed in U.S. Patent Application No. 09/035,739, filed March 5, 1998. This declaration establishes invention in this country before August 22, 1997, and thus before the U.S. filing date of U.S. Patent No. 5,920,513 issued to Jacobson.

2. Before August 22, 1997, we conceived the invention currently presented in claims 1-12 of the above-captioned patent application. Our conception of the invention is corroborated by the Micron Electronics, Inc. drawing entitled "2MX64 SDRAM DIMM (DQ4 – DQ7 BAD)," dated March 6, 1997, attached hereto as Exhibit A.

3. As shown in Exhibit A, we did conceive a method of accessing a memory module, and particularly the memory cells of the memory module. Exhibit A illustrates a structure through which a row address may be presented to a plurality of partially defective SDRAM components that have unreliable and reliable data outputs, and a column address may be presented to the SDRAM address inputs. Further, a particular bank may be selected. Aggregation of the valid data outputs of each of the SDRAM components to provide a data path is also shown. Data may then be communicated from the valid data outputs to a microprocessor. In another embodiment, the invention includes a method of enabling data access between a memory module having data outputs and a microprocessor. The illustrated memory module may result from determining which SDRAM data outputs of a group of SDRAM components are defective, and assembling a set of SDRAM components from the group of SDRAM components, wherein at least one of the SDRAM components has defective SDRAM data outputs, such that each memory module data output is connected to an operative SDRAM data output. A clock signal may then be processed to synchronously apply operating signals to the memory module and the microprocessor to effect data access between the memory module and the microprocessor.

4. After conceiving this invention, we proceeded diligently by preparing schematic drawings, accomplishing testing, disclosing the invention to our employer, working through an initial invention review procedure, and participating in the preparation of the present patent application. Diligence, without unusual or undue delay, from prior to August 22, 1997 to constructive reduction to practice is shown by the following:

(1) June 13, 1997 – letter from Micron Electronics Patent Secretary to inventors requesting review of a second draft application (see Exhibit B);

(2) August 20, 1997 – letter from Micron Electronics Patent Secretary transmitting application changes to outside counsel, Dorsey & Whitney (see Exhibit C);

(3) October 2-6, 1997 – email chain between Micron Electronics Patent Secretary and Dorsey & Whitney requesting and reporting status of subject patent application (see Exhibit D, other unrelated application information has been redacted from this email);

(4) October 9, 1997 – letter from Dorsey & Whitney to Micron Electronics transmitting a third draft application (see Exhibit E);

(5) October 13, 1997 – letter from Micron Electronics Patent Secretary to inventors requesting review of the third draft application (see Exhibit F);

(6) October 16, 1997 – letter from Dorsey & Whitney to Micron Electronics transmitting a fourth draft application (see Exhibit G);

(7) October 24, 1997 – letter from Micron Electronics Patent Secretary to inventors requesting review of the fourth draft application (see Exhibit H);

(8) January 27, 1998 – letter from Dorsey & Whitney to Micron Electronics transmitting a fifth draft application (see Exhibit I);

(9) January 30, 1998 – letter from Micron Electronics Patent Secretary to inventor requesting review of fifth [mislabeled as third] draft application (see Exhibit J); and

(10) February 20, 1998 – letter from Micron Electronics Patent Secretary to Dorsey & Whitney requesting expedited, missing parts filing of the fifth [mislabeled as third] draft application once changes as marked were incorporated (see Exhibit K).

On March 5, 1998, we constructively reduced this invention to practice with the filing of the present application.

5. We further declare that all statements herein made of our own knowledge are true, and that all statements made on information or belief are believed to be true; and further, that the statements are made with the knowledge that the making of willful or false statements or the like is punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and may jeopardize the validity of any patent issuing from this patent application.

Dated this 5 day of February, 2001.

Richard Weber

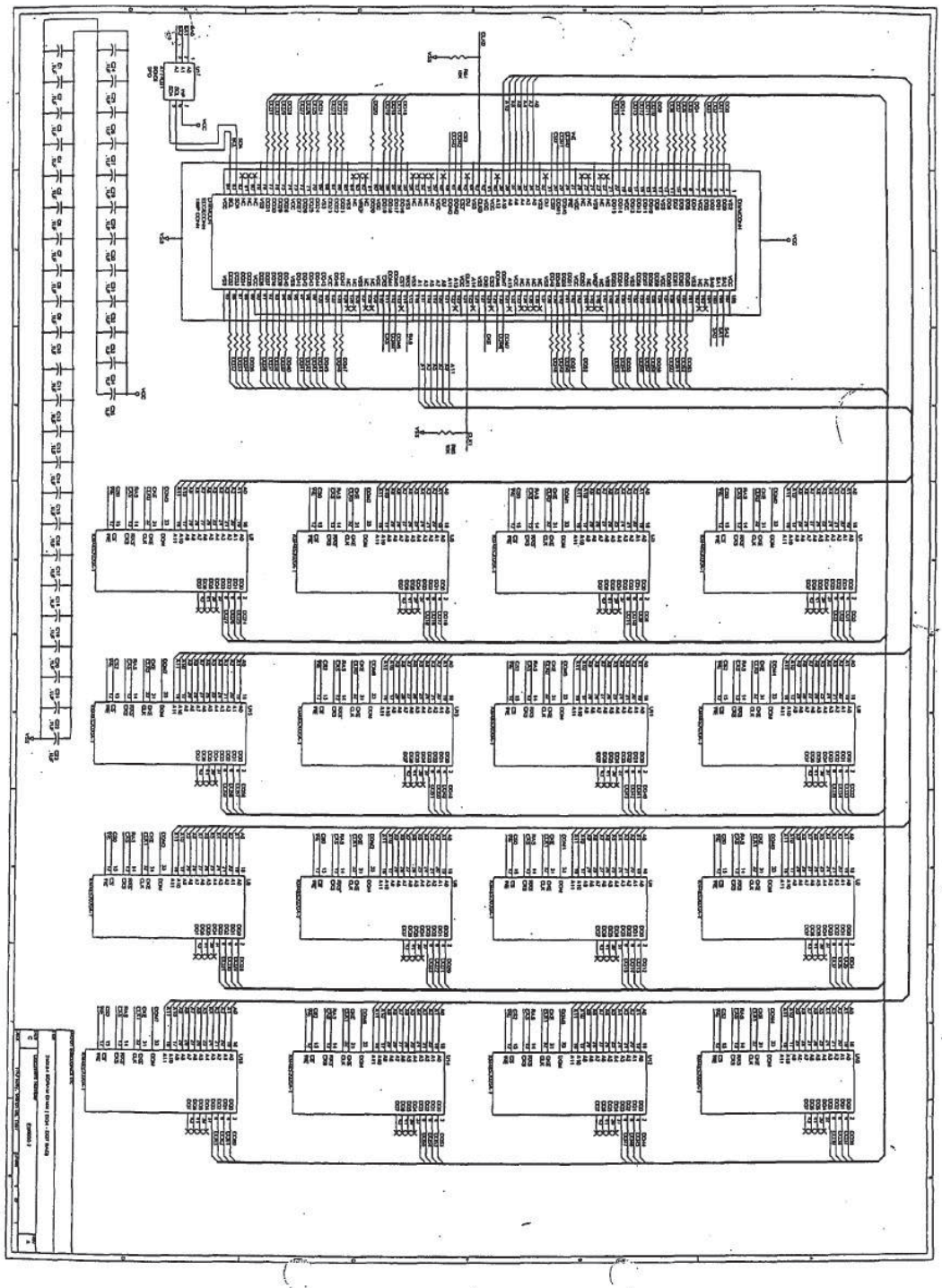
Residence	:	Boise, County of Ada State of Idaho
Citizenship	:	United States
P.O. Address	:	2972 N. Woodcreek Ln. Boise, Idaho 83704

Dated this 1 day of February, 2001.

Corey Larsen

Residence	:	Marsing, County of Owyhee State of Idaho
Citizenship	:	United States
P.O. Address	:	P.O. Box 383 Marsing, Idaho 83639

EXHIBIT A



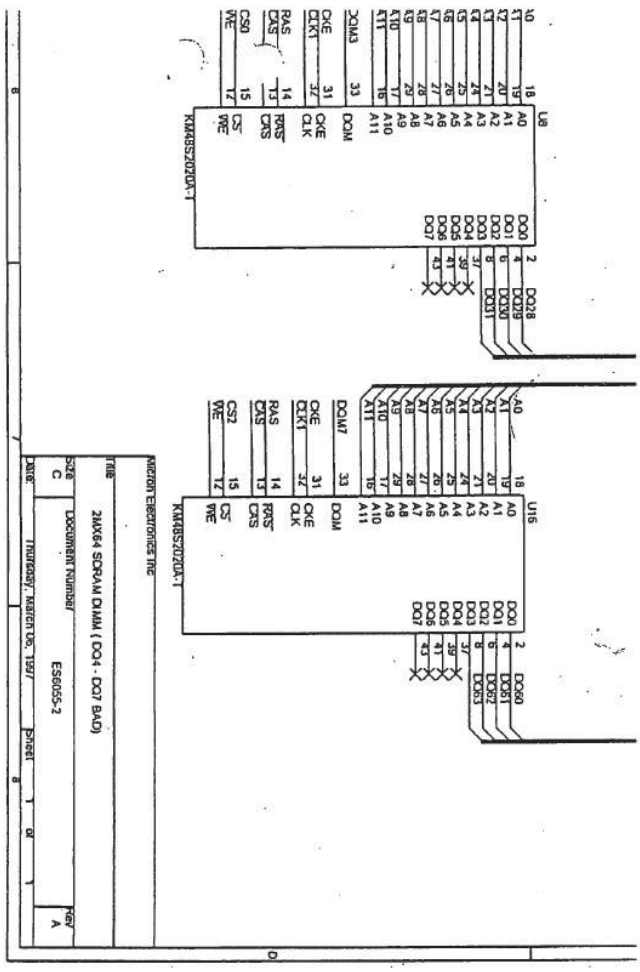

U8
KM48S2020A-1
U16
KM48S2020A-1
Micron Electronics Inc
2MX64 SDRAM DIMM (DQ4 - DQ7 BAD)
Document Number
ES6055-2
Rev
A
Thursday, March 06, 1997
Sheet
8
1
of
1

EXHIBIT B

MICRON
ELECTRONICS, INC.

WRITER'S DIRECT DIAL: (208) 893-4792
WRITER'S FAX: (208) 893-7411
E-MAIL: njjohnson@micron.com

June 13, 1997

Via Interoffice Mail

Corey Larsen
Richard Weber
Micron Electronics, Inc.
900 East Karcher Road
Nampa, ID 83687

Re: Micron Reference Number: 97.00031
Title: "Design To Optimize Recovery Of Useful Areas of Partial SDRAM on a SDRAM DIMM"

Dear Corey and Richard:

Enclosed you will find a second draft applications. If you have changes, please mark them on the copies enclosed and return the edited copies to me so that Hoyt can review the marked-up drafts. If there are no changes, please call or e-mail me so that I may send the Declaration and Power of Attorney and Assignment documents (remember the Assignment must be signed in the presence of a notary) for you to sign. After signing and notarizing all applicable sections, return all documents to me.

If you have any questions, please do not hesitate to call.

Sincerely,

Nancey Johnson

Nancey Johnson
Patent Secretary

/nj

Enclosure

f:/legal/njjohnson/prosecut/ltrprose/docinv.exa.doc

EXHIBIT C

MICRON
ELECTRONICS, INC.

WRITER'S DIRCT DIAL: (208) 898-4792
WRITER'S FAX: (208) 898-7411
E-MAIL: njhammond@micron.com

August 20, 1997

Via Federal Express (612)340-2600

Mark A. Wolfe, Esq.
Dorsey & Whitney
Pillsbury Center South
220 South Sixth Street
Minneapolis, MN 55402-1498

Re: Micron Reference Number: 97.00031
Your Reference Number : 6142
Title: "Design To Optimize Recovery Of Useful Areas Of Partial SDRAM on a SDRAM DIMM"

Dear Mark:

Enclosed please find the edited draft application for the above case. The inventor and Hoyt Fleming have reviewed and made changes. Please make the necessary changes and send back a clean copy along with a redlined version for the inventor to review.

Thank you.

Sincerely,

Nancey Hammond

Nancey Hammond
Patent Secretary

/nh

Enclosures

f:/legal/hammondprosecut/ltrprose/drtapcou.doc

900 E. Karcher Road Nampa, Idaho 83687-3045 (208) 893-3434 FAX (208) 893-3424

EXHIBIT D

Nancey Hammond 97,10031

To: Wolfe, Mark
Subject: RE: Status

Go ahead and send the revised draft on 6142 for the inventor to review. I don't need the other three in any specific order, whichever you are working on first.

Thank you,

Nancey/MEI-Legal

From: Wolfe, Mark[SMTP:wolfe.mark@dorseylaw.com]
Sent: Monday, October 06, 1997 7:57 AM
To: NJHAMMOND@micron.com
Subject: RE: Status

Nancey: Here's the status for these applications:

6142: We have made the changes to the application, and are preparing additional method claims for filing in the "method claims" application. We expect that we'll have the revised draft to you this week. Also, our current directions are to return the revised draft to you for review prior to filing. Would you prefer that we go ahead and file the applications instead?

To: Wolfe, Mark
Cc: Hemphill, Stuart; HAFLEMING@meigate
From: NJHAMMOND@micron.com on Thu, Oct 2, 1997 11:46 AM
Subject: Status
RFC Header:Received: by dorseylaw.com with SMTP;2 Oct 1997 11:45:52 -0600
Received: from fwext.micron.com ([204.134.212.40]) by fwnt.dorseylaw.com
via smtpd (for mail.dorseylaw.com [170.112.253.3]) with SMTP; 2 Oct 1997 16:42:56 UT
Received: from admin-srv21.micron.com by fwext.micron.com
via smtpd (for FWNT.DORSEYLAW.COM [170.112.1.34]) with SMTP; 2 Oct 1997 16:44:45 UT
Received: from exm01imc1.micron.com (meigate [137.201.204.115]) by admin-srv21.micron.com (8.7.5/8.7.3) with SMTP id KAA00416; Thu, 2 Oct 1997 10:44:42 -0600 (MDT)
Received: by exm01imc1.micron.com with Microsoft Exchange (IMC 4.0.837.3)
id <01BCCF20.33C1E720@exm01imc1.micron.com>; Thu, 2 Oct 1997 10:44:47 -0600
Message-ID: <c=US%a=_%p=MICRON%l=_EXCHMEI01E-971002164448Z-79494@exm01imc1.micron.com>
From: <NJHAMMOND@micron.com>
To: <wolfe.mark@dorseylaw.com>
Cc: <hemphill.stuart@dorseylaw.com>, <HAFLEMING@meigate>
Subject: Status
Date: Thu, 2 Oct 1997 10:44:48 -0600
X-Mailer: Microsoft Exchange Server Internet Mail Connector Version 4.0.837.3
Encoding: 9 TEXT

Mark, just checking on the status of the first draft applications for your docket numbers and the second draft for 6142. Please let me know if you are waiting for further information from the inventors so that I can start calling them.

Thank you,

Nancey/MEI-Legal
(208) 898-4792

EXHIBIT E

DORSEY & WHITNEY LLP

MINNEAPOLIS
WASHINGTON, D.C.
LONDON
BRUSSELS
HONG KONG
DES MOINES
ROCHESTER
COSTA MESA

PILLSBURY CENTER SOUTH
220 SOUTH SIXTH STREET
MINNEAPOLIS, MINNESOTA 55402-1498
TELEPHONE: (612) 340-2600
FAX: (612) 340-2868

MARK A. WOLFE
(612) 340-5659
Fax: (612) 340-8856
wolfe.mark@dorseylaw.com

NEW YORK
DENVER
SEATTLE
FARGO
BILLINGS
MISSOULA
GREAT FALLS

October 9, 1997

Via Federal Express

Mr. Hoyt Fleming
Micron Electronics Inc.
900 E. Karcher Road
Trailer #12
Nampa, ID 83687

Re: New U.S. Patent Application for
Design to Optimize Recovery of Useful Areas of
Partial SDRAM on a SDRAM DIMM
Our Docket: 6142 Your Ref. 97.00031

Dear Hoyt:

Enclosed is a revised version of an application (clean copy and redlined copy) for the above-identified invention. The suggested changes have been made, and additional claims have been added. After you have had an opportunity to look over this revised draft, please call so that we can get the application on file.

Very truly yours,

Mark A. Wolfe

MAW:jrc
Enclosures

EXHIBIT F

MICRON
ELECTRONICS, INC.

WRITER'S DIRECT DIAL: (208) 898-4792
WRITER'S FAX: (208) 898-7211
E-MAIL: njhammond@micron.com

October 13, 1997

Via Interoffice Mail

Corey Larsen
Richard Weber
Micron Electronics, Inc.
900 East Karcher Road
Nampa, ID 83687

Re: Micron Reference Number: 97.00031
Title: "Partial SDRAM on a SDRAM DIMM"

Dear Corey and Rick:

Enclosed you will find a third draft application. If you have changes, please mark them on the copy enclosed and return the edited copy to me so that Hoyt can review the marked-up draft. If there are no changes, please e-mail with the docket number and title of your application so that Hoyt may review and we can get your application filed

If you have any questions, please do not hesitate to call.

Sincerely,

Nancey Hammond

Nancey Hammond
Patent Secretary

/nh

Enclosure

f:/legal/hammond/prosecut/ltrprose/app.inv.id.doc

EXHIBIT G

DORSEY & WHITNEY LLP

MINNEAPOLIS
WASHINGTON, D.C.
LONDON
BRUSSELS
HONG KONG
DES MOINES
ROCHESTER
COSTA MESA

PILLSBURY CENTER SOUTH
220 SOUTH SIXTH STREET
MINNEAPOLIS, MINNESOTA 55402-1498
TELEPHONE: (612) 340-2600
FAX: (612) 340-2868

MARK A. WOLFE
(612) 340-5659
Fax: (612) 340-8856
wolfe.mark@dorseylaw.com

NEW YORK
DENVER
SEATTLE
FARGO
BILLINGS
MISSOULA
GREAT FALLS

October 16, 1997

Mr. Corey Larson
c/o Nancey Hammond
Micron Electronics, Inc.
Trailer #12
900 East Karcher Road
Nampa, ID 83687

Re: New U.S. Patent Application for
RECOVERY OF USEFUL AREAS OF PARTIALLY DEFECTIVE SYNCHRONOUS MEMORY COMPONENTS
Our Docket: 6142 Your Ref. 97.00031

Dear Corey:

Enclosed is the revised draft for the above application.

Very truly yours,

Mark A. Wolfe

MAW:jrc
Enclosure

EXHIBIT H

MICRON
ELECTRONICS, INC.

WRITER'S DIRECT DIAL: (208) 898-4792
WRITER'S FAX: (208) 898-7211
E-MAIL: njhammond@micron.com

October 24, 1997

Via Interoffice Mail

Corey Larson
Micron Electronics, Inc.
900 East Karcher Road
Nampa, ID 83687

Re: Micron Reference Number: 97.00031
Title: "Recovery of Useful Areas of Partially Defective Synchronous Memory Components"

Dear Corey:

Enclosed you will find a fourth draft application. **(I just recently sent you a third draft and then received this fourth draft this week)** If you have changes, please mark them on the copy enclosed and return the edited copy to me so that Hoyt can review the marked-up draft. If there are no changes, please e-mail with the docket number and title of your application so that Hoyt may review and we can get your application filed

If you have any questions, please do not hesitate to call.

Sincerely,

Nancey Hammond

Nancey Hammond
Patent Secretary

/nh

Enclosure

f:/legal/hammond/prosecut/ltrprose/app.inv.id.doc

EXHIBIT I

DORSEY & WHITNEY LLP

MINNEAPOLIS
WASHINGTON, D.C.
LONDON
BRUSSELS
HONG KONG
DES MOINES
ROCHESTER
COSTA MESA

PILLSBURY CENTER SOUTH
220 SOUTH SIXTH STREET
MINNEAPOLIS, MINNESOTA 55402-1498
TELEPHONE: (612) 340-2600
FAX: (612) 340-2868

MARK A. WOLFE
(612) 340-5659
Fax: (612) 340-8856
wolfe.mark@dorseylaw.com

NEW YORK
DENVER
SEATTLE
FARGO
BILLINGS
MISSOULA
GREAT FALLS

January 27, 1998

Mr. Hoyt Fleming
Micron Electronics Inc.
900 E. Karcher Road
Trailer #12
Nampa, ID 83687

via Federal Express

MICRON LEGAL
JAN 28 1998

Re: New U.S. Patent Application for
Design to Optimize Recovery of Useful Areas of
Partial SDRAM on a SDRAM DIMM
Our Docket: 6142 Your Ref. 97.00031

Dear Hoyt:

Enclosed is another revised version of an application (clean copy and redlined copy) for the above-identified invention, reflecting changes suggested this week by Corey Larsen. The suggested changes have been made, and additional claims have been added. After you and Corey have had an opportunity to look over this revised draft, please call so that we can get the application on file.

Very truly yours,

Mark A. Wolfe

MAW:jrc
Enclosures

EXHIBIT J

900 East Karcher Road
Nampa, Idaho 83687

WRITER'S DIRECT DIAL: (208) 898-4792
WRITER'S FAX: (208) 898-7211

E-MAIL: njhammond@micronpc.com

January 30, 1998

Via Interoffice Mail

Corey Larsen
Micron Electronics, Inc.
900 East Karcher Road
Nampa, ID 83687

Re: Micron Reference Number: 97.00031
Title: "Partial SDRAM on a SDRAM DIMM

Dear Corey:

Enclosed you will find a third draft application and redlined version. If you have changes, please mark them on the copy enclosed and return the edited copy to me so that Hoyt can review the marked-up draft. If there are no changes, please e-mail me with the docket number and title of your application so that Hoyt may review and we can get your application filed

If you have any questions, please do not hesitate to call.

Sincerely,

Nancey Hammond

Nancey Hammond
Patent Secretary

/nh

Enclosure

f:/legal/hammond/prosecut/ltrprose/app.inv.id.doc

Phone: 208-898-3434
Fax: 208-898-3424
www.micronpc.com

EXHIBIT K

WRITER'S DIRECT DIAL: (208) 898-4792
WRITER'S FAX: (208) 898-7211
E-MAIL: nhammond@micronpc.com
900 East Karcher Road
Nampa, Idaho 83687

February 20, 1998

Via Federal Express (612) 340-2600

Stuart Hemphill, Esq.
Pillsbury Center South
220 South Sixth Street
Minneapolis, MN 55402-1498

Re: Micron Reference Number: 97.00031
Your Reference Number: 6142
Title: "Design to Optimize Recovery of Useful Areas of Design to Optimize Recovery of Useful Areas of Partial SDRAM on a SDRAM DIMM"

Dear Mr. Hemphill:

Enclosed please find a third draft application which both the inventor and Hoyt have reviewed. Please the marked changes and file this application, without signatures, at this time.

If you need anything or have any further questions, feel free to call.

Sincerely,

Nancey Hammond

Nancey Hammond
Patent Secretary

/nh

Enclosures

f:/legal/legal/hammond/prosecut/ltrprose/final.dw.doc

Phone: 208-898-3434
Fax: 208-898-3424
www.micronpc.com

In re application of:
Richard Weber and Corey Larsen

Serial No.: 09/035,739

Filed: March 5, 1998

For: METHOD FOR RECOVERY OF USEFUL AREAS OF PARTIALLY DEFECTIVE SYNCHRONOUS MEMORY COMPONENTS

§ Group Art Unit: 2751
§ Examiner: Kevin Ellis
§ Atty. Docket: 97.00031.01

PETITION FOR EXTENSION OF TIME UNDER 37 C.F.R. § 1.136(a)

Assistant Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

Applicant hereby petitions to extend the period for response to the Third Office Action mailed September 7, 2000 for one (2) month(s), from December 7, 2000 to February 7, 2001.

Accordingly, the requisite fee is $ 390. The Commissioner is requested to charge this fee, and any additional fee which may be required to Micron Electronics, Inc. Deposit 500659. A duplicate copy of this petition is enclosed.

Respectfully submitted,

Date: 2/5/1

Paul A. Revis, Reg No. 45,040
Micron Electronics, Inc.
900 East Karcher Road
Nampa, ID 83687
(208) 898-1316

02/09/2001 WABRHAM1 00000010 500659 09035739
01 FC:116 390.00 CH

G:\patent\patents\proforms\extoflim (2/29/96)

PTO/SB/17 (11-00)
Approved for use through 10/31/2002. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

FEE TRANSMITTAL for FY 2001

Patent fees are subject to annual revision.

TOTAL AMOUNT OF PAYMENT ($) 390.00

Complete If Known	
Application Number	09/035,739
Filing Date	March 5, 1998
First Named Inventor	Rick Weber
Examiner Name	Kevin Ellis
Group Art Unit	2751
Attorney Docket No.	97.00031.01

OIPE TC 2100 FEB 08 2001 PATENT & TRADEMARK OFFICE

METHOD OF PAYMENT

1. [x] The Commissioner is hereby authorized to charge indicated fees and credit any overpayments to:
   Deposit Account Number: 500659
   Deposit Account Name: Micron Electronics
   [x] Charge Any Additional Fee Required Under 37 CFR 1.16 and 1.17
   [ ] Applicant claims small entity status. See 37 CFR 1.27
2. [ ] Payment Enclosed: [ ] Check [ ] Credit card [ ] Money Order [ ] Other

FEE CALCULATION

1. BASIC FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
101	710	201	355	Utility filing fee	
106	320	206	160	Design filing fee	
107	490	207	245	Plant filing fee	
108	710	208	355	Reissue filing fee	
114	150	214	75	Provisional filing fee	

SUBTOTAL (1) ($)

2. EXTRA CLAIM FEES

	Extra Claims		Fee from below	Fee Paid
Total Claims		-20** =		X =
Independent Claims		- 3** =		X =
Multiple Dependent				=

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
103	18	203	9	Claims in excess of 20
102	80	202	40	Independent claims in excess of 3
104	270	204	135	Multiple dependent claim, if not paid
109	80	209	40	** Reissue independent claims over original patent
110	18	210	9	** Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($)

**or number previously paid, if greater; For Reissues, see above

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
105	130	205	65	Surcharge - late filing fee or oath	
127	50	227	25	Surcharge - late provisional filing fee or cover sheet	
139	130	139	130	Non-English specification	
147	2,520	147	2,520	For filing a request for *ex parte* reexamination	
112	920*	112	920*	Requesting publication of SIR prior to Examiner action	
113	1,840*	113	1,840*	Requesting publication of SIR after Examiner action	
115	110	215	55	Extension for reply within first month	
116	390	216	195	Extension for reply within second month	390
117	890	217	445	Extension for reply within third month	
118	1,390	218	695	Extension for reply within fourth month	
128	1,890	228	945	Extension for reply within fifth month	
119	310	219	155	Notice of Appeal	
120	310	220	155	Filing a brief in support of an appeal	
121	270	221	135	Request for oral hearing	
138	1,510	138	1,510	Petition to institute a public use proceeding	
140	110	240	55	Petition to revive - unavoidable	
141	1,240	241	620	Petition to revive - unintentional	
142	1,240	242	620	Utility issue fee (or reissue)	
143	440	243	220	Design issue fee	
144	600	244	300	Plant issue fee	
122	130	122	130	Petitions to the Commissioner	
123	50	123	50	Processing fee under 37 CFR 1.17(q)	
126	180	126	180	Submission of Information Disclosure Stmt	
581	40	581	40	Recording each patent assignment per property (times number of properties)	
146	710	246	355	Filing a submission after final rejection (37 CFR § 1.129(a))	
149	710	249	355	For each additional invention to be examined (37 CFR § 1.129(b))	
179	710	279	355	Request for Continued Examination (RCE)	
169	900	169	900	Request for expedited examination of a design application	

Other fee (specify) _____

*Reduced by Basic Filing Fee Paid SUBTOTAL (3) ($) 390

RECEIVED FEB 14 2001 Technology Center 2100

SUBMITTED BY				Complete (if applicable)	
Name (Print/Type)	Paul A. Reyls	Registration No. (Attorney/Agent)	45,040	Telephone	(208) 898-1316
Signature				Date	2/5/01

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

Burden Hour Statement: This form is estimated to take 0.2 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Assistant Commissioner for Patents, Washington, DC 20231.

09/035,739

UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

APPLICATION NUMBER	FILING DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NO.
09/035,739	03/05/98	WEBER	R 6325

EXAMINER

020995 TM02/0424
KNOBBE MARTENS OLSON & BEAR LLP
620 NEWPORT CENTER DRIVE
SIXTEENTH FLOOR
NEWPORT BEACH CA 92660

ART UNIT	PAPER NUMBER
2185	20

DATE MAILED: 04/24/01

This is a communication from the examiner in charge of your application.
COMMISSIONER OF PATENTS AND TRADEMARKS

NOTICE OF ALLOWABILITY

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance and Issue Fee Due or other appropriate communication will be mailed in due course.

☒ This communication is responsive to the declaration & response filed 2/8/01.

☒ The allowed claim(s) is/are 1-12.

☐ The drawings filed on _____ are acceptable.

☐ Acknowledgement is made of a claim for foreign priority under 35.U.S.C. § 119(a)-(d).

☐ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number) _____.

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____.

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

A SHORTENED STATUTORY PERIOD FOR REPLY to comply with the requirements noted below is set to EXPIRE **THREE MONTHS** FROM THE "DATE MAILED" of this Office action. Failure to timely comply will result in ABANDONMENT of this application. ~~Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).~~

☐ Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL APPLICATION, PTO-152, which discloses that the oath or declaration is deficient. A SUBSTITUTE OATH OR DECLARATION IS REQUIRED.

☒ Applicant MUST submit NEW FORMAL DRAWINGS

☒ because the originally filed drawings were declared by applicant to be informal.

☐ including changes required by the Notice of Draftperson's Patent Drawing Review, PTO-948, attached hereto or to Paper No. _____.

☐ including changes required by the proposed drawing correction filed on _____, which has been approved by the examiner.

☐ including changes required by the attached Examiner's Amendment/Comment.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the reverse side of the drawings. The drawings should be filed as a separate paper with a transmittal letter addressed to the Official Draftperson.

☐ Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Any reply to this notice should include, in the upper right hand corner, the APPLICATION NUMBER (SERIES CODE/SERIAL NUMBER). If applicant has received a Notice of Allowance and Issue Fee Due, the ISSUE BATCH NUMBER and DATE of the NOTICE OF ALLOWANCE should also be included.

Attachment(s)

☐ Notice of References Cited, PTO-892

☒ Information Disclosure Statement(s), PTO-1449, Paper No(s). 15

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

☐ Interview Summary, PTO-413

☒ Examiner's Amendment/Comment

☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material

☐ Examiner's Statement of Reasons for Allowance

PTOL-37 (Rev. 8/97)

*U.S. GPO: 1998-433-221/82108

Detailed Action

Declaration Under 37 CFR § 1.131

1. The declaration filed on 2/8/01 under 37 CFR § 1.131 has been considered and is sufficient to overcome the Jacobson reference. As such the claims have been passed to allowance.

Information Disclosure Statement

2. The cited U.S. patent applications listed on the IDS have been considered but were lined through as they will not be printed on the front of the patent.

Conclusion

3. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Kevin Ellis whose telephone number is (703) 305-9659. The Examiner can normally be reached on the weekdays from 6:00am to 2:30pm.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Matt Kim, can be reached on (703) 305-3821. The fax phone number for this Group is (703) 308-6606.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-9600.

Kevin L. Ellis
Patent Examiner
April 23, 2001

Kevin L. Ellis

Detailed Action

Declaration Under 37 CFR § 1.131

1. The declaration filed on 2/8/01 under 37 CFR § 1.131 has been considered and is sufficient to overcome the Jacobson reference. As such the claims have been passed to allowance.

Information Disclosure Statement

2. The cited U.S. patent applications listed on the IDS have been considered but were lined through as they will not be printed on the front of the patent.

Conclusion

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Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-9600.

Kevin L. Ellis
Patent Examiner
April 23, 2001

Kevin L. Ellis

BEST COPY

UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office

NOTICE OF ALLOWANCE AND ISSUE FEE DUE

020995 TM02/0424
KNOBBE MARTENS OLSON & BEAR LLP
620 NEWPORT CENTER DRIVE
SIXTEENTH FLOOR
NEWPORT BEACH CA 92660

APPLICATION NO.	FILING DATE	TOTAL CLAIMS	EXAMINER AND GROUP ART UNIT		DATE MAILED
09/035,739	03/05/98	012	ELLIS, K	2185	04/24/01

First Named Applicant		
WEBER,	35 USC 154(b) term ext. =	0 Days.

TITLE OF INVENTION: METHOD FOR RECOVERY OF USEFUL AREAS OF PARTIALLY DEFECTIVE SYNCHRONOUS MEMORY COMPONENTS

ATTY'S DOCKET NO.	CLASS-SUBCLASS	BATCH NO.	APPLN. TYPE	SMALL ENTITY	FEE DUE	DATE DUE
2 6325	711-170.000	F36	UTILITY	NO	$1240.00	07/24/01

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED.

THE ISSUE FEE MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED.

HOW TO RESPOND TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is changed, pay twice the amount of the FEE DUE shown above and notify the Patent and Trademark Office of the change in status, or.

B. If the status is the same, pay the FEE DUE shown above.

If the SMALL ENTITY is shown as NO:

A. Pay FEE DUE shown above, or

B. File verified statement of Small Entity Status before, or with, payment of 1/2 the FEE DUE shown above.

II. Part B-Issue Fee Transmittal should be completed and returned to the Patent and Trademark Office (PTO) with your ISSUE FEE. Even if the ISSUE FEE has already been paid by charge to deposit account, Part B Issue Fee Transmittal should be completed and returned. If you are charging the ISSUE FEE to your deposit account, section "4b" of Part B-Issue Fee Transmittal should be completed and an extra copy of the form should be submitted.

III. All communications regarding this application must give application number and batch number. Please direct all communications prior to issuance to Box ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PATENT AND TRADEMARK OFFICE COPY

PTOL-85 (REV. 10-96) Approved for use through 08/30/99. (0651-0033)

035 739

07/20/01 08:28 FAX 1 619 235 0176 KMOB SAN DIEGO

atch & Return

001/007

#22

Knobbe Martens Olson & Bear LLP

Intellectual Property Law

550 West C Street
Suite 1200
San Diego CA 92101
Tel 619-235-8550
Fax 619-235-0176
kmob.com

INFORMATION COMMUNICATION
PLEASE HAND-DELIVER TO EXAMINER

July 20, 2001
8:50 AM

ORIGINAL WILL FOLLOW VIA:

- o Mail
- o International Airmail
- o With Enclosures
- o Hand Delivery
- o Without Enclosures
- o Courier
- v Will Not Follow

OFFICIAL

Facsimile Transmittal Sheet

Confidentiality Notice:

The documents accompanying this facsimile transmission contain confidential information which may be legally privileged. The information is intended only for the use of the recipient named below. If you have received this facsimile in error, please immediately notify us by telephone to arrange for return of the original documents to us. Any disclosure, copying, distribution or the taking of any action in reliance on the contents of this faxed information is strictly prohibited.

To:	EXAMINER K. ELLIS; ART UNIT 2751
FIRM:	USPTO
FACSIMILE NO.:	703 305 9659
FROM:	DREW S. HAMILTON/MONICA (619) 687-8684
CLIENT CODE:	SERIAL NO. 09/035,739; OUR REF. MTIPAT.057A
PAGES:	7 (INCLUDING THIS SHEET)

IF YOU DID NOT RECEIVE ALL OF THE PAGES, PLEASE CALL BACK IMMEDIATELY.

MESSAGE: PER OUR TELEPHONE CONVERSATION, ATTACHED IS THE IDS THAT WE REQUEST SIGNATURE. PLEASE CONFIRM RECEIPT OF THIS FACSIMILE TRANSMISSION. THANK YOU.

620 Newport Center Drive
Sixteenth Floor
Newport Beach, CA 92660
Tel 949-760-0404
Fax 949-760-9502

201 California Street
Suite 1150
San Francisco CA 94111
Tel 415-954-4114
Fax 415-954-4111

1900 Avenue of the Stars
Suite 1425
Los Angeles CA 90067
Tel 310-551-3450
Fax 310-551-3458

3801 University Avenue
Suite 710
Riverside CA 92501
Tel 909-781-9231
Fax 909-781-4507

6/01

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:
RICHARD WEBER and COREY LARSEN

Serial No.: 09/035,739

Filed: March 5, 1998

For:
METHOD FOR RECOVERY OF USEFUL AREAS OF PARTIALLY DEFECTIVE SYNCHRONOUS MEMORY COMPONENTS

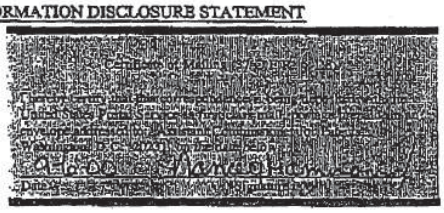
§ Group Art Unit: 2751
§ Examiner: *Kevin Ellis*
§ Atty. Docket: 97.00031.01
§ Paper No.

RECEIVED 7/6/07

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

OFFICIAL

Assistant Commissioner for Patents
Washington, D.C. 20231



Dear Sir:

In compliance with the duty of disclosure under 37 C.F.R. § 1.56, Applicant[s] respectfully request[s] that this Supplemental Information Disclosure Statement be entered and that the references listed on the attached Form PTO-1449 be considered by the Examiner and made of record. Copies of the listed references are enclosed for the convenience of the Examiner.

In accordance with 37 C.F.R. § 1.97(b), this Supplemental Information Disclosure Statement is not to be construed as a representation that a search has been made or that no other possible material information as defined in 37 C.F.R. § 1.56(a) exists.

The following references are submitted for the Examiner's review:

U.S. Patents

U.S. Patent No.	Issue Date	Inventor
3,800,294	3/26/74	Lawlor
4,376,300	3/8/83	Tsang
4,450,560	5/22/84	Conner

4,479,214	10/23/84	Ryan
4,646,299	2/24/87	Schmabeck
4,807,191	2/21/89	Flannagan
4,876,685	10/24/89	Rich
4,881,200	11/14/89	Urai
4,908,798	3/13/90	Urai
4,918,662	4/17/90	Kondo
4,935,899	6/19/90	Morigami
5,060,197	10/22/91	Park & Kim
5,124,948	6/23/92	Takizawa
5,134,584	7/28/92	Boler & Lukanc
5,200,959	4/6/93	Gross & Norman
5,233,614	8/3/93	Singh
5,315,552	5/24/94	Yoneda
5,327,380	7/5/94	Karsh, et al.
5,331,188	7/19/94	Acovic, et al.
5,337,277	8/9/94	Jang
5,371,866	12/6/94	Cady
5,379,415	1/3/95	Papenberg, et al.
5,390,129	2/14/95	Rhodes
5,400,263	3/21/95	Rohrbaugh, et al.
5,400,342	3/21/95	Matsumura, et al.
5,410,545	4/25/95	Porter & Myers
5,424,989	6/13/95	Hagiwara & Sakihama
5,434,792	7/18/95	Saka, et al.
5,469,390	11/21/95	Sasaki & Tanaka
5,475,695	12/12/95	Caywood, et al.
5,491,664	2/13/96	Phelan
5,497,381	3/5/96	O'Donoghue & Cheek
5,502,333	3/26/96	Bertin, et al.
5,535,328	7/9/96	Harari, et al.
5,538,115	7/23/96	Koch
5,544,106	8/6/96	Koike
5,548,553	8/20/96	Cooper & Leary
5,553,231	9/3/96	Papenberg, et al.
5,588,115	12/24/96	Augarten
5,600,258	2/4/97	Graham, et al.
5,602,987	2/11/97	Harari
5,631,868	5/20/97	Terrullo, et al.
5,633,826	5/27/97	Tsukada
5,654,204	8/5/97	Anderson
5,717,694	2/10/98	Ohsawa
5,734,621	3/31/98	Ito
5,745,673	4/28/98	Di Zenzo & Grimani
5,754,753	5/19/98	Smelser
5,758,056	5/26/98	Barr
5,841,710	11/24/98	Larsen
5,862,314	1/19/99	Jeddeloh
5,913,020	6/15/99	Rohwer
5,920,512	7/6/99	Larsen
5,963,463	10/5/99	Rondeau & Magee
5,966,724	10/12/99	Ryan
5,974,564	10/26/99	Jeddeloh
5,991,215	11/23/99	Brunelle

5,995,409	11/30/99	Holland
6,009,536	12/28/99	Rohwer

Other References:

"MindShare, Inc., Anderson and Shanley," Pentium ™ Processor System Architecture, Second Edition, PC System Architecture Series: 126-132, 221-234, 1995.
09/035,629 – "Recovery of Partially Defective Synchronous Memory Components" filed 3/5/98
08/903,819 – "System For Remapping Defective Memory Bit Sets" filed 7/31/97
09/217,781 – "Use of Partially Dysfunctional Memory Devices" filed 12/21/98
09/067,347 – "A System For Decoding Addresses For A Defective Memory Array" filed 4/28/98
09/067,467 – "A Method For Decoding Addresses For A Defective Memory Array" filed 4/28/98
09/519,641 – "Method and Apparatus For Recovery of Useful Areas of Partially Defective Direct Rambus Rimm Components" filed 3/6/00
09/548,826 – "Method and Apparatus For Storing Failing Part Locations In A Module" – filed 4/13/00

Applicant understands that no fee or certification is required for the submission and consideration of this information at this time. If the fee of 37 C.F.R. § 1.17(p) is required at this time, the Commissioner is authorized to charge such fee to Deposit Account No. 500659

****

A Form PTO-1449 is enclosed herewith.

Respectfully submitted,

Date: 9/6/10

Paul A. Revis
Reg. No. 45,040
Micron Electronics, Inc.
900 East Karcher Road
Nampa, ID 83687
(208) 898-1316
AGENT FOR APPLICANT

FORM: PTO-1449 (REV: 7-80)	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	Atty Docket No: 97.00031.01	Serial No: 09/035,739
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (37 CFR 1.98(b)) *(use several sheets if necessary)*		Applicant: Richard Weber and Corey Larsen	
		Filing Date: March 5, 1998	Group: 2751

U.S. PATENT DOCUMENTS

Examiner Initial		Document Number	Date	Name	Class	Subclass	
	AA	3,800,294	3/26/74	Lawlor	340	172.5	
	AB	4,376,300	3/8/83	Tsang	365	200	
	AC	4,450,560	5/22/84	Conner	371	25	
	AD	4,479,214	10/23/84	Ryan	371	11	
	AE	4,646,299	2/24/87	Schinabeck & Murdock	371	20	
	AF	4,807,191	2/21/89	Flannagan	365	189	
	AG	4,876,685	10/24/89	Rich	371	21.6	
	AH	4,881,200	11/14/89	Urai	365	189.04	
	AI	4,908,798	3/13/90	Urai	365	230.03	
	AJ	4,918,662	4/17/90	Kondo	365	210	
	AK	4,935,899	6/19/90	Morigami	365	200	
	AL	5,060,197	10/22/91	Park & Kim	365	200	
	AM	5,124,948	6/23/92	Takizawa, et al.	365	200	
	AN	5,134,584	7/28/92	Boler & Lukanc	365	200	
	AO	5,200,959	4/6/93	Gross & Norman	371	21.6	
	AP	5,233,614	8/3/93	Singh	371	21.6	
	AQ	5,315,552	5/24/94	Yoneda	365	200	
	AR	5,327,380	7/5/94	Kersh & Norwood	365	195	
	AS	5,331,188	7/19/94	Acovic, et al.	257	298	
	AT	5,337,277	8/9/94	Jang	365	200	
	AU	5,371,866	12/6/94	Cady	395	400	
	AV	5,379,415	1/3/95	Papenberg, et al.	395	575	
	AW	5,390,129	2/14/95	Rhodes	364	480	

FOREIGN PATENT DOCUMENTS

Examiner Initial		Document Number	Date	Country	Class	Subclass	Translation Yes	Translation No
	AX						☐	☐

OTHER ART (including author, title, date, pertinent pages, etc.)

Initial			
	AY		"MipdShare, Inc., Anderson and Shanley," Pentium™ Processor System Architecture, Second Edition, PC System Architecture Series: 126-132, 221-234, 1995.
	AZ		09/035,629 – "Recovery of Partially Defective Synchronous Memory Components" filed 3/5/98
	BA		08/903,819 – "System For Remapping Defective Memory Bit Sets" filed 7/31/97
	BB		09/217,781 – "Use of Partially Dysfunctional Memory Devices" filed 12/21/98
	BC		09/067,347 – "A System For Decoding Addresses For A Defective Memory Array" filed 4/28/98

Examiner:	Date Considered:

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication with applicant.

FORM: PTO-1449 (REV: 7-80)	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	Atty Docket No: 97.00031.01	Serial No: 09/035,739
INFORMATION DISCLOSURE STATEMENT BY APPLICANT		Applicant: Richard Weber and Corey Larsen	
(37 CFR 1.98(b))	*(use several sheets if necessary)*	Filing Date: March 5, 1998	Group: 2751

U.S. PATENT DOCUMENTS

Examiner Initial		Document Number	Date	Name	Class	Subclass	
	BD	5,400,263	3/21/95	Rohrbaugh, et al.	364	490	
	BE	5,400,342	3/21/95	Matsumura, et al.	371	21.2	
	BF	5,410,545	4/25/95	Porter & Myers	371	21.6	
	BG	5,424,989	6/13/95	Hagiwara & Sakihama	365	201	
	BH	5,434,792	7/18/95	Saka, et al.	364	468	
	BI	5,469,390	11/21/95	Sasaki & Tanaka	365	200	
	BJ	5,475,695	12/12/95	Caywood, et al.	371	27	
	BK	5,491,664	2/13/96	Phelan	365	200	
	BL	5,497,381	3/5/96	O'Donoghue & Check	371	28	
	BM	5,502,333	3/26/96	Bertin, et al.	257	685	
	BN	5,535,328	7/9/96	Harari, et al.	395	182.05	
	BO	5,538,115	7/23/96	Koch	188	299	
	BP	5,544,106	8/6/96	Koike	365	200	
	BQ	5,548,553	8/20/96	Cooper & Leary	365	200	
	BR	5,553,231	9/3/96	Papenberg, et al.	395	182.03	
	BS	5,588,115	12/24/96	Aitgarten	395	183.05	
	BT	5,600,258	2/4/97	Graham, et al.	324	758	
	BU	5,602,987	2/11/97	Harari, et al.	395	182.06	
	BV	5,631,868	5/20/97	Terrnullo, et al.	365	200	
	BW	5,633,826	5/27/97	Tsukada	365	200	
	BX	5,654,204	8/5/97	Anderson	438	15	
	BY	5,717,694	2/10/98	Ohsawa	371	5.1	
	BZ	5,734,621	3/21/98	Ito	365	230.03	

FOREIGN PATENT DOCUMENTS

Examiner Initial		Document Number	Date	Country	Class	Subclass	Translation Yes	Translation No
	CA						☐	☐

Initial			OTHER ART (including author, title, date, pertinent pages, etc.)
	CB		09/067,467 – "A Method For Decoding Addresses For A Defective Memory Array" filed 4/28/98
	CC		09/519,641 – "Method And Apparatus For Recovery of Useful Areas of Partially Defective Direct Rambus RIMM Components" filed 3/6/00
	CD		09/548,826 – "Method and Apparatus For Storing Failing Part Locations In a Module" filed 4/13/00

Examiner:	Date Considered:

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication with applicant.

FORM: PTO-1449 (REV: 7-80)	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	Atty Docket No: 97.00031.01	Serial No: 09/035,739
INFORMATION DISCLOSURE STATEMENT BY APPLICANT		Applicant: Richard Weber and Corey Larsen	
(37 CFR 1.98(b))	*(use several sheets if necessary)*	Filing Date: March 5, 1998	Group: 2751

U.S. PATENT DOCUMENTS

Examiner Initial		Document Number	Date	Name	Class	Subclass	
	CE	5,745,673	4/28/98	Di Zenzo & Grimani	395	182.05	
	CF	5,754,753	5/19/98	Smelser	395	182.06	
	CG	5,758,056	5/26/98	Barr	395	182.05	
	CH	5,841,710	11/24/98	Larsen	365	200	
	CI	5,862,314	1/19/99	Jeddeloh	395	182.06	
	CJ	5,913,020	6/15/99	Rohwer	395	182.06	
	CK	5,920,512	7/6/99	Larsen	365	200	
	CL	5,963,463	10/5/99	Rondeau & Mages	365	52	
	CM	5,966,724	10/12/99	Ryan	711	105	
	CN	5,974,564	10/26/99	Jeddeloh	714	8	
	CO	5,991,215	11/23/99	Brunelle	365	201	
	CP	5,995,409	11/30/99	Holland	365	149	
	CQ	6,009,536	12/28/99	Rohwer	714	8	

FOREIGN PATENT DOCUMENTS

Examiner Initial		Document Number	Date	Country	Class	Subclass	Translation Yes	Translation No
	CA						☐	☐

Initial		**OTHER ART** (including author, title, date, pertinent pages, etc.)
	CB	
	CC	
	CD	

Examiner:	Date Considered:

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Other Prior Art

According to the information contained in form PTO-1449 or PTO-892, there are one or more other prior art/non-patent literature documents missing from the original file history record obtained from the United States Patent and Trademark Office. Upon your request we will attempt to obtain these documents from alternative resources. Please note that additional charges will apply for this service.

PATENT

Case Docket No. MTIPAT.057A
Date: July 23, 2001

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#24
MB

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s)	:	Weber, et al.
Appl. No.	:	09/035,739
Filed	:	March 5, 1998
For	:	METHOD FOR RECOVERY OF USEFUL AREAS OF PARTIALLY DEFECTIVE SYNCHRONOUS MEMORY COMPONENTS
Group Art Unit	:	2185
Batch No.	:	F36
Examiner	:	K. Ellis

I hereby certify that this correspondence and all marked attachments are being deposited with the United States Postal Service as first class mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231, on

July 23, 2001
(Date)
Drew S. Hamilton
Drew S. Hamilton, Reg. No. 29,801

TRANSMITTAL LETTER

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WASHINGTON, D.C. 20231

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Dear Sir:

Enclosed for filing is the Issue Fee for the above-identified application:

(X) Form PTOL-85b.

(X) Thirty-Two (32) pages of formal drawings.

(X) A check in the amount of $1,270 to cover the issue fee, plus ten copies of the issued patent is enclosed.

(X) The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment, to Account No. 11-1410.

(X) Return prepaid postcard.

Drew S. Hamilton
Registration No. 29,801
Attorney of Record

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06/01

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OIPE JUL 25 2001

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Drew S. Hamilton (Depositor's name)
Drew S. Hamilton (Signature)
July 23, 2001 (Date)

APPLICATION NO.	FILING DATE	TOTAL CLAIMS	EXAMINER AND GROUP ART UNIT		DATE MAILED
09/035,739	03/05/98	012	ELLIS, K	2185	04/24/01

First Named Applicant: WEBER, 35 USC 154(b) term ext. = 0 Days.

TITLE OF INVENTION: METHOD FOR RECOVERY OF USEFUL AREAS OF PARTIALLY DEFECTIVE SYNCHRONOUS MEMORY COMPONENTS

ATTY'S DOCKET NO.	CLASS-SUBCLASS	BATCH NO.	APPLN. TYPE	SMALL ENTITY	FEE DUE	DATE DUE
2 6325	711-170.000	F36	UTILITY	NO	$1240.00	07/24/01

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363). Use of PTO form(s) and Customer Number are recommended, but not required.

☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

☐ "Fee Address" indication (or "Fee Address" indication form PTO/SB/47) attached.

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1 KNOBBE, MARTENS,
2 OLSON & BEAR, LLP
3

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(B) RESIDENCE: (CITY & STATE OR COUNTRY)
BOISE, IDAHO

Please check the appropriate assignee category indicated below (will not be printed on the patent)
☐ individual ☒ corporation or other private group entity ☐ government

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The COMMISSIONER OF PATENTS AND TRADEMARKS IS requested to apply the Issue Fee to the application identified above.

(Authorized Signature) Drew S. Hamilton (Date) 7/23/01

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01 FC:142 1240.00 OP
02 FC:561 30.00 OP

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PTOL-85B (REV.10-96) Approved for use through 06/30/99. OMB 0651-0033 Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

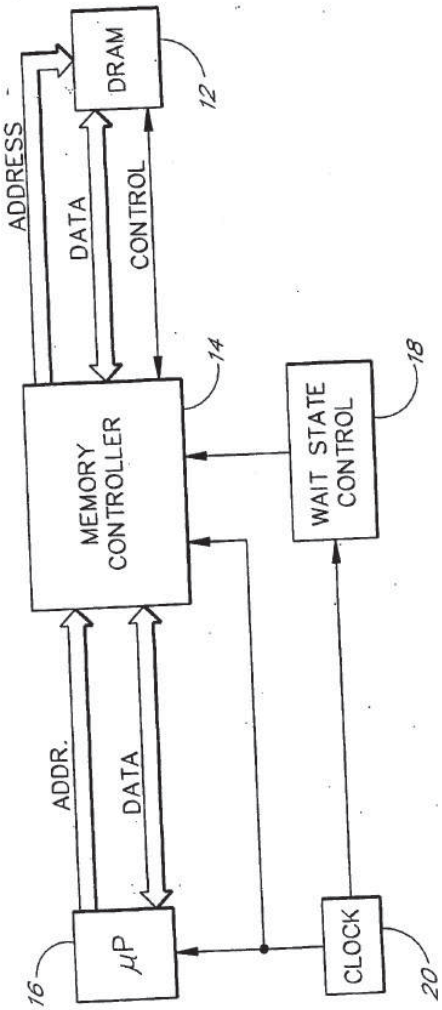
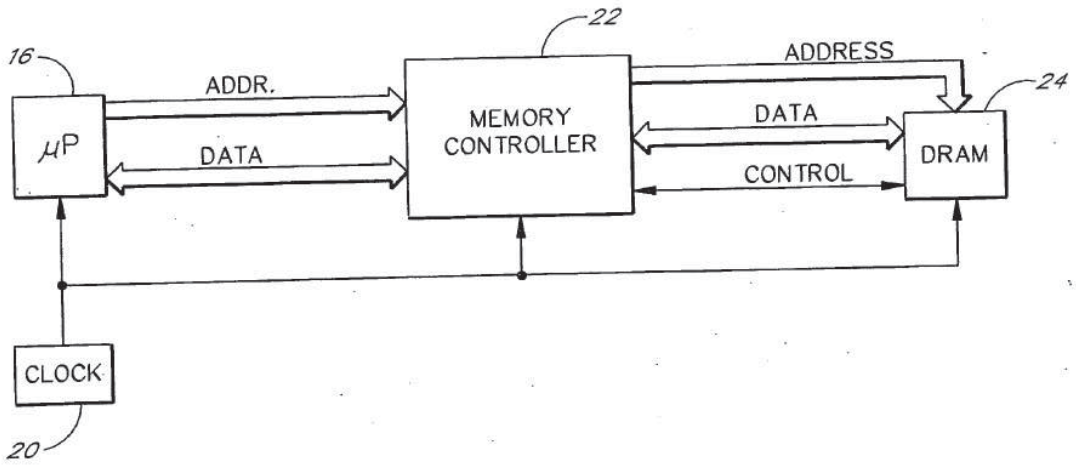


FIG. 1
(PRIOR ART)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CONTROL
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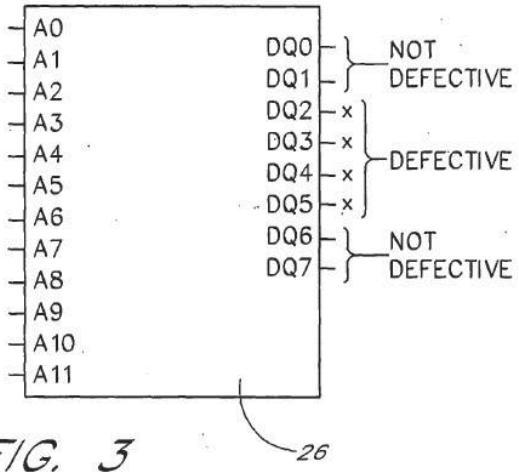
DRAM
CLOCK
20

FIG. 2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A1
A2
A3
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A5
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A11
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DQ1
DQ2
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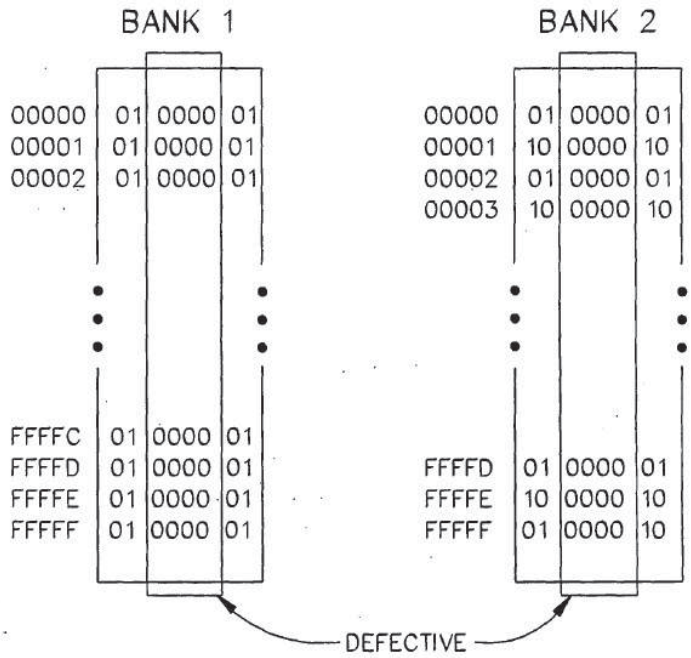
DQ5
DQ6
DQ7
x
x
x
x
NOT DEFECTIVE
DEFECTIVE
NOT DEFECTIVE
26

FIG. 3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BANK 2
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00002 01 0000 01
FFFFC 01 0000 01
FFFFD 01 0000 01
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FFFFF 01 0000 01
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FFFFD 01 0000 01
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FFFFF 01 0000 10
DEFECTIVE

FIG. 4

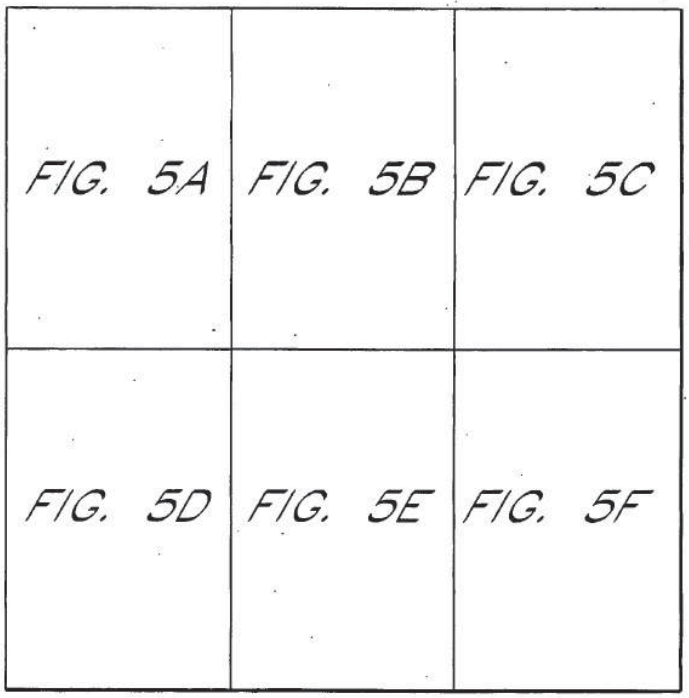
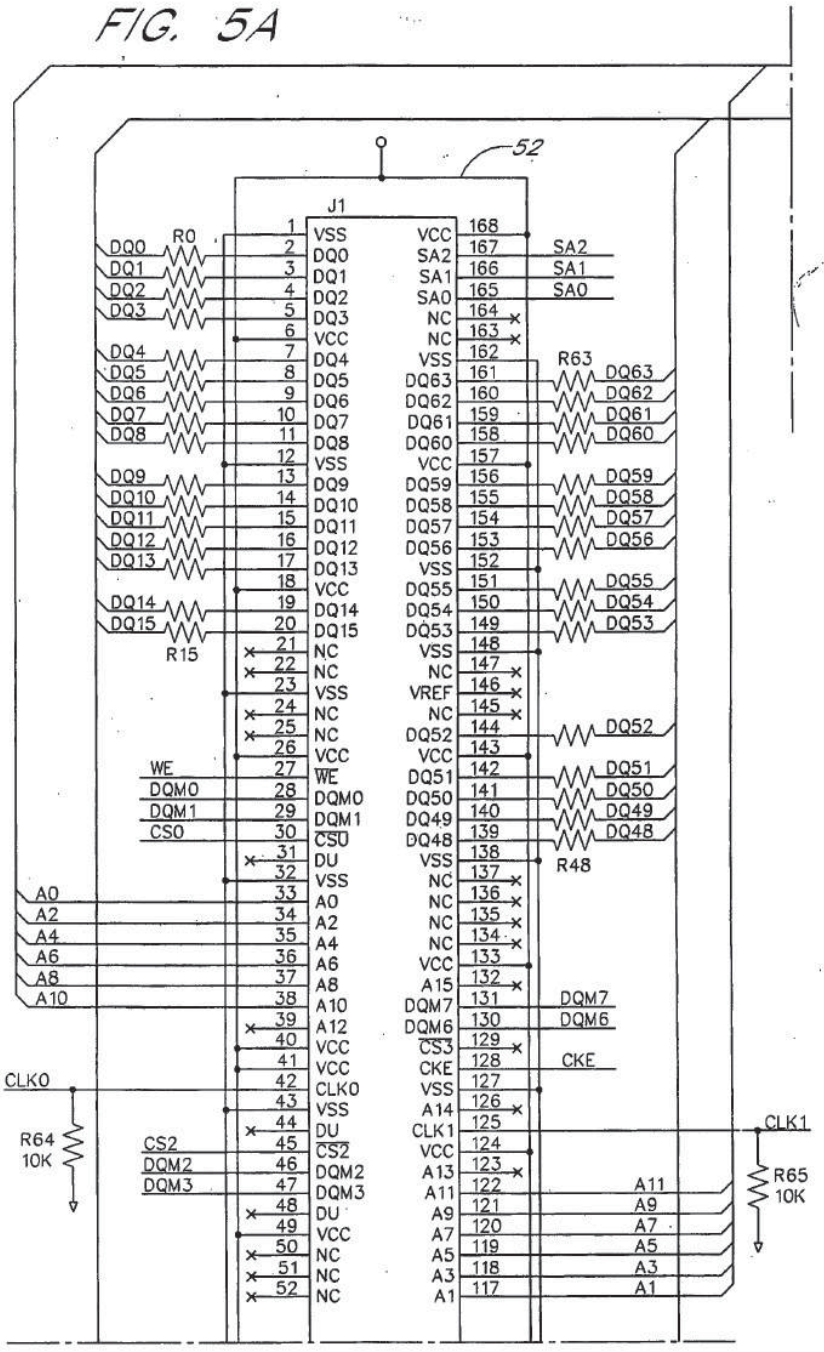


FIG. 5

FIG. 5A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CS0
CS2
DQM2
DQM3
CKE
DQM7
DQM6
SA2
SA1
SA0
A0
A2
A4
A6
A8
A10
A12
A15
A14
A13
A11
A9
A7
A5
A3
A1
DU
VREF
VSS
VCC
NC
DQ0
DQ1
DQ2
DQ3
DQ4
DQ5
DQ6
DQ7
DQ8
DQ9
DQ10
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DQ48
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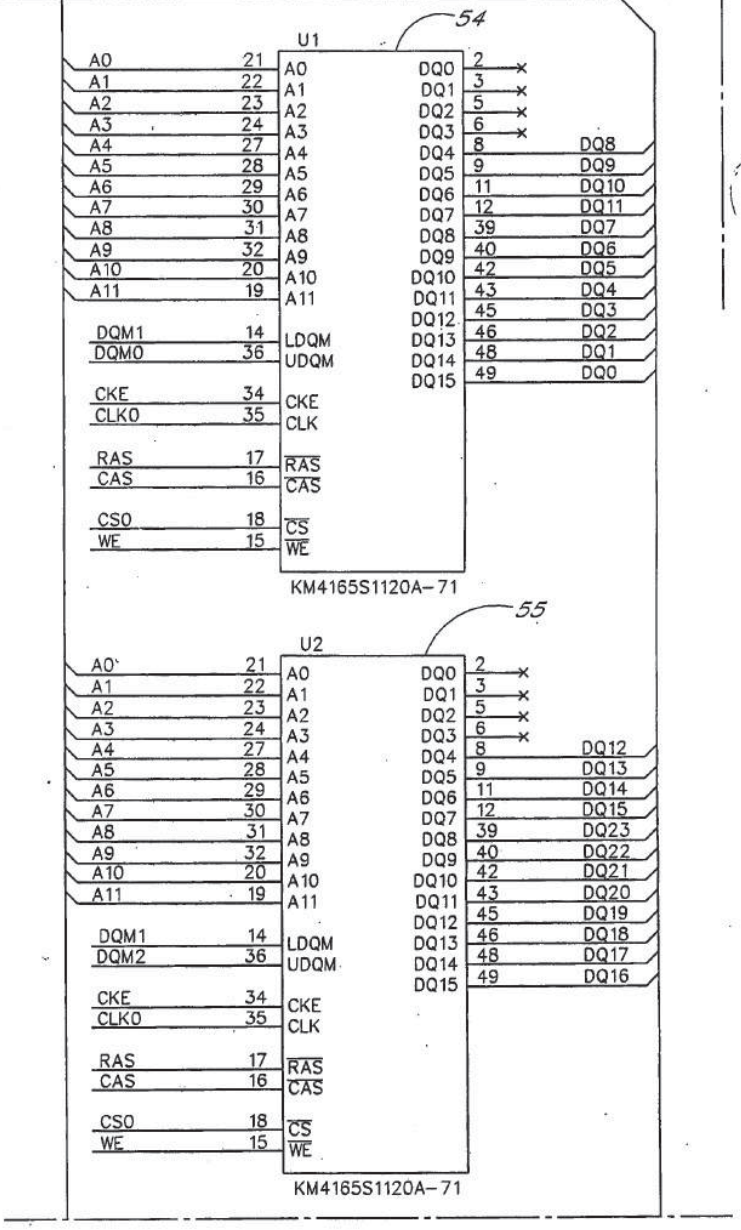
DQ63

FIG. 5B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A11 19
DQM1 14
DQM0 36
CKE 34
CLK0 35
RAS 17
CAS 16
CS0 18
WE 15
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LDQM
UDQM
CKE
CLK
RAS
CAS
CS
WE
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DQ7 12 DQ11
DQ8 39 DQ7
DQ9 40 DQ6
DQ10 42 DQ5
DQ11 43 DQ4
DQ12 45 DQ3
DQ13 46 DQ2
DQ14 48 DQ1
DQ15 49 DQ0
KM4165S1120A-71
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A9 32
A10 20
A11 19
DQM1 14
DQM2 36
CKE 34
CLK0 35
RAS 17
CAS 16
CS0 18
WE 15
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LDQM
UDQM
CKE
CLK
RAS
CAS
CS
WE
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DQ3 6
DQ4 8 DQ12
DQ5 9 DQ13
DQ6 11 DQ14
DQ7 12 DQ15
DQ8 39 DQ23
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DQ15 49 DQ16
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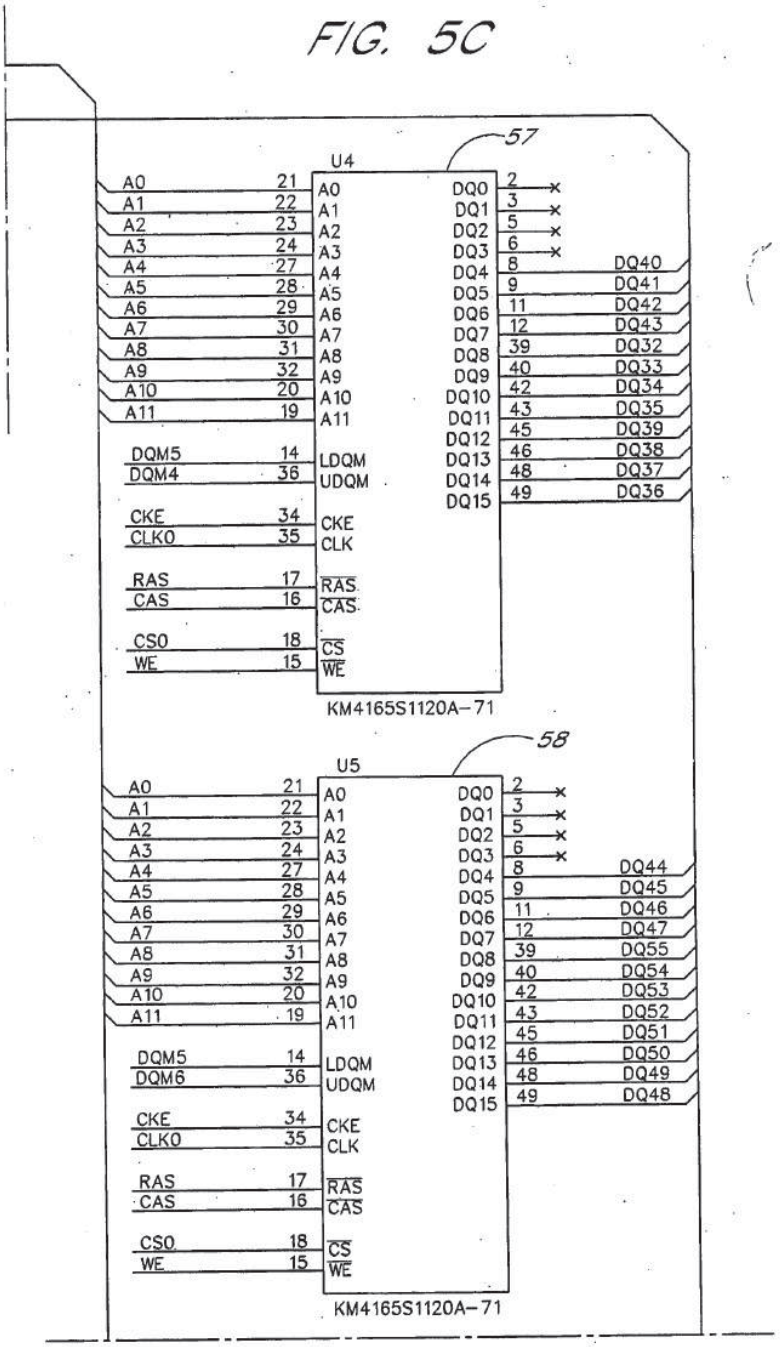
FIG. 5C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U4
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A3 24 A3
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A6 29 A6
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A9 32 A9
A10 20 A10
A11 19 A11
DQM5 14 LDQM
DQM4 36 UDQM
CKE 34 CKE
CLK0 35 CLK
RAS 17 RAS
CAS 16 CAS
CS0 18 CS
WE 15 WE
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DQ1 3
DQ2 5
DQ3 6
DQ4 8 DQ40
DQ5 9 DQ41
DQ6 11 DQ42
DQ7 12 DQ43
DQ8 39 DQ32
DQ9 40 DQ33
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DQ12 45 DQ39
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DQ14 48 DQ37
DQ15 49 DQ36
KM4165S1120A-71
58
U5
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A1 22 A1
A2 23 A2
A3 24 A3
A4 27 A4
A5 28 A5
A6 29 A6
A7 30 A7
A8 31 A8
A9 32 A9
A10 20 A10
A11 19 A11
DQM5 14 LDQM
DQM6 36 UDQM
CKE 34 CKE
CLK0 35 CLK
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CS0 18 CS
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DQ0 2
DQ1 3
DQ2 5
DQ3 6
DQ4 8 DQ44
DQ5 9 DQ45
DQ6 11 DQ46
DQ7 12 DQ47
DQ8 39 DQ55
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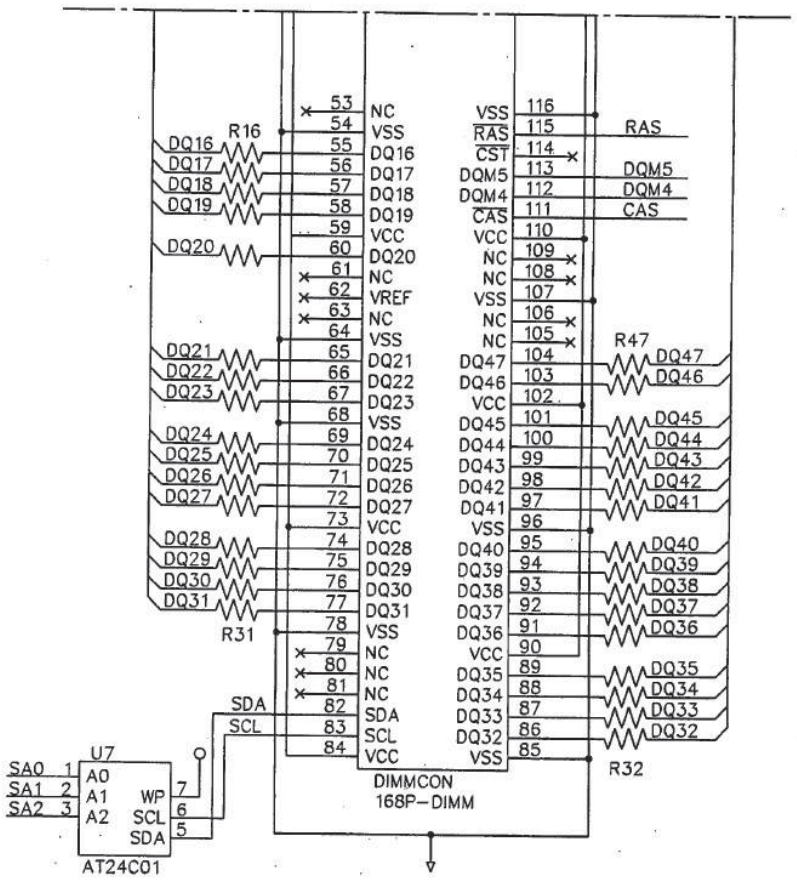
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DQ17
DQ18
DQ19
DQ20
DQ21
DQ22
DQ23
DQ24
DQ25
DQ26
DQ27
DQ28
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R31
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55 DQ16
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57 DQ18
58 DQ19
59 VCC
60 DQ20
61 NC
62 VREF
63 NC
64 VSS
65 DQ21
66 DQ22
67 DQ23
68 VSS
69 DQ24
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71 DQ26
72 DQ27
73 VCC
74 DQ28
75 DQ29
76 DQ30
77 DQ31
78 VSS
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80 NC
81 NC
82 SDA
83 SCL
84 VCC
VSS 116
RAS 115
CST 114
DQM5 113
DQM4 112
CAS 111
VCC 110
NC 109
NC 108
VSS 107
NC 106
NC 105
DQ47 104
DQ46 103
VCC 102
DQ45 101
DQ44 100
DQ43 99
DQ42 98
DQ41 97
VSS 96
DQ40 95
DQ39 94
DQ38 93
DQ37 92
DQ36 91
VCC 90
DQ35 89
DQ34 88
DQ33 87
DQ32 86
VSS 85
RAS
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DQ45
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DQ43
DQ42
DQ41
DQ40
DQ39
DQ38
DQ37
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SDA
SCL
U7
SA0 1
SA1 2
SA2 3
A0
A1
A2
WP 7
SCL 6
SDA 5
AT24C01

FIG. 5D

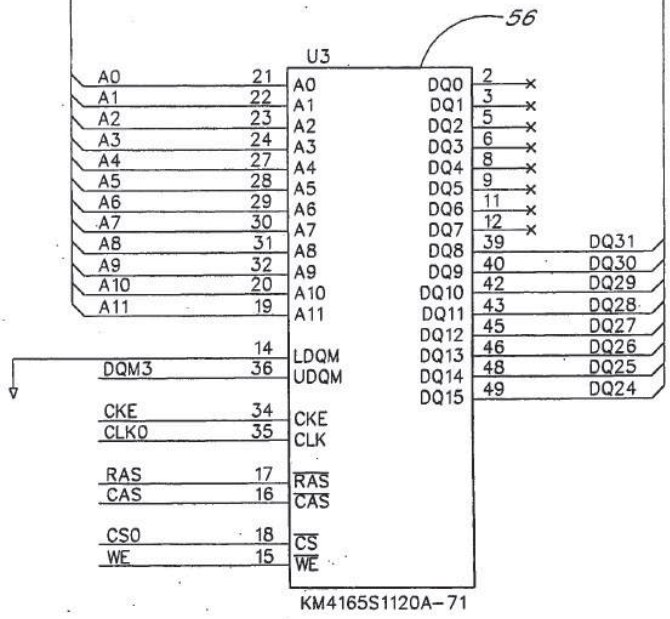

56
U3
A0 21 A0
A1 22 A1
A2 23 A2
A3 24 A3
A4 27 A4
A5 28 A5
A6 29 A6
A7 30 A7
A8 31 A8
A9 32 A9
A10 20 A10
A11 19 A11
14 LDQM
DQM3 36 UDQM
CKE 34 CKE
CLK0 35 CLK
RAS 17 RAS
CAS 16 CAS
CS0 18 CS
WE 15 WE
DQ0 2
DQ1 3
DQ2 5
DQ3 6
DQ4 8
DQ5 9
DQ6 11
DQ7 12
DQ8 39 DQ31
DQ9 40 DQ30
DQ10 42 DQ29
DQ11 43 DQ28
DQ12 45 DQ27
DQ13 46 DQ26
DQ14 48 DQ25
DQ15 49 DQ24
KM4165S1120A-71

FIG. 5E

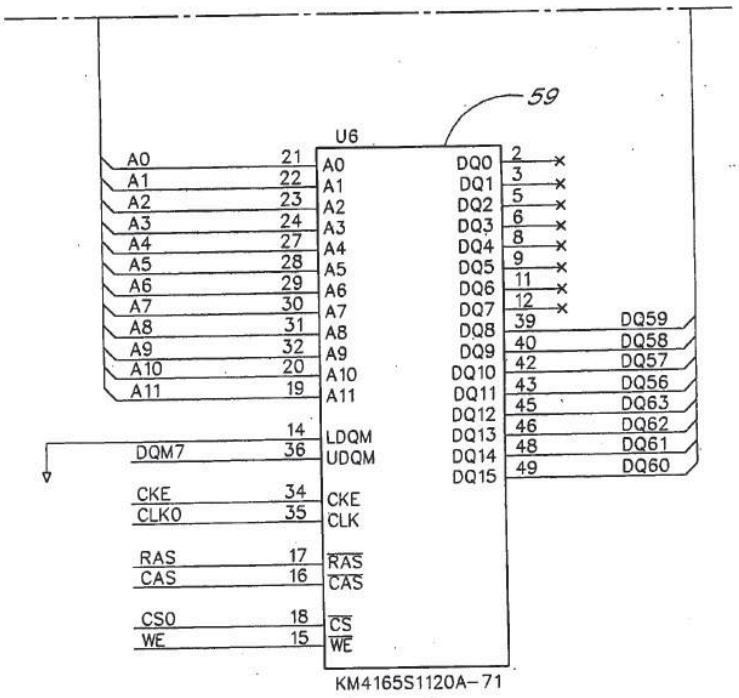

59
U6
A0 21 A0
A1 22 A1
A2 23 A2
A3 24 A3
A4 27 A4
A5 28 A5
A6 29 A6
A7 30 A7
A8 31 A8
A9 32 A9
A10 20 A10
A11 19 A11
14 LDQM
DQM7 36 UDQM
CKE 34 CKE
CLK0 35 CLK
RAS 17 RAS
CAS 16 CAS
CS0 18 CS
WE 15 WE
DQ0 2
DQ1 3
DQ2 5
DQ3 6
DQ4 8
DQ5 9
DQ6 11
DQ7 12
DQ8 39 DQ59
DQ9 40 DQ58
DQ10 42 DQ57
DQ11 43 DQ56
DQ12 45 DQ63
DQ13 46 DQ62
DQ14 48 DQ61
DQ15 49 DQ60
KM4165S1120A-71

FIG. 5F

FIG. 6A	FIG. 6B	FIG. 6C	FIG. 6D	FIG. 6E
FIG. 6F	FIG. 6G	FIG. 6H	FIG. 6I	FIG. 6J

FIG. 6

FIG. 6A

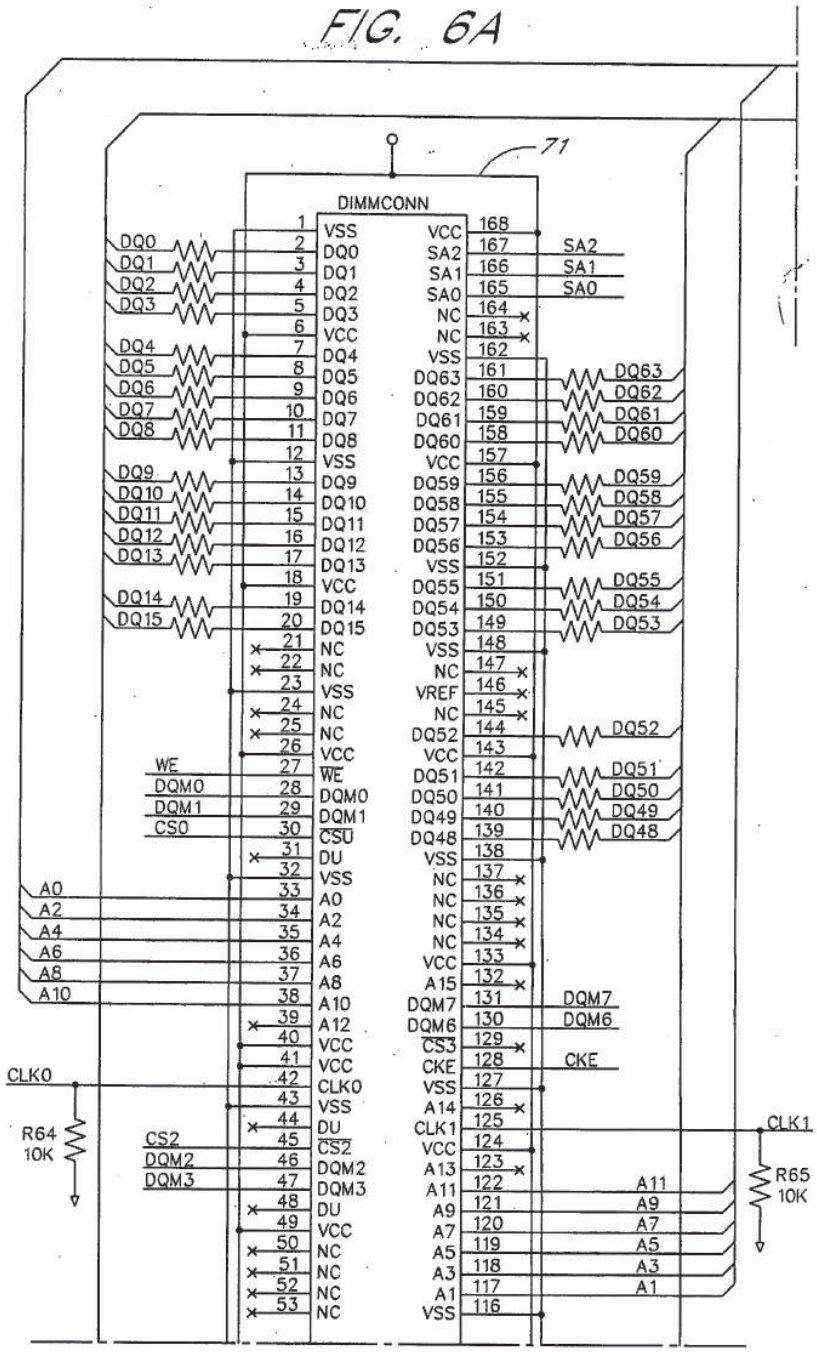

71
DIMMCONN
1 VSS
2 DQ0
3 DQ1
4 DQ2
5 DQ3
6 VCC
7 DQ4
8 DQ5
9 DQ6
10 DQ7
11 DQ8
12 VSS
13 DQ9
14 DQ10
15 DQ11
16 DQ12
17 DQ13
18 VCC
19 DQ14
20 DQ15
21 NC
22 NC
23 VSS
24 NC
25 NC
26 VCC
27 WE
28 DQM0
29 DQM1
30 CS0
31 DU
32 VSS
33 A0
34 A2
35 A4
36 A6
37 A8
38 A10
39 A12
40 VCC
41 VCC
42 CLK0
43 VSS
44 DU
45 CS2
46 DQM2
47 DQM3
48 DU
49 VCC
50 NC
51 NC
52 NC
53 NC
168 VCC
167 SA2
166 SA1
165 SA0
164 NC
163 NC
162 VSS
161 DQ63
160 DQ62
159 DQ61
158 DQ60
157 VCC
156 DQ59
155 DQ58
154 DQ57
153 DQ56
152 VSS
151 DQ55
150 DQ54
149 DQ53
148 VSS
147 NC
146 VREF
145 NC
144 DQ52
143 VCC
142 DQ51
141 DQ50
140 DQ49
139 DQ48
138 VSS
137 NC
136 NC
135 NC
134 NC
133 VCC
132 A15
131 DQM7
130 DQM6
129 CS3
128 CKE
127 VSS
126 A14
125 CLK1
124 VCC
123 A13
122 A11
121 A9
120 A7
119 A5
118 A3
117 A1
116 VSS
DQ0
DQ1
DQ2
DQ3
DQ4
DQ5
DQ6
DQ7
DQ8
DQ9
DQ10
DQ11
DQ12
DQ13
DQ14
DQ15
WE
DQM0
DQM1
CS0
A0
A2
A4
A6
A8
A10
CLK0
R64
10K
CS2
DQM2
DQM3
SA2
SA1
SA0
DQ63
DQ62
DQ61
DQ60
DQ59
DQ58
DQ57
DQ56
DQ55
DQ54
DQ53
DQ52
DQ51
DQ50
DQ49
DQ48
DQM7
DQM6
CKE
CLK1
R65
10K
A11
A9
A7
A5
A3
A1

FIG. 6B

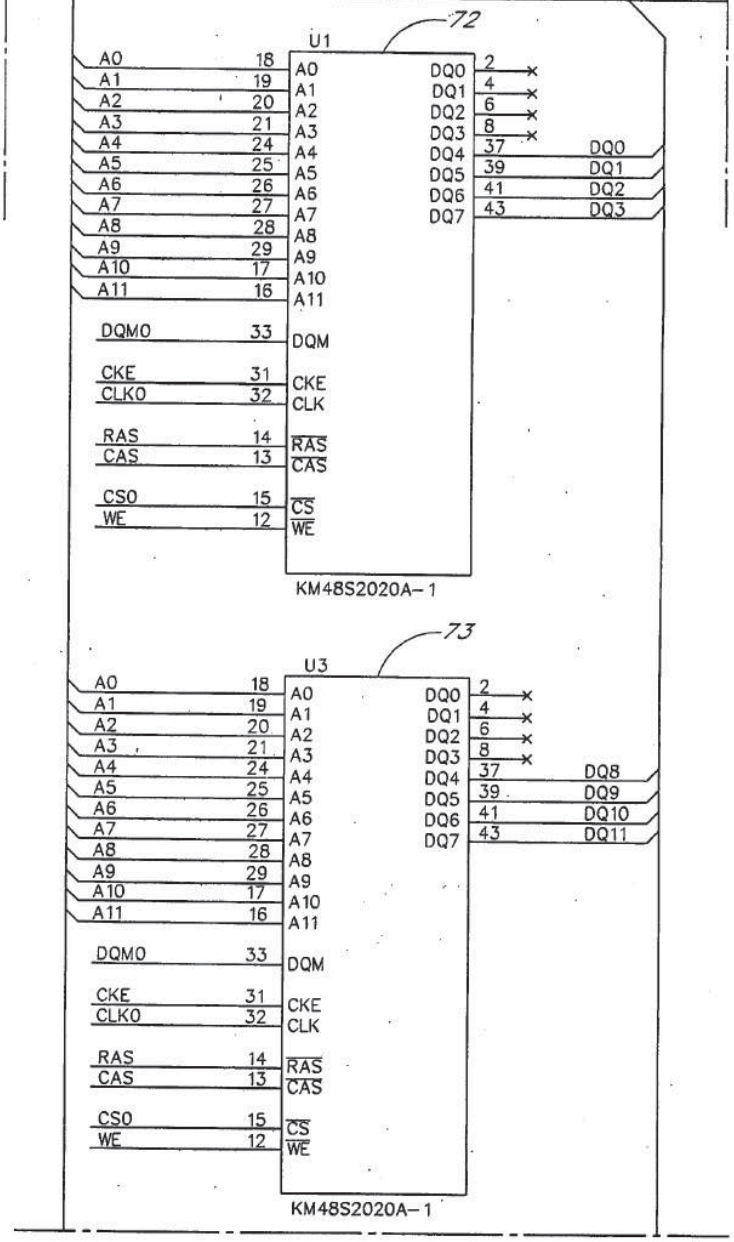

72
U1
A0 18
A1 19
A2 20
A3 21
A4 24
A5 25
A6 26
A7 27
A8 28
A9 29
A10 17
A11 16
DQM0 33
CKE 31
CLK0 32
RAS 14
CAS 13
CS0 15
WE 12
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
DQM
CKE
CLK
RAS
CAS
CS
WE
DQ0 2
DQ1 4
DQ2 6
DQ3 8
DQ4 37
DQ5 39
DQ6 41
DQ7 43
DQ0
DQ1
DQ2
DQ3
KM48S2020A-1
73
U3
A0 18
A1 19
A2 20
A3 21
A4 24
A5 25
A6 26
A7 27
A8 28
A9 29
A10 17
A11 16
DQM0 33
CKE 31
CLK0 32
RAS 14
CAS 13
CS0 15
WE 12
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
DQM
CKE
CLK
RAS
CAS
CS
WE
DQ0 2
DQ1 4
DQ2 6
DQ3 8
DQ4 37
DQ5 39
DQ6 41
DQ7 43
DQ8
DQ9
DQ10
DQ11
KM48S2020A-1

FIG. 6C

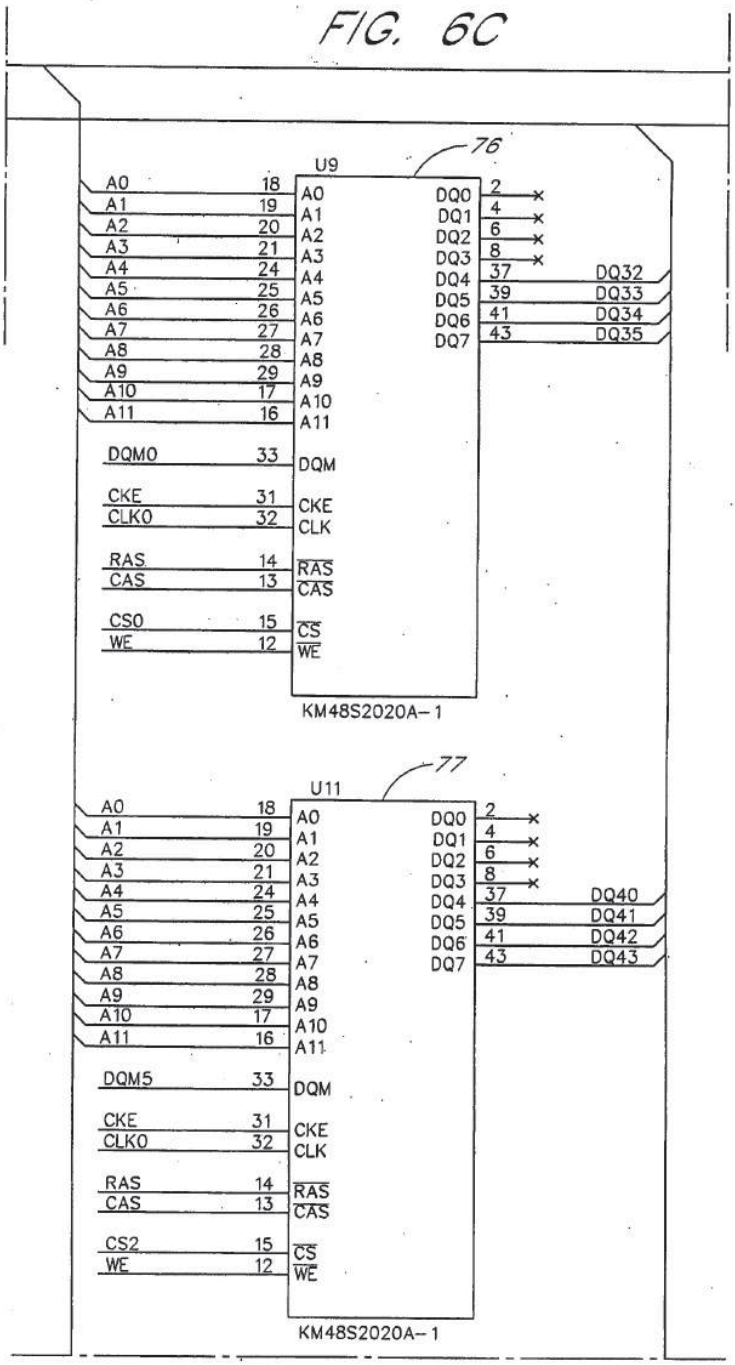

U9
76
A0 18
A1 19
A2 20
A3 21
A4 24
A5 25
A6 26
A7 27
A8 28
A9 29
A10 17
A11 16
DQM0 33
CKE 31
CLK0 32
RAS 14
CAS 13
CS0 15
WE 12
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
DQM
CKE
CLK
RAS
CAS
CS
WE
DQ0 2
DQ1 4
DQ2 6
DQ3 8
DQ4 37 DQ32
DQ5 39 DQ33
DQ6 41 DQ34
DQ7 43 DQ35
KM48S2020A-1
U11
77
A0 18
A1 19
A2 20
A3 21
A4 24
A5 25
A6 26
A7 27
A8 28
A9 29
A10 17
A11 16
DQM5 33
CKE 31
CLK0 32
RAS 14
CAS 13
CS2 15
WE 12
DQ0 2
DQ1 4
DQ2 6
DQ3 8
DQ4 37 DQ40
DQ5 39 DQ41
DQ6 41 DQ42
DQ7 43 DQ43
KM48S2020A-1

FIG. 6D

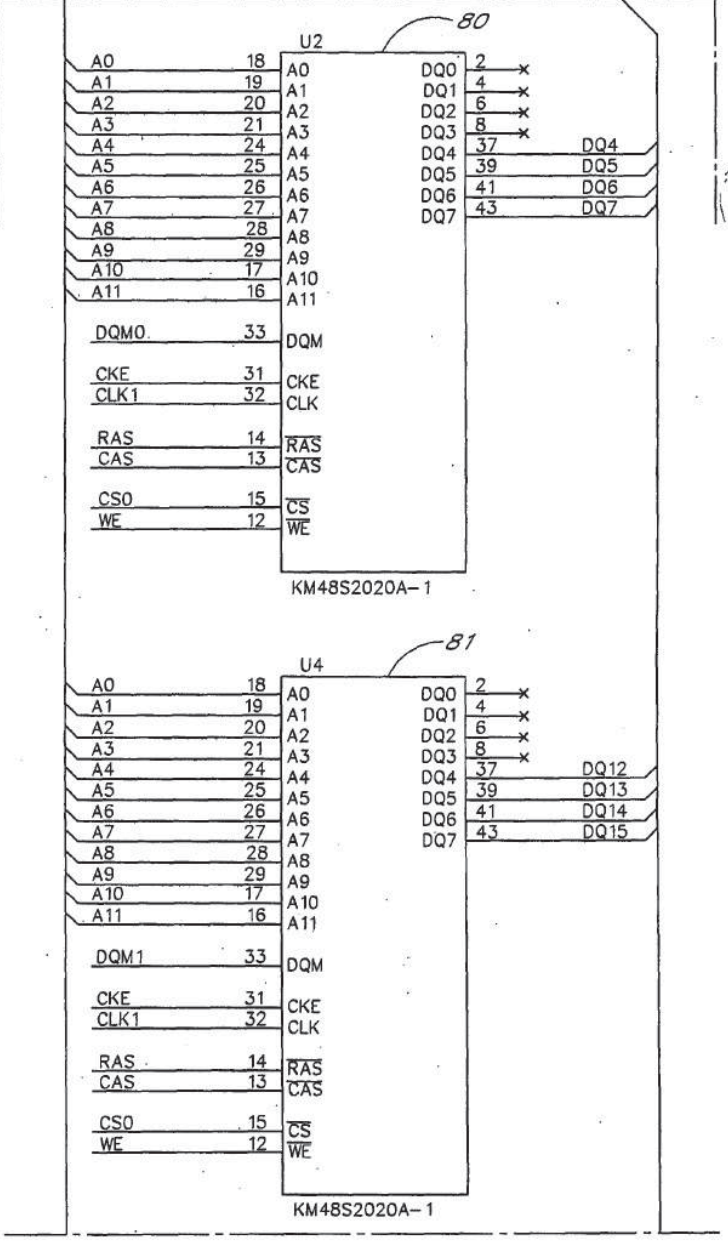
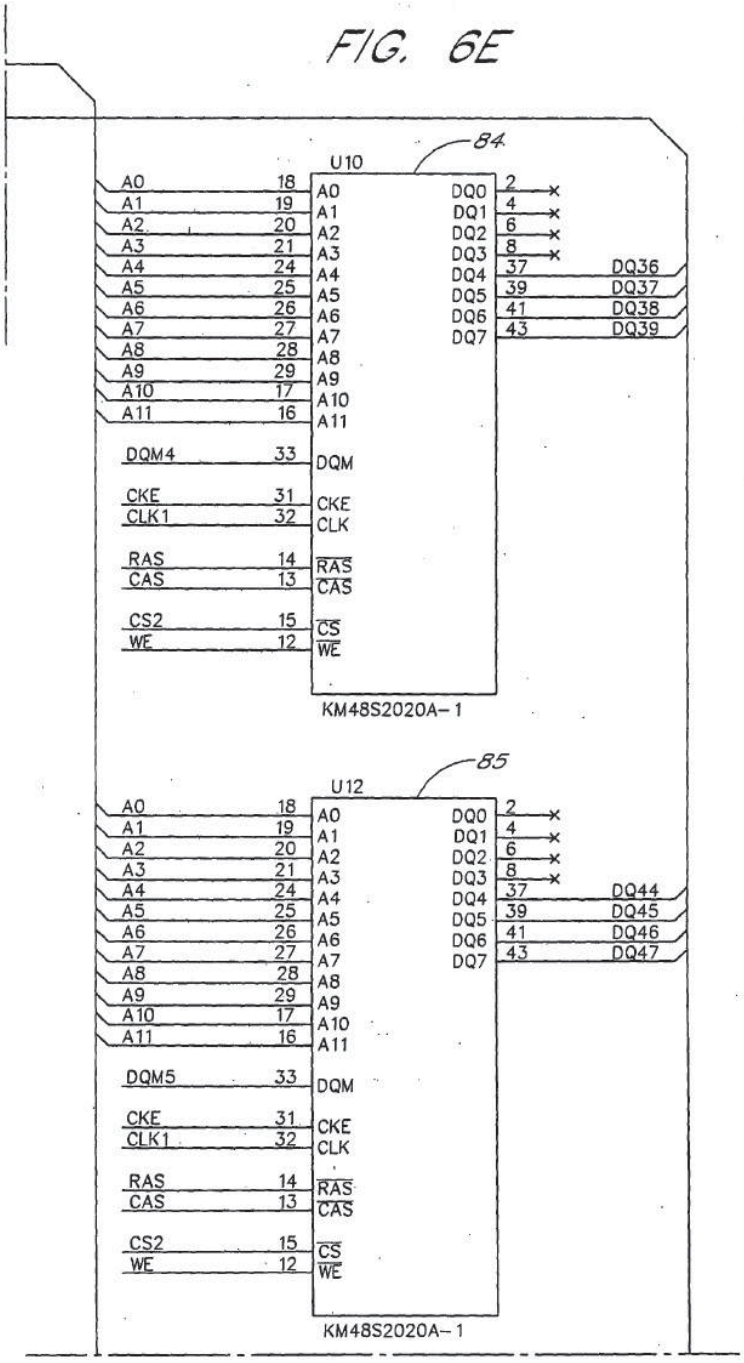

80
U2
A0 18
A1 19
A2 20
A3 21
A4 24
A5 25
A6 26
A7 27
A8 28
A9 29
A10 17
A11 16
DQM0 33
CKE 31
CLK1 32
RAS 14
CAS 13
CS0 15
WE 12
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
DQM
CKE
CLK
RAS
CAS
CS
WE
DQ0 2
DQ1 4
DQ2 6
DQ3 8
DQ4 37 DQ4
DQ5 39 DQ5
DQ6 41 DQ6
DQ7 43 DQ7
KM48S2020A-1
81
U4
A0 18
A1 19
A2 20
A3 21
A4 24
A5 25
A6 26
A7 27
A8 28
A9 29
A10 17
A11 16
DQM1 33
CKE 31
CLK1 32
RAS 14
CAS 13
CS0 15
WE 12
DQ0 2
DQ1 4
DQ2 6
DQ3 8
DQ4 37 DQ12
DQ5 39 DQ13
DQ6 41 DQ14
DQ7 43 DQ15
KM48S2020A-1

FIG. 6E


84
U10
A0 18
A1 19
A2 20
A3 21
A4 24
A5 25
A6 26
A7 27
A8 28
A9 29
A10 17
A11 16
DQM4 33
CKE 31
CLK1 32
RAS 14
CAS 13
CS2 15
WE 12
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
DQM
CKE
CLK
RAS
CAS
CS
WE
DQ0 2
DQ1 4
DQ2 6
DQ3 8
DQ4 37 DQ36
DQ5 39 DQ37
DQ6 41 DQ38
DQ7 43 DQ39
KM48S2020A-1
85
U12
A0 18
A1 19
A2 20
A3 21
A4 24
A5 25
A6 26
A7 27
A8 28
A9 29
A10 17
A11 16
DQM5 33
CKE 31
CLK1 32
RAS 14
CAS 13
CS2 15
WE 12
DQ0 2
DQ1 4
DQ2 6
DQ3 8
DQ4 37 DQ44
DQ5 39 DQ45
DQ6 41 DQ46
DQ7 43 DQ47
KM48S2020A-1

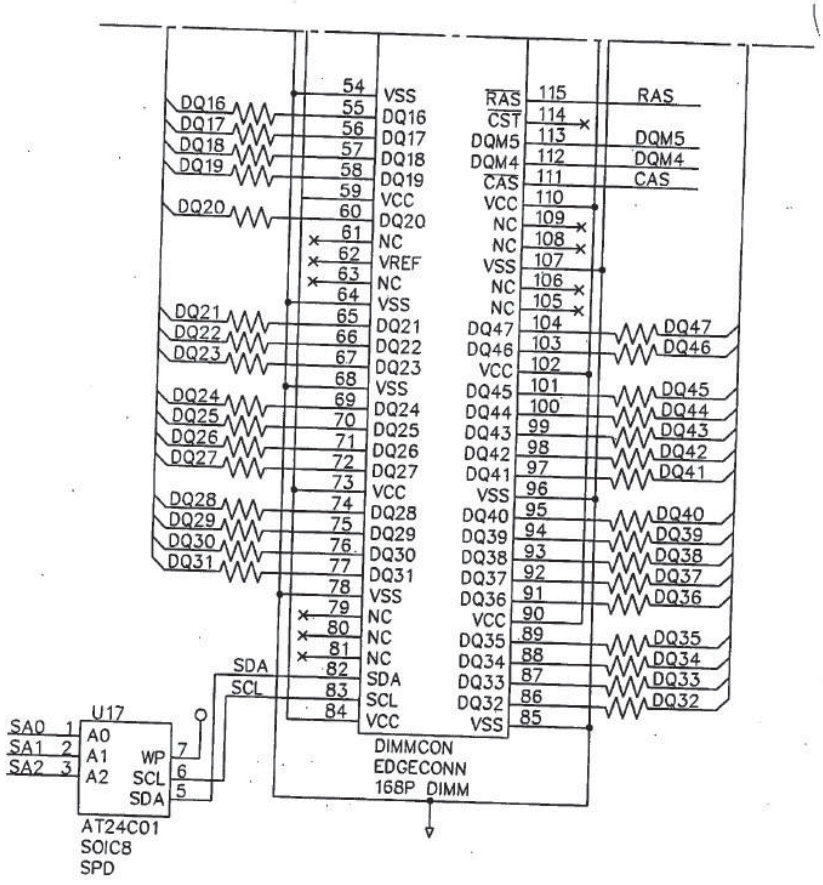

DQ16
DQ17
DQ18
DQ19
DQ20
DQ21
DQ22
DQ23
DQ24
DQ25
DQ26
DQ27
DQ28
DQ29
DQ30
DQ31
54 VSS
55 DQ16
56 DQ17
57 DQ18
58 DQ19
59 VCC
60 DQ20
61 NC
62 VREF
63 NC
64 VSS
65 DQ21
66 DQ22
67 DQ23
68 VSS
69 DQ24
70 DQ25
71 DQ26
72 DQ27
73 VCC
74 DQ28
75 DQ29
76 DQ30
77 DQ31
78 VSS
79 NC
80 NC
81 NC
82 SDA
83 SCL
84 VCC
RAS 115
CST 114
DQM5 113
DQM4 112
CAS 111
VCC 110
NC 109
NC 108
VSS 107
NC 106
NC 105
DQ47 104
DQ46 103
VCC 102
DQ45 101
DQ44 100
DQ43 99
DQ42 98
DQ41 97
VSS 96
DQ40 95
DQ39 94
DQ38 93
DQ37 92
DQ36 91
VCC 90
DQ35 89
DQ34 88
DQ33 87
DQ32 86
VSS 85
RAS
DQM5
DQM4
CAS
DQ47
DQ46
DQ45
DQ44
DQ43
DQ42
DQ41
DQ40
DQ39
DQ38
DQ37
DQ36
DQ35
DQ34
DQ33
DQ32
DIMMCON
EDGECONN
168P DIMM
SDA
SCL
U17
SA0 1
SA1 2
SA2 3
A0
A1
A2
WP 7
SCL 6
SDA 5
AT24C01
SOIC8
SPD

FIG. 6F

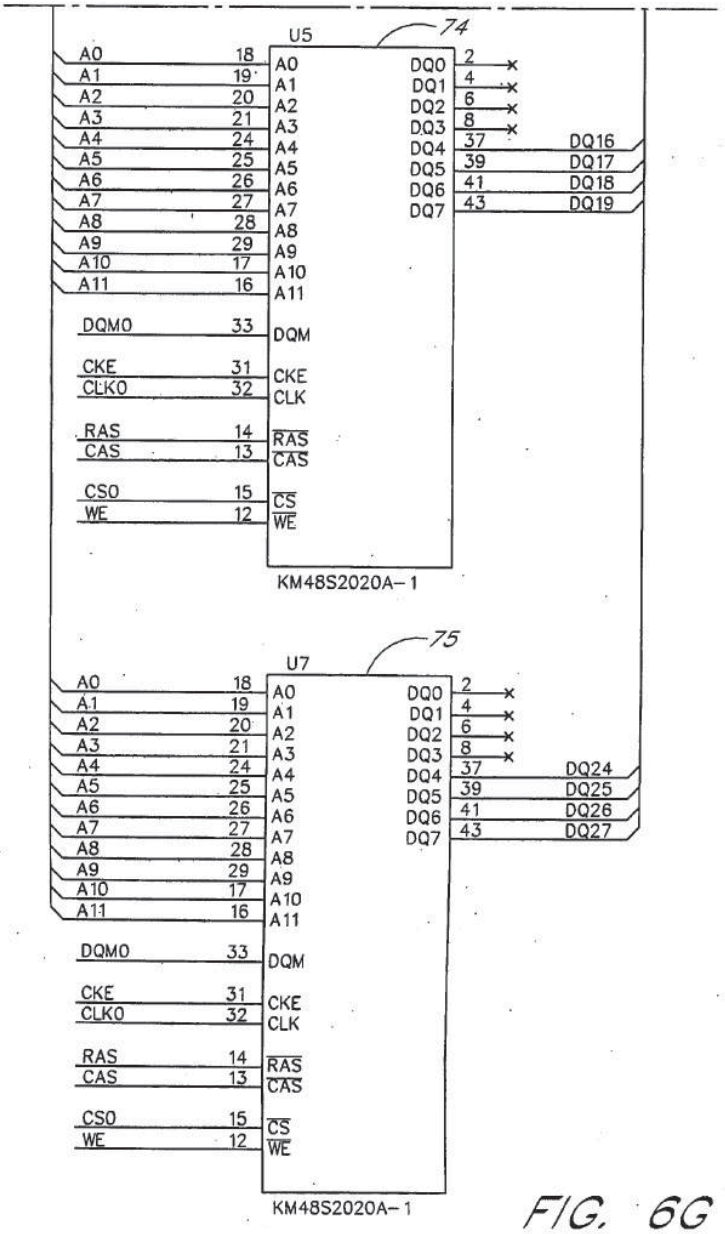

U5
74
A0 18
A1 19
A2 20
A3 21
A4 24
A5 25
A6 26
A7 27
A8 28
A9 29
A10 17
A11 16
DQM0 33
CKE 31
CLK0 32
RAS 14
CAS 13
CS0 15
WE 12
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
DQM
CKE
CLK
RAS
CAS
CS
WE
DQ0 2
DQ1 4
DQ2 6
DQ3 8
DQ4 37 DQ16
DQ5 39 DQ17
DQ6 41 DQ18
DQ7 43 DQ19
KM48S2020A-1
U7
75
A0 18
A1 19
A2 20
A3 21
A4 24
A5 25
A6 26
A7 27
A8 28
A9 29
A10 17
A11 16
DQM0 33
CKE 31
CLK0 32
RAS 14
CAS 13
CS0 15
WE 12
DQ0 2
DQ1 4
DQ2 6
DQ3 8
DQ4 37 DQ24
DQ5 39 DQ25
DQ6 41 DQ26
DQ7 43 DQ27
KM48S2020A-1

FIG. 6G

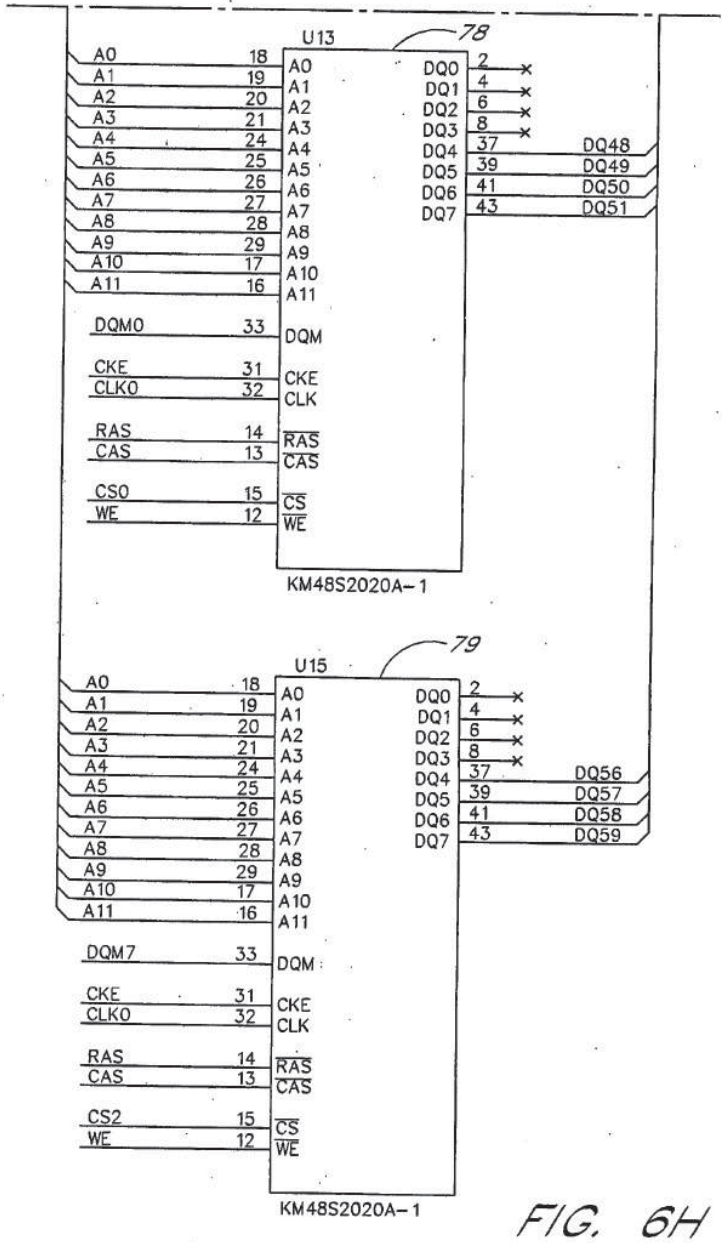

U13
78
A0 18
A1 19
A2 20
A3 21
A4 24
A5 25
A6 26
A7 27
A8 28
A9 29
A10 17
A11 16
DQM0 33
CKE 31
CLK0 32
RAS 14
CAS 13
CS0 15
WE 12
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
DQM
CKE
CLK
RAS
CAS
CS
WE
DQ0 2
DQ1 4
DQ2 6
DQ3 8
DQ4 37
DQ5 39
DQ6 41
DQ7 43
DQ48
DQ49
DQ50
DQ51
KM48S2020A-1
79
U15
A0 18
A1 19
A2 20
A3 21
A4 24
A5 25
A6 26
A7 27
A8 28
A9 29
A10 17
A11 16
DQM7 33
CKE 31
CLK0 32
RAS 14
CAS 13
CS2 15
WE 12
DQ0 2
DQ1 4
DQ2 6
DQ3 8
DQ4 37
DQ5 39
DQ6 41
DQ7 43
DQ56
DQ57
DQ58
DQ59
KM48S2020A-1

FIG. 6H

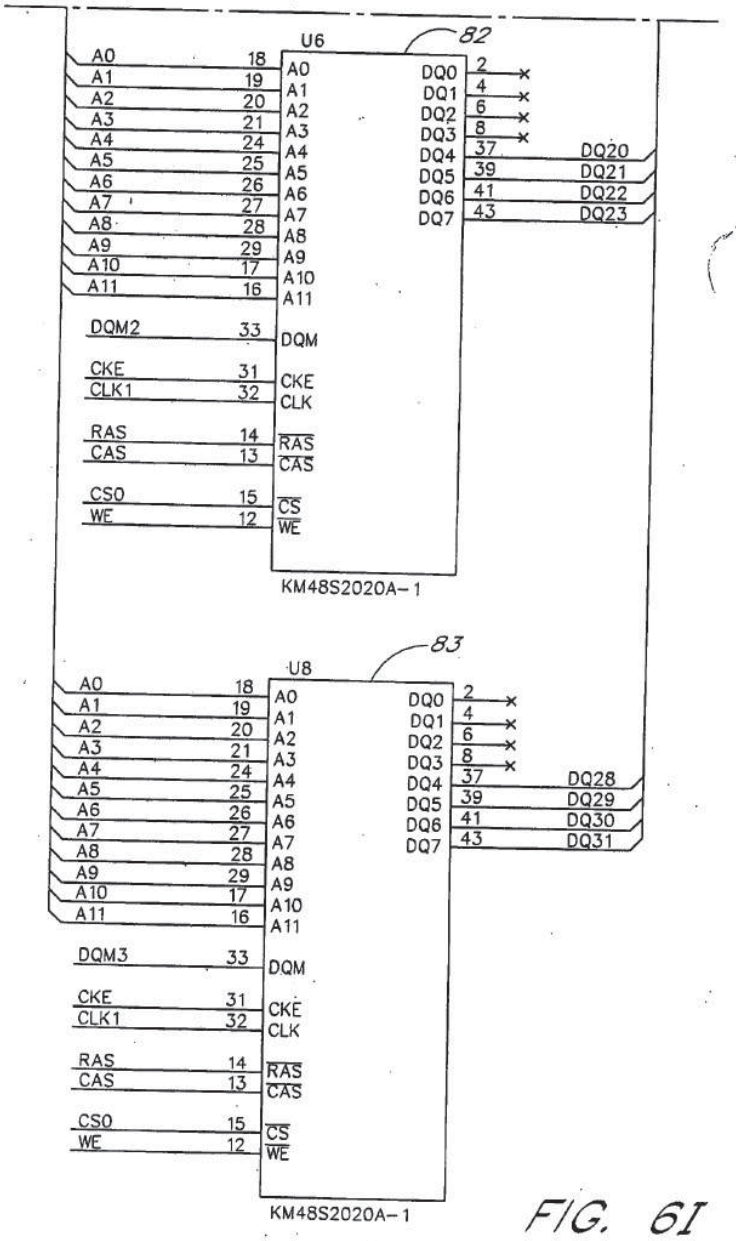

U6
82
A0 18
A1 19
A2 20
A3 21
A4 24
A5 25
A6 26
A7 27
A8 28
A9 29
A10 17
A11 16
DQM2 33
CKE 31
CLK1 32
RAS 14
CAS 13
CS0 15
WE 12
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
DQM
CKE
CLK
RAS
CAS
CS
WE
DQ0 2
DQ1 4
DQ2 6
DQ3 8
DQ4 37
DQ5 39
DQ6 41
DQ7 43
DQ20
DQ21
DQ22
DQ23
KM48S2020A-1
U8
83
A0 18
A1 19
A2 20
A3 21
A4 24
A5 25
A6 26
A7 27
A8 28
A9 29
A10 17
A11 16
DQM3 33
CKE 31
CLK1 32
RAS 14
CAS 13
CS0 15
WE 12
DQ0 2
DQ1 4
DQ2 6
DQ3 8
DQ4 37
DQ5 39
DQ6 41
DQ7 43
DQ28
DQ29
DQ30
DQ31
KM48S2020A-1

FIG. 6I

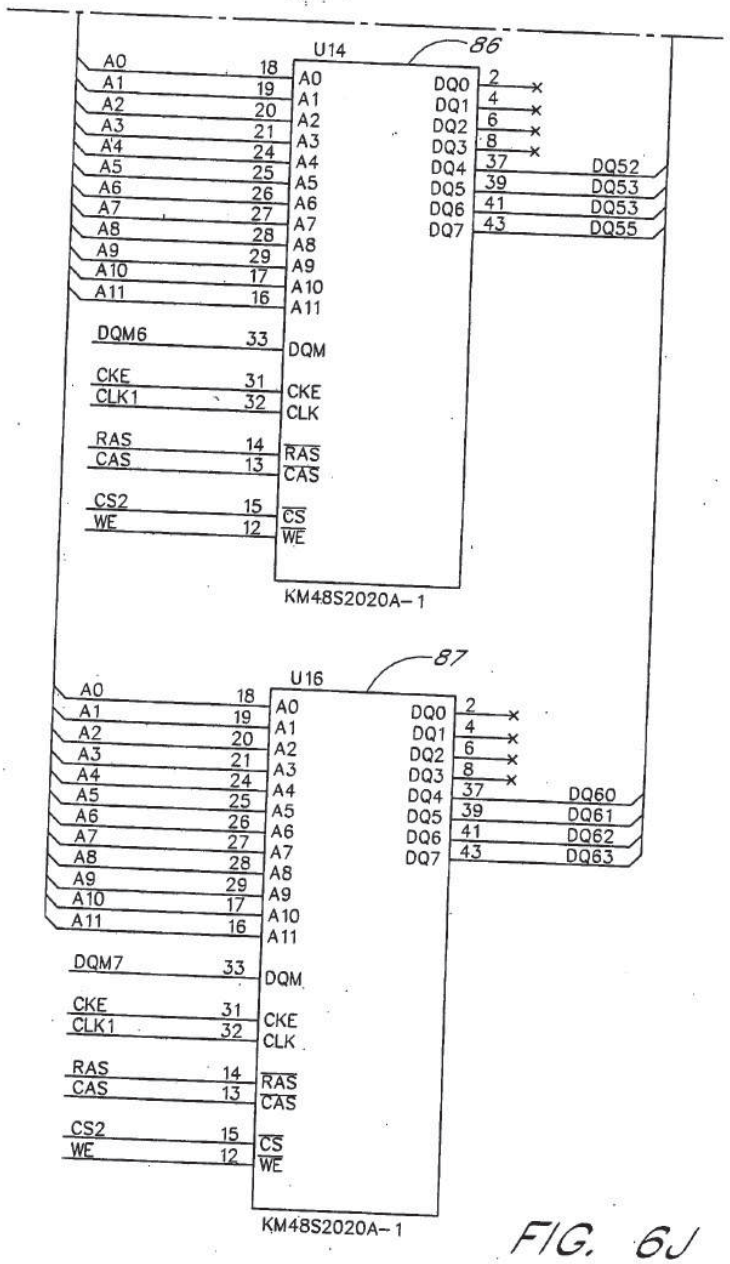

U14
86
A0 18
A1 19
A2 20
A3 21
A4 24
A5 25
A6 26
A7 27
A8 28
A9 29
A10 17
A11 16
DQM6 33
CKE 31
CLK1 32
RAS 14
CAS 13
CS2 15
WE 12
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
DQM
CKE
CLK
RAS
CAS
CS
WE
DQ0 2
DQ1 4
DQ2 6
DQ3 8
DQ4 37 DQ52
DQ5 39 DQ53
DQ6 41 DQ53
DQ7 43 DQ55
KM48S2020A-1
U16
87
A0 18
A1 19
A2 20
A3 21
A4 24
A5 25
A6 26
A7 27
A8 28
A9 29
A10 17
A11 16
DQM7 33
CKE 31
CLK1 32
RAS 14
CAS 13
CS2 15
WE 12
DQ0 2
DQ1 4
DQ2 6
DQ3 8
DQ4 37 DQ60
DQ5 39 DQ61
DQ6 41 DQ62
DQ7 43 DQ63
KM48S2020A-1

FIG. 6J

FIG. 7A	FIG. 7B	FIG. 7C	FIG. 7D	FIG. 7E
FIG. 7F	FIG. 7G	FIG. 7H	FIG. 7I	FIG. 7J

FIG. 7

FIG. 7A

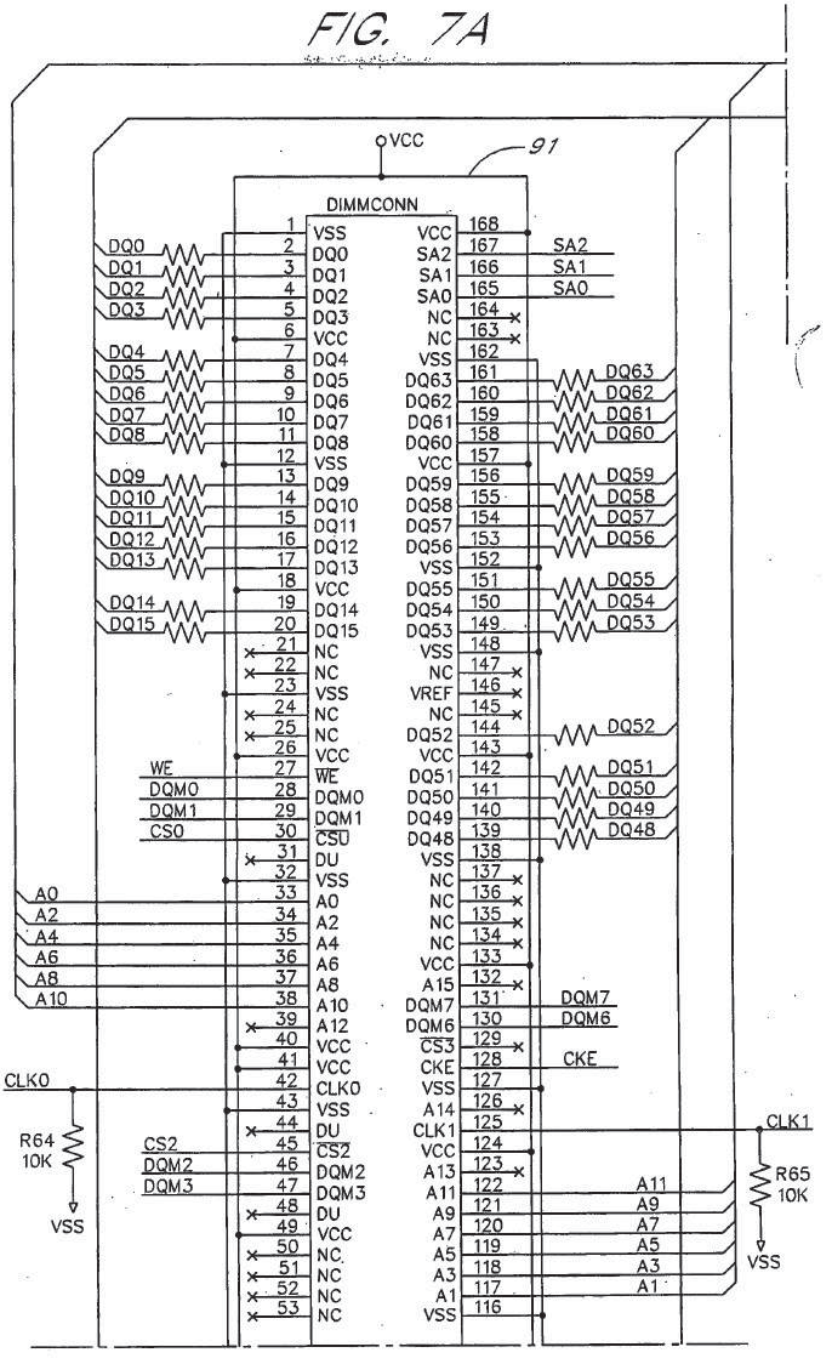

VCC
91
DIMMCONN
1 VSS
2 DQ0
3 DQ1
4 DQ2
5 DQ3
6 VCC
7 DQ4
8 DQ5
9 DQ6
10 DQ7
11 DQ8
12 VSS
13 DQ9
14 DQ10
15 DQ11
16 DQ12
17 DQ13
18 VCC
19 DQ14
20 DQ15
21 NC
22 NC
23 VSS
24 NC
25 NC
26 VCC
27 WE
28 DQM0
29 DQM1
30 CS0
31 DU
32 VSS
33 A0
34 A2
35 A4
36 A6
37 A8
38 A10
39 A12
40 VCC
41 VCC
42 CLK0
43 VSS
44 DU
45 CS2
46 DQM2
47 DQM3
48 DU
49 VCC
50 NC
51 NC
52 NC
53 NC
168 VCC
167 SA2
166 SA1
165 SA0
164 NC
163 NC
162 VSS
161 DQ63
160 DQ62
159 DQ61
158 DQ60
157 VCC
156 DQ59
155 DQ58
154 DQ57
153 DQ56
152 VSS
151 DQ55
150 DQ54
149 DQ53
148 VSS
147 NC
146 VREF
145 NC
144 DQ52
143 VCC
142 DQ51
141 DQ50
140 DQ49
139 DQ48
138 VSS
137 NC
136 NC
135 NC
134 NC
133 VCC
132 A15
131 DQM7
130 DQM6
129 CS3
128 CKE
127 VSS
126 A14
125 CLK1
124 VCC
123 A13
122 A11
121 A9
120 A7
119 A5
118 A3
117 A1
116 VSS
SA2
SA1
SA0
DQ63
DQ62
DQ61
DQ60
DQ59
DQ58
DQ57
DQ56
DQ55
DQ54
DQ53
DQ52
DQ51
DQ50
DQ49
DQ48
DQM7
DQM6
CKE
CLK1
A11
A9
A7
A5
A3
A1
DQ0
DQ1
DQ2
DQ3
DQ4
DQ5
DQ6
DQ7
DQ8
DQ9
DQ10
DQ11
DQ12
DQ13
DQ14
DQ15
WE
DQM0
DQM1
CS0
A0
A2
A4
A6
A8
A10
CLK0
R64
10K
VSS
CS2
DQM2
DQM3
R65
10K
VSS

FIG. 7B

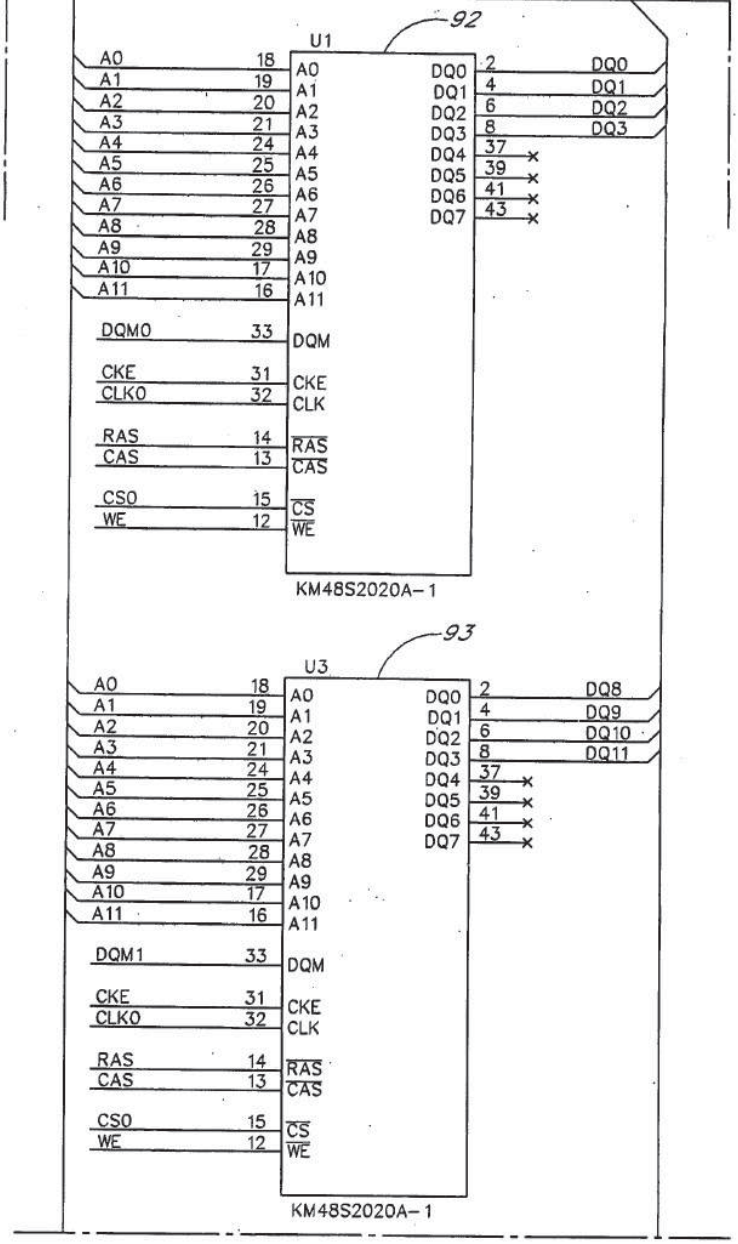
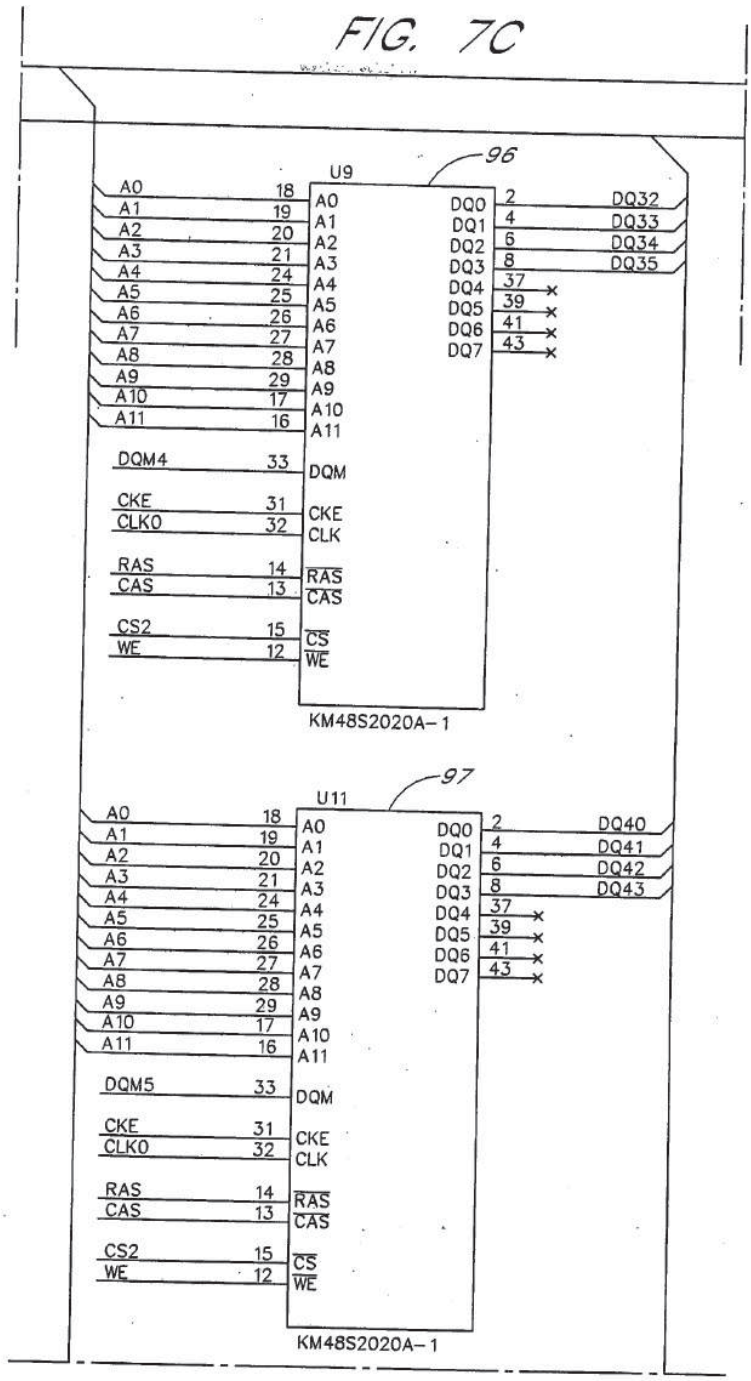

92
U1
A0 18
A1 19
A2 20
A3 21
A4 24
A5 25
A6 26
A7 27
A8 28
A9 29
A10 17
A11 16
DQM0 33
CKE 31
CLK0 32
RAS 14
CAS 13
CS0 15
WE 12
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
DQM
CKE
CLK
RAS
CAS
CS
WE
DQ0 2
DQ1 4
DQ2 6
DQ3 8
DQ4 37
DQ5 39
DQ6 41
DQ7 43
DQ0
DQ1
DQ2
DQ3
KM48S2020A-1
93
U3
A0 18
A1 19
A2 20
A3 21
A4 24
A5 25
A6 26
A7 27
A8 28
A9 29
A10 17
A11 16
DQM1 33
CKE 31
CLK0 32
RAS 14
CAS 13
CS0 15
WE 12
DQ0 2
DQ1 4
DQ2 6
DQ3 8
DQ4 37
DQ5 39
DQ6 41
DQ7 43
DQ8
DQ9
DQ10
DQ11
KM48S2020A-1

FIG. 7C


96
U9
A0 18
A1 19
A2 20
A3 21
A4 24
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A11 16
DQM4 33
CKE 31
CLK0 32
RAS 14
CAS 13
CS2 15
WE 12
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
DQM
CKE
CLK
RAS
CAS
CS
WE
DQ0 2
DQ1 4
DQ2 6
DQ3 8
DQ4 37
DQ5 39
DQ6 41
DQ7 43
DQ32
DQ33
DQ34
DQ35
KM48S2020A-1
97
U11
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A2 20
A3 21
A4 24
A5 25
A6 26
A7 27
A8 28
A9 29
A10 17
A11 16
DQM5 33
CKE 31
CLK0 32
RAS 14
CAS 13
CS2 15
WE 12
DQ0 2
DQ1 4
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DQ3 8
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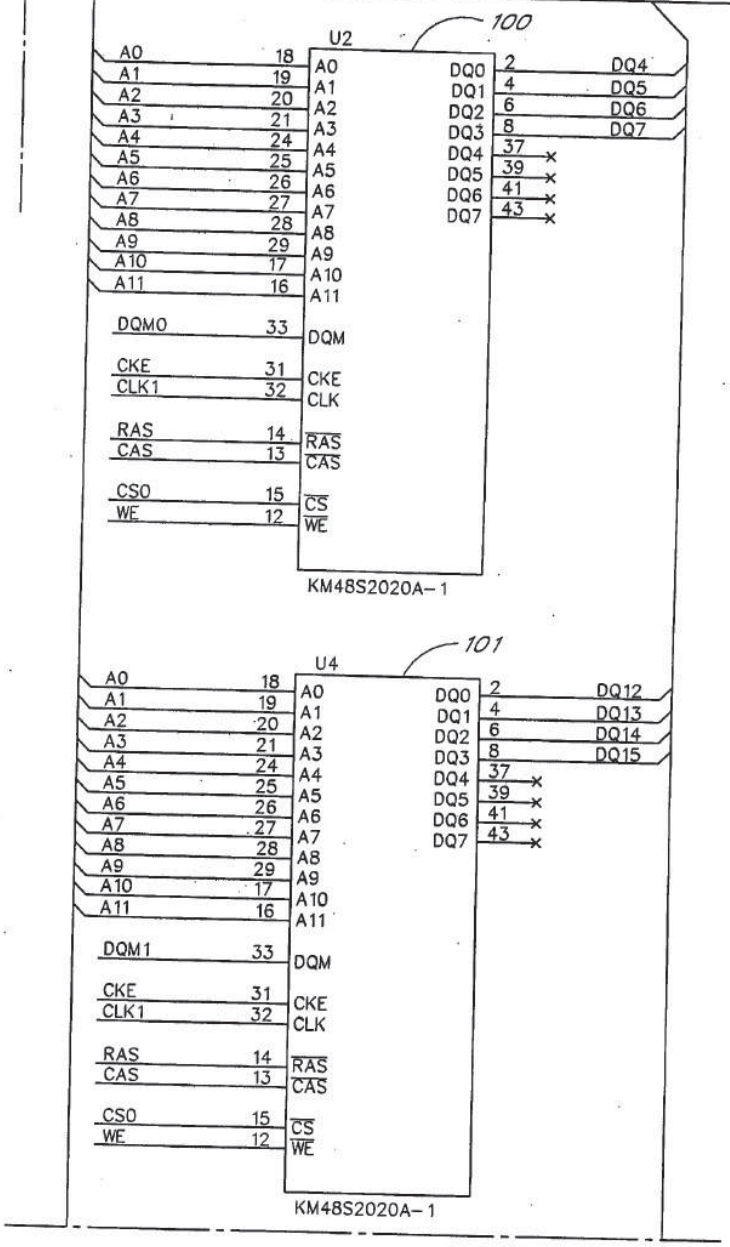
DQ40
DQ41
DQ42
DQ43
KM48S2020A-1

FIG. 7D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A1 19
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DQM0 33
CKE 31
CLK1 32
RAS 14
CAS 13
CS0 15
WE 12
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
DQM
CKE
CLK
RAS
CAS
CS
WE
DQ0 2
DQ1 4
DQ2 6
DQ3 8
DQ4 37
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DQ7 43
DQ4
DQ5
DQ6
DQ7
KM48S2020A-1
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U4
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A9 29
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A11 16
DQM1 33
CKE 31
CLK1 32
RAS 14
CAS 13
CS0 15
WE 12
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A1
A2
A3
A4
A5
A6
A7
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A9
A10
A11
DQM
CKE
CLK
RAS
CAS
CS
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DQ0 2
DQ1 4
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DQ3 8
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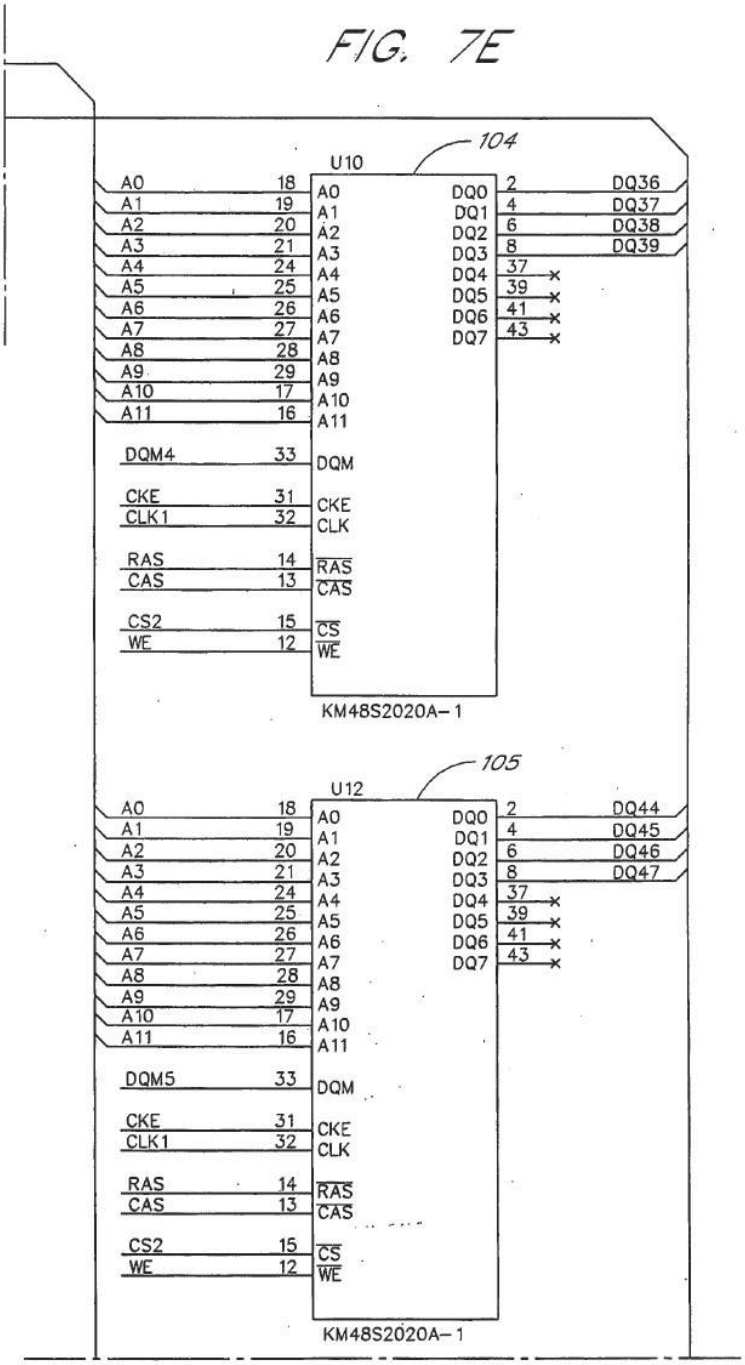
DQ14
DQ15
KM48S2020A-1

FIG. 7E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A3 21
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CLK1 32
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CAS 13
CS2 15
WE 12
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A1
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A3
A4
A5
A6
A7
A8
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A10
A11
DQM
CKE
CLK
RAS
CAS
CS
WE
DQ0 2
DQ1 4
DQ2 6
DQ3 8
DQ4 37
DQ5 39
DQ6 41
DQ7 43
DQ36
DQ37
DQ38
DQ39
KM48S2020A-1
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A2 20
A3 21
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A9 29
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A11 16
DQM5 33
CKE 31
CLK1 32
RAS 14
CAS 13
CS2 15
WE 12
DQ0 2
DQ1 4
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DQ5 39
DQ6 41
DQ7 43
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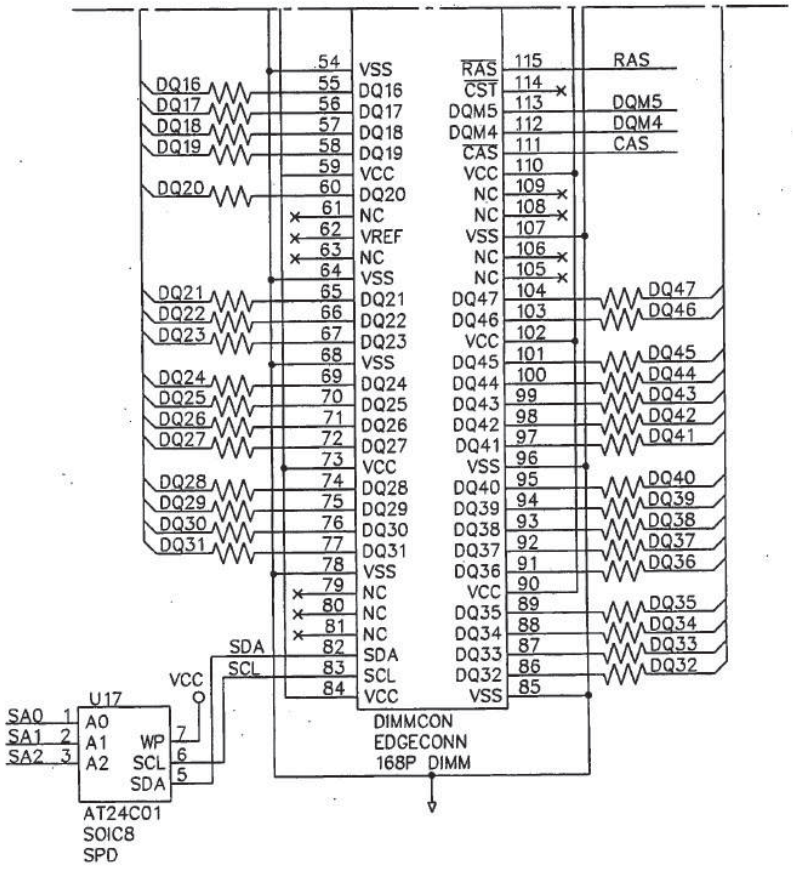
DQ45
DQ46
DQ47
KM48S2020A-1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WP
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DQM4
CAS
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DQ32
DQ33
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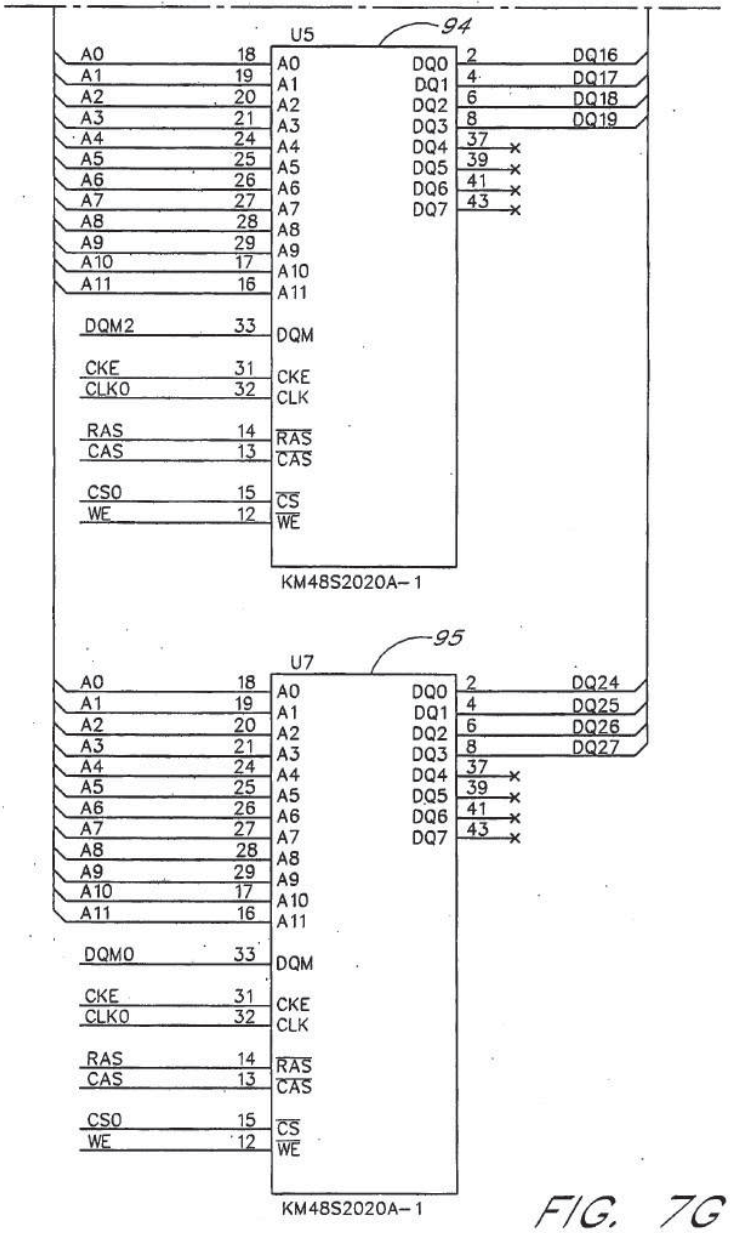
FIG. 7F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A10
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DQM
CKE
CLK
RAS
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DQ0 2
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DQ2 6
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DQ5 39
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DQ7 43
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DQ17
DQ18
DQ19
KM48S2020A-1
U7
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A0 18
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A2 20
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A4 24
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A9 29
A10 17
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DQM0 33
CKE 31
CLK0 32
RAS 14
CAS 13
CS0 15
WE 12
DQ0 2
DQ1 4
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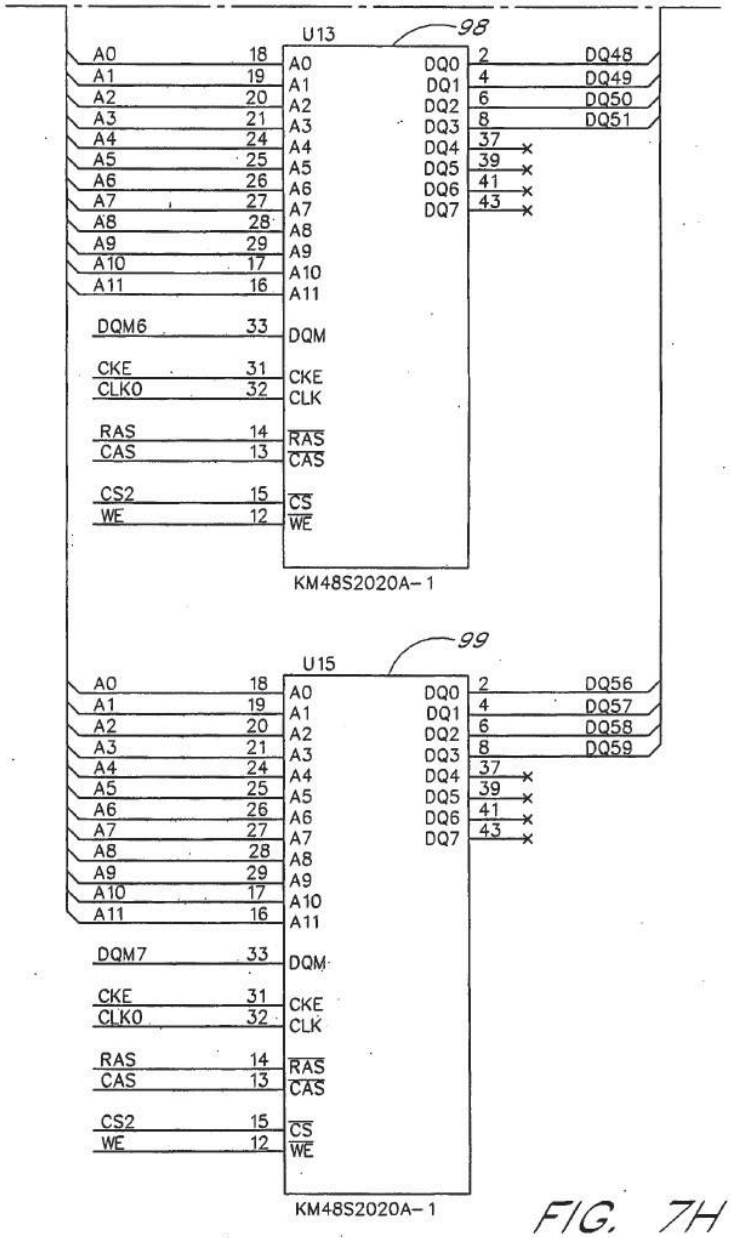
DQ6 41
DQ7 43
DQ24
DQ25
DQ26
DQ27
KM48S2020A-1

FIG. 7G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CLK0 32
RAS 14
CAS 13
CS2 15
WE 12
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DQ1 4
DQ2 6
DQ3 8
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DQ5 39
DQ6 41
DQ7 43
DQ48
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DQ50
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KM48S2020A-1
U15
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CLK0 32
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CAS 13
CS2 15
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DQ1 4
DQ2 6
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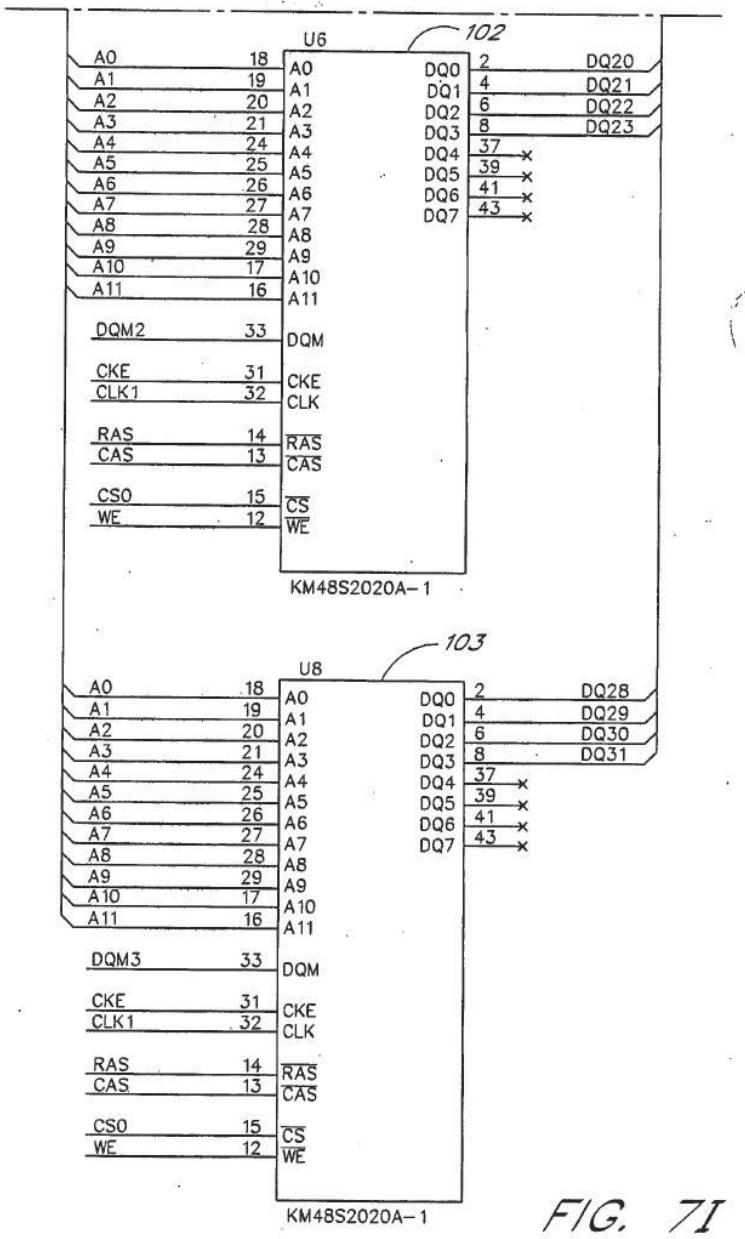
KM48S2020A-1

FIG. 7H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CKE 31
CLK1 32
RAS 14
CAS 13
CS0 15
WE 12
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
DQM
CKE
CLK
RAS
CAS
CS
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CKE 31
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CS0 15
WE 12
DQ0 2
DQ1 4
DQ2 6
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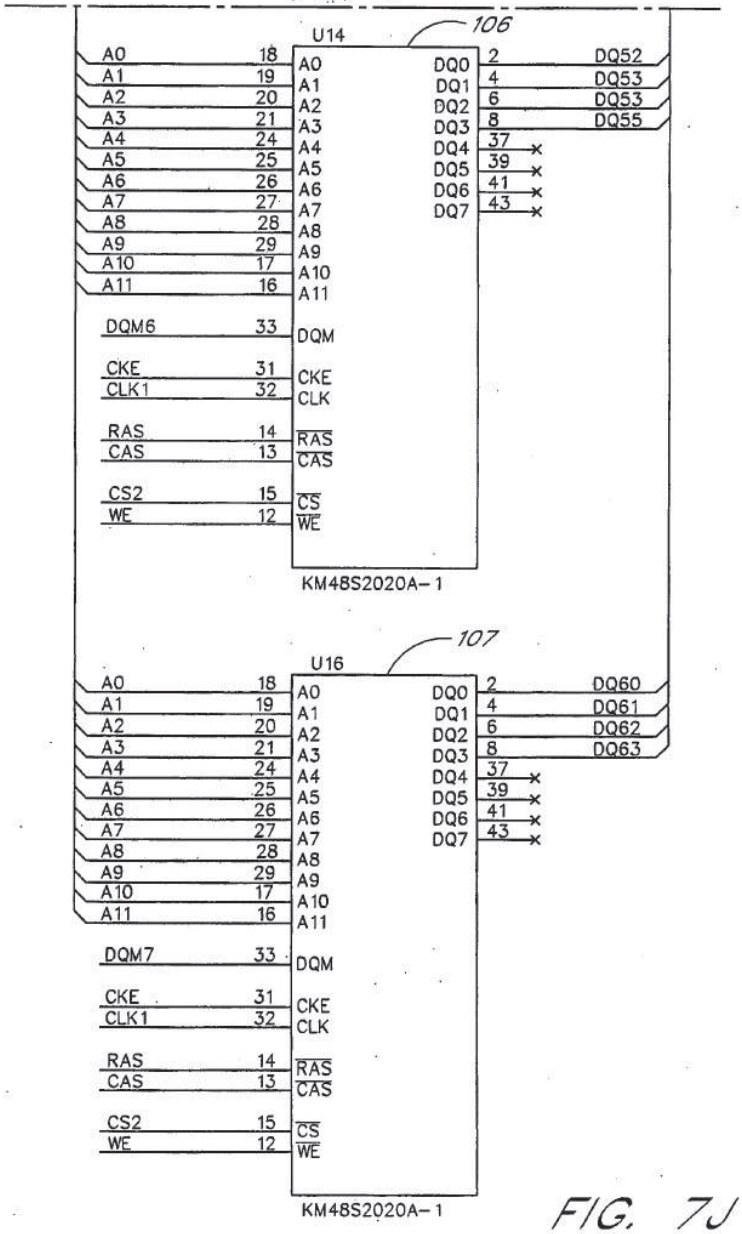
DQ30
DQ31
KM48S2020A-1

FIG. 7I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CKE 31
CLK1 32
RAS 14
CAS 13
CS2 15
WE 12
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DQ53
DQ53
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KM48S2020A-1
107
U16
DQM7 33
DQ60
DQ61
DQ62
DQ63
KM48S2020A-1

FIG. 7J

UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

SERIAL NUMBER	FILING DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NO.
09/035,739	03/05/98	WEBER R	6325

020995 TM21/1002
KNOBBE MARTENS OLSON & BEAR LLP
620 NEWPORT CENTER DRIVE
SIXTEENTH FLOOR
NEWPORT BEACH CA 92660

EXAMINER	
ELLIS,K	
ART UNIT	PAPER NUMBER
2185	23

DATE MAILED: 10/02/01

Please find below a communication from the EXAMINER in charge of this application.

Commissioner of Patents

Please find enclosed a copy of the IDS initialed and signed.

Kwai L. Ellis
10/2/01

PTOL-90 (Rev. 6/84)

1- PATENT APPLICATION FILE COPY

File History Content Report

The following content is missing from the original file history record obtained from the United States Patent and Trademark Office. No additional information is available.

Document Date - 2001-10-02

Document Title - List of References cited by applicant and considered by examiner

File History Content Report

The following content is missing from the original file history record obtained from the United States Patent and Trademark Office. No additional information is available.

Document Date - 2001-12-18

Document Title - USPTO Grant

CHECKLIST FOR PROCESSING NEW APPLICATIONS

SERIAL NUMBER 09/035739 revised 6/29/95

INSTRUCTIONS:
1. Make a checkmark beside each item IF verified.
2. If corrections are required, write notes to the examiner or supervisor on reverse side.

1. FACE OF THE FILE

- ✓ 1. Printed and stamped serial numbers match the bar code label.
- ✓ 2. Filing Date present.
- ✓ 3. Class/Subclass present.
- ✓ 4. Applicant(s) name present.
- ✓ 5. Total number of drawings present.
- ✓ 6. Total number of claims present.
- ✓ 7. Total number of independent claims present.
- ✓ 8. Filing fee received present.
- ✓ 9. Mailing address present.
- ✓ 10. Title of invention present.

2. CENTER OF THE FILE

A. DRAWINGS

- 1. None (go to B)
- ✓ 2. Serial Number present and correct on each sheet.
- ✓ 3. Number of sheets entered on line 1 of contents.

B. SMALL ENTITY STATEMENT

- ✓ 1. None and not recorded on face of file (go to C)
- 2. Statement present.
- 3. Small Entity recorded on face of file.

C. DECLARATION OR OATH

- ✓ 1. Title matches face of file and specification.
- ✓ 2. Declaration phrase present. (I hereby declare all...)
- ✓ 3. (Original and first inventor or inventors...) phrase present.
- ✓ 4. (Reviewed and understand the contents of the application, including claims...) phrase present.
- ✓ 5. (Acknowledge duty to disclose information in accordance with 1.56(a)...) phrase present.
- ✓ 6. Residence, citizenship, post office address of all applicants present.
- ✓ 7. Signed by all applicants.
- ✓ 8. Less than 3 months before filing date, or less than six months after filing date.

D. CLAIMS (as filed)

- ✓ 1. Complete form 1360 and 875: (forms on right side of file)
- ✓ 2. Circle independent claims on the Index of Claims.
- ✓ 3. Draw line under the last claim number on the Index of Claims.

E. SPECIFICATION

- ✓ 1. Serial Number present and correct.
- ✓ 2. Specification in permanent ink.
- ✓ 3. Brief Description of each drawing figure.
- ✓ 4. No missing or duplicate pages.
- ✓ 5. No holes punched in text.

F. ABSTRACT

- 1. None (go to G)
- ✓ 2. Serial Number present and correct.
- ✓ 3. Abstract on seperate page.
- ✓ 4. 25 lines or less.
- ✓ 5. One paragraph ONLY.

G. PTO-1556

- ✓ 1. Present

H. PRE-AMENDMENTS (found on right side of file)

- ✓ 1. None (go to I)
- 2. Enter on Contents of filewrapper.
- 3. Instruction to cancel claims.
- 4. Claims canceled on Index of Claims.
- 5. Instruction to add claims.
- 6. Circle new independent claims on the Index of Claims.
- 7. Draw line under the new last claim number on Index of Claims.
- 8. Complete forms 1360 and 875.

I. PTO-948

- ✓ 1. Present

3. RIGHT SIDE OF FILE

- 1. PALM File Data sheet present.
- ✓ 2. Transmittal letters present.
- ✓ 3. Forms 1360 & 875 present/complete.
- 4. Miscellaneous Papers present/entered.
- 5. Petition to Make Special present. (Enter and place in the center)
- ✓ 6. Drawing prints present. (2 copies)

FEES

____1. Correct filing fee paid.
____2. Excess claims fees paid:
____a. Excess total claims more than 20.
____b. Excess independent claims more than 3.
____c. First multiple dependent claim fee paid.
____3. Miscellaneous paper fee paid.

FINAL STEPS

____1. Sign and date center of filewrapper, under flap.
____2. Docketed to examiner.

NOTES TO SUPERVISOR:

NOTES TO EXAMINER:

SIGNATURE OF PREPARER: _____ DATE: 10/22/98

PATENT APPLICATION FEE DETERMINATION RECORD

Effective October 1, 1997

Application or Docket Number

CLAIMS AS FILED - PART I

	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA
FOR		
BASIC FEE		
TOTAL CLAIMS	8 minus 20 =	*
INDEPENDENT CLAIMS	2 minus 3 =	*
MULTIPLE DEPENDENT CLAIM PRESENT		

* If the difference in column 1 is less than zero, enter "0" in column 2

920

SMALL ENTITY TYPE ☐	RATE	FEE	OR	OTHER THAN SMALL ENTITY	RATE	FEE
BASIC FEE		395.00	OR	BASIC FEE		790.00
TOTAL CLAIMS	x$11=		OR	TOTAL CLAIMS	x$22=	
INDEPENDENT CLAIMS	x41=		OR	INDEPENDENT CLAIMS	x82=	
MULTIPLE DEPENDENT CLAIM PRESENT	+135=		OR	MULTIPLE DEPENDENT CLAIM PRESENT	+270=	
	TOTAL		OR		TOTAL	790

CLAIMS AS AMENDED - PART II

AMENDMENT A

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	* 8	Minus	** 20	=
Independent	* 2	Minus	*** 3	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				

SMALL ENTITY	RATE	ADDITIONAL FEE	OR	OTHER THAN SMALL ENTITY	RATE	ADDITIONAL FEE
Total	x$11=		OR	Total	x$22=	
Independent	x41=		OR	Independent	x82=	
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM	+135=		OR	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM	+270=	
	TOTAL ADDIT. FEE		OR		TOTAL ADDIT. FEE	

AMENDMENT B

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				

SMALL ENTITY	RATE	ADDITIONAL FEE	OR	OTHER THAN SMALL ENTITY	RATE	ADDITIONAL FEE
Total	x$11=		OR	Total	x$22=	
Independent	x41=		OR	Independent	x82=	
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM	+135=		OR	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM	+270=	
	TOTAL ADDIT. FEE		OR		TOTAL ADDIT. FEE	

AMENDMENT C

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				

SMALL ENTITY	RATE	ADDITIONAL FEE	OR	OTHER THAN SMALL ENTITY	RATE	ADDITIONAL FEE
Total	x$11=		OR	Total	x$22=	
Independent	x41=		OR	Independent	x82=	
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM	+135=		OR	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM	+270=	
	TOTAL ADDIT. FEE		OR		TOTAL ADDIT. FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20."
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3."
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

FORM PTO-875 (Rev. 8/97) *U.S. Government Printing Office: 1997 - 430-571/69194 Patent and Trademark Office, U.S. DEPARTMENT OF COMMERCE

CPA

PATENT APPLICATION FEE DETERMINATION RECORD
Effective November 10, 1998

Application or Docket Number
09/035739

CLAIMS AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA
BASIC FEE		
TOTAL CLAIMS	12 minus 20=	* —
INDEPENDENT CLAIMS	2 minus 3 =	* —
MULTIPLE DEPENDENT CLAIM PRESENT		

* If the difference in column 1 is less than zero, enter "0" in column 2

SMALL ENTITY TYPE ☐ RATE	FEE	OR	OTHER THAN SMALL ENTITY RATE	FEE
	380.00	OR		~~760.00~~ 690
X$ 9=		OR	X$18=	
X39=		OR	X78=	
+130=		OR	+260=	
TOTAL		OR	TOTAL	Copy pd.

CLAIMS AS AMENDED - PART II

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
AMENDMENT A	Total	*	Minus	**	=
	Independent	*	Minus	***	=
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				

SMALL ENTITY RATE	ADDITIONAL FEE	OR	OTHER THAN SMALL ENTITY RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	
X39=		OR	X78=	
+130=		OR	+260=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
AMENDMENT B	Total	*	Minus	**	=
	Independent	*	Minus	***	=
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				

SMALL ENTITY RATE	ADDITIONAL FEE	OR	OTHER THAN SMALL ENTITY RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	
X39=		OR	X78=	
+130=		OR	+260=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
AMENDMENT C	Total	*	Minus	**	=
	Independent	*	Minus	***	=
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				

SMALL ENTITY RATE	ADDITIONAL FEE	OR	OTHER THAN SMALL ENTITY RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	
X39=		OR	X78=	
+130=		OR	+260=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20."
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3."
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

FORM PTO-875
(Rev. 11/98)

Patent and Trademark Office, U.S. DEPARTMENT OF COMMERCE

06485 M.P.

Form PTO 1130 (REV 2/94)

U.S. DEPARTMENT OF COMMERCE Patent and Trademark Office

PACE DATA ENTRY CODING SHEET

1ST EXAMINER D. JONES DATE 5-18

2ND EXAMINER DATE

APPLICATION NUMBER	TYPE APPL	FILING DATE MONTH DAY YEAR	SPECIAL HANDLING	GROUP ART UNIT	CLASS	SHEETS OF DRAWING
09035739	1	03 05 98	0	2312	711	6

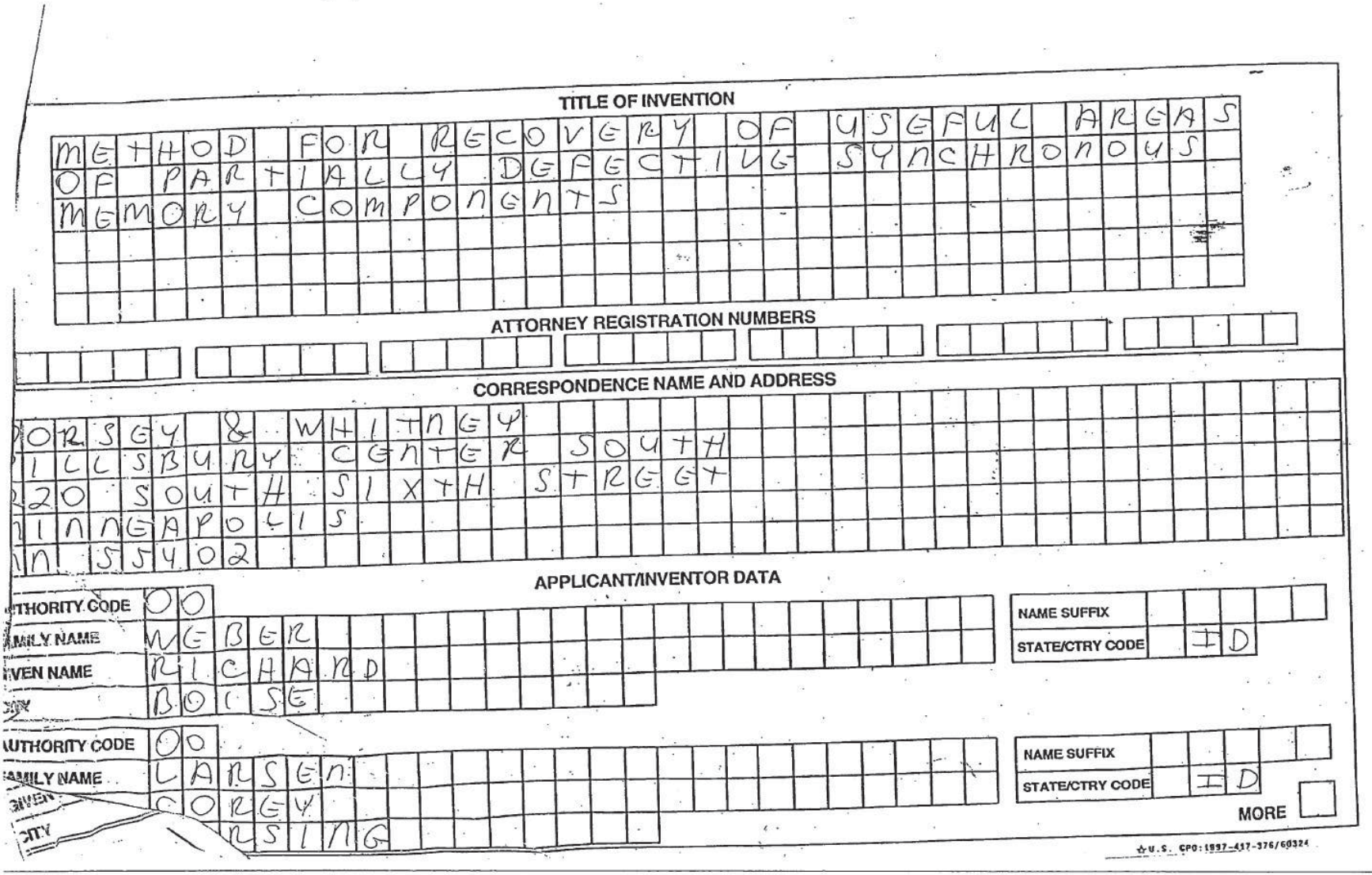
TOTAL CLAIMS	INDEPENDENT CLAIMS	SMALL ENTITY?	FILING FEE	FOREIGN LICENSE	ATTORNEY DOCKET NUMBER
8	2	0	790		6325

CONTINUITY DATA

CONT CODE	STATUS CODE	PARENT APPLICATION SERIAL NUMBER	PCT APPLICATION SERIAL NUMBER	PARENT PATENT NUMBER	PARENT FILING DATE MONTH DAY YEAR
			PCT/		
			PCT/		
			PCT/		
			PCT/		
			PCT/		

PCT/FOREIGN APPLICATION DATA

FOREIGN PRIORITY CLAIMED	COUNTRY CODE	PCT/FOREIGN APPLICATION SERIAL NUMBER	FOREIGN FILING DATE MONTH DAY YEAR
N			



TITLE OF INVENTION

METHOD FOR RECOVERY OF USEFUL AREAS OF PARTIALLY DEFECTIVE SYNCHRONOUS MEMORY COMPONENTS

ATTORNEY REGISTRATION NUMBERS

CORRESPONDENCE NAME AND ADDRESS

ORSEY & WHITNEY
ILLSBURY CENTER SOUTH
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MORE

☆U.S. GPO:1997-417-376/60324

MULTIPLE DEPENDENT CLAIM
FEE CALCULATION SHEET
(FOR USE WITH FORM PTO-875)

SERIAL NO.

FILING DATE

APPLICANT(S)

CLAIMS

	AS FILED		AFTER 1st AMENDMENT		AFTER 2nd AMENDMENT	
	IND.	DEP.	IND.	DEP.	IND.	DEP.
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TOTAL	1	8				

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Thomson Innovation Patent Export, 2016-06-14 01:53:08 -0500

Table of Contents

1. US6332183B1 Method for recovery of useful areas of partially defective synchronous memory components

Family 1/1
1 record(s) per family

Record 1/1 US6332183B1 Method for recovery of useful areas of partially defective synchronous memory components

Publication Number: US6332183B1 20011218

Title: Method for recovery of useful areas of partially defective synchronous memory components
Title - DWPI: Memory module accessing method in computer system, involves aggregating valid data outputs of partially defective SDRAM components to provide data path
Priority Number: US199835739A
Priority Date: 1998-03-05
Application Number: US199835739A
Application Date: 1998-03-05
Publication Date: 2001-12-18
IPC Class Table:

IPC	Section	Class	Subclass	Class Group	Subgroup
G06F001100	G	G06	G06F	G06F0011	G06F001100
G06F001202	G	G06	G06F	G06F0012	G06F001202
G11C002900	G	G11	G11C	G11C0029	G11C002900

IPC Class Table - DWPI:

IPC - DWPI	Section - DWPI	Class - DWPI	Subclass - DWPI	Class Group - DWPI	Subgroup - DWPI
G06F001202	G	G06	G06F	G06F0012	G06F001202
G06F001100	G	G06	G06F	G06F0011	G06F001100

Assignee/Applicant: Micron Technology Inc.,Boise,ID
JP F Terms:
JP FI Codes:
Assignee - Original: Micron Technology Inc.
Any CPC Table:

Type	Invention	Additional	Version	Office
Current Current	**G11C 29/88** G11C 29/886	-	20130101 20130101	EP EP

ECLA: G11C002988 | G11C0029886

Abstract:

Memory module using partially defective synchronous memory devices, such as SDRAM components. Multiple partially defective SDRAM components are configured to provide a reliable and nondefective memory module that takes advantage of the manner in which defective cells are localized on each SDRAM component.

Language of Publication: EN

INPADOC Legal Status Table:

Gazette Date	Code	INPADOC Legal Status Impact
2013-05-22	FPAY	+
Description: FEE PAYMENT		
2010-01-04	AS	-
Description: ASSIGNMENT ROUND ROCK RESEARCH, LLC, NEW YORK ASSIGNMENT OF ASSIGNORS INTEREST; ASSIGNOR:MICRON TECHNOLOGY, INC.; REEL/FRAME:023786/0416 2009-12-23		
2009-05-20	FPAY	+
Description: FEE PAYMENT		
2005-05-26	FPAY	+
Description: FEE PAYMENT		
2001-10-22	AS	-
Description: ASSIGNMENT MICRON TECHNOLOGY, INC., IDAHO ASSIGNMENT OF ASSIGNORS INTEREST; ASSIGNOR:MEI CALIFORNIA INC; REEL/FRAME:012232/0436 2001-03-22		
2001-03-30	AS	-
Description: ASSIGNMENT MEI CALIFORNIA, INC., CALIFORNIA ASSIGNMENT OF ASSIGNORS INTEREST; ASSIGNOR:MICRON ELECTRONICS, INC.; REEL/FRAME:011658/0956 2001-03-22		

1998-08-10	AS	-
Description: ASSIGNMENT MICRON ELECTRONICS, INC., IDAHO ASSIGNMENT OF ASSIGNORS INTEREST; ASSIGNORS:WEBER, RICHARD; LARSEN, COREY; REEL/FRAME:009378/0800 1998-05-21		

Post-Issuance (US):

Reassignment (US) Table:

Assignee	Assignor	Date Signed	Reel/Frame	Date
ROUND ROCK RESEARCH LLC,MT. KISCO,NY,US	MICRON TECHNOLOGY, INC.	2009-12-23	023786/0416	2010-01-04
Conveyance: ASSIGNMENT OF ASSIGNORS INTEREST (SEE DOCUMENT FOR DETAILS).				
Corresponent: CHRISTOPHER C. HENRY ROPES & GRAY LLP 1211 AVENUE OF THE AMERICAS NEW YORK, NEW YORK 10036				
MICRON TECHNOLOGY INC.,BOISE,ID,US	MEI CALIFORNIA INC	2001-03-22	012232/0436	2001-10-22
Conveyance: ASSIGNMENT OF ASSIGNORS INTEREST (SEE DOCUMENT FOR DETAILS).				
Corresponent: KNOBBE, MARTENS, OLSON & BEAR LLP DREW S. HAMILTON SIXTEENTH FLOOR 620 NEWPORT CENTER DRIVE NEWPORT BEACH, CA 92660				
MEI CALIFORNIA INC.,MILPITAS,CA,US	MICRON ELECTRONICS, INC.	2001-03-22	011658/0956	2001-03-30
Conveyance: ASSIGNMENT OF ASSIGNORS INTEREST (SEE DOCUMENT FOR DETAILS).				
Corresponent: MICRON ELECTRONICS, INC. STEVEN P. ARNOLD 900 EAST KARCHER ROAD NAMPA, ID 83687				
MICRON ELECTRONICS INC.,NAMPA,ID,US	WEBER, RICHARD	1998-05-21	009378/0800	1998-08-10
	LARSEN, COREY	1998-05-21	-	-
Conveyance: ASSIGNMENT OF ASSIGNORS INTEREST (SEE DOCUMENT FOR DETAILS).				
Corresponent: DORSEY & WHITNEY LLP STUART R. HEMPHILL 220 SOUTH SIXTH STREET MINNEAPOLIS, MN 55402				

Maintenance Status (US):

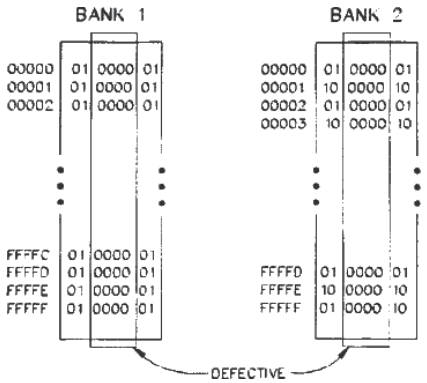
Litigation (US):

Opposition (EP):

License (EP):

EPO Procedural Status:

Front Page Drawing:



Assignee - Current US: ROUND ROCK RESEARCH LLC

United States Patent and Trademark Office

Office of the Commissioner for Patents

METHOD FOR RECOVERY OF USEFUL AREAS OF PARTIALLY DEFECTIVE SYNCHRONOUS MEMORY COMPONENTS

PATENT #	APPLICATION #	FILING DATE	ISSUE DATE
6332183	09035739	03/05/1998	12/18/2001

Payment Window Status

No maintenance fees are due.

WINDOW	STATUS	FEES
11.5 Year	Closed	Paid

Window	First Day to Pay	Surcharge Starts	Last Day to Pay	Status	Fees
3.5 Year	12/18/2004	06/21/2005	12/19/2005	Closed	Paid
7.5 Year	12/18/2008	06/19/2009	12/18/2009	Closed	Paid
11.5 Year	12/18/2012	06/19/2013	12/18/2013	Closed	Paid

Patent Holder Information

Customer # 26809

Entity Status UNDISCOUNTED

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