

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re Patent of: Benisek et al.

US Patent No.: 6,850,414

Attorney Docket No.: 37307-0007IP1

Issue Date: February 1, 2005

Appl. Serial No.: 10/187,763

§ 371 (c)(1) Date: July 2, 2002

Title: ELECTRONIC PRINTED CIRCUIT BOARD HAVING A  
PLURALITY OF IDENTICALLY DESIGNED, HOUSING-  
ENCAPSULATED SEMICONDUCTOR MEMORIES

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**DECLARATION OF VIVEK SUBRAMANIAN**

I, Vivek Subramanian, declare as follows:

**I. Introduction.**

1. I am making this declaration at the request of the Real Party in Interest (Kingston Technology Company, Inc.) in the matter of *Inter Partes* Review of U.S. Patent No. 6,850,414 (the “’414 patent”).
2. I am being compensated for my work. My compensation does not depend on the outcome of this proceeding.
3. I have been asked to consider whether certain references disclose or render obvious the claims of the ’414 Patent, either alone or in combination with each other.

4. I have been advised that a patent claim may be invalid as obvious if the differences between the subject matter patented and the prior art are such that the subject matter as a whole would have been obvious at the time of the invention to a person having ordinary skill in the art. I have also been advised that several factual inquiries underlie a determination of obviousness. These inquiries include the scope and content of the prior art, the level of ordinary skill in the field of the invention, the differences between the claimed invention and the prior art, and any objective evidence of non-obviousness.

5. I have been advised that objective evidence of non-obviousness directly attributable to the claimed invention, known as “secondary considerations of non-obviousness,” may include commercial success, satisfaction of a long-felt but unsolved need, failure of others, copying, skepticism or disbelief before the invention, and unexpected results. I am not aware of any such objective evidence of non-obviousness that is directly attributable to the subject matter claimed in the ’414 patent at this time.

6. In addition, I have been advised that the law requires a “common sense” approach of examining whether the claimed invention is obvious to a person skilled in the art. For example, I have been advised that combining familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results. I have further been advised that this is especially

true in instances where there are a limited numbers of possible solutions to technical problems or challenges.

7. I have been informed that all claims of the '414 Patent are subject to this *inter partes* review.

## **II. Materials Reviewed**

8. In forming the opinions that I express below, I considered my own knowledge of the art plus at least the following references:

- a. The '414 Patent
- b. UK Patent Application GB 2 289 573 A (“Simpson”)
- c. Intel PC SDRAM Unbuffered DIMM Specification Rev. 1 (“Intel Specification”)
- d. U.S. Patent Application Publication US2002/0196612 A1 (“Gall”)
- e. PC133 SDRAM Registered DIMM Design Specification Rev. 1.1 (“PC133 Specification”)
- f. The File History of U.S. Patent No. 6,850,414
- g. The File History of U.S. Patent No. 6,332,183

## **III. Qualifications**

9. I summarize my relevant knowledge and experience below. My *Curriculum Vitae* contains additional information and is attached as Exhibit 1010.

10. I received a B.S. in electrical engineering from Louisiana State University in 1994, an M.S. in electrical engineering from Stanford University in 1996, and a Ph.D. in electrical engineering from Stanford University in 1998.

11. I co-founded Matrix Semiconductor, Inc. in 1998 to develop high density memory technology.

12. I have been teaching in the Electrical Engineering and Computer Sciences Department at the University of California, Berkeley since 2000. I was an Assistant Professor from 2000 to 2005, an Associate Professor from 2005 to 2011, and a Professor from 2011 to the present.

13. I have been an adjunct professor at the Sunchon National University in Sunchon, Korea since 2009, leading research in printed electronics.

14. I have been an independent consultant in the semiconductor industry since 2000, focusing on memory technology, flexible electronics, and RFID technology.

15. I have published more than 200 technical papers in journals and at conferences.

16. I am a named inventor on over 40 U.S. Patents, many of which are in the field of memory design.

#### **IV. Person of Ordinary Skill in the Art and State of The Art**

17. In my opinion, a person of ordinary skill in the art as of the time of the '414 Patent would have a Bachelor's degree in Electrical Engineering and at least 2

years' experience working in the field of semiconductor memory design. I believe this to be a reasonable statement of the level of ordinary skill in the art for the patent and claims at issue. I also believe that I was one of ordinary skill in the art through my education and work experience during the time that I was in University.

18. The opinions that I provide in this declaration are consistent with the knowledge and experience of one of ordinary skill in the art at the priority date of the '414 Patent.

19. At the time of the '414 Patent's priority date, those of ordinary skill in the art recognized that, within specified design dimensions and tolerances, memory modules and/or error correction devices could be interchanged and oriented in a finite number of ways within the physical size constraints set forth by the industry standards. *See* Ex. 1002, Simpson, 2:10-15 and Ex. 1003 (Intel Specification).

#### **V. Overview of the '414 Patent**

20. The '414 Patent is directed to a printed circuit board ("PCB") that has at least nine memories chips that are arranged to appreciably reduce the height of the printed circuit board. Ex. 1001, 2:45-3:10. The specification discloses that one of the at least nine chips be an error correction chip and that one be arranged vertically on the printed circuit board, such that the error correction chip

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