

# **PC SDRAM UNBUFFERED DIMM SPECIFICATION**

**REVISION 1.0**

THIS DOCUMENT IS PROVIDED "AS IS" WITH NO WARRANTIES WHATSOEVER, INCLUDING ANY WARRANTY OF MERCHANTABILITY, FITNESS FOR ANY PARTICULAR PURPOSE, OR ANY WARRANTY OTHERWISE ARISING OUT OF ANY PROPOSAL, SPECIFICATION, OR SAMPLE.

No other license, express or implied, by estoppel or otherwise, to any other intellectual property rights is granted herein. Intel disclaims all liability, including liability for infringement of any proprietary rights, relating to implementation of information in this specification. Intel does not warrant or represent that such implementation(s) will not infringe such rights.

\* Other brands and names are the property of their respective owners.

Copyright Intel Corporation, 1997

## Changes:

### Revision 0.9 Oct., 1997

Changed example stackup spacing to 7-11-7-11-7 with 0.5 oz. Copper  
Added Section for DIMM PCB and Assembly labeling requirements.  
Changed topology diagram notes to allow additional vias.  
Modified mechanicals to include heat sink notches.

### Revision 1.0 Feb., 1998

Changed example stackup spacing to 7-10-9-10-7.  
Removed specifications relating to 64Mbit / 2-bank SDRAM components.  
Increased max overall thickness to 4.33mm to account for height of SOIC EEPROM.  
Changed topology diagrams to allow additional vias.  
Added note to mechanicals to indicate that heat sink notches are optional.  
Increased max interval between vias connecting ground rings to 0.7".  
Included specifications for outer layer clock trace lengths for x16 based designs.  
Removed outer layer clock trace length placeholder for x8 based designs.  
Modified mixed mode DIMM wiring diagrams and clock loading table to indicate that the higher density DRAMs must always be placed on the primary side of the DIMM.  
Added information on Intel clock simulation assumptions to allow independent simulation of scenarios for which specific lengths are not specified.  
Added configuration listings for 256MB and 512MB DIMMs based on 128Mbit and 256Mbit components respectively.  
Removed the requirement that the vendor name and part number be provided in etch or silkscreen on the DIMM.

## TABLE OF CONTENTS

<b>LIST OF TABLES</b>	<b>5</b>
<b>LIST OF FIGURES</b>	<b>6</b>
<b>1.0 INTRODUCTION</b>	<b>7</b>
<b>2.0 ENVIRONMENTAL REQUIREMENTS</b>	<b>10</b>
<b>3.0 MECHANICAL DESIGN</b>	<b>11</b>
<b>4.0 MODULE PINOUT</b>	<b>18</b>
<b>5.0 SDRAM DIMM BLOCK DIAGRAMS</b>	<b>19</b>
<b>6.0 DIMM PCB LAYOUT AND SIGNAL ROUTING</b>	<b>32</b>
<b>7.0 DIMM PCB AND FINAL ASSEMBLY LABELING REQUIREMENTS</b>	<b>46</b>
<b>8.0 SDRAM COMPONENT SPECIFICATIONS</b>	<b>46</b>
<b>9.0 EEPROM COMPONENT SPECIFICATIONS</b>	<b>46</b>

**LIST OF TABLES**

TABLE 1: RELATED DOCUMENTS	7
TABLE 2: SDRAM NON MIXED-MODE MODULE CONFIGURATIONS	8
TABLE 3: SDRAM MIXED-MODE MODULE CONFIGURATIONS	9
TABLE 4: DIMM TEMPERATURE, HUMIDITY & BAROMETRIC PRESSURE REQUIREMENTS	10
TABLE 5: DIMM DIMENSIONS AND TOLERANCES	11
TABLE 6: DIMM DIMENSIONS AND TOLERANCES (CONTINUED)	12
TABLE 7: SDRAM DIMM PINOUT	18
TABLE 8: PCB CALCULATED PARAMETERS	32
TABLE 9: SIGNAL TOPOLOGY CATEGORIES	35
TABLE 10: TRACE LENGTH TABLE FOR CLOCK TOPOLOGIES	39
TABLE 11: TRACE LENGTH TABLE FOR DATA TOPOLOGIES	40
TABLE 12: TRACE LENGTH TABLE FOR DATA MASK TOPOLOGIES (1/2 LOADS)	41
TABLE 13: TRACE LENGTH TABLE FOR DATA MASK TOPOLOGIES (1/2/3 LOADS)	42
TABLE 14: TRACE LENGTH TABLE FOR CHIP SELECT TOPOLOGIES	43
TABLE 15: TRACE LENGTH TABLES FOR CLOCK ENABLE TOPOLOGIES	44
TABLE 16: TRACE LENGTH TABLE FOR DOUBLE CYCLE SIGNAL TOPOLOGIES	45

# Explore Litigation Insights

Docket Alarm provides insights to develop a more informed litigation strategy and the peace of mind of knowing you're on top of things.

## Real-Time Litigation Alerts



Keep your litigation team up-to-date with **real-time alerts** and advanced team management tools built for the enterprise, all while greatly reducing PACER spend.

Our comprehensive service means we can handle Federal, State, and Administrative courts across the country.

## Advanced Docket Research



With over 230 million records, Docket Alarm's cloud-native docket research platform finds what other services can't. Coverage includes Federal, State, plus PTAB, TTAB, ITC and NLRB decisions, all in one place.

Identify arguments that have been successful in the past with full text, pinpoint searching. Link to case law cited within any court document via Fastcase.

## Analytics At Your Fingertips



Learn what happened the last time a particular judge, opposing counsel or company faced cases similar to yours.

Advanced out-of-the-box PTAB and TTAB analytics are always at your fingertips.

## API

Docket Alarm offers a powerful API (application programming interface) to developers that want to integrate case filings into their apps.

## LAW FIRMS

Build custom dashboards for your attorneys and clients with live data direct from the court.

Automate many repetitive legal tasks like conflict checks, document management, and marketing.

## FINANCIAL INSTITUTIONS

Litigation and bankruptcy checks for companies and debtors.

## E-DISCOVERY AND LEGAL VENDORS

Sync your system to PACER to automate legal marketing.