PC SDRAM UNBUFFERED DIMM SPECIFICATION

REVISION 1.0

Changes:

Revision 0.9 Oct., 1997

Changed example stackup spacing to 7-11-7-11-7 with 0.5 oz. Copper
Added Section for DIMM PCB and Assembly labeling requirements.
Changed topology diagram notes to allow additional vias.
Modified mechanicals to include heat sink notches.

Revision 1.0 Feb., 1998

Changed example stackup spacing to 7-10-9-10-7.
Removed specifications relating to 64Mbit / 2-bank SDRAM components.
Increased max overall thickness to 4.33mm to account for height of SOIC EEPROM.
Changed topology diagrams to allow additional vias.
Added note to mechanicals to indicate that heat sink notches are optional.
Increased max interval between vias connecting ground rings to 0.7".
Included specifications for outer layer clock trace lengths for x16 based designs.
Removed outer layer clock trace length placeholder for x8 based designs.
Modified mixed mode DIMM wiring diagrams and clock loading table to indicate that the higher density DRAMs must always be placed on the primary side of the DIMM.
Added information on Intel clock simulation assumptions to allow independent simulation of scenarios for which specific lengths are not specified.
Added configuration listings for 256MB and 512MB DIMMs based on 128Mbit and 256Mbit components respectively.
Removed the requirement that the vendor name and part number be provided in etch or silkscreen on the DIMM.

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