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Paper 7
Entered: February 15, 2017

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

KINGSTON TECHNOLOGY COMPANY, INC.,
Petitioner,

v.

POLARIS INNOVATIONS LTD.,
Patent Owner.

Case IPR2016-01622
Patent 6,850,414 B2

Before SALLY C. MEDLEY, JEAN R. HOMERE, and MATTHEW R. CLEMENTS, *Administrative Patent Judges*.

CLEMENTS, *Administrative Patent Judge*.

DECISION
Institution of *Inter Partes* Review
35 U.S.C. § 314 and 37 C.F.R. § 42.108

I. INTRODUCTION

Kingston Technology Company, Inc. ("Petitioner") filed a Petition requesting *inter partes* review of claims 1–8 ("the challenged claims") of U.S. Patent No. 6,850,414 (Ex. 1001, "the '414 patent"). Paper 2 ("Pet."). Polaris Innovations Ltd. ("Patent Owner") filed a Preliminary Response. Paper 6 ("Prelim. Resp."). We review the Petition pursuant to 35 U.S.C. § 314, which provides that an *inter partes* review may be authorized only if "the information presented in the petition . . . and any [preliminary] response . . . shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition." 35 U.S.C. § 314(a); 37 C.F.R. § 42.4(a). Upon consideration of the Petition and the Preliminary Response, we determine that the information presented by Petitioner establishes that there is a reasonable likelihood that Petitioner would prevail in showing the unpatentability of at least one of the challenged claims of the '414 patent. Accordingly, pursuant to 35 U.S.C. § 314, we institute an *inter partes* review of claims 1 and 5–8 of the '414 patent.

A. Related Proceedings

The '414 patent is involved in *Polaris Innovations Ltd. v. Kingston Tech. Co., Inc.*, Case No. 8:16-cv-300 (C.D. Cal.). Pet. 1; Paper 4, 1. Petitioner also has filed other petitions seeking *inter partes* review of related patents: Case IPR2016-01621 and Case IPR2016-01623.

B. The '414 patent

The '414 patent, titled "Electronic printed circuit board having a plurality of identically designed, housing-encapsulated semiconductor

memories," issued February 1, 2005, from U.S. Patent Application No. 10/187,763. Ex. 1001 at [54], [45], [21].

The '414 patent generally relates to an electronic printed circuit board having a memory module comprised of identically designed semiconductor memories configured on the printed circuit board. *Id.* at Abstract. According to the '414 patent, "Printed circuit boards of this type are inserted into motherboards of personal computers or network computers and serve as the main memory." *Id.* at 1:21–23. Figures 1A and 1B are reproduced below.

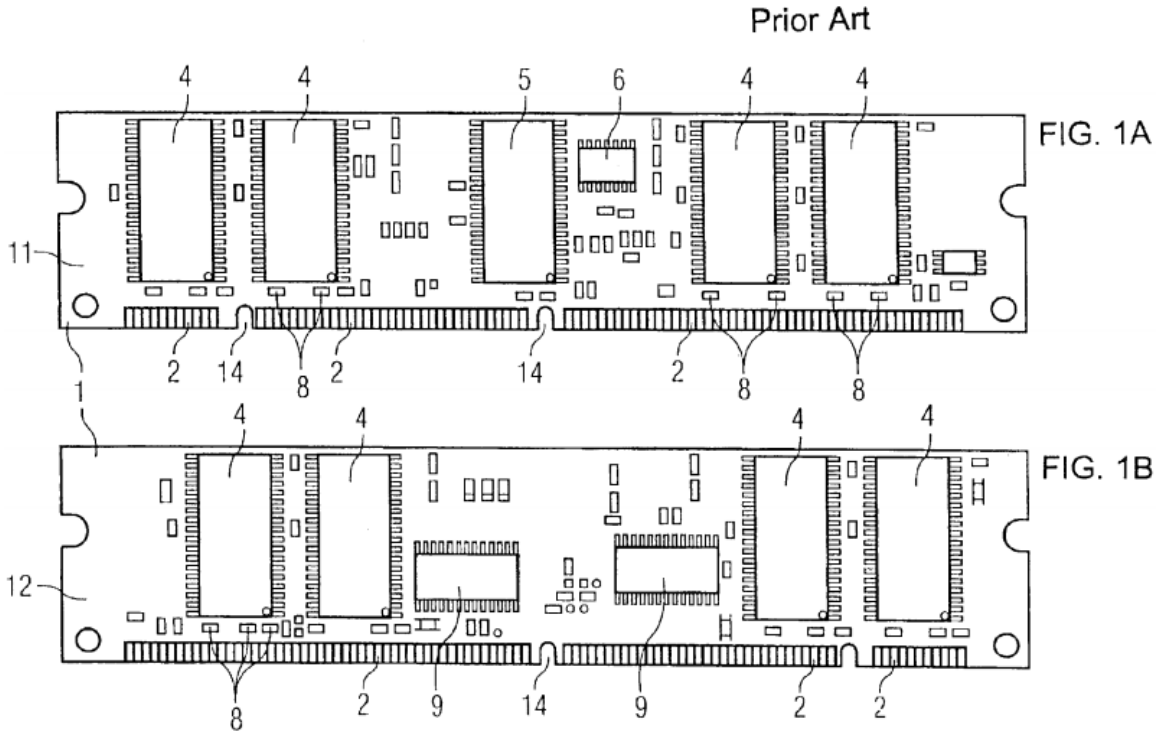

Figure 1A shows the front side of a conventional printed circuit board and Figure 1B shows the rear side of a conventional printed circuit board. *Id.* at 5:6–10. In a conventional arrangement, semiconductor memories 4 are arranged on the front and rear sides of the printed circuit board in the same orientation as error correction chip 5. *Id.* at 1:62–67. "In the case of this

conventional arrangement . . . there is no more leeway for a further reduction of the circuit board height (the height of the printed circuit board perpendicular to the contact strip)." *Id.* at 2:37–41. In network computers, however, "the printed circuit boards are inserted into compartment-type elements having a small height, for which reason the printed circuit boards themselves should also have only a small height." *Id.* at 1:23–27.

To address this problem, the '414 patent discloses an electronic printed circuit board in which the error correction chip remains oriented perpendicular to the contact strip but the other semiconductor memories are oriented parallel to the contact strip, such that it is "possible to reduce the height of the printed circuit board while enabling the rectangular housing to keep the same physical form." *Id.* at Abstract. Figure 2 is reproduced below.

FIG 3

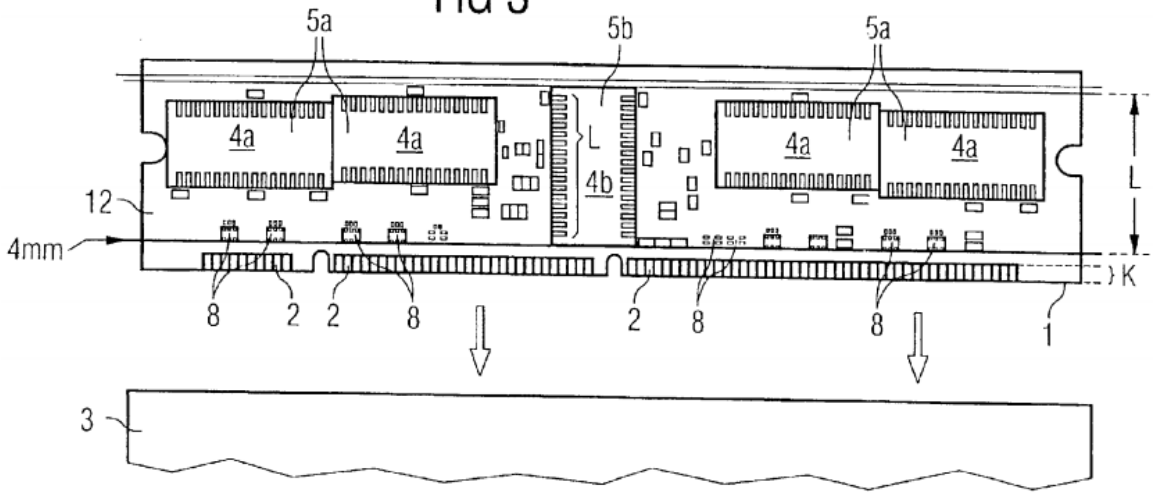

Figure 3 shows the rear side of a printed circuit board according to an embodiment of the '414 patent. *Id.* at 5:13–14. In this arrangement, housings 5a of semiconductor memories 4a are arranged horizontally on printed circuit board 1, and only housing 5b of error correction chip 4b is arranged vertically. *Id.* at 6:19–28. Housing 5b is "brought up to [] contact

strip 2 as close as possible" because "there is no need for any resistors 8 [between housing 5b and contact strip 2], as in the case of all of the other identically designed semiconductor memories 4*a* that are configured horizontally." *Id.* at 6:28–35. "As a result, the height of printed circuit board 1 can be reduced from a value of H_1 to a smaller value H_2" (*id.* at 6:41–42), as shown in Figure 2, which is reproduced below.

FIG 2

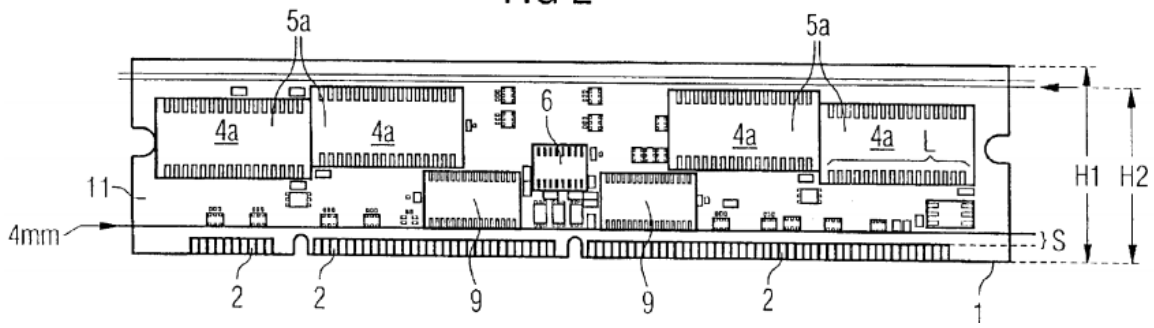

Figure 2 shows the front side of a printed circuit board according to an embodiment of the '414 patent. *Id.* at 5:11–12.

C. Illustrative Claim

Of the challenged claims, claim 1 is independent and claims 2–8 depend from claim 1. Independent claim 1 is illustrative of the challenged claims and is reproduced below:

> 1. An electronic printed circuit board configuration, comprising:
>
> an electronic printed circuit board having a contact strip for insertion into another electronic unit; and
>
> a memory module having at least nine identically designed integrated semiconductor memories;
>
> each one of said semiconductor memories being encapsulated in a rectangular housing having a shorter dimension and a longer dimension;

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