Paper 33

Entered: January 29, 2018

### UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

KINGSTON TECHNOLOGY COMPANY, INC., Petitioner,

v.

POLARIS INNOVATIONS LTD., Patent Owner.

Case IPR2016-01621 Patent 6,438,057 B2

Before SALLY C. MEDLEY, JEAN R. HOMERE, and KEN B. BARRETT, *Administrative Patent Judges*.

HOMERE, Administrative Patent Judge.

FINAL WRITTEN DECISION

Inter Partes Review

35 U.S.C. § 318(a) and 37 C.F.R. § 42.73



### I. INTRODUCTION

In this *inter partes* review, instituted pursuant to 35 U.S.C. § 314, Kingston Technology Company, Inc. ("Petitioner") challenges claims 1–17 ("the challenged claims") of U.S. Patent No. 6,438,057 B1 (Ex. 1001, "the '057 patent"), owned by Polaris Innovations Ltd. ("Patent Owner"). We have jurisdiction under 35 U.S.C. § 6. This Final Written Decision is entered pursuant to 35 U.S.C. § 318(a) and 37 C.F.R. § 42.73. For the reasons discussed below, Petitioner has shown by a preponderance of the evidence that the challenged claims are unpatentable.

### A. Procedural History

Petitioner filed a Petition requesting an *inter partes* review of claims 1–17 of the '057 patent. Paper 2 ("Pet."). Patent Owner filed a Preliminary Response. Paper 7 ("Prelim. Resp."). On February 15, 2017, we instituted *inter partes* review of claims 1, 3, 5–9, 12, 13, and 16 of the '057 patent under 35 U.S.C. § 103(a) as being unpatentable over the combination of Atkinson,<sup>2</sup> and Broadwater.<sup>3</sup> Paper 8 ("Inst. Dec."), 17. Further, we instituted *inter partes* review of claims 2, 4, 10, 11, 14, 15, and 17 of the '057 patent under 35 U.S.C. § 103(a) as being unpatentable over the combination of Atkinson, Broadwater, and Miller.<sup>4</sup> *Id.* at 20.

Thereafter, Patent Owner filed a Patent Owner Response (Paper 18, "PO Resp."), to which Petitioner filed a Reply (Paper 21, "Reply").

<sup>&</sup>lt;sup>4</sup> U.S. Patent No. 3,812,717, issued May 28, 1974 (Ex. 1015) ("Miller").



<sup>&</sup>lt;sup>1</sup>Patent Owner identifies Polaris Innovations Ltd., Wi-LAN Inc., and Quarterhill Inc. as real parties-in-interest. Paper 4, 2; Paper 20, 2.

<sup>&</sup>lt;sup>2</sup> U.S. Patent No. 6,134,167, issued Oct. 17, 2000 (Ex. 1010) ("Atkinson").

<sup>&</sup>lt;sup>3</sup> U.S. Patent No. 4,970,497, issued Nov. 13, 1990 (Ex. 1006) ("Broadwater").

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Pursuant to an Order (Paper 22), Patent Owner filed a listing of alleged statements and evidence in connection with Petitioner's Reply that Patent Owner considered to be beyond the proper scope of a reply. Paper 23. Petitioner filed a response to Patent Owner's listing. Paper 24.

We held a consolidated hearing on November 14, 2017, for this case and related Cases IPR2016-01622 and IPR2016-01623, and a transcript of the hearing is included in the record. Paper 32 ("Tr.").

## B. Related Proceedings

The parties state that the '057 patent is the subject of a pending lawsuit in the Central District of California Southern Division that includes assertions against Petitioner. Pet. 2; Paper 4 (Patent Owner's Mandatory Notice), 1; Ex. 1002.

## *C. The '057 patent (Ex. 1001)*

The '057 patent is directed to a method and system for refreshing the contents of a dynamic random access memory (DRAM) array. Ex. 1001, 1:5–7. In particular, the temperature of the DRAM array is utilized to adjust a refresh rate at which the contents of the DRAM array are updated. *Id.* at 1:7–10. Figure 3 of the '057 patent is reproduced below:



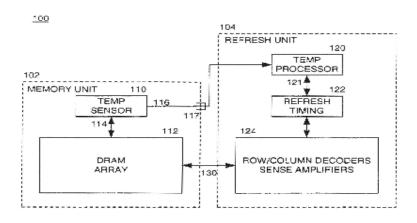


FIG. 3

Figure 3 illustrates system 100 for storing data in DRAM array 112. *Id.* at 4:11–12. In particular, Figure 3 depicts memory unit 102 containing temperature sensor 110 coupled to DRAM array 112, wherein memory unit 102 is connected to refresh unit 104 containing temperature processor 120 coupled to refresh timing 122 and row/column decoders sense amplifiers 124. *Id.* at 4:12–30. According to the '057 patent, "the DRAM array 112 may be implemented on a semiconductor chip and the temperature sensor 110 may be thermally coupled to the same semiconductor chip or to an intermediate member that is in thermal communication with the semiconductor chip." *Id.* at 4:22–26.

More specifically, in system 100 illustrated in Figure 3, upon receiving signal 116 from temperature sensor 110 indicating a temperature sensed from DRAM array 112, refresh unit 104 produces refresh signal 130 to refresh DRAM array 112 at a rate that varies in response to received temperature signal 116. *Id.* at 4:30–32. Preferably, DRAM array 112 is refreshed at a rate that decreases as the temperature of DRAM array 112 decreases. Conversely, DRAM array 112 is refreshed at a rate that increases



as the temperature of DRAM array 112 increases. *Id.* at 4:33–37. Further, according to the '057 patent, "the temperature sensor 110 and the DRAM array 112 are preferably disposed in a semiconductor package where the package includes at least one connection pin 117 operable to provide the signal on line 116 to external circuitry, such as the refresh unit 104." *Id.* at 4:49–53. "[T]he temperature sensor 110 preferably includes at least one diode 140 having a forward voltage drop that varies as a function of the temperature of the DRAM array 112." *Id.* at 5:17–20.

### D. Illustrative Claim

Of the instituted claims, claims 1, 13, and 16 are independent. Claims 2–12 depend from independent claim 1. Claims 14 and 15 depend from independent claim 13. Claim 17 depends from independent claim 16. Independent claim is illustrative of the challenged claims, and is reproduced below:

## 1. An apparatus, comprising:

a semiconductor package including at least one connection pin;

at least one dynamic random access memory (DRAM) array disposed within the package; and

at least one temperature sensor in thermal communication with the DRAM array, operable to produce a signal indicative of a temperature of the DRAM array, and coupled to the at least one connection pin such that the signal may be provided to external circuitry,

wherein the DRAM array is refreshed at a rate that decreases as the temperature of the DRAM array decreases and that increases as the temperature of the DRAM array increases.

Ex. 1001, 5:60-6:7.



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