

- [54] **STROBED DC-DC CONVERTER WITH CURRENT REGULATION**
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- [58] Field of Search **323/222, 225, 271, 272, 323/282, 284, 285, 223**

- 4,712,169 12/1987 Albach 323/282
- 4,717,867 1/1988 Forehand 323/223
- 4,837,495 6/1989 Zansky 323/222

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[57] **ABSTRACT**

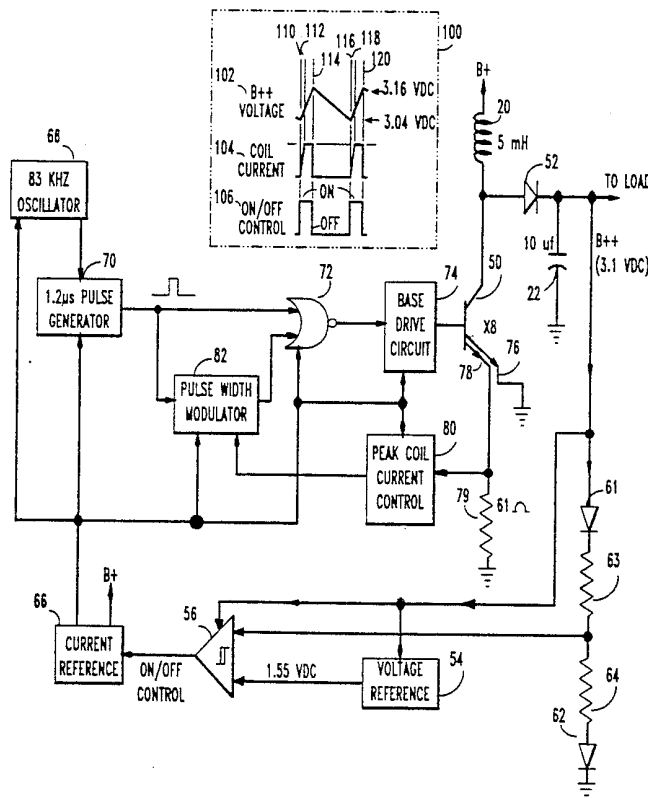
A DC-DC converter regulates the maximum current through an inductor. The DC-DC converter operates within a paging receiver and boosts a voltage from a single cell battery to substantially 3.1 VDC in order to operate circuits which require more voltage than that produced by the single cell battery. Such circuits include CMOS microcomputers and code plug. The DC-DC converter is current regulated thus providing for improved power conversion efficiency. The DC-DC converter is active when the voltage is below a minimum voltage and inactive when above a maximum voltage. The DC-DC converter provides for a wide range of load currents from the converted voltage without being controlled by a microcomputer and while delivering the power to the loads with an improved efficiency.

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14 Claims, 2 Drawing Sheets



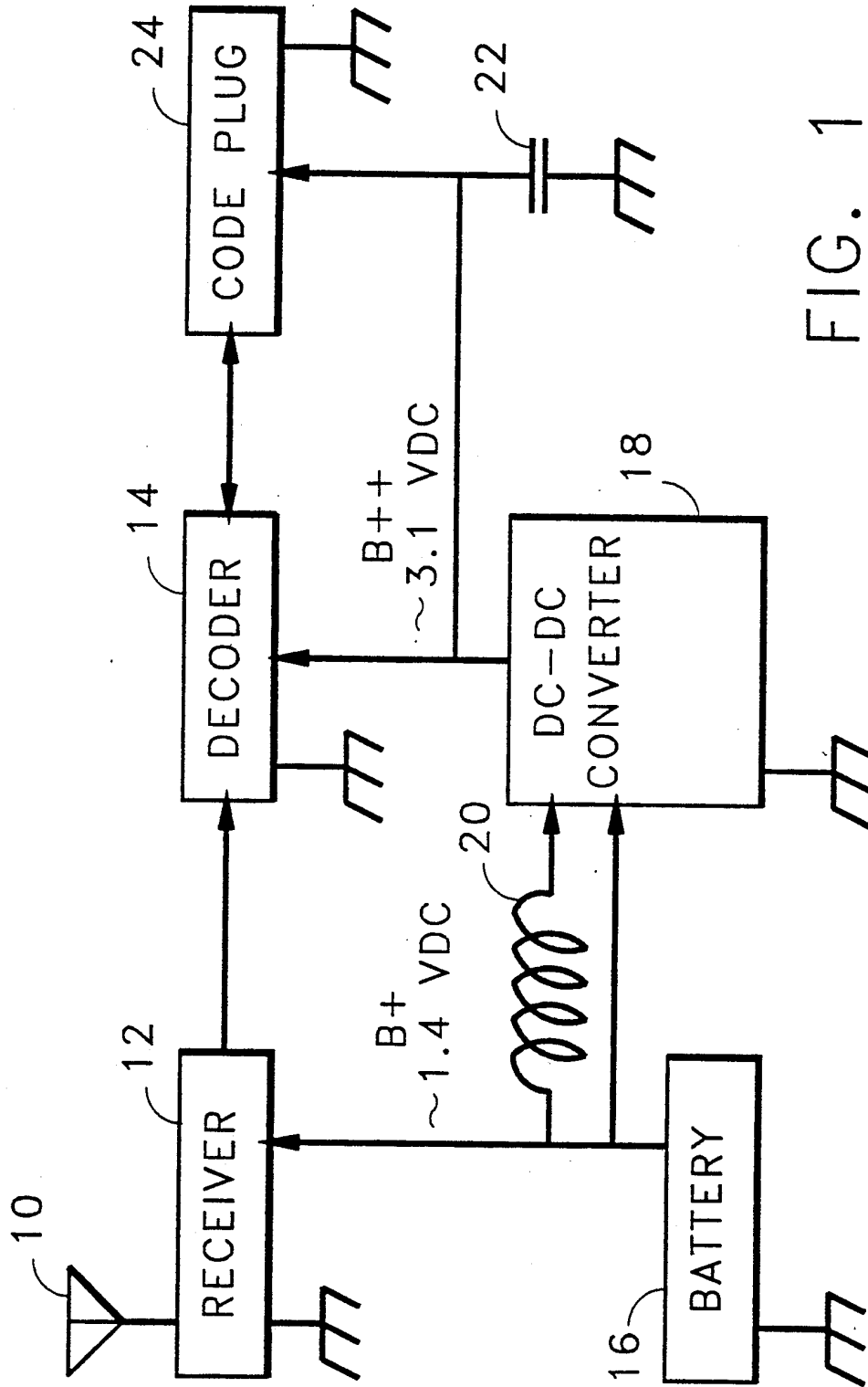
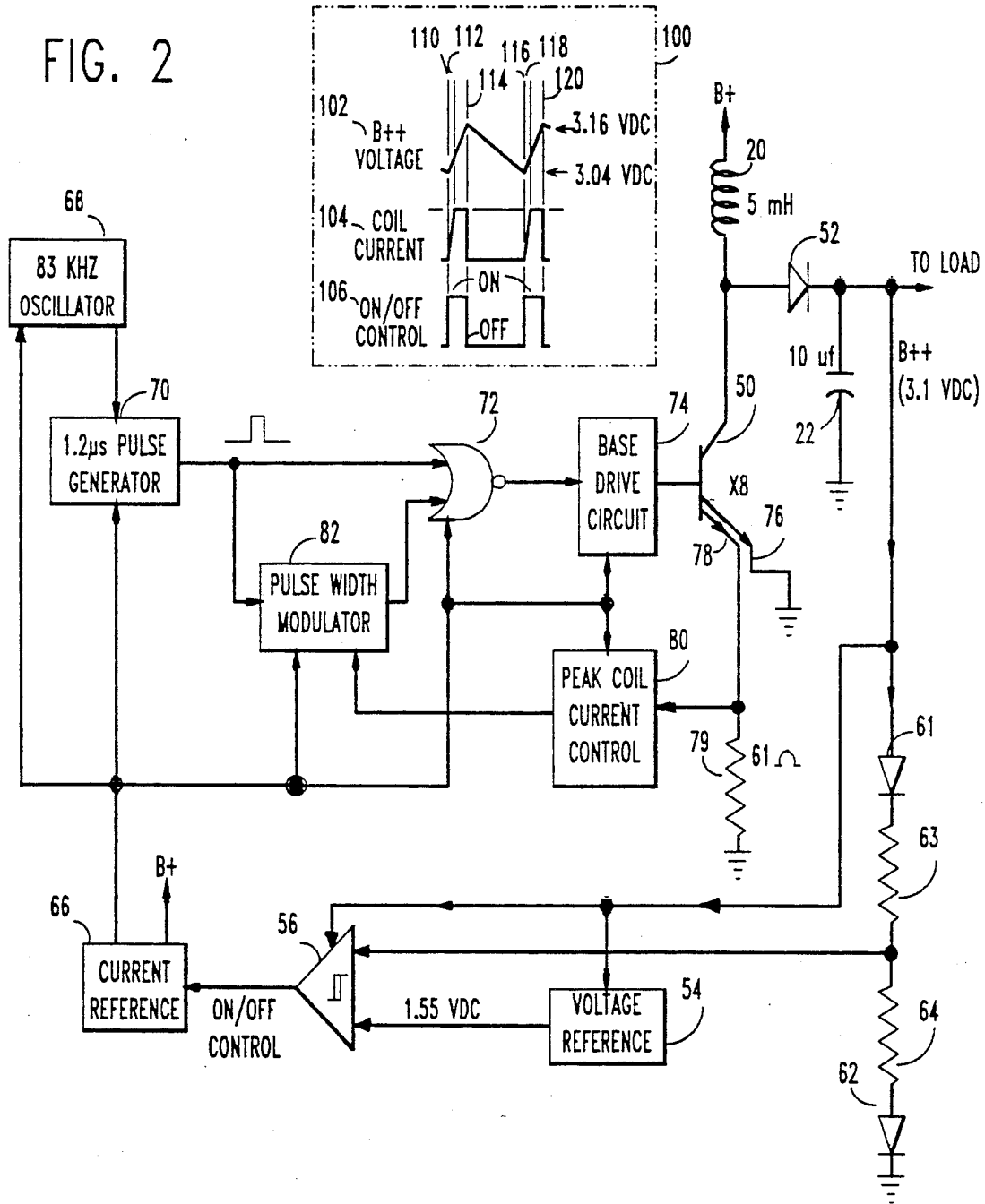


FIG. 1

FIG. 2



STROBED DC-DC CONVERTER WITH CURRENT REGULATION

BACKGROUND OF THE INVENTION

This invention relates in general to the field of DC-DC converters. In particular, this invention relates to boost mode DC-DC converters operating within portable receivers.

Portable receivers such as pagers operate from a single cell battery. The pagers may be controlled by a microcomputer which requires more operating voltage than is available from the single cell battery. Consequently, a DC-DC converter is used to boost the battery voltage to a converted voltage high enough to operate the microcomputer. In place of, or in addition to the microcomputer, the boosted voltage may supply power to other circuits.

In portable battery operated products, such as pagers, it is desirable to have the lowest possible current drain in order to maximize battery life. Since the bias circuits of DC-DC converters consume current, it is desirable to switch the bias circuits off when power conversion is not required. In the past, DC-DC converters have been switched off with a predetermined duty cycle and a predetermined period. Such a method is shown in U.S. Pat. No. 4,634,956 to Davis et. al.

The DC-DC converter described in said patent, periodically switched an inductor to ground using an NPN switching transistor, and in releasing the inductor, developed a voltage potential across the inductor. When the voltage exceeded a predetermined voltage, a rectifying diode transferred the energy in the inductor to a storage capacitor to develop a converted voltage potential. Using a closed loop feedback system, the duty cycle of the periodic switching to ground of the inductor was adjusted to maintain a regulated voltage. However, when the converted voltage was substantially below the regulated voltage, a predetermined maximum duty cycle was selected for operation under worst case conditions. As a result of the predetermined maximum duty cycle, the current through the inductor builds to a large value. This large value caused the inductor to saturate, the NPN switching transistor to be driven out of saturation, and excessive current to be delivered through the rectifying diode. This reduced the conversion efficiency of the DC-DC converter.

When the DC-DC converter was switched off for a predetermined time, circuits were powered by the energy stored within a capacitor coupled to the converted voltage. The capacitor was allowed to discharge during the predetermined time when the DC-DC converter was switched off. Then when the DC-DC converter was switched back on for a second predetermined time, the capacitor was recharged. During the recharge process, the DC-DC converter operated at the aforementioned maximum duty cycle, thereby decreasing the efficiency of the conversion process.

Additionally, the DC-DC converter was powered off and on with a fixed period and for a fixed "on" duration with a signal generated by a microcomputer based pager decoder. The period and "on" duration were selected to insure that the converted voltage does not decay excessively during the off interval under worst case load and circuit parameter conditions. As a result, under typical conditions the "on" duration was excessive which further degraded efficiency. Additionally, the microcomputer had to remain in a relatively high

power operating state in order to power off and on at the fixed period.

Thus, although said patent described a method for the substantial reduction of current within a paging receiver when operating in a reduced power mode, the conversion efficiency of the DC-DC converter degraded, and the microcomputer operated in a relatively high power operating state in order to provide for the substantial current reduction.

Additionally, the DC-DC converter of the aforementioned patent had three operating modes, the first being a low current mode wherein the DC-DC converter powers off and on, which was typically used while the pager operated in a battery saving mode. The second being a medium current load, which was typically used while receiving and processing data. And the third being a high current load, which was typically used while the pager was reading the code plug. The second and third modes are described in U.S. Pat. No. 4,355,277 to Davis et al. The microcomputer issued commands which operated the DC-DC converter in each of these three modes, which was an additional burden for the microcomputer.

SUMMARY OF THE INVENTION

It is therefore an object of this invention to resolve the aforementioned problems.

It is an object of the invention to power a DC-DC converter off and on without the aid of a microcomputer.

It is an object of the present invention to provide a means of powering a DC-DC converter off and on at an optimal period and duty cycle.

It is an object of the present invention to provide a DC-DC converter which has improved conversion efficiency.

It is an object of the present invention to provide a DC-DC converter capable of supplying power at the various load requirements of a paging decoder without the aid of a microcomputer.

In accordance with the present invention, a DC-DC converter comprises a means for converting a first DC voltage to a converted DC voltage with a regulated maximum current, and a power conservation means for powering on said converting means in response to the converted DC voltage being less than a minimum voltage, and for powering off said converting means in response to the converted DC voltage being greater than a maximum voltage.

In accordance with the present invention, a DC-DC converter comprises a switching means for increasing the current flow through an inductor, a current sensing means for sensing the current flow through said switching means, and a regulating means governed by said current sensing means to deactivate said switching means in response to the current flow through the inductor exceeding a predetermined value, thereby decreasing the current flow through the inductor.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 shows a block diagram of a pager operating in accordance with the present invention.

FIG. 2 shows a block diagram of the DC-DC converter operating in accordance with the present invention.

DESCRIPTION OF A PREFERRED EMBODIMENT

FIG. 1 shows a block diagram of a pager operating in accordance with the present invention. Paging signals are received by antennas 10 and demodulated by receiver 12. The paging signals are then decoded by decoder 14. The receiver is powered by a single cell battery 16 which generates a "B+" voltage of typically 1.4V. The decoder is powered by a "B++" voltage which is substantially 3.1V. The B++ voltage is generated by a DC-DC converter 18 which boosts the B+ voltage by switching inductor 20. The B++ voltage is stored on capacitor 22. The B++ voltage also supplies power for the code plug 24.

Receiving and decoding paging signals is well known in the art. The paging signals may be received on any of a plurality of paging protocols such as the GSC, POC-SAG, or 5 tone sequential protocols. In response to the reception of the paging signals, the receiver is periodically activated. Additionally, the decoder operates in a low power mode while the receiver is inactive and operates in a high power mode while the receiver is active. The decoder searches the paging signal for an address which matches an address stored in the code plug. The code plug is powered on in order to read the address, and powered off otherwise. In response to detecting the address, an alert is generated.

Consequently, it can be appreciated that the power consumption from B++ may vary dramatically. The decoder periodically enters high and low current modes, wherein the decoder low current mode may be one twentieth of the current of the decoder high current mode. The code plug is periodically activated, and while activated may consume more than twice the current of decoder high current mode. The prior art DC-DC converters required the decoder to control the DC-DC converter in order to operate over all of the current loads. The DC-DC converter of the present invention however, provides for all of these loading conditions without the microcomputer control, and the efficiency of the conversion process is improved.

FIG. 2 shows a block diagram of the DC-DC converter operating in accordance with the present invention. Battery voltage, B+, is coupled to an input to inductor 20. The output of the inductor is periodically coupled to the common potential of ground through switching transistor 50. While coupled to ground, the current in the inductor builds to a predetermined level, or the inductor is grounded for a predetermined time, in response to either transistor 50 is switched off. Switching the transistor off causes the voltage across the inductor to rise until it substantially equals the voltage on capacitor 22, in response to which diode 52 conducts causing the inductor to deliver energy to the capacitor. Transistor 50 may be switched on and off substantially 83,000 times per second providing for a continuous supply of converted energy. Thus, energy at a boosted voltage is supplied to the capacitor which in turn provides B++ voltage to other circuits such as decoder 14, and code plug 24 of FIG. 1. Inductor 20 is preferably a 5 mH inductor, capacitor 22 is preferably a 10 μ F capacitor and diode 52 is preferably a Schottky diode.

B++ voltage is regulated using a voltage sensing means which enables the energy conversion process in response to the B++ voltage being less than a first predetermined voltage and disables the energy conversion process in response to the B++ voltage being

greater than a second predetermined voltage. Since circuits which provide for the energy conversion process draw power when enabled, disabling the circuits which provide for the energy conversion process also conserves power. Referring to FIG. 2, B++ voltage is used to power a voltage reference 54 which produces a regulated 1.55V. B++ also powers a comparator 56 having effectively 120 mV of hysteresis with respect to B++. One input to the comparator is coupled to the 1.55V signal and the other input is coupled to a voltage derived from B++ voltage, which is divided by diodes 61 and 62 and resistors 63 and 64. The comparator, voltage reference, and voltage divider operate such that the output of the comparator generates an ON signal in response to B++ being less than 3.04V and generates an OFF signal in response to B++ being greater than 3.16V.

The output of the comparator is coupled to current reference 66 which derives power from B+ and powers the circuits which provide for the energy conversion process. These circuits which provide for the energy conversion process include: 83 kHz oscillator 68, 1.2 μ S pulse generator 70, NOR gate 72, base drive circuit 74, peak inductor current control 80, and pulse width modulator 82. The 83 kHz oscillator provides a clocking frequency which eventually switches transistor 50 ON substantially 83,000 time per second. The 1.2 μ S pulse generator provides for a maximum ON duty cycle of transistor 50 of substantially 90%. The output of the 1.2 μ S pulse generator travels through NOR gate 72 and through base drive circuit 74 which causes the transistor 50 to switch ON and OFF.

At the maximum duty cycle, the current through the conversion devices; inductor 20, transistor 50, and diode 52, would build to a very high level. As previously detailed this reduces the efficiency of the energy conversion process. The invention provides a means for regulating this current to a maximum thereby improving the efficiency. The regulating means itself dissipates very little power, thereby only marginally impacting the efficiency of the energy conversion process.

The current through the conversion devices is regulated by reducing the duty cycle of the switching transistor when the current reaches a predetermined level, thereby regulating the current. The current through the conversion devices is sensed by sensing the current through switching transistor 50. Switching transistor 50 is a multiple emitter NPN transistor wherein the emitters have a predetermined ratio established by the geometry of the transistor. The first emitter 76 is coupled directly to the common potential while the second emitter is coupled to the common potential through a sensing resistor 79. A substantially greater current flows through emitter 76 than through emitter 78. Thus the voltage developed across resistor 79 is a function of the current through the conversion devices. Since the majority of the current flows through emitter 76, very little power is dissipated in resistor 79, thereby only marginally impacting the efficiency of the energy conversion process.

In the preferred embodiment, the ratio between the emitters is 8:1. In the preferred embodiment resistor 79 is 61 μ and voltage across the resistor typically does not exceed 18 mV while transistor 50 activated. Since the current is regulated to typically deliver 1 mA at 3.1V, thus 3.1 mW, it can be appreciated that the powered dissipated in resistor 79 is relatively small.

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