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Paper 11
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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SEMICONDUCTOR COMPONENTS INDUSTRIES, LLC
(d/b/a ON SEMICONDUCTOR),
Petitioner,

v.

POWER INTEGRATIONS, INC.,
Patent Owner.

Case IPR2016-01600
Patent 7,834,605 B2

Before THOMAS L. GIANNETTI, BRIAN J. McNAMARA, and LYNNE E. PETTIGREW, *Administrative Patent Judges*.

PETTIGREW, *Administrative Patent Judge*.

DECISION
Institution of *Inter Partes* Review
37 C.F.R. § 42.108

I. INTRODUCTION

Petitioner, Semiconductor Components Industries, LLC, d/b/a ON Semiconductor, filed a Petition for *inter partes* review of claims 1, 2, 5,

and 9 of U.S. Patent No. 7,834,605 B2 (Ex. 1001, "the '605 patent"). Paper 1 ("Pet."). Patent Owner, Power Integrations, Inc., filed a Preliminary Response. Paper 8 ("Prelim. Resp."). Institution of an *inter partes* review is authorized by statute when "the information presented in the petition . . . and any response . . . shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition." 35 U.S.C. § 314(a); *see* 37 C.F.R. § 42.108. Upon consideration of the Petition and Preliminary Response, we conclude the information presented shows there is a reasonable likelihood that Petitioner would prevail in establishing the unpatentability of at least one of the challenged claims of the '605 patent.

A. Related Matters

The '605 patent was involved in the following district court proceeding: *Power Integrations, Inc. v. Fairchild Semiconductor Int'l, Inc.*, No. 1:08-cv-00309 (D. Del.). Pet. 2; Paper 4, 2. An appeal from the district court to the United States Court of Appeals for the Federal Circuit was pending at the time the Petition and Preliminary Response in this case were filed. *See* Pet. 2, 25–26; Paper 4, 2. On December 12, 2016, the Federal Circuit reversed the jury verdict that claims 1 and 2 of the '605 patent were not anticipated by U.S. Patent No. 4,763,238 to Maige (Ex. 1008). *Power Integrations, Inc. v. Fairchild Semiconductor Int'l, Inc.*, 843 F.3d 1315, 1335–39 (Fed. Cir. 2016); *see* Paper 9, 2.

B. The '605 Patent

The '605 patent describes a switch mode power supply with an approximately constant output voltage when the output current is below an output current threshold and an approximately constant output current when

the output voltage is below an output voltage threshold. Ex. 1001, 1:32–38, 1:51–53. In a described embodiment, the power supply includes a regulator circuit that controls the voltage and current at the output of the power supply. *Id.* at 5:31–49, Fig. 4. The regulator includes an internal switch (e.g., a power metal oxide semiconductor field effect transistor (MOSFET)) coupled to the primary winding of the power supply's energy transfer element (e.g., a transformer). *Id.* at 5:37–43, Fig. 4. The regulator may modify the duty cycle of the switch to control the output voltage based on feedback from the output of the power supply. *Id.* at 4:50–53, 5:37–39. The regulator also may modify the duty cycle by turning off the switch when the switch current reaches a current limit. *Id.* at 5:40–43.

According to the '605 patent, there is a fixed delay between the time the switch current reaches a current limit threshold and the time the switch is finally disabled. *Id.* at 3:18–24. This results in a current "overshoot" that will vary based on the input voltage of the power supply. *Id.* at 3:24–27. More specifically, at higher direct current (DC) input voltages, the actual current ramps to a higher level above the current limit threshold than at lower DC input voltages. *Id.* at 3:31–33.

The '605 patent attempts to overcome the problem of current variations and thereby achieve a power supply with an approximately constant output current. *Id.* at 2:45–50, 3:14–17. The purported solution is a power supply regulator circuit that creates a variable current limit threshold that increases during the on-time of the switch. *Id.* at Abstract, 1:53–59. Because the current overshoot is greater at higher DC input voltages than at lower DC input voltages, a variable current limit threshold should be lower for higher DC input voltages to compensate for the excess current during the

delay time. *Id.* at 3:40–44; *see* Ex. 1003 ¶ 22 (Declaration of Dr. Douglas Holberg). Further, because the switch current increases more quickly when the DC input voltage is high, a current limit will be reached earlier in a switching cycle when the DC input voltage is higher than when it is lower. Ex. 1001, 3:45–49; *see* Ex. 1003 ¶¶ 22–23. Thus, a variable current limit threshold that increases from a first level to a second level during the on-time of the switch results in an effective current limit (the sum of the variable current limit and the excess current during the delay) that is approximately constant across different input voltages. Ex. 1001, 3:50–62; *see* Ex. 1003 ¶ 23.

Figure 1 of the '605 patent is reproduced below:

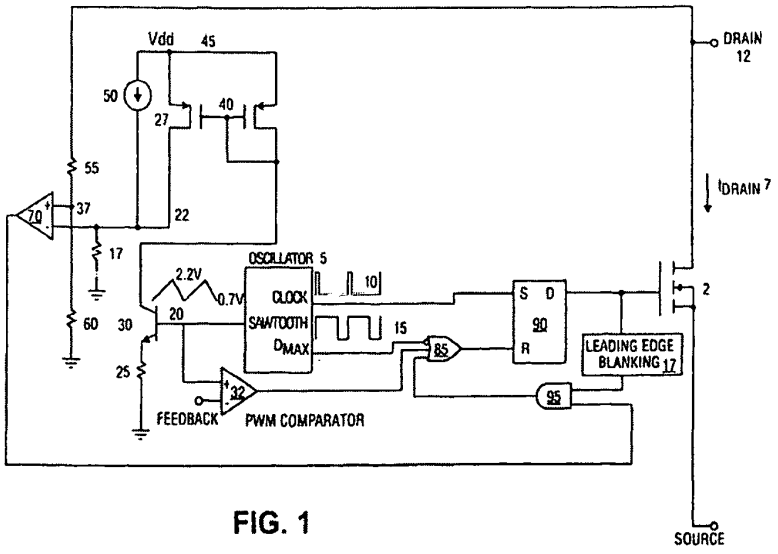

FIG. 1

Figure 1 illustrates an embodiment of a power supply regulator circuit described in the '605 patent. Clock signal 10 sets latch 90 to enable power MOSFET 2 (i.e., turn the switch on). Ex. 1001, 4:19–24. Power MOSFET 2 is disabled (i.e., the switch is turned off) when latch 90 is reset by any one of three inputs to OR gate 85. *Id.* at 4:24–53. First,

comparator 32 may reset latch 90 based on the feedback voltage from the output of the power supply. *Id.* at 4:50–53. Second, comparator 70 may reset latch 90 when the drain current of MOSFET 2 exceeds a variable current limit threshold. *Id.* at 4:29–49. The variable current limit threshold at node 22 is the combination of constant current source 50 and linearly increasing current source 27. *Id.* at 4:32–42. Finally, maximum duty cycle signal D_{MAX} 15 may reset latch 90. *Id.* at 4:24–25.

C. Illustrative Claim

Claim 1 is the only independent claim of the '605 patent and is illustrative of the subject matter of the challenged claims:

> 1. A power supply regulator, comprising:
>
> a comparator having a first input coupled to sense a voltage representative of a current flowing through a switch during an on time of the switch, the comparator having a second input coupled to receive a variable current limit threshold that increases during the on time of the switch;
>
> a feedback circuit coupled to receive a feedback signal representative of an output voltage at an output of a power supply; and
>
> a control circuit coupled to generate a control signal in response to an output of the comparator and in response to an output of the feedback circuit, the control signal to be coupled to a control terminal of the switch to control switching of the switch.

Id. at 6:10–23.

D. Asserted Ground of Unpatentability

Petitioner contends that claims 1, 2, 5, and 9 of the '605 patent are anticipated under 35 U.S.C. § 102(b) by de Sartre.[1] Pet. 21–37.

II. DISCUSSION

A. Statutory Bar under 35 U.S.C. § 315(b)

On November 18, 2015, Petitioner entered into a Merger Agreement with Fairchild Semiconductor International, Inc. ("Fairchild"). Prelim. Resp. 1; Ex. 2001. The Petition was filed on August 11, 2016. The merger was completed five weeks later, on September 19, 2016. Ex. 1012; Paper 6 (Petitioner's Revised Mandatory Notices).

Patent Owner asserts this Petition is time-barred under 35 U.S.C. § 315(b). Prelim. Resp. 1. Under § 315(b), "[a]n inter partes review may not be instituted if the petition requesting the proceeding is filed more than 1 year after the date on which the petitioner, real party in interest, or privy of the petitioner is served with a complaint alleging infringement of the patent." Patent Owner asserts Fairchild was served with a complaint for infringement of the '605 patent on June 6, 2011, more than a year prior to the filing of this Petition.[2] Prelim. Resp. 1. Patent Owner alleges that prior to the merger, Petitioner and Fairchild entered into a Confidentiality Agreement "that addressed the parties' ongoing legal proceedings, acknowledging that they 'share a common legal and commercial interest' and 'are or may become joint defendants in proceedings.'" *Id.* at 8 (quoting

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[1] U.S. Patent No. 4,692,853, issued Sept. 8, 1987 (Ex. 1005).
[2] Case No. 1:08-cv-00309-LPS in the U.S. District Court for the District of Delaware. *See* Ex. 2003 ("Amended Complaint for Patent Infringement").

Ex. 2007, 7). Patent Owner further alleges: "Since Petitioner now owns Fairchild, Petitioner is successor-in-interest to the products that were found to infringe the '605 patent." *Id.* at 6. In addition, Patent Owner asserts: "Petitioner is a privy of Fairchild, despite the fact that the merger was not finalized until just after the filing of the Petition." *Id.* at 8. Finally, Patent Owner argues: "Petitioner has even admitted to the Office that Fairchild is now one of the 'real parties in interest' along with Petitioner." *Id.* (citing Paper 6, 3).

Petitioner maintains that "Fairchild and its subsidiaries had no role in the decision to file the Petition, the content of the Petition, or the preparation of the Petition [and] did not contribute in any manner to the funding for the Petition." Paper 6, 3. Thus, Petitioner contends, Fairchild and its subsidiaries "were not real parties in interest or a privy of Petitioner as of the filing of the Petition or at any time before the close of the merger on September 19, 2016." *Id.*

For the reasons presented by Petitioner, on this record, we are not persuaded by Patent Owner's contention that the Petition should be barred under 35 U.S.C. § 315(b). Panels of the Board have interpreted this statute (and associated rule 37 C.F.R. § 42.101(b)) to mean "it is only privity relationships up until the time a petition is filed that matter." *Synopsys, Inc. v. Mentor Graphics Corp.*, Case IPR2012-00042, slip op. at 12 (PTAB Feb. 19, 2014) (Paper 60); *see also ARRIS Group, Inc. v. TQ Delta LLC*, Case IPR2016-00430, slip op. at 6 (PTAB July 1, 2016) (Paper 9). We agree with the reasoning of those decisions. On this record, therefore, and for the reasons that follow, we are not persuaded that there is sufficient evidence that Fairchild was a privy of Petitioner before the filing of the Petition and,

thus, we are not persuaded 35 U.S.C. § 315(b) bars institution of *inter partes* review.

There is no allegation of privity at the time the complaint was served on Fairchild, in 2011, or that Petitioner controlled or could have controlled the lawsuit between Fairchild and Patent Owner. *See Aruze Gaming Macau, Ltd. v. MGT Gaming, Inc.*, Case IPR2014-01288, 2015 WL 780607, at *8 (PTAB Feb. 20, 2015) ("In the context of § 315(b), the goal of the preclusion is to prevent successive challenges to a patent by those who previously have had the opportunity to make such challenges in prior litigation. As such, the focus of our privity inquiry is on the relationship between the parties *during the prior lawsuit*."). Patent Owner's allegations of privity are directed, instead, to the events surrounding the merger and to the allegation that Petitioner is a proxy for Fairchild. Prelim. Resp. 5–8.

Although not the exclusive factor for establishing privity, control of the requested review procedure is an important factor to establish privity in this context. Our *Office Patent Trial Practice Guide* explains that "[w]hether a party who is not a named participant in a given proceeding nonetheless constitutes a . . . 'privy' to that proceeding is a highly fact-dependent question." 77 Fed. Reg. 48,756, 48,759 (Aug. 14, 2012). "There are multiple factors relevant to the question of whether a non-party may be recognized as a . . . 'privy.'" *Id.* "A common consideration is whether the non-party exercised or could have exercised control over a party's participation in a proceeding." *Id.* However, it is recognized that there is no definitive test regarding the degree of participation required to establish such control and, hence, to establish a privity relationship. *Id.*

In *ARRIS*, the panel determined that patent owner's evidence of an agreement of a future merger was insufficient to show any degree of control over the requested review procedure or even the opportunity to do so. IPR2016-00430, slip op. at 7 (Paper 9). Here, we are not persuaded, on the present record, that Patent Owner's assertions regarding the Merger Agreement detailing a future merger, which was not yet completed at the time of filing this Petition, are sufficient to demonstrate the opportunity for control by Fairchild over this proceeding.

Similarly, Patent Owner's assertions regarding the pre-merger Confidentiality Agreement are insufficient to demonstrate that Fairchild exercised, or could have exercised, any control over this proceeding. The mere exchange of unidentified confidential information and recitations that the parties could be joint defendants in the future, without more, do not provide sufficient evidence that Fairchild has exercised, or could have exercised, any control over this proceeding. *See* Prelim. Resp. 7–8. Thus, the record lacks sufficient evidence to demonstrate even the opportunity to control this review and, thus, to establish privity between Petitioner and Fairchild.

Nor is there any persuasive evidence to support a conclusion that Petitioner is acting as a proxy for Fairchild. Compare *RPX Corp. v. VirnetX, Inc.*, IPR2014-00171, slip op. at 9 (PTAB July 14, 2014) (Paper 57), where the Board concluded RPX was "at most, a 'nominal plaintiff' with 'no substantial interest' in [the] IPR challenges apart from those of its client, Apple." Such is not the situation here.

Accordingly, we determine that, based on the evidence presented at this stage of the proceeding, 35 U.S.C. § 315(b) does not bar institution of this *inter partes* review.

B. Claim Construction

In an *inter partes* review, we construe claim terms in an unexpired patent according to their broadest reasonable construction in light of the specification of the patent in which they appear. 37 C.F.R. § 42.100(b); *Cuozzo Speed Techs., LLC v. Lee*, 136 S. Ct. 2131, 2144–46 (2016) (upholding the use of the broadest reasonable interpretation standard). Consistent with the broadest reasonable construction, claim terms are presumed to have their ordinary and customary meaning as understood by a person of ordinary skill in the art in the context of the entire patent disclosure. *In re Translogic Tech., Inc.*, 504 F.3d 1249, 1257 (Fed. Cir. 2007). An inventor may provide a meaning for a term that is different from its ordinary meaning by defining the term in the specification with reasonable clarity, deliberateness, and precision. *In re Paulsen*, 30 F.3d 1475, 1480 (Fed. Cir. 1994).

Petitioner contends that resolution of this *inter partes* review does not require express construction of any claim terms. Pet. 21. Patent Owner proposes a construction for "a variable current limit threshold that increases during the on time of the switch," recited in independent claim 1. Prelim. Resp. 29–35. We address that claim phrase below. For purposes of this decision, we determine that no other claim terms require express construction.

Patent Owner argues that to be consistent with the specification, the "variable current limit threshold" in claim 1 "must increase in a way that is

detectable and usable by the circuit as a function of the time elapsed during each switching cycle." *Id.* at 29. Petitioner does not propose a construction for this claim language but asserts in the context of its unpatentability analysis that the claims "do not require any particular amount of increase in the current limit threshold during the on-time of the switch." Pet. 27. Based on the plain language of the claim, Petitioner argues that "any increase, regardless the magnitude, during the on-time of the switch satisfies this claim element." *Id.* (citing Ex. 1003 ¶ 46).

Patent Owner begins its argument for limiting the scope of the claim language by quoting the stated goal of the invention described in the '605 patent—"to maintain a constant actual current limit over DC input voltage variations." Ex. 1001, 3:39–40; *see* Prelim. Resp. 29. Patent Owner further asserts that "the purpose of using an increasing current limit threshold is to create an intrinsic current limit that decreases relative to the DC input voltage in order to compensate for the relatively larger overshoot that accompanies relatively higher DC input voltages." Prelim Resp. 30. The '605 patent, however, does not claim a regulator with a variable current limit threshold used to maintain a constant output current in a power supply or to compensate for current overshoot. *See* Pet. 13, 15. As explained in the Petition, an earlier patent in the chain of continuations that includes the '605 patent does contain claims reciting both an increasing current limit threshold and a power supply having a constant output current that results from the variable current limit threshold. Pet. 13–14 (citing Ex. 1002, 6:47–63 (claim 6 of U.S. Patent No. 7,110,270 B2)). But claim 1 of the '605 patent was drafted more broadly to exclude the "constant output current" limitation. *See id.* at 15; Ex. 1001, 6:10–23. Thus, claim 1 of the

'605 patent recites a variable current limit threshold that increases during the on-time of the switch but does not include a limitation requiring the increasing current limit threshold to be used for a particular purpose, such as providing a power supply with a constant output current.

Patent Owner further argues that "[b]oth logic and consistency with the specification demonstrate that there must be *some minimum bound* to the amount of increase that constitutes 'a variable current limit threshold that increases during the on time of the switch.'" Prelim. Resp. 34. According to Patent Owner, this "minimum bound" must encompass an increase that is "detectable" and "must be measurable to be used as a mechanism to determine the elapsed on-time of the switch." *Id.* at 35. For support, Patent Owner cites the following sentence from the '605 patent: "It is simply necessary to increase the intrinsic current limit as a function of the time elapsed during the cycle." Ex. 1001, 3:54–55; *see* Prelim. Resp. 35. Contrary to Patent Owner's argument, this sentence does not require that an increase in the current limit be sufficiently detectable that it can be used to determine the elapsed on-time of the switch. Rather, it simply provides that the current limit threshold must increase as a function of elapsed time during the switch cycle, i.e., during the on-time of the switch, which is exactly what claim 1 recites.

On the present record, Patent Owner has not persuaded us that anything in the claim language or written description of the '605 patent requires the recited variable current limit threshold to increase by a minimum amount or be used to achieve a particular goal. Instead, for purposes of this decision, we agree with Petitioner that the broadest reasonable interpretation of "a variable current limit threshold that increases

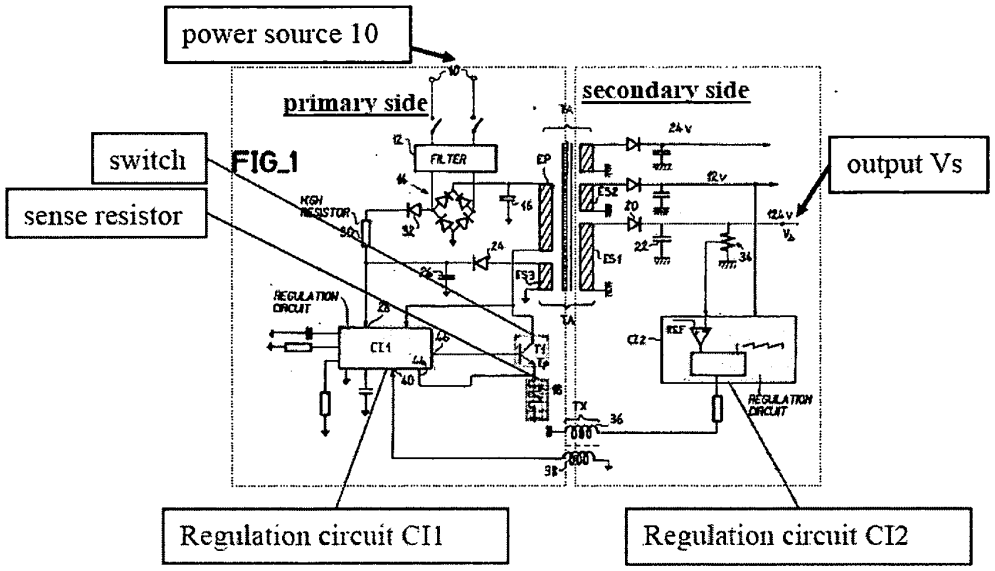
during the on time of the switch" does not require any particular amount of increase during the on-time of the switch.

C. Asserted Anticipation by de Sartre

Petitioner contends that claims 1, 2, 5, and 9 of the '605 patent are unpatentable under 35 U.S.C. § 102(b) as anticipated by de Sartre. Pet. 21–36. Relying on the testimony of Dr. Holberg, Petitioner explains how de Sartre allegedly discloses all limitations of the challenged claims. *Id.* (citing Ex. 1003).

1. Overview of de Sartre

de Sartre discloses a switch mode power supply that includes two integrated circuits—regulation circuits CI1 and CI2. Ex. 1005, Fig. 1. Figure 1 of de Sartre (annotated by Petitioner) is reproduced below:



Pet. 17; Ex. 1005, Fig. 1. Figure 1 illustrates a power supply with regulation circuits CI1 and CI2 on the primary and secondary side, respectively, of a transformer. Ex. 1005, 4:11–14. Regulation circuit CI1 controls the base of

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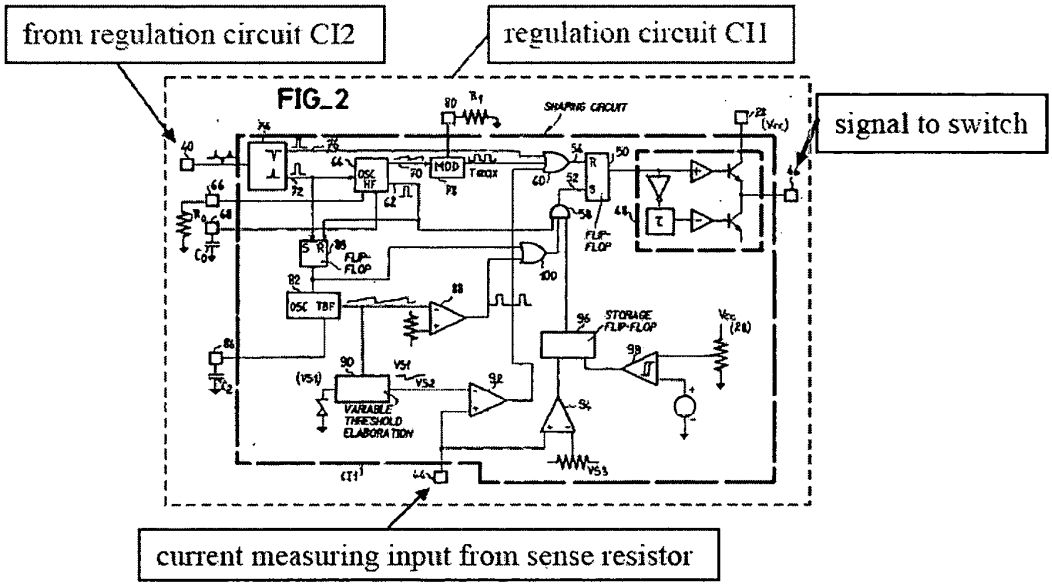
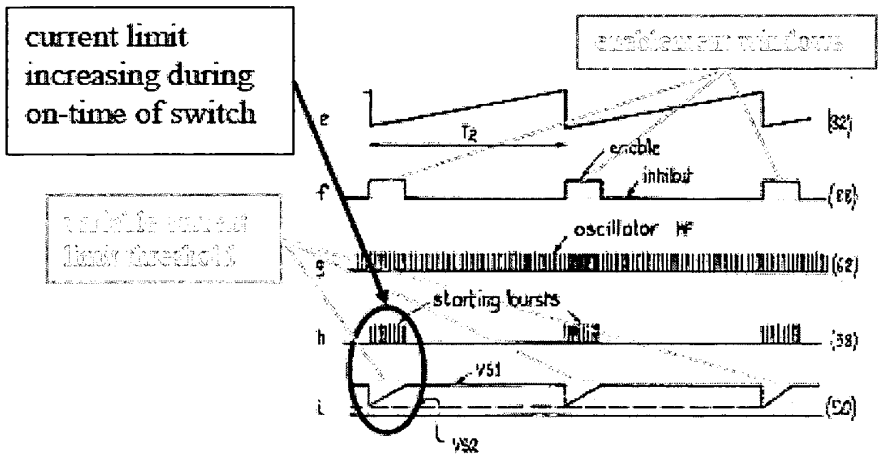
power transistor T_p (i.e., a switch), which controls the flow of current from electric mains line 10 (i.e., a power source) into the primary winding of the transformer. *Id.* at 1:30–36, 1:41–45. Regulation circuit CI2 monitors the output voltage of the power supply and sends feedback to regulation circuit CI1. *Id.* at 1:36–41. During normal operation of the power supply, regulation circuit CI2 sends regulation signals to regulation circuit CI1 to cause the switch to turn on and off. *Id.* at 10:45–50.

Figure 2 of de Sartre (annotated by Petitioner) is reproduced below:



Pet. 18; Ex. 1005, Fig. 2. Figure 2 illustrates detail of regulation circuit CI1. Ex. 1005, 4:15–17. To protect the switch, the power supply may use a safety mode during start-up or when an overcurrent condition is detected. *Id.* at 2:48–53. In safety mode, regulation circuit CI1 gradually increases current through the switch. *Id.* at 2:53–3:11.

Figure 4 of de Sartre (annotated by Petitioner) illustrates timing diagrams of signals at different nodes in CI1 during start-up:



Pet. 19; Ex. 1005, Fig. 4. Figure 4, above, shows signals (e)–(i) at oscillator 82, comparator 88, high-frequency oscillator 62, AND gate 58, and variable threshold elaboration circuit 90 of regulation circuit CI1, respectively. Ex. 1005, 10:14–39. During short enablement windows (f), bursts of triggering pulses (h) are sent to transistor T_p while the current limit threshold (i) is increased gradually from a low value, Vs2, to the current limit used during normal operation, Vs1. *Id.* at 7:8–28, 8:52–64, 9:37–42. Each triggering pulse may enable, or turn on, transistor T_p. *Id.* at 8:55–65, 10:45–48; *see* Ex. 1003 ¶ 34.

2. Analysis

After the Petition and Preliminary Response in this case were filed, the Federal Circuit reversed a jury verdict that claims 1 and 2 of the '605 patent are not anticipated by Maige. *Power Integrations*, 843 F.3d at 1335–38. Although the mandate has issued, the time for filing a petition for writ of certiorari has not expired. Furthermore, the remaining challenged claims depend from claim 1 or claim 2 and thus incorporate the limitations of those claims. *See* Ex. 1001, 6:35–38, 6:51–53 (claims 5 and 9). For these

reasons, we include claims 1 and 2 in our analysis of Petitioner's asserted anticipation ground.

a. Claim 1

Petitioner contends that de Sartre discloses a power supply regulator that satisfies all the limitations of independent claim 1. Pet. 21–32. We address the parties' arguments for each limitation.

"comparator having a first input [and] a second input"

First, Petitioner argues that comparator 92 in de Sartre's regulator circuit CI1 is "a comparator having a first input coupled to sense a voltage representative of a current flowing through a switch during an on time of the switch, [and] a second input coupled to receive a variable current limit threshold that increases during the on time of the switch." *Id.* at 23–28. Petitioner asserts that the recited first input is input 44, which is the voltage across current sense resistor 18 created by current from the emitter of transistor T_p (i.e., the switch) when the switch is on. *Id.* at 23–24 (citing Ex. 1005, 4:38–41, 5:58–59, Fig. 1, Fig. 2; Ex. 1003 ¶ 40). Petitioner further asserts that the recited second input to the comparator is the threshold signal produced by circuit 90 when the power supply is in safety mode. *Id.* at 24–25 (citing Ex. 1005, 7:41–45, 7:49–50, 8:55–65, 9:25–26, 9:39–42, 10:45–46, Fig. 4; Ex. 1003 ¶¶ 41–42). With reference to Figure 4 of de Sartre, Petitioner contends that each burst of triggering pulses (h) to turn on transistor T_p during an enablement window (f) is subject to the progressively increasing current limit threshold (i) produced by circuit 90. *Id.* Petitioner further argues that during each triggering pulse, which may turn on transistor T_p,, the output signal of circuit 90 is a "variable current limit threshold that increases during an on time of the switch," as recited in claim 1. *Id.* at 25.

Patent Owner responds that de Sartre does not disclose a variable current limit threshold that increases during an on-time of the switch because "de Sartre teaches only a current limit signal that for any given single switch on-time would be essentially fixed and not provide a detectable increase." Prelim. Resp. 36. Patent Owner argues that although there may be an increase in the current limit threshold during a given on-time of the switch, the increase is too small to be easily detectable with, for example, an oscilloscope. *Id.* at 40–44. Patent Owner further argues that de Sartre does not address the same problem as the '605 patent—maintaining a constant actual current limit over DC voltage variations. *Id.* at 36. Instead, Patent Owner continues, de Sartre is directed to addressing problems that arise when a power supply first starts up. *Id.* at 37.

On the present record, we are not persuaded by Patent Owner's arguments. As discussed above, for purposes of this decision we agree with Petitioner that the broadest reasonable construction of the "variable current limit threshold" does not require any particular amount of increase during the on-time of the switch. Although we agree with Patent Owner that the annotated excerpt of de Sartre's Figure 4 on page 25 of the Petition does not accurately show the number of triggering pulses (switch on-times) that occur while the current limit threshold increases from Vs2 to Vs1, *see* Prelim. Resp. 39–40,[3] the Petition and supporting evidence nevertheless indicate there is some increase during an on-time of the switch. *See* Pet. 23–25, 27—28; Ex. 1003 ¶ 42. Under our claim construction, that is all that is required.

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[3] *See also* Ex. 1005, 10:19–22 ("The high frequency pulses have however been shown symbolically in FIG. 4, in a more limited number than in reality for facilitating the representation.").

Furthermore, as discussed previously, claim 1 is not directed to the particular problem of maintaining a constant output current, so de Sartre may anticipate claim 1 as long as it discloses a variable current limit threshold that increases during the on-time of the switch, even if used for a different purpose than the increasing current limit threshold described in the '605 patent.

For these reasons, we determine that Petitioner has shown sufficiently for purposes of this decision that de Sartre discloses a comparator as recited in claim 1, including a variable current limit threshold that increases during the on-time of the switch. Our determination is consistent with the Federal Circuit's decision regarding anticipation of claim 1 by Maige. *See Power Integrations*, 843 F.3d at 1335–38. As Petitioner indicates, Maige and de Sartre share a common inventor and have overlapping, but not identical, disclosures. *See* Pet. 27; Ex. 1008, 6:63–65 (referring to Maige's Figures 1 and 2, which are similar to Figures 1 and 2 of de Sartre, as "prior art"). *Compare* Ex. 1005, Figs. 1 & 2, and Ex. 1005, 4:25–8:26 (describing Figures 1 and 2 of de Sartre), *with* Ex. 1008, Figs. 1 & 2, and Ex. 1008, 1:32–5:49 (describing similar Figures 1 and 2 of Maige). In the district court case and subsequent appeal, Fairchild apparently relied on the same disclosure of a current threshold during start-up mode in regulation circuit CI1 cited by Petitioner here, although Maige does not include the timing diagrams of de Sartre's Figure 4 that further explain the operation of regulator circuit CI1 in Figure 2. *See Power Integrations*, 843 F.3d at 1336; Pet. 27. The Federal Circuit ultimately found that Patent Owner's expert conceded in his trial testimony that Maige's current threshold increases during the on-time of the switch, and therefore concluded the jury lacked

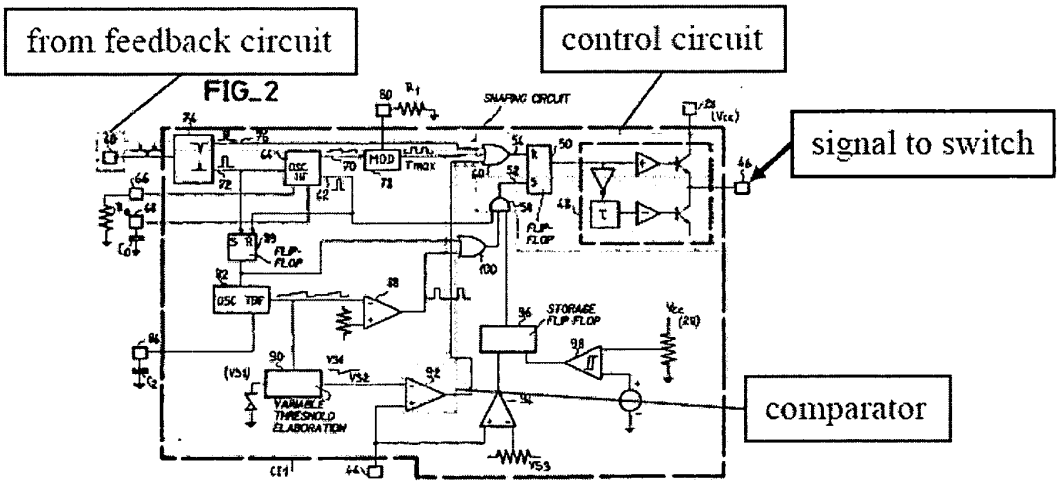
substantial evidence to find that Maige did not anticipate claim 1 of the '605 patent. *Power Integrations*, 843 F.3d at 1337–38.

"feedback circuit"

Petitioner contends that de Sartre's regulation circuit CI2 is a "feedback circuit coupled to receive a feedback signal representative of an output voltage at an output of a power supply," as recited in claim 1, because it receives information concerning the value of Vs, the output voltage of the power supply, and feeds a signal representative of that output voltage back to regulation circuit CI1. Pet. 28–29 (citing Ex. 1005, 5:21–25, 5:36–41, Fig. 1). Patent Owner does not respond to this argument. For purposes of this decision, Petitioner has shown sufficiently that de Sartre discloses this limitation.

"control circuit"

Petitioner asserts that OR gate 60, AND gate 58, flip flop 50, and amplification stage 48 collectively serve as "a control circuit coupled to generate a control signal in response to an output of the comparator and in response to an output of the feedback circuit, the control signal to be coupled to a control terminal of the switch to control switching of the switch," as recited in claim 1. Pet. 30–31. The Petition includes the following annotated version of Figure 2 of de Sartre:



Id. at 30. As shown in annotated Figure 2, Petitioner asserts that OR gate 60 of the control circuit receives one input from regulation circuit CI2 (i.e., the claimed "output of the feedback circuit") via terminal 40, and a second input from comparator 92 (i.e., the claimed "output of the comparator"). *Id.*; *see* Ex. 1005, Fig. 2. Petitioner further submits that the output of OR gate 60 is coupled to reset input 54 of flip flop 50 to control transistor T_P (i.e., the switch) through output 46, so that a control signal is generated "in response to an output of the comparator and in response to an output of the feedback circuit." Pet. 30 (citing Ex. 1005, 6:14–17).

Patent Owner argues that de Sartre does not disclose this limitation because de Sartre's control circuit cannot respond to both of the recited inputs during any given switch on-time. Prelim. Resp. 44–49. Patent Owner points out that regulation circuit CI2 sends feedback regulation signals to regulation circuit CI1 only during normal operations, when the regulator is not in start-up mode and the threshold elaboration circuit that provides an input to comparator 92 is fixed, not variable. *Id.* at 46–48 (citing Ex. 1005, 3:33–34, 3:52–53, 3:65–66, 8:46–51, 9:10–14, 9:56–60). In other words, the

"output of the feedback circuit" relied on by Petitioner exists in de Sartre only during normal operations, and the "output of the comparator" relied on by Petitioner exists only during start-up mode. Therefore, in Patent Owner's view, de Sartre's control circuit is not within the scope of the claim because it never has the capability to generate a control signal in response to two different inputs, i.e., at any given time it can generate a control signal in response to only one of the inputs. *Id.* at 45–46.

On the present record, we do not agree with Patent Owner's reading of the claim language. Nothing in the claim requires the control circuit to be able to generate a control signal that is responsive to both the comparator output and the feedback circuit output at the same time. Indeed, OR gate 60 in de Sartre's control circuit appears to perform the same function as OR gate 85 in the regulator circuit disclosed in the '605 patent—generating a control signal in response to any of the inputs to the OR gate. *Compare* Ex. 1005, Fig. 2, *with* Ex. 1001, Fig. 1. Thus, we determine that Petitioner has shown sufficiently for purposes of institution that de Sartre discloses the "control circuit" limitation.

Conclusion

For the foregoing reasons, based on the present record, we are persuaded Petitioner has shown sufficiently for purposes of this decision that de Sartre discloses all the limitations of claim 1 of the '605 patent. Accordingly, we determine the information presented shows a reasonable likelihood that Petitioner would prevail in establishing that de Sartre anticipates claim 1.

b. Claims 2, 5, and 9

Claims 2 and 9 depend from claim 1, and claim 5 depends from claim 2. Petitioner contends that de Sartre discloses the additional limitations of these dependent claims. Pet. 32–36. Patent Owner does not present any arguments in the Preliminary Response addressing these claims. Having reviewed the Petition and supporting evidence, we are persuaded Petitioner has shown sufficiently for purposes of this decision that de Sartre describes the additional limitations recited in these claims. Accordingly, we determine the information presented shows a reasonable likelihood that Petitioner would prevail in establishing that de Sartre anticipates claims 2, 5, and 9.

III. CONCLUSION

For the foregoing reasons, we determine the information presented establishes a reasonable likelihood that Petitioner would prevail in showing that claims 1, 2, 5, and 9 of the '605 patent are unpatentable. At this preliminary stage, we have not made a final determination with respect to the patentability of the challenged claims or any underlying factual and legal issues.

IV. ORDER

Accordingly, it is:

ORDERED that pursuant to 35 U.S.C. § 314(a), an *inter partes* review is instituted as to claims 1, 2, 5, and 9 of the '605 patent on the ground of anticipation by de Sartre; and

FURTHER ORDERED that pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4, notice is hereby given of the institution of a trial, which commences on the entry date of this decision.

PETITIONER:

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PATENT OWNER:

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UNITED STATES PATENT AND TRADEMARK OFFICE

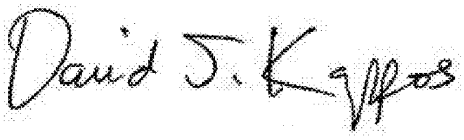
CERTIFICATE OF CORRECTION

PATENT NO.	: 7,834,605 B2
APPLICATION NO.	: 12/581054
DATED	: November 16, 2010
INVENTOR(S)	: Balakrishnan et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In Column 6, Line 55, delete “minor” and replace with -- mirror --.

Signed and Sealed this
Seventeenth Day of May, 2011



David J. Kappos
Director of the United States Patent and Trademark Office

PTO/SB/44 (09-07)
Approved for use through 08/31/2010. OMB 0651-0033
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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(Also Form PTO-1050)

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 7,834,605 B2

APPLICATION NO.: 12/581,054

ISSUE DATE : November 16, 2010

INVENTOR(S) : Balakrishnan et al.

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In Column 6, Line 55, delete “minor” and replace with -- mirror --.

MAILING ADDRESS OF SENDER (Please do not use customer number below):

BLAKELY SOKOLOFF TAYLOR & ZAFMAN LLP
1279 Oakmead Parkway
Sunnyvale, California 94085

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The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

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5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
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9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Acknowledgement Receipt	
EFS ID:	9875240
Application Number:	12581054
International Application Number:	
Confirmation Number:	1732
Title of Invention:	METHOD AND APPARATUS FOR MAINTAINING A CONSTANT LOAD CURRENT WITH LINE VOLTAGE IN A SWITCH MODE POWER SUPPLY
First Named Inventor/Applicant Name:	Balu Balakrishnan
Customer Number:	08791
Filer:	James Go/Steven Welch
Filer Authorized By:	James Go
Attorney Docket Number:	5510P064C4
Receipt Date:	13-APR-2011
Filing Date:	16-OCT-2009
Time Stamp:	19:10:15
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Transmittal Letter	5510P064C4_COC_transmittal_Ltr_041311.PDF	22662 e17e28a8e37708f885b742356a522785e2df3838	no	1
Warnings:					
Information:					

2	Request for Certificate of Correction	5510P064C4_CertCorrection.pdf	35302 5ddea0fedf342272aa792e4f8d71902e8714447e	no	2
Warnings:					
Information:					
			Total Files Size (in bytes):	57964	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

BLAKELY SOKOLOFF
TAYLOR ZAFMAN LLP

601 Union Street, Suite 3000
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www.bstz.com | mail@bstz.com

April 13, 2011

Attention: Certificate of Correction Branch
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Re: **CERTIFICATE OF CORRECTION**
U.S. Letters Patent No. 7,834,605 B2
Issued: November 16, 2010
For: METHOD AND APPARATUS FOR MAINTAINING A CONSTANT LOAD CURRENT WITH LINE VOLTAGE IN A SWITCH MODE POWER SUPPLY
Inventors: Balakrishnan et al.
Our File No. 5510P064C4

Dear Sir:

Enclosed is a Certificate of Correction for the above-identified Letters Patent.

This request for correction of Column 6, Line 55 is made under rule 37 C.F.R. 1.322 and 35 U.S.C. 254, and so no fee is required.

Respectfully submitted,

BLAKELY SOKOLOFF TAYLOR & ZAFMAN LLP

James Y. Go
Reg. No. 40,621

JYG/sew

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APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/581,054	11/16/2010	7834605	5510P064C4	1732

8791 7590 10/27/2010

BLAKELY SOKOLOFF TAYLOR & ZAFMAN LLP
1279 OAKMEAD PARKWAY
SUNNYVALE, CA 94085-4040

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 0 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

Balu Balakrishnan, Saratoga, CA;
Alex B. Djenguerian, Saratoga, CA;
Kent Wong, Fremont, CA;
David Michael Hugh Matthews, Windsor, UNITED KINGDOM;

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
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INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

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8791 7590 07/13/2010

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1279 OAKMEAD PARKWAY
SUNNYVALE, CA 94085-4040

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Certificate of Mailing or Transmission via EFS-web
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

Kristy A. Marvel	(Depositor's name)
Kristy A Marvel	(Signature)
October 12, 2010	(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/581,054	10/16/2009	Balu Balakrishnan	5510P064C4	1732

TITLE OF INVENTION: METHOD AND APPARATUS FOR MAINTAINING A CONSTANT LOAD CURRENT WITH LINE VOLTAGE IN A SWITCH MODE POWER SUPPLY

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1510	$300	$0	$1810	10/13/2010

EXAMINER	ART UNIT	CLASS-SUBCLASS
PATEL, RAJNIKANT B	2838	323-282000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 Blakely Sokoloff Taylor
2 & Zafman, LLP
3

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE: Power Integrations, Inc.

(B) RESIDENCE: (CITY and STATE OR COUNTRY): San Jose, California, U.S.A.

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:
☒ Issue Fee
☒ Publication Fee (No small entity discount permitted)
☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**
☐ A check is enclosed.
☐ Payment by credit card. Form PTO-2038 is attached.
☒ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number 02-2666 (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)
☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.
☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____ Date October 12, 2010

Typed or printed name James Y. Go Registration No. 40,621

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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Electronic Patent Application Fee Transmittal

Application Number:	12581054
Filing Date:	16-Oct-2009
Title of Invention:	METHOD AND APPARATUS FOR MAINTAINING A CONSTANT LOAD CURRENT WITH LINE VOLTAGE IN A SWITCH MODE POWER SUPPLY
First Named Inventor/Applicant Name:	Balu Balakrishnan
Filer:	James Go/Kristy Marvel
Attorney Docket Number:	5510P064C4
Filed as Large Entity	

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Utility Appl issue fee	1501	1	1510	1510
Publ. Fee- early, voluntary, or normal	1504	1	300	300

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
		Total in USD ($)		**1810**

Electronic Acknowledgement Receipt	
EFS ID:	8610237
Application Number:	12581054
International Application Number:	
Confirmation Number:	1732
Title of Invention:	METHOD AND APPARATUS FOR MAINTAINING A CONSTANT LOAD CURRENT WITH LINE VOLTAGE IN A SWITCH MODE POWER SUPPLY
First Named Inventor/Applicant Name:	Balu Balakrishnan
Customer Number:	08791
Filer:	James Go/Kristy Marvel
Filer Authorized By:	James Go
Attorney Docket Number:	5510P064C4
Receipt Date:	12-OCT-2010
Filing Date:	16-OCT-2009
Time Stamp:	18:01:12
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	$1810
RAM confirmation Number	5669
Deposit Account	022666
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees) Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)	

Charge any Additional Fees required under 37 C.F.R. Section 1.19 (Document supply fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.20 (Post Issuance fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Issue Fee Payment (PTO-85B)	5510P064C4_IssueFee_101210.PDF	47653 4e223365edc7994caae941013f7d511f135a2c75	no	1
Warnings:					
Information:					
2	Fee Worksheet (PTO-875)	fee-info.pdf	32443 5e0456b242d87d1cbc6acb7b1902fde282a94e9a	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	80096		

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<u>New Applications Under 35 U.S.C. 111</u>
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

<u>National Stage of an International Application under 35 U.S.C. 371</u>
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

<u>New International Application Filed with the USPTO as a Receiving Office</u>
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Substitute for Form 1449/PTO				Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)				Application Number	*New Patent Application*
				Filing Date	*Concurrently herewith*
				First Named Inventor:	Balakrishnan et al.
				Art Unit	*Not Yet Assigned*
				Examiner Name	*Not Yet Assigned*
Sheet	1	**of**	4	Attorney Docket Number	5510P064C4

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number		Publication Date MM/DD/YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
			Number-Kind Code[2] (If known)			
	1.	US-	3,694,772	09/26/1972	Sordello	
	2.	US-	4,032,828	06/28/1977	Strobl et al.	
	3.	US-	4,357,572	11/02/1982	Andersen et al.	
	4.	US-	4,371,824	02/01/1983	Gritter	
	5.	US-	4,392,103	07/05/1983	O'Sullivan et al.	
	6.	US-	4,674,020	06/16/1987	Hill	
	7.	US-	4,764,856	08/16/1988	Rausch	
	8.	US-	5,014,178	05/07/1991	Balakrishnan	
	9.	US-	5,045,800	09/03/1991	Kung	
	10.	US-	5,170,333	12/08/1992	Niwayama	
	11.	US-	5,189,599	02/23/1993	Messman	
	12.	US-	5,268,631	12/07/1993	Gorman et al.	
	13.	US-	5,285,366	02/08/1994	Zaretsky	
	14.	US-	5,313,381	05/17/1994	Balakrishnan	
	15.	US-	5,335,162	08/02/1994	Martin-Lopez et al.	
	16.	US-	5,465,201	11/07/1995	Cohen	
	17.	US-	5,479,090	12/26/1995	Schultz	
	18.	US-	5,583,752	12/10/1996	Sugimoto et al.	
	19.	US-	5,657,211	08/12/1997	Brockmann	
	20.	US-	5,680,034	10/21/1997	Redl	
	21.	US-	5,729,120	03/17/1998	Stich et al.	
	22.		5,729,443	03/17/1998	Pavlin	
	23.	US-	5,995,386	11/30/1999	John et al.	
	24.	US-	6,037,674	03/14/2000	Hargedon et al.	
	25.	US-	6,154,377	11/28/2000	Balakrishnan et al.	
	26.	US-	6,166,521	12/26/2000	Mercer et al.	
	27.	US-	6,222,356 B1	04/24/2001	Taghizadeh-Kaschani	
	28.	US-	6,226,190 B1	05/01/2001	Balakrishnan et al.	

Examiner Signature	/Rajnikant Patel/	Date Considered	09/07/10

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1]Applicant's unique citation designation number (optional). [2]See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. [3]Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). [4]For Japanese patent documents, the indication of the year of reign of the Emperor must precede the serial number of the patent document. [5]Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. [6]Applicant is to place a check mark here if English language translation is attached.

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SENT FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.**

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /R.P./

Substitute for Form 1449/PTO				Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(use as many sheets as necessary)*				Application Number	~~New Patent Application~~ 12/581054
				Filing Date	*Concurrently herewith*
				First Named Inventor:	Balakrishnan et al.
				Art Unit	~~*Not Yet Assigned*~~ 2838
				Examiner Name	*Not Yet Assigned*
Sheet	2	**of**	4	Attorney Docket Number	5510P064C4

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] (If known)		Publication Date MM/DD/YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	29.	US-	6,233,161 B1	05/15/2001	Balakrishnan et al.	
	30.	US-	6,297,623 B1	10/02/2001	Balakrishnan et al.	
	31.	US-	6,333,624 B1	12/25/2001	Ball et al.	
	32.	US-	6,404,607 B1	06/11/2002	Burgess et al.	
	33.	US-	6,411,119 B1	06/25/2002	Feldtkeller	
	34.	US-	6,498,466 B1	12/24/2002	Edwards	
	35.	US-	6,525,514 B1	02/25/2003	Balakrishnan et al.	
	36.	US-	6,580,593 B2	06/17/2003	Balakrishnan et al.	
	37.	US-	6,583,994 B2	06/24/2003	Clayton et al.	
	38.	US-	6,665,197 B2	12/16/2003	Gong et al.	
	39.	US-	6,674,656 B1	01/06/2004	Yang et al.	
	40.	US-	6,747,443 B2	06/08/2004	Balakrishnan et al.	
	41.	US-	6,781,357 B2	08/24/2004	Balakrishnan et al.	
	42.	US-	6,833,692 B2	12/21/2004	Balakrishnan et al.	
	43.	US-	7,110,270 B2	09/19/2006	Balakrishnan et al.	
	44.		7,215,105 B2	05/08/2007	Balakrishnan et al.	
	45.	US-	2007/0182394 A1	08/09/2007	Balakrishnan et al.	
	46.	US-	90/009,393	Filed 01/20/2009	Power Integrations, Inc.	

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3] Number[4] Kind Code[5] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]
	47.	EP 0 744 818 A1	11/27/1996	Nokia Technology GmbH		
	48.	JP 09-074748	03/18/1997	Matsushita Electric Ind. Co. Ltd.		

Examiner Signature	/Rajnikant Patel/	Date Considered	09/07/10

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1]Applicant's unique citation designation number (optional). [2]See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. [3]Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). [4]For Japanese patent documents, the indication of the year of reign of the Emperor must precede the serial number of the patent document. [5]Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. [6]Applicant is to place a check mark here if English language translation is attached.

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ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /R.P./

Substitute for Form 1449/PTO				Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Application Number	~~New Patent Application~~ 12/581,054
(use as many sheets as necessary)				Filing Date	*Concurrently herewith*
				First Named Inventor:	Balakrishnan et al.
				Art Unit	~~*Not Yet Assigned*~~ 2838
				Examiner Name	*Not Yet Assigned*
Sheet	3	**of**	4	Attorney Docket Number	5510P064C4

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	T[2]
	49.	JP 2002-284064, Notice of the Reason for Refusal (with English Translation), mailed October 21, 2008.	
	50.	European Search Report, EP 02256760, February 2, 2005.	
	51.	Infineon Technologies Preliminary Datasheet, "ICE2AS01; Off-Line SMPS Current Mode Controller," Datasheet, Version 2.1, February 2001, Infineon Technologies AG, München, Germany.	
	52.	National Semiconductor: Linear and Switching Voltage Regulator Fundamentals, 'Online: XP002316042 Retrieved from the Internet: URL: No date http://web.archive.org/web/20010602192453/http://www.national.com/appinfo/powerfiles/f4.pdf>	
	53.	Linear Technology, LT1375/LT1376, "1.5A, 500kHz Step-Down Switching Regulators," 1995, pp. 1-28. No Date	
	54.	Infineon Technologies AG, Edition 2000-04-11, "Off-Line Current Mode Controller with CoolMOS™ on board," CoolSET™-F1 TDA 16822, Datasheet, V1.0, April 11, 2000, pp 1-15.	
	55.	Infineon Technologies, "Off-Line Current Mode Controller with CoolMOS™ on board," CoolSET™-F1 TDA 16822, Datasheet, V2.0, April 11, 2000, pp 1-14.	
	56.	TEA 1566 GreenChip™; SMPS Module, Preliminary Specifications, Integrated Circuits, Philips Semiconductors, April 20, 1999, pp.1-24.	
	57.	PAUL HOROWITZ & WINFIELD HILL, "The Art of Electronics", Second Edition, Published by Cambridge University Press, New York, 1989, Chapter 5, pp 263-305. No date	
	58.	Analog Devices, "Secondary Side, Off-Line Battery Charger Controllers," ADP3810/ADP3811," October 1996, pp. 1-16.	

Examiner Signature	/Rajnikant Patel/	Date Considered	09/07/10

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ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /R.P./

Substitute for Form 1449/PTO				Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(use as many sheets as necessary)*				Application Number	~~New Patent Application~~ 12/581,054
				Filing Date	*Concurrently herewith*
				First Named Inventor:	Balakrishnan et al.
				Art Unit	~~*Not Yet Assigned*~~ 2838
				Examiner Name	*Not Yet Assigned*
Sheet	4	**of**	4	Attorney Docket Number	5510P064C4

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	T[2]
	59.	Unitrode Integrated Circuits, Title Page, Introduction, and Table of Contents from "Product and Application Handbook 1993-94," (10 pages). No date available	
	60.	Unitrode Integrated Circuits, " Application Note U-100A: The UC3842/3/4/5 Series of Current-Mode PWM IC's," published in "Product and Application Handbook 1994-95," June 1993, at pp. 9-64 through 9-75; (12 pages).	
	61.	Office Action mailed September 24, 2009, Reexamination Control No. 90/009,393, filed January 20, 2009.	

Examiner Signature	/Rajnikant Patel/	Date Considered	09/07/10

*Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1]Applicant's unique citation designation number (optional). [2]Applicant is to place a check mark here if English translation is attached.

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If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /R.P./

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/581,054	10/16/2009	Balu Balakrishnan	5510P064C4	1732

8791 7590 09/09/2010

BLAKELY SOKOLOFF TAYLOR & ZAFMAN LLP
1279 OAKMEAD PARKWAY
SUNNYVALE, CA 94085-4040

EXAMINER	
PATEL, RAJNIKANT B	
ART UNIT	PAPER NUMBER
2838	

MAIL DATE	DELIVERY MODE
09/09/2010	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

UNITED STATES DEPARTMENT OF COMMERCE
U.S. Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450

APPLICATION NO./ CONTROL NO.	FILING DATE	FIRST NAMED INVENTOR / PATENT IN REEXAMINATION	ATTORNEY DOCKET NO.
12581054	10/16/2009	BALAKRISHNAN ET AL.	5510P064C4

BLAKELY SOKOLOFF TAYLOR & ZAFMAN LLP
1279 OAKMEAD PARKWAY
SUNNYVALE, CA 94085-4040

EXAMINER
RAJNIKANT B.. PATEL

ART UNIT	PAPER
2838	20100908

DATE MAILED:

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner for Patents

See attached corrected considered IDS dated 5 April 2010.

/RAJNIKANT B. PATEL/
Primary Examiner, Art Unit 2838

PTO-90C (Rev.04-03)

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

8791 7590 07/13/2010

BLAKELY SOKOLOFF TAYLOR & ZAFMAN LLP
1279 OAKMEAD PARKWAY
SUNNYVALE, CA 94085-4040

EXAMINER	
PATEL, RAJNIKANT B	
ART UNIT	PAPER NUMBER
2838	

DATE MAILED: 07/13/2010

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/581,054	10/16/2009	Balu Balakrishnan	5510P064C4	1732

TITLE OF INVENTION: METHOD AND APPARATUS FOR MAINTAINING A CONSTANT LOAD CURRENT WITH LINE VOLTAGE IN A SWITCH MODE POWER SUPPLY

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1510	$300	$0	$1810	10/13/2010

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PTOL-85 (Rev. 08/07) Approved for use through 08/31/2010.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

8791 7590 07/13/2010

BLAKELY SOKOLOFF TAYLOR & ZAFMAN LLP
1279 OAKMEAD PARKWAY
SUNNYVALE, CA 94085-4040

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/581,054	10/16/2009	Balu Balakrishnan	5510P064C4	1732

TITLE OF INVENTION: METHOD AND APPARATUS FOR MAINTAINING A CONSTANT LOAD CURRENT WITH LINE VOLTAGE IN A SWITCH MODE POWER SUPPLY

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1510	$300	$0	$1810	10/13/2010

EXAMINER	ART UNIT	CLASS-SUBCLASS
PATEL, RAJNIKANT B	2838	323-282000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.
1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. The following fee(s) are submitted:
❑ Issue Fee
❑ Publication Fee (No small entity discount permitted)
❑ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**
❑ A check is enclosed.
❑ Payment by credit card. Form PTO-2038 is attached.
❑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)
❑ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27. ❑ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

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UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/581,054	10/16/2009	Balu Balakrishnan	5510P064C4	1732

8791 7590 07/13/2010

BLAKELY SOKOLOFF TAYLOR & ZAFMAN LLP
1279 OAKMEAD PARKWAY
SUNNYVALE, CA 94085-4040

EXAMINER	
PATEL, RAJNIKANT B	
ART UNIT	PAPER NUMBER
2838	

DATE MAILED: 07/13/2010

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 0 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 0 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

PTOL-85 (Rev. 08/07) Approved for use through 08/31/2010.

Notice of Allowability	Application No.	Applicant(s)	
	12/581,054	BALAKRISHNAN ET AL.	
	Examiner	Art Unit	
	RAJNIKANT B. PATEL	2838	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *12 June 2010*.

2. ☒ The allowed claim(s) is/are *1-12*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☐ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

/RAJNIKANT B. PATEL/
Primary Examiner, Art Unit 2838

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	12581054	BALAKRISHNAN ET AL.
	Examiner	**Art Unit**
	RAJNIKANT B PATEL	2838

ORIGINAL		INTERNATIONAL CLASSIFICATION	
CLASS	SUBCLASS	CLAIMED	NON-CLAIMED
323	282	G 0 5 F 1 / 40 (2006.01.01)	

CROSS REFERENCE(S)

CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)				
323	273				

☒ Claims renumbered in the same order as presented by applicant ☐ CPA ☒ T.D. ☐ R.1.47

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original

NONE ----------		**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	12	
/RAJNIKANT B PATEL/ Primary Examiner.Art Unit 2838	07/07/10	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	1

U.S. Patent and Trademark Office — Part of Paper No. 20100707

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	12581054	BALAKRISHNAN ET AL.
	Examiner	Art Unit
	RAJNIKANT B PATEL	2838

SEARCHED			
Class	Subclass	Date	Examiner
323	282-288,235-239,220-223,272-275	03/30/10	/RP/
363	79,80,97,131,63,89		
	UPDATED SEARCH	07/07/10	/RP/

SEARCH NOTES		
Search Notes	Date	Examiner
EAST	03/30/10	/RP/

INTERFERENCE SEARCH			
Class	Subclass	Date	Examiner
323	282,273	07/07/10	/RP/

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L4	366	oscillator near3 (((saw adj tooth) or sawtooth) near waveform)	US-PGPUB; USPAT; USOCR	OR	OFF	2010/04/01 08:41
L5	877	latch near3 oscillator	US-PGPUB; USPAT; USOCR	OR	OFF	2010/04/01 08:42
L6	4	((variable or varying or changing) and waveform) near3 (generate or generating or generation) near3 ((variable or varying or adjusting) adj (current adj limit $3))	US-PGPUB; USPAT; USOCR	OR	OFF	2010/04/01 08:45
L7	4	((variable or varying or changing) and waveform) near5 (generate or generating or generation) near5 ((variable or varying or adjusting) adj (current adj limit $3))	US-PGPUB; USPAT; USOCR	OR	OFF	2010/04/01 08:45

L8	195430	((variable or varying or changing) and waveform) and5 (generate or generating or generation) near5 ((variable or varying or adjusting) adj (current adj limit $3))	US-PGPUB; USPAT; USOCR	OR	OFF	2010/04/01 08:45
L9	6	((variable or varying or changing) and waveform) and (generate or generating or generation) near5 ((variable or varying or adjusting) adj (current adj limit $3))	US-PGPUB; USPAT; USOCR	OR	OFF	2010/04/01 08:46
L10	11	4 and 5	US-PGPUB; USPAT; USOCR	OR	OFF	2010/04/01 08:48

EAST Search History (Interference)

<This search history is empty>

4/1/2010 10:28:51 AM
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EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S640	26	comparator and ((variable or adjust$3 or changeble) and ((current adj limit) and threshold)) and (((on adj time) or on-time) near switch)	USPAT	OR	OFF	2010/03/30 15:45
S641	10	("4084103").URPN.	USPAT	OR	OFF	2010/03/30 16:06
S642	20	S640 and feedback	USPAT	OR	OFF	2010/03/30 16:09
S643	4	("4392103" | "4459539" | "4553082" | "4555655"). PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2010/03/30 18:05
S644	3	(("5041777") or ("4346342") or ("4032828")).PN.	USPAT; USOCR	OR	OFF	2010/03/30 18:10
S645	0	((variable near (current adj limit)) near comparator)	USPAT	OR	OFF	2010/03/31 08:45
S646	2	((variable near5 (current adj (limit or limiting or limiter))) near comparator)	USPAT	OR	OFF	2010/03/31 08:46
S647	11	((variable near5 (current adj (limit or limiting or limiter))) near5 comparator)	USPAT	OR	OFF	2010/03/31 08:46
S648	7	("5229707").URPN.	USPAT	OR	OFF	2010/03/31 08:51
S649	6	("4674020" | "4750079" | "4837495" | "4937697" | "5028861" | "5138516"). PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2010/03/31 08:54
S650	6	("4674020" | "4750079" | "4837495" | "4937697" | "5028861" | "5138516"). PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2010/03/31 09:01
S651	5	("4021701" | "4322770" | "4441136" | "4575673" | "4979066").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2010/03/31 09:01

S652	23	("2977524" | "3012181" | "3127551" | "3213344" | "3316445" | "3863128" | "3931566" | "4068151" | "4071884" | "4355277" | "4392103" | "4610521" | "4634956" | "4678983" | "4695785" | "4712169" | "4717867" | "4837495").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2010/03/31 10:57
S653	6	S652 and (current and limit)	US-PGPUB; USPAT; USOCR	OR	OFF	2010/03/31 10:59
S654	4	S652 and ((varying or variable or adjustable or adjusting) and (current and limit))	US-PGPUB; USPAT; USOCR	OR	OFF	2010/03/31 11:00
S655	3	S652 and ((varying or variable or adjustable or adjusting) and (current and limit)) and feedback	US-PGPUB; USPAT; USOCR	OR	OFF	2010/03/31 11:01
S656	0	S652 and ((varying or variable or adjustable or adjusting) and (current and limit)) and feedback and (sawtooth or (saw adj tooth))	US-PGPUB; USPAT; USOCR	OR	OFF	2010/03/31 11:01
S657	2	S652 and ((varying or variable or adjustable or adjusting) and (current and limit)) and feedback and wave	US-PGPUB; USPAT; USOCR	OR	OFF	2010/03/31 11:02
S658	1	("5859768").PN.	USPAT; USOCR	OR	OFF	2010/03/31 11:35
S659	205	((BALU) near2 (BALAKRISHNAN)).INV.	US-PGPUB; USPAT; USOCR	OR	OFF	2010/03/31 16:05
S660	2	S659 and ((current adj mirror) same (coupled or connected) same (oscillator))	USPAT	OR	OFF	2010/03/31 16:08
S661	144	((ALEX) near2 (DJENGUERIAN)).INV.	US-PGPUB; USPAT; USOCR	OR	OFF	2010/03/31 16:10
S662	92	((KENT) near2 (WONG)).INV.	US-PGPUB; USPAT; USOCR	OR	OFF	2010/03/31 16:11

S663	2	S660 and ((current adj mirror) same (coupled or connected) same (oscillator))	USPAT	OR	OFF	2010/03/31 16:12
S664	1	S662 and ((current adj mirror) same (coupled or connected) same (oscillator))	USPAT	OR	OFF	2010/03/31 16:12
S665	141	S659 or S661 or S662	USPAT	OR	OFF	2010/03/31 16:15
S666	1	S659 and (comparator and on-time and ((current adj limit) adj threshold))	USPAT	OR	OFF	2010/03/31 16:16
S667	1	S659 and (comparator and on-time and ((current adj limit) adj threshold)) and feedback	USPAT	OR	OFF	2010/03/31 16:17
S668	0	S659 and (comparator and on-time and ((current adj limit) adj threshold)) and feedback and (cuurent and (limit or limiting or limitation))	USPAT	OR	OFF	2010/03/31 16:19
S669	0	S661 and (comparator and on-time and ((current adj limit) adj threshold)) and feedback and (cuurent and (limit or limiting or limitation))	USPAT	OR	OFF	2010/03/31 16:19
S670	0	S662 and (comparator and on-time and ((current adj limit) adj threshold)) and feedback and (cuurent and (limit or limiting or limitation))	USPAT	OR	OFF	2010/03/31 16:19
S671	0	(comparator and on-time and ((current adj limit) adj threshold)) and feedback and (cuurent and (limit or limiting or limitation))	USPAT	OR	OFF	2010/03/31 16:20
S672	0	((comparator and on-time) and ((current adj limit) adj threshold)) and feedback and (cuurent and (limit or limiting or limitation))	USPAT	OR	OFF	2010/03/31 16:20
S673	0	((current adj limit) adj threshold) and feedback and (cuurent and (limit or limiting or limitation))	USPAT	OR	OFF	2010/03/31 16:21

S674	0	((current adj limit) and threshold) and feedback and (cuurent and (limit or limiting or limitation))	USPAT	OR	OFF	2010/03/31 16:22
S675	0	(comparator and on-time) and feedback and (cuurent and (limit or limiting or limitation))	USPAT	OR	OFF	2010/03/31 16:22
S676	2	S662 and (comparator and on-time and ((current adj limit) adj threshold)) and feedback and (current and (limit or limiting or limitation))	USPAT	OR	OFF	2010/03/31 16:23
S677	1	S659 and (comparator and on-time and ((current adj limit) adj threshold)) and feedback and (current and (limit or limiting or limitation))	USPAT	OR	OFF	2010/03/31 16:23
S678	2	S661 and (comparator and on-time and ((current adj limit) adj threshold)) and feedback and (current and (limit or limiting or limitation))	USPAT	OR	OFF	2010/03/31 16:24
S679	7	(comparator and on-time and ((current adj limit) adj threshold)) and feedback and (current and (limit or limiting or limitation))	USPAT	OR	OFF	2010/03/31 16:24
S680	2	(comparator and on-time and ((current adj limit) adj threshold)) and feedback and (current and (limit or limiting or limitation)) and mirror	USPAT	OR	OFF	2010/03/31 16:24
S681	2	("4451876" | "4931920").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2010/03/31 18:24
S682	15	("5973945").URPN.	USPAT	OR	OFF	2010/03/31 18:26
S683	5	("5014178" | "5313381" | "5973945" | "6147883" | "6169444").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2010/03/31 18:27

EAST Search History (Interference)

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Application Number	Application/Control No.	Applicant(s)/Patent under Reexamination	
	12/581,054	BALAKRISHNAN ET AL.	

Document Code - DISQ	Internal Document – DO NOT MAIL

TERMINAL DISCLAIMER	☒ APPROVED	☐ DISAPPROVED
Date Filed : 5/28/10	This patent is subject to a Terminal Disclaimer	

Approved/Disapproved by:
j.proctor

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	)	
	)	
Balu Balakrishnan et al.	)	Examiner: Rajnikant B. Patel
	)	
Application No.: 12/581,054	)	Art Unit: 2838
	)	
Filing Date: October 16, 2009	)	Confirmation No.: 1732
	)	
For: METHOD AND APPARATUS FOR MAINTAINING A CONSTANT LOAD CURRENT WITH LINE VOLTAGE IN A SWITCH MODE POWER SUPPLY	)	

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

RESPONSE TO OFFICE ACTION

Dear Sir:

In response to the Office Action mailed April 5, 2010, the Applicant requests the Examiner to consider the following remarks. No amendments have been made.

Pending Claims are reflected in the listing of claims, which begins on page 2 of this paper.

Remarks/Arguments begin on page 5 of this paper.

Pending Claims:

The claims have not been amended. The listing of claims is provided herewith for convenience and ease of prosecution.

Listing of Claims:

1. (Original) A power supply regulator, comprising:

a comparator having a first input coupled to sense a voltage representative of a current flowing through a switch during an on time of the switch, the comparator having a second input coupled to receive a variable current limit threshold that increases during the on time of the switch;

a feedback circuit coupled to receive a feedback signal representative of an output voltage at an output of a power supply; and

a control circuit coupled to generate a control signal in response to an output of the comparator and in response to an output of the feedback circuit, the control signal to be coupled to a control terminal of the switch to control switching of the switch.

2. (Original) The power supply regulator of claim 1 further comprising an oscillator having a first output to generate a sawtooth waveform, wherein the variable current limit threshold is generated in response to the sawtooth waveform.

3. (Original) The power supply regulator of claim 2 wherein the feedback circuit is coupled to receive the sawtooth waveform.

4. (Original) The power supply regulator of claim 2 wherein the oscillator further has a second output to generate a maximum duty cycle signal, wherein the control circuit is coupled to generate the control signal further in response to the maximum duty cycle signal.

5. (Original) The power supply regulator of claim 2 wherein the control circuit includes a latch to provide the control signal, wherein the latch includes a reset input coupled to the output of the comparator.

6. (Original) The power supply regulator of claim 5 wherein the latch further includes a set input coupled to be responsive to a clock signal generated from a third output of the oscillator.

7. (Original) The power supply regulator of claim 5 wherein the reset input of the latch is further coupled to be responsive to a maximum duty cycle signal from a second output of the oscillator.

8. (Original) The power supply regulator of claim 5 wherein the feedback circuit comprises a feedback comparator coupled to receive the feedback signal and the sawtooth waveform, wherein the reset input of the latch is coupled to be responsive to an output of the feedback comparator.

9. (Original) The power supply regulator of claim 1 wherein a duty cycle of the control signal is modulated in response to an output of the feedback circuit.

10. (Original) The power supply of regulator of claim 2 further comprising a current mirror coupled to the oscillator to receive the sawtooth waveform, wherein the variable current limit threshold is generated in response to the current mirror.

11. (Original) The power supply regulator of claim 1 wherein the switching of the switch provides at the output of the power supply an output characteristic having an approximately constant output current below an output voltage threshold.

12. (Original) The power supply regulator of claim 11 wherein the approximately constant output current remains substantially constant at all line voltages.

REMARKS/ARGUMENTS

Claims pending in the instant application are numbered 1-12. Claims 1-12 presently stand rejected. The Applicant respectfully requests that the instant application be reconsidered in view of the following remarks.

35 U.S.C. § 102 Rejections

In the April 5, 2010, Office Action, claims 1-4, 6-7, 9 and 11 are rejected under 35 U.S.C. § 102(b) as being anticipated by Pace et al., US Patent No. 5,028,861 (hereinafter Pace).

With regard to a rejection under 35 U.S.C. § 102, MPEP § 2131 sets forth that

> "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).

Independent claim 1 of the instant application expressly recites, among other things, a comparator having "...a second input coupled to receive ***a variable current limit threshold*** that increases during the on time of the switch . . . ." Therefore, independent claim 1 expressly recites that an input of the comparator is coupled to receive a variable current limit threshold.

The April 5, 2010 Office Action asserts at page 3, that Pace allegedly discloses ". . . a comparator (figure 2, item 56) . . . " and ". . . a variable current limit (column 4, line 15-50) . . . ." The Applicant disagrees and respectfully submits that Pace fails to disclose a variable current limit threshold, much less a comparator having an input coupled to receive a variable current limit threshold, as expressly claimed by Applicant. Indeed, a fair reading of Pace simply reveals that comparator 56, such as shown in figure 2, includes one input coupled to receive a ***regulated*** 1.55V signal and the other input is coupled to receive a voltage derived from the "***B++ voltage***" (***i.e., the output of the DC-DC converter***). (Pace, col. 4, lines 5-12). Pace fails to disclose that

either of the inputs to comparator 56 are a variable current limit threshold, as is more fully explained below.

First, the 1.55V signal coupled to one input of comparator 56 of Pace is *not* a variable current limit threshold. To be sure, attention is kindly directed to Pace, col. 4, lines 5-12, which explicitly states ". . . voltage reference 54 . . . produces a regulated 1.55V," and "[o]ne input to the comparator is coupled to the 1.55V signal . . . ." ***Since Pace states that the 1.55V signal is regulated, the reference necessarily fails to disclose that the 1.55V signal is a variable current limit threshold, as claimed by Applicant.***

Second, not only is the 1.55V signal *not* a variable current limit threshold, but the voltage coupled to the other input of comparator 56 of Pace is also, *not* a variable current limit threshold. Instead, Pace states that the other input of comparator 56 is ". . . coupled to a voltage derived from the B++ voltage." (Pace, col. 4, lines 10-11). Pace further states, at col. 4, lines 12-17 that ". . . [t]he comparator, voltage reference, and voltage divider operate such that the output of the comparator generates an ON signal in response to B++ being less than 3.04V and generates an OFF signal in response to B++ being greater than 3.16V." That is, the voltage at the other input of comparator 56 is a voltage derived from the B++ ***voltage*** (i.e., the output of the DC-DC converter). ***Since Pace states that the voltage at the other input of comparator 56 is derived from the B++ voltage (i.e., the output of the DC-DC converter), the reference necessarily fails to disclose that the voltage at the other input of comparator 56 is a variable current limit threshold, as claimed by Applicant.***

Moreover, neither of the inputs to comparator 56 are variable current limit thresholds because comparator 56 is not used to *limit current*. Instead, comparator 56 is coupled to enable and disable the energy conversion process to ***regulate*** **the B++** ***voltage***. (Pace, col. 3, lines 64-68). Thus, contrary to the suggestion in the Office Action, comparator 56 of Pace regulates the

B++ *voltage* and does not limit *current*.

Furthermore, Pace expressly discloses a different element (see Figure 2, peak inductor current control 80) that is coupled to sense current in a switch. This element, however, includes a **fixed** threshold. To be sure, attention is kindly directed to col. 4, lines 55-57, which states ". . . the voltage developed across resistor 79 is a function of the current through the conversion devices [i.e., inductor 20, transistor 50, and diode 52 (Pace, col. 4, lines 35-36)]." Pace further states at col. 5, lines 1-9, that "[t]he voltage across resistor 79 is monitored by the peak current control 80," and "[w]hen the voltage reaches a predetermined level, 18mV in the preferred embodiment, the peak current control generates a peak signal . . . ." Since Pace teaches using a fixed threshold (e.g., predetermined level of 18mV in the preferred embodiment) in peak inductor current control 80, the Pace reference actually teaches away from a *variable current limit threshold*, as expressly claimed by Applicant.

Thus, Pace fails to disclose, teach or even fairly suggest at least the above-discussed elements. Consequently, Pace fails to disclose each and every element of claim 1, as required under M.P.E.P. § 2131. Accordingly, the Applicant requests that the instant §102 rejection of claim 1 be withdrawn.

Dependent claims 2-4, 6, 7, 9, and 11 depend either directly or indirectly from independent claim 1. Thus, claims 2-4, 6, 7, 9, and 11 are novel for at least the same reasons as independent claim 1 in addition to adding further limitations of their own. For example, dependent claim 2 expressly recites, in part, ". . . an oscillator having a first output to generate a sawtooth waveform . . . ." Nowhere in this reference, does Pace disclose an oscillator having a first output to generate a sawtooth waveform, as claimed by Applicants. To be sure, attention is kindly directed to FIG. 2 of Pace, which clearly illustrates element 68 as an 83kHz Oscillator which provides a clocking frequency. (Pace, col. 4, lines 25-27). However, nowhere does Pace

disclose that the 83kHz Oscillator has an output to generate a sawtooth waveform, as claimed by Applicants. Therefore, dependent claim 2 and all of its dependent claims are further distinguishable from Pace for at least these additional reasons.

By way of another example, dependent claim 11 expressly recites, in part, ". . . wherein the switching of the switch provides at the output of the power supply an *output characteristic* having an approximately *constant output current below an output voltage threshold . . . .*" Applicants respectfully assert that Pace fails to disclose a power supply regulator to control switching of a switch to provide an output characteristic where the output characteristic includes an approximately constant output current below an output voltage threshold for at least the following reasons.

Pace fails to disclose providing a constant output ***current***. Instead, Pace teaches regulating an output (i.e., B++) ***voltage***. (Pace, col. 3, lines 64-68). Pace fails to disclose switching of the switch to provide an output characteristic having an approximately constant output ***current*** below an output voltage threshold. Nowhere in this reference does Pace disclose providing a constant ***output*** current. While Pace does teach regulating a current through the energy conversion devices (i.e., inductor 20, transistor 50, and diode 52) (Pace, col. 4, lines 34-48), nowhere does this reference disclose providing a constant ***output*** current, as claimed by Applicants.

Accordingly, the Applicant respectfully requests that the instant §102 rejections of dependent claims 2-4, 6, 7, 9, and 11 also be withdrawn.

35 U.S.C. § 103 Rejections

In the April 5, 2010, Office Action, claims 5, 8, 10, and 12 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Pace in combination with Redl, US Patent No. 5,680,034

(hereinafter Redl).

When combining prior art elements to establish a prima facie case of obviousness, the M.P.E.P. requires a factual finding "*...that the prior art include* ***each*** *element claimed....*" M.P.E.P. § 2143 (A)(1). "All words in a claim must be considered in judging the patentability of that claim against the prior art." M.P.E.P. § 2143.03.

As discussed above, Pace fails to disclose, teach or suggest at least a variable current limit threshold. Redl also fails to disclose, teach or suggest at least a variable current limit threshold and thus fails to cure at least the above-noted deficiencies of Pace. For example, Redl does teach a comparator (see Fig 15, reference 610) that is coupled to sense current in a switch. This comparator, however, includes a fixed threshold and, accordingly, Redl actually expressly teaches away from a variable current limit threshold. (See Redl at 8:58-9:13.)

Dependent claims 5, 8, and 10 depend either directly or indirectly from independent claim 1 and dependent claim 2. Thus, claims 5, 8, and 10 are nonobvious for at least the same reasons as discussed above with respect to independent claim 1 and dependent claim 2 in addition to adding further limitations of their own. For example, dependent claim 10 expressly recites ". . . a current mirror coupled to the oscillator to receive the sawtooth waveform . . . ." As discussed above, Pace fails to disclose, teach or suggest an oscillator having a first output to generate a sawtooth waveform. Thus, Pace necessarily fails to disclose, teach or suggest a current mirror that is coupled to the oscillator to receive the sawtooth waveform. Redl also fails to disclose, teach or suggest a current mirror that is coupled to an oscillator to receive a sawtooth waveform as claimed by Applicants and thus further fails to cure this deficiency of Pace.

Dependent claim 12 depends from independent claim 1 and dependent claim 11. Thus, claim 12 is nonobvious for at least the same reasons as discussed above with respect to independent claim 1 and dependent claim 11 in addition to adding further limitations of its own.

By way of example, dependent claim 12 expressly recites ". . . wherein the approximately constant output current remains substantially constant at all line voltages." As discussed above with respect to dependent claim 11, Pace fails to disclose, teach or suggest a power supply regulator wherein the switching of the switch provides at the output of the power supply an output characteristic having an *approximately constant* ***output current*** below an output voltage threshold, as recited in Applicants' claim 11. Since Pace fails to disclose, teach or suggest an output characteristic including an approximately constant output current, as claimed, the reference necessarily fails to disclose, teach or suggest that the claimed approximately constant output current remains substantially constant at all line voltages, as further recited in dependent claim 12. Redl also fails to disclose, teach or suggest an approximately constant output current that remains substantially constant at all line voltages, as claimed by Applicants, and thus further fails to cure this deficiency of Pace.

Accordingly, the cited references fail to disclose each element of claims 5, 8, 10, and 12 as required under M.P.E.P. §2143. The Applicant respectfully request that the §103(a) rejections of claims 5, 8, 10, and 12 be withdrawn.

Double Patenting

Claims 1-12 stand rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims of U.S. 7,646,184.

The Applicant respectfully requests that the enclosed timely filed terminal disclaimer in compliance with 37 CFR § 1.321(c) be entered to overcome the instant nonstatutory double patenting rejection, as suggested in the April 5, 2010 Office Action.

The Applicants wish to note that the filing of the enclosed terminal disclaimer in compliance with 37 CFR § 1.321(c) is not an admission to the propriety of the rejection.

M.P.E.P. § 804.02; Quad Environmental Technologies Corp. v. Union Sanitary District, 20 USPQ.2d. 1392 (Fed. Cir. 1991). As stated by the Federal Circuit in the Quad Environmental Technologies decision, the "filing of a terminal disclaimer simply serves the statutory function of removing the rejection of double patenting, and raises neither a presumption nor estoppel on the merits of the rejection."

Charge Deposit Account

If there is a deficiency in fees, please charge our Deposit Acct. No. 02-2666.

The Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Respectfully submitted,

BLAKELY SOKOLOFF TAYLOR & ZAFMAN LLP

Date: May 28, 2010

/James Y. Go/
James Y. Go
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CERTIFICATE OF MAILING/TRANSMISSION
I hereby certify that this correspondence is being submitted electronically via EFS Web on the date shown below.

/Kristy A. Marvel/ May 28, 2010
Kristy A. Marvel ***Date***

PTO/SB/26 (07-09)
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TERMINAL DISCLAIMER TO OBVIATE A DOUBLE PATENTING REJECTION OVER A "PRIOR" PATENT	Docket Number (Optional) 5510P064C4

In re Application of: Balu Balakrishnan et al.

Application No.: 12/581,054

Filed: October 16, 2009

For: METHOD AND APPARATUS FOR MAINTAINING A CONSTANT LOAD CURRENT WITH LINE VOLTAGE IN A SWITCH MODE POWER SUPPLY

The owner*, Power Integrations, Inc., of 100 percent interest in the instant application hereby disclaims, except as provided below, the terminal part of the statutory term of any patent granted on the instant application which would extend beyond the expiration date of the full statutory term **prior patent** No. 7,646,184 as the term of said prior patent is defined in 35 U.S.C. 154 and 173, and as the term of said **prior patent** is presently shortened by any terminal disclaimer. The owner hereby agrees that any patent so granted on the instant application shall be enforceable only for and during such period that it and the **prior patent** are commonly owned. This agreement runs with any patent granted on the instant application and is binding upon the grantee, its successors or assigns.

In making the above disclaimer, the owner does not disclaim the terminal part of the term of any patent granted on the instant application that would extend to the expiration date of the full statutory term as defined in 35 U.S.C. 154 and 173 of the **prior patent**, "as the term of said **prior patent** is presently shortened by any terminal disclaimer," in the event that said **prior patent** later:

expires for failure to pay a maintenance fee;
is held unenforceable;
is found invalid by a court of competent jurisdiction;
is statutorily disclaimed in whole or terminally disclaimed under 37 CFR 1.321;
has all claims canceled by a reexamination certificate;
is reissued; or
is in any manner terminated prior to the expiration of its full statutory term as presently shortened by any terminal disclaimer.

Check either box 1 or 2 below, if appropriate.

1. ☐ For submissions on behalf of a business/organization (e.g., corporation, partnership, university, government agency, etc.), the undersigned is empowered to act on behalf of the business/organization.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

2. ☑ The undersigned is an attorney or agent of record. Reg. No. 40,621

/James Y. Go/ — Signature
May 28, 2010 — Date

James Y. Go — Typed or printed name

(206) 292-8600 — Telephone Number

☑ Terminal disclaimer fee under 37 CFR 1.20(d) included.

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

*Statement under 37 CFR 3.73(b) is required if terminal disclaimer is signed by the assignee (owner).
Form PTO/SB/96 may be used for making this certification. See MPEP § 324.

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Patent Application Fee Transmittal	
Application Number:	12581054
Filing Date:	16-Oct-2009
Title of Invention:	METHOD AND APPARATUS FOR MAINTAINING A CONSTANT LOAD CURRENT WITH LINE VOLTAGE IN A SWITCH MODE POWER SUPPLY
First Named Inventor/Applicant Name:	Balu Balakrishnan
Filer:	James Go/Kristy Marvel
Attorney Docket Number:	5510P064C4
Filed as Large Entity	

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
Statutory disclaimer	1814	1	140	140
		Total in USD ($)		**140**

Electronic Acknowledgement Receipt	
EFS ID:	7709377
Application Number:	12581054
International Application Number:	
Confirmation Number:	1732
Title of Invention:	METHOD AND APPARATUS FOR MAINTAINING A CONSTANT LOAD CURRENT WITH LINE VOLTAGE IN A SWITCH MODE POWER SUPPLY
First Named Inventor/Applicant Name:	Balu Balakrishnan
Customer Number:	08791
Filer:	James Go/Kristy Marvel
Filer Authorized By:	James Go
Attorney Docket Number:	5510P064C4
Receipt Date:	28-MAY-2010
Filing Date:	16-OCT-2009
Time Stamp:	14:36:04
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	$140
RAM confirmation Number	786
Deposit Account	022666
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees) Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)	

Charge any Additional Fees required under 37 C.F.R. Section 1.19 (Document supply fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.20 (Post Issuance fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Amendment/Req. Reconsideration-After Non-Final Reject	5510P064C4_Response_052810.pdf	63809 90f8a029ad094828c5b94ae715596c025d5220e6	no	11
Warnings:					
Information:					
2	Terminal Disclaimer Filed	5510P064C4_TerminalDisclaimer_052810.pdf	55855 e5b094aeee11e516e38238e085fb71c1fbbc79db	no	2
Warnings:					
Information:					
3	Fee Worksheet (PTO-875)	fee-info.pdf	30438 e7397b1b7beca334f8a2512d23ea00f7c2e750d3	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	150102		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/06 (07-06)
Approved for use through 1/31/2007. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number	Filing Date	☐ To be Mailed
12/581,054	10/16/2009	

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY ☐ RATE ($)	SMALL ENTITY ☐ FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =		OR	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =			X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY ADDITIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE ($)
	05/28/2010									
	Total (37 CFR 1.16(i))	* 12	Minus	** 20	= 0	X $ =		OR	X $52=	0
	Independent (37 CFR 1.16(h))	* 1	Minus	***3	= 0	X $ =		OR	X $220=	0
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	0

AMENDMENT		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =		OR	X $ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =		OR	X $ =	
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

Legal Instrument Examiner:
/PATIENCE RESPER/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

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UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
12/581,054	10/16/2009	2838	1090	5510P064C4	12	1

CONFIRMATION NO. 1732

CORRECTED FILING RECEIPT

8791
BLAKELY SOKOLOFF TAYLOR & ZAFMAN LLP
1279 OAKMEAD PARKWAY
SUNNYVALE, CA 94085-4040

OC000000041140884

Date Mailed: 04/20/2010

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Applicant(s)

Balu Balakrishnan, Saratoga, CA;
Alex B. Djenguerian, Saratoga, CA;
Kent Wong, Fremont, CA;
David Michael Hugh Matthews, Windsor, UNITED KINGDOM;

Assignment For Published Patent Application

Power Integrations, Inc., San Jose, CA

Power of Attorney:

Edwin Taylor--25129
Eric Hyman--30139
Michael Bernadicou--35934
Michael Mallie--36591
William Schaal--39018
Gregory Caldwell--39926
James Go--40621
Jan Little-Washington--41181
Todd Becker--43487
Mark Watson--46322

Domestic Priority data as claimed by applicant

This application is a CON of 11/784,560 04/06/2007 PAT 7,646,184
which is a CON of 11/397,524 04/03/2006 PAT 7,215,105
which is a CON of 10/892,300 07/15/2004 PAT 7,110,270
which is a CON of 10/253,307 09/23/2002 PAT 6,781,357
which claims benefit of 60/325,642 09/27/2001

Foreign Applications

If Required, Foreign Filing License Granted: 10/29/2009

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 12/581,054**

Projected Publication Date: Not Applicable

Non-Publication Request: No

Early Publication Request: No

Title

METHOD AND APPARATUS FOR MAINTAINING A CONSTANT LOAD CURRENT WITH LINE VOLTAGE IN A SWITCH MODE POWER SUPPLY

Preliminary Class

323

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4158).

LICENSE FOR FOREIGN FILING UNDER

Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

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This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign AssetsControl, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

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CERTIFICATE OF EFS-WEB TRANSMISSION		
I hereby certify that this correspondence is being submitted electronically via EFS Web on the date shown below.		
Kristy A. Marvel	/Kristy A. Marvel/	April 8, 2010
(Name)	(Signature)	(Date)

Attorney Docket No. 5510P064C4 *Patent*

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	)	
	)	
Balu Balakrishnan et al.	)	Examiner: *Not yet assigned*
	)	
Application No. 12/581,054	)	Art Unit: 2816
	)	
Filed: October 16, 2009	)	Confirmation No.: 1732
	)	
For: METHOD AND APPARATUS FOR MAINTAINING A CONSTANT LOAD CURRENT WITH LINE VOLTAGE IN A SWITCH MODE POWER SUPPLY	)	

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

REQUEST TO CORRECT AN ERROR IN THE FILING RECEIPT

Dear Sir:

Applicants respectfully note the misspelling of an Applicant's name on the Filing Receipt for the above-identified application. The Filing Receipt lists the Applicant as, "**Alx** B. Djenguerian, Saratoga, CA" (emphasis added.) The Applicant should be listed as, "**Alex** B. Djenguerian, Saratoga, CA" (emphasis added). The enclosed copy of the Filing Receipt has been redlined to indicate the correct spelling of the Applicant's name for the above-identified application.

Therefore, Applicants respectfully request that a new filing receipt with the corrected spelling of the Applicant's name be issued for the present application.

Respectfully submitted,
BLAKELY SOKOLOFF TAYLOR & ZAFMAN LLP

Dated: April 8, 2010 /James Y. Go/
James Y. Go
Reg. No. 40,621

1279 Oakmead Parkway
Sunnyvale, California 94085-4040
206-292-8600

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
12/581,054	10/16/2009	2816	1090	5510P064C4	12	1

CONFIRMATION NO. 1732

8791
BLAKELY SOKOLOFF TAYLOR & ZAFMAN LLP
1279 OAKMEAD PARKWAY
SUNNYVALE, CA 94085-4040

FILING RECEIPT

OC000000038536261

Date Mailed: 11/03/2009

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Applicant(s)

Alex
Balu Balakrishnan, Saratoga, CA;
Alx B. Djenguerian, Saratoga, CA;
Kent Wong, Fremont, CA;
David Michael Hugh Matthews, Windsor, UNITED KINGDOM;

Assignment For Published Patent Application

Power Integrations, Inc., San Jose, CA

Power of Attorney:

Edwin Taylor--25129	Gregory Caldwell--39926
Eric Hyman--30139	James Go--40621
Michael Bernadicou--35934	Jan Little-Washington--41181
Michael Mallie--36591	Todd Becker--43487
William Schaal--39018	Mark Watson--46322

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Projected Publication Date: 02/11/2010

Non-Publication Request: No

Early Publication Request: No
Title

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Preliminary Class

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Title 37, Code of Federal Regulations, 5.11 & 5.15

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The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where the conditions for issuance of a license have been met, regardless of whether or not a license may be required as set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign AssetsControl, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

Electronic Acknowledgement Receipt	
EFS ID:	7379656
Application Number:	12581054
International Application Number:	
Confirmation Number:	1732
Title of Invention:	METHOD AND APPARATUS FOR MAINTAINING A CONSTANT LOAD CURRENT WITH LINE VOLTAGE IN A SWITCH MODE POWER SUPPLY
First Named Inventor/Applicant Name:	Balu Balakrishnan
Customer Number:	08791
Filer:	James Go/Kristy Marvel
Filer Authorized By:	James Go
Attorney Docket Number:	5510P064C4
Receipt Date:	08-APR-2010
Filing Date:	16-OCT-2009
Time Stamp:	19:10:41
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Request for Corrected Filing Receipt	5510P064C4_RequestCorrectErrorFilingRecpt_040810.pdf	24742 5c9040ce8d62363e1bb06377eafbc56f2c40bacb	no	1
Warnings:					
Information:					

2	Miscellaneous Incoming Letter	5510P064C4_RedlinedFilingReceipt_040810.PDF	257331 1ec6df7f269bc82b9b1425b969be50a03c11056c	no	3
Warnings:					
Information:					
			Total Files Size (in bytes):	282073	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

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www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/581,054	10/16/2009	Balu Balakrishnan	5510P064C4	1732

8791 7590 04/05/2010

BLAKELY SOKOLOFF TAYLOR & ZAFMAN LLP
1279 OAKMEAD PARKWAY
SUNNYVALE, CA 94085-4040

EXAMINER	
PATEL, RAJNIKANT B	
ART UNIT	PAPER NUMBER
2838	

MAIL DATE	DELIVERY MODE
04/05/2010	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	12/581,054	BALAKRISHNAN ET AL.	
	Examiner	Art Unit	
	RAJNIKANT B. PATEL	2838	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 October 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *10/09 and 11/09*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) The invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) The invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

(e) The invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

2. Claims 1-4, 6-7, 9 and 11 are rejected under 35 U.S.C.102 (b) as being anticipated by Pace et al. (U.S. Patent # 5,028,861).

Pace et al. disclose the claimed subject matters a power supply (figure 2), including a comparator (figure 2, item 56), a variable current limit (column 4, line 15-50), a saw tooth wave form (column 5, line 1-50), a feedback, a maximum duty cycle circuit (column 1, line 10-45), an oscillator, a clock signal (column 5, line 1-65).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 5, 8, 10 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over by Pace et al. (U.S. Patent # 5,028,861) in combinations with Redl (U. S. Patent # 5,680,034).

Pace et al. disclose the claimed subject matters as explained in the claims 1-4, 6-7, 9 and 11, above, except the utilization of the technique for latch technique, Redl teaches the utilization of the similar technique for a latch. It would have been obvious one having ordinary sill in the art at the time the invention was made to modify Pace et al.'s power supply circuit by utilizing the technique taught by Redl for the purpose of increasing efficiency of the power supply.

Double Patenting

5. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims1-12 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims of U.S. Patent No. 7,646,184. Although the conflicting claims are not identical, they are not patentably distinct from each other because both sets of claims are drawn to same subject matters such as "a power supply regulator comprising a comparator having first and second input, a first input is sense current flowing through switch, a variable current limit threshold, the control signal to be coupled to a control terminal of the switch, oscillator is a saw tooth waveform, a maximum duty cycle signal a latch and reset input of the latch. .

Any inquiry concerning this communication or earlier communications from the examiner should be directed to RAJNIKANT B. PATEL whose telephone number is (571)272-2082. The examiner can normally be reached on M-Th 7-5.30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lewis Monica can be reached on 571-272-1838. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/RAJNIKANT B. PATEL/
Primary Examiner, Art Unit 2838

***

Notice of References Cited	Application/Control No. 12/581,054	Applicant(s)/Patent Under Reexamination BALAKRISHNAN ET AL.	
	Examiner RAJNIKANT B. PATEL	Art Unit 2838	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-5,028,861	07-1991	Pace et al.	323/222
*	B	US-5,680,034	10-1997	Redl, Richard	363/21.03
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	12581054	BALAKRISHNAN ET AL.
	Examiner	Art Unit
	RAJNIKANT B PATEL	2838

SEARCHED			
Class	Subclass	Date	Examiner
323	282-288,235-239,220-223,272-275	03/30/10	/RP/
363	79,80,97,131,63,89		

SEARCH NOTES		
Search Notes	Date	Examiner
EAST	03/30/10	/RP/

INTERFERENCE SEARCH			
Class	Subclass	Date	Examiner

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	12581054	BALAKRISHNAN ET AL.
	Examiner	Art Unit
	RAJNIKANT B PATEL	2838

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	03/30/2010								
	1	✓								
	2	✓								
	3	✓								
	4	✓								
	5	✓								
	6	✓								
	7	✓								
	8	✓								
	9	✓								
	10	✓								
	11	✓								
	12	✓								

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BIB DATA SHEET

CONFIRMATION NO. 1732

SERIAL NUMBER	FILING or 371(c) DATE RULE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
12/581,054	10/16/2009	323	2838	5510P064C4

APPLICANTS
Balu Balakrishnan, Saratoga, CA;
Alx B. Djenguerian, Saratoga, CA;
Kent Wong, Fremont, CA;
David Michael Hugh Matthews, Windsor, UNITED KINGDOM;

**** CONTINUING DATA ***************************
This application is a CON of 11/784,560 04/06/2007 PAT 7,646,184
which is a CON of 11/397,524 04/03/2006 PAT 7,215,105
which is a CON of 10/892,300 07/15/2004 PAT 7,110,270
which is a CON of 10/253,307 09/23/2002 PAT 6,781,357
which claims benefit of 60/325,642 09/27/2001

**** FOREIGN APPLICATIONS ***************************

**** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ****
10/29/2009

Foreign Priority claimed ☐ Yes ☑ No 35 USC 119(a-d) conditions met ☐ Yes ☑ No Verified and Acknowledged /RAJNIKANT B PATEL/ Examiner's Signature	☐ Met after Allowance Initials	STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
		CA	5	12	1

ADDRESS
BLAKELY SOKOLOFF TAYLOR & ZAFMAN LLP
1279 OAKMEAD PARKWAY
SUNNYVALE, CA 94085-4040
UNITED STATES

TITLE
METHOD AND APPARATUS FOR MAINTAINING A CONSTANT LOAD CURRENT WITH LINE VOLTAGE IN A SWITCH MODE POWER SUPPLY

FILING FEE RECEIVED		
1090	FEES: Authority has been given in Paper No._____ to charge/credit DEPOSIT ACCOUNT No._____ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit

Substitute for Form 1449/PTO				Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(use as many sheets as necessary)*				Application Number	12/581,054 ~~New Patent Application~~
				Filing Date	*Concurrently herewith*
				First Named Inventor:	Balakrishnan et al.
				Art Unit	*Not Yet Assigned* 2838
				Examiner Name	*Not Yet Assigned*
Sheet	1	**of**	4	Attorney Docket Number	5510P064C4

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] (If known)		Publication Date MM/DD/YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
/R.P./	1.	US-	3,694,772	09/26/1972	Sordello	
/R.P./	2.	US-	4,032,828	06/28/1977	Strobl et al.	
	3.	US-	4,357,572	11/02/1982	Andersen et al.	
	4.	US-	4,371,824	02/01/1983	Gritter	
	5.	US-	4,392,103	07/05/1983	O'Sullivan et al.	
	6.	US-	4,674,020	06/16/1987	Hill	
	7.	US-	4,764,856	08/16/1988	Rausch	
	8.	US-	5,014,178	05/07/1991	Balakrishnan	
	9.	US-	5,045,800	09/03/1991	Kung	
	10.	US-	5,170,333	12/08/1992	Niwayama	
	11.	US-	5,189,599	02/23/1993	Messman	
	12.	US-	5,268,631	12/07/1993	Gorman et al.	
	13.	US-	5,285,366	02/08/1994	Zaretsky	
	14.	US-	5,313,381	05/17/1994	Balakrishnan	
	15.	US-	5,335,162	08/02/1994	Martin-Lopez et al.	
	16.	US-	5,465,201	11/07/1995	Cohen	
	17.	US-	5,479,090	12/26/1995	Schultz	
	18.	US-	5,583,752	12/10/1996	Sugimoto et al.	
	19.	US-	5,657,211	08/12/1997	Brockmann	
	20.	US-	5,680,034	10/21/1997	Redl	
	21.	US-	5,729,120	03/17/1998	Stich et al.	
	22.		5,729,443	03/17/1998	Pavlin	
	23.	US-	5,995,386	11/30/1999	John et al.	
	24.	US-	6,037,674	03/14/2000	Hargedon et al.	
	25.	US-	6,154,377	11/28/2000	Balakrishnan et al.	
	26.	US-	6,166,521	12/26/2000	Mercer et al.	
	27.	US-	6,222,356 B1	04/24/2001	Taghizadeh-Kaschani	
/R.P./	28.	US-	6,226,190 B1	05/01/2001	Balakrishnan et al.	

Examiner Signature	/Rajnikant Patel/	Date Considered	03/30/10

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in con considered. Include copy of this form with next communication to applicant. [1]Applicant's unique citation designation number (optional). [2]See USPTO Patent Documents at www.uspto.gov or MPEP 901.04. [3]Enter Office that issued the document, by the two-letter code (WIPO Standa Japanese patent documents, the indication of the year of reign of the Emperor must precede the serial number of the patent document. [5]Kin the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. [6]Applicant is to place a check mark here if translation is attached.

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public whic the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SENT FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.**

Based on Form PTO/SB/08A (04-03) as modified by BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP on 05/09/03

Substitute for Form 1449/PTO				Complete if Known 12/581054	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(use as many sheets as necessary)*				Application Number	~~New Patent Application~~
				Filing Date	*Concurrently herewith*
				First Named Inventor:	Balakrishnan et al.
				Art Unit	*Not Yet Assigned* 2838
				Examiner Name	*Not Yet Assigned*
Sheet	2	**of**	4	Attorney Docket Number	5510P064C4

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] (If known)		Publication Date MM/DD/YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
/R.P./	29.	US-	6,233,161 B1	05/15/2001	Balakrishnan et al.	
/R.P./	30.	US-	6,297,623 B1	10/02/2001	Balakrishnan et al.	
	31.	US-	6,333,624 B1	12/25/2001	Ball et al.	
	32.	US-	6,404,607 B1	06/11/2002	Burgess et al.	
	33.	US-	6,411,119 B1	06/25/2002	Feldtkeller	
	34.	US-	6,498,466 B1	12/24/2002	Edwards	
	35.	US-	6,525,514 B1	02/25/2003	Balakrishnan et al.	
	36.	US-	6,580,593 B2	06/17/2003	Balakrishnan et al.	
	37.	US-	6,583,994 B2	06/24/2003	Clayton et al.	
	38.	US-	6,665,197 B2	12/16/2003	Gong et al.	
	39.	US-	6,674,656 B1	01/06/2004	Yang et al.	
	40.	US-	6,747,443 B2	06/08/2004	Balakrishnan et al.	
	41.	US-	6,781,357 B2	08/24/2004	Balakrishnan et al.	
/R.P./	42.	US-	6,833,692 B2	12/21/2004	Balakrishnan et al.	
/R.P./	43.	US-	7,110,270 B2	09/19/2006	Balakrishnan et al.	
/R.P./	44.		7,215,105 B2	05/08/2007	Balakrishnan et al.	
/R.P./	45.	US-	2007/0182394 A1	08/09/2007	Balakrishnan et al.	
/R.P./	46.	US-	90/009,393	Filed 01/20/2009	Power Integrations, Inc.	

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3] Number[4] Kind Code[5] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]
/R.P./	47.	EP 0 744 818 A1	11/27/1996	Nokia Technology GmbH		
/R.P./	48.	JP 09-074748	03/18/1997	Matsushita Electric Ind. Co. Ltd.		

Examiner Signature	/Rajnikant Patel/	Date Considered	03/30/10

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Substitute for Form 1449/PTO				Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Application Number	~~New Patent Application~~ 12/581054
(use as many sheets as necessary)				Filing Date	*Concurrently herewith*
				First Named Inventor:	Balakrishnan et al.
				Art Unit	*Not Yet Assigned*
				Examiner Name	*Not Yet Assigned*
Sheet	3	**of**	4	Attorney Docket Number	5510P064C4

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	T[2]
	49.	JP 2002-284064, Notice of the Reason for Refusal (with English Translation), mailed October 21, 2008.	
	50.	European Search Report, EP 02256760, February 2, 2005.	
	51.	Infineon Technologies Preliminary Datasheet, "ICE2AS01; Off-Line SMPS Current Mode Controller," Datasheet, Version 2.1, February 2001, Infineon Technologies AG, München, Germany.	
	52.	National Semiconductor: Linear and Switching Voltage Regulator Fundamentals, 'Online: XP002316042 Retrieved from the Internet: URL: http://web.archive.org/web/20010602192453/http://www.national.com/appinfo/powerfiles/f4.pdf> No date	
	53.	Linear Technology, LT1375/LT1376, "1.5A, 500kHz Step-Down Switching Regulators," 1995, pp. 1-28. No date	
	54.	Infineon Technologies AG, Edition 2000-04-11, "Off-Line Current Mode Controller with CoolMOS™ on board," CoolSET™-F1 TDA 16822, Datasheet, V1.0, April 11, 2000, pp 1-15.	
	55.	Infineon Technologies, "Off-Line Current Mode Controller with CoolMOS™ on board," CoolSET™-F1 TDA 16822, Datasheet, V2.0, April 11, 2000, pp 1-14.	
	56.	TEA 1566 GreenChip™; SMPS Module, Preliminary Specifications, Integrated Circuits, Philips Semiconductors, April 20, 1999, pp.1-24.	
	57.	PAUL HOROWITZ & WINFIELD HILL, "The Art of Electronics", Second Edition, Published by Cambridge University Press, New York, 1989, Chapter 5, pp 263-305. No date available	
	58.	Analog Devices, "Secondary Side, Off-Line Battery Charger Controllers," ADP3810/ADP3811," October 1996, pp. 1-16.	

Examiner Signature	/Rajnikant Patel/	Date Considered	03/30/10

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Substitute for Form 1449/PTO				Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(use as many sheets as necessary)*				Application Number	New Patent Application
				Filing Date	*Concurrently herewith*
				First Named Inventor:	Balakrishnan et al.
				Art Unit	*Not Yet Assigned* 2838
				Examiner Name	*Not Yet Assigned*
Sheet	4	**of**	4	Attorney Docket Number	5510P064C4

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published No date	T[2]
	59.	Unitrode Integrated Circuits, Title Page, Introduction, and Table of Contents from "Product and Application Handbook 1993-94," (10 pages). No date available	
	60.	Unitrode Integrated Circuits, " Application Note U-100A: The UC3842/3/4/5 Series of Current-Mode PWM IC's," published in "Product and Application Handbook 1994-95," June 1993, at pp. 9-64 through 9-75; (12 pages).	
	61.	Office Action mailed September 24, 2009, Reexamination Control No. 90/009,393, filed January 20, 2009.	

Examiner Signature	/Rajnikant Patel/	Date Considered	03/30/10

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Substitute for Form 1449/PTO				Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)				Application Number	12/581,054
				Filing Date	October 16, 2009
				First Named Inventor:	Balakrishnan et al.
				Art Unit	*Not Yet Assigned* 2838
				Examiner Name	*Not Yet Assigned*
Sheet	1	**of**	1	Attorney Docket Number	5510P064C4

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	T[2]
/R.P./	1.	MAXIM, "How to Design Battery Charger Applications that Require External Microcontrollers and Related System-Level Issues," Application Note 680: http://www.maxim-ic.com/an680, March 15, 2000. (16 pages)	
/R.P./	2.	CHESTER SIMPSON, "Battery Charging," National Semiconductor, No Available Publication Date. (17 pages) No date	

Examiner Signature	/Rajnikant Patel/	Date Considered	03/30/10

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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
12/581,054	10/16/2009	Balu Balakrishnan	5510P064C4

CONFIRMATION NO. 1732

8791
BLAKELY SOKOLOFF TAYLOR & ZAFMAN LLP
1279 OAKMEAD PARKWAY
SUNNYVALE, CA 94085-4040

PUBLICATION NOTICE

OC000000040074592

Title:METHOD AND APPARATUS FOR MAINTAINING A CONSTANT LOAD CURRENT WITH LINE VOLTAGE IN A SWITCH MODE POWER SUPPLY

Publication No.US-2010-0033147-A1
Publication Date:02/11/2010

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

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Substitute for Form 1449/PTO				Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(use as many sheets as necessary)*				Application Number	12/581,054
				Filing Date	October 16, 2009
				First Named Inventor:	Balakrishnan et al.
				Art Unit	*Not Yet Assigned*
				Examiner Name	*Not Yet Assigned*
Sheet	1	**of**	1	Attorney Docket Number	5510P064C4

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	T[2]
	1.	MAXIM, "How to Design Battery Charger Applications that Require External Microcontrollers and Related System-Level Issues," Application Note 680: http://www.maxim-ic.com/an680, March 15, 2000. (16 pages)	
	2.	CHESTER SIMPSON, "Battery Charging," National Semiconductor, No Available Publication Date. (17 pages)	

Examiner Signature		Date Considered	

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EFS ID:	6525961
Application Number:	12581054
International Application Number:	
Confirmation Number:	1732
Title of Invention:	METHOD AND APPARATUS FOR MAINTAINING A CONSTANT LOAD CURRENT WITH LINE VOLTAGE IN A SWITCH MODE POWER SUPPLY
First Named Inventor/Applicant Name:	Balu Balakrishnan
Customer Number:	08791
Filer:	James Go/Kristy Marvel
Filer Authorized By:	James Go
Attorney Docket Number:	5510P064C4
Receipt Date:	25-NOV-2009
Filing Date:	16-OCT-2009
Time Stamp:	14:08:02
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Transmittal Letter	5510P064C4_IDS_112509.pdf	24525 1bab7a997d3db158b9aae71cc2861a6a6ecce515	no	2

Warnings:	
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2	Information Disclosure Statement (IDS) Filed (SB/08)	5510P064C4_PTO1449_112509.pdf	41396 877f05d5d4baee4b6e10bd7802dbc9f0f669cec0	no	1
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4	NPL Documents	5510P064C4_NPL2_112509.pdf	122094 90e13c52ba850556c15c00b1fb72d4a89bd6be68	no	17
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:	)	
	)	
Balu Balakrishnan et al.	)	Examiner: *Not yet assigned*
	)	
Application No.: 12/581,054	)	Art Unit: *Not yet assigned*
	)	
Filed: October 16, 2009	)	Confirmation No.: 1732
	)	
For: METHOD AND APPARATUS FOR MAINTAINING A CONSTANT LOAD CURRENT WITH LINE VOLTAGE IN A SWITCH MODE POWER SUPPLY	)	

Mail Stop Amendment
Commissioner for Patents
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Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Date: November 25, 2009

/James Y. Go/
James Y. Go
Reg. No. 40,621

1279 Oakmead Parkway
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/Kristy A. Marvel/ November 25, 2009

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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
12/581,054	10/16/2009	2816	1090	5510P064C4	12	1

CONFIRMATION NO. 1732

8791
BLAKELY SOKOLOFF TAYLOR & ZAFMAN LLP
1279 OAKMEAD PARKWAY
SUNNYVALE, CA 94085-4040

FILING RECEIPT

OC00000038536261

Date Mailed: 11/03/2009

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Applicant(s)

Balu Balakrishnan, Saratoga, CA;
Alx B. Djenguerian, Saratoga, CA;
Kent Wong, Fremont, CA;
David Michael Hugh Matthews, Windsor, UNITED KINGDOM;

Assignment For Published Patent Application

Power Integrations, Inc., San Jose, CA

Power of Attorney:

Edwin Taylor--25129
Eric Hyman--30139
Michael Bernadicou--35934
Michael Mallie--36591
William Schaal--39018
Gregory Caldwell--39926
James Go--40621
Jan Little-Washington--41181
Todd Becker--43487
Mark Watson--46322

Domestic Priority data as claimed by applicant

This application is a CON of 11/784,560 04/06/2007
which is a CON of 11/397,524 04/03/2006 PAT 7,215,105
which is a CON of 10/892,300 07/15/2004 PAT 7,110,270
which is a CON of 10/253,307 09/23/2002 PAT 6,781,357
which claims benefit of 60/325,642 09/27/2001

Foreign Applications

If Required, Foreign Filing License Granted: 10/29/2009

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 12/581,054**

Projected Publication Date: 02/11/2010

Non-Publication Request: No

Early Publication Request: No

Title

METHOD AND APPARATUS FOR MAINTAINING A CONSTANT LOAD CURRENT WITH LINE VOLTAGE IN A SWITCH MODE POWER SUPPLY

Preliminary Class

327

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				Filing Date	*Concurrently herewith*
				First Named Inventor:	Balakrishnan et al.
				Art Unit	*Not Yet Assigned*
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Sheet	1	**of**	4	Attorney Docket Number	5510P064C4

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Examiner Initials*	Cite No.[1]	Document Number		Publication Date MM/DD/YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
			Number-Kind Code[2] (If known)			
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NON PATENT LITERATURE DOCUMENTS

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	59.	Unitrode Integrated Circuits, Title Page, Introduction, and Table of Contents from "Product and Application Handbook 1993-94," (10 pages).	
	60.	Unitrode Integrated Circuits, " Application Note U-100A: The UC3842/3/4/5 Series of Current-Mode PWM IC's," published in "Product and Application Handbook 1994-95," June 1993, at pp. 9-64 through 9-75; (12 pages).	
	61.	Office Action mailed September 24, 2009, Reexamination Control No. 90/009,393, filed January 20, 2009.	

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(54) A method and circuit for controlling the output characteristics of a switched-mode power supply

(57) The invention relates to a method and a circuit to control the output voltage and current of a switched-mode power supply. In order to restrict the output current, a voltage value proportional to the primary current of a switched-mode power supply is measured and compared to a variable reference voltage U_{ext} the value of which is determined by the total effect of the constant charging current of a capacitor C_{ext} and a discharge circuit operating in step with the secondary diode of the power supply. If the voltage value proportional to the primary current is bigger than said reference voltage, the switching pulses of the primary current switch are shortened. In order to restrict the output voltage, an image voltage is generated for the secondary voltage of the power supply transformer which is filtered and rectified and combined with the aforementioned reference voltage in order to produce pulse-width-modulated switching pulses of the primary current switch.

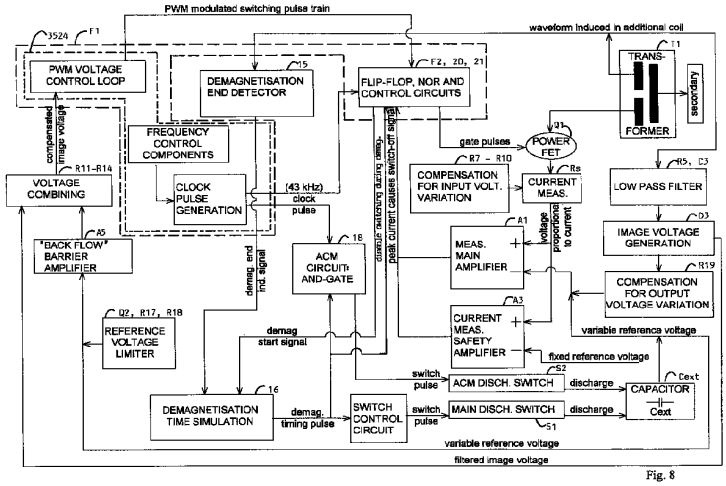

Fig. 8

EP 0 744 818 A1

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Description

The invention relates to a method and circuit to restrict the output current and voltage of a switched-mode power supply.

Modern power converter systems often use various switched-mode power supplies (SMPS) to convert a DC voltage (or also an AC voltage, if the coupling includes suitable rectifying means) to a more suitable voltage level and to stabilize the voltage and current fed to the load in conditions where the supply power and the electrical characteristics of the load may vary. In many different applications it is necessary to restrict the output current and voltage of the power supply below a certain maximum value so as not to harm the load and the power supply itself. In addition, it is often advantageous that the output voltage and current can be simultaneously controlled in such a way that there is a connection between their values. An example of such an application is a charging device for charging batteries. When a discharged battery is coupled to the charging device, its terminal voltage is relatively low at first. During charging, the terminal voltage increases towards a maximum value which depends on the materials and construction of the battery. The temperature of the charging device increases with the terminal voltage of the battery, and the charging current must be limited so as to avoid disadvantageous phenomena, such as excessive warming. Towards the end of the charging process, the current reception capability of the battery falls, whereupon it is advantageous to reduce the output current of the charging device and to limit its output voltage below a certain maximum value so as to avoid losses and other disadvantageous phenomena.

Fig. 1 shows, by way of example, the limit values of the output characteristics of a battery charging device, represented by the area confined by the boundary lines in the figure. The device in question is used to charge a battery the terminal voltage of which is 10 V when fully charged. When a discharged battery is coupled to the charger, its terminal voltage rises in a few seconds to a certain minimum value, which in this case is about 5 V. The figure shows that the accurately defined current-voltage region, or the narrow "channel" between the boundary lines, starts at five volts, where the output current must be at least 0.76 A and no more than 0.84 A. Below this voltage level the output characteristics of the charger are of little importance as long the charger does not produce a current peak of more than 0.84 A upon switch-on.

During the charging process, the output current of the charger described must be kept substantially constant at about 0.8 amps. The boundary lines confine a tolerance region which represents the allowed ±5% variation range for the current value. It is not practical to specify the current value more accurately than this, because the electrical characteristics of components always vary within certain tolerances. The terminal voltage of the battery charged increases until it begins to near the nominal maximum value of 10.0 V. At this point, the voltage limiter of the charger starts limiting its output voltage to prevent it from exceeding the upper limit value. The voltage limiter is designed for 10.0 volts, but there is a ±5% variation range about the nominal value just as in the case of current limiting. When the charging process ends, the output current of the charger is substantially zero and its output voltage at least 9.5 V and not more than 10.5 V. After this, it is known to continue charging using a so-called trickle charge function, where a switch on the secondary side, i.e. on the load side of the charger switches the charging repeatedly on and off. Also in this case the limiter functions of the charger must keep the output current and voltage within allowed limits.

A switched-mode power supply which can be used to realize the charging function described above typically comprises a transformer which divides the power supply into a primary part and a secondary part. Input voltage is connected to the input terminals in the primary. Typically the power supply includes a switching element, advantageously a MOSFET or bipolar transistor which chops the input voltage into pulses that supply current to the primary winding of the transformer. Variation of the primary voltage and current stores magnetic energy in the magnetic field of the transformer. With suitable polarity in the primary and secondary windings of the transformer and using rectifier diodes the stored energy is transferred to the secondary winding and therefrom to the secondary part of the switched-mode power supply, where it produces an output voltage at the power supply output terminals. There are several known circuit topologies, or ways to arrange the components in the power supply apparatus described in relation to each other in order to achieve the desired operation. The most popular of these are the buck, boost and flyback topologies.

The traditional approach in implementing stabilization of output characteristics in a switched-mode power supply like the one described here has been to measure the output current and voltage in the secondary and take the measuring data to the circuit element in the primary that determines the duty cycle, or the ratio of the ON and OFF times of the switching transistor used to chop the primary voltage. The longer the ON time in proportion to the OFF time, the greater the amount of energy stored in the transformer's magnetic field during an ON-OFF cycle, and the greater the amount of energy transferred through the secondary winding to the secondary of the circuit and further to the load. It depends on the construction of the secondary part and on the electrical characteristics of the load, whether it is the output voltage, the output current or both that increases. Correspondingly, decreasing the pulse ratio, or the proportion of the ON time, reduces the amount of energy transferred and hence the output voltage or the output current or both.

In a switched-mode power supply like the one described the power and voltages may be relatively

high. As regards electrical safety, it is often preferable that there is no galvanic contact between the primary and the secondary. If it is desired to transfer the current or voltage information measured in the secondary to stabilize the output characteristics to the primary side, it must be conveyed through an opto-isolator or a corresponding component which realizes galvanic isolation. The price and limited reliability and life of the opto-isolator are disadvantageous factors from the manufacturing standpoint.

The development of switched-mode power supplies has been towards concentrating the control and limiting functions in the primary part only. The idea is based on the fact that the output characteristics can be determined on the basis of certain parameters of the primary part. It is known to add to a transformer like the one described a third, or additional, winding to generate an image of the voltage waveform induced in the secondary winding during one cycle. It is also known to measure the primary current by connecting a small current measuring resistor in series with the switching element and measuring the voltage loss across said resistor. It is beneficial to concentrate the control and limiting functions in the primary because most of the necessary measuring and adjusting connections can be integrated in one IC which also advantageously contains means to produce the switching element ON and OFF signals. The switching element can also be integrated in the same circuit. The disadvantages of opto-isolators are thus avoided.

Fig. 2 illustrates a known method to limit the output current I_{OUT} in a flyback-type switched-mode power supply. Transformer T1 includes a primary winding 11, a secondary winding 12 and an additional winding 13. The primary side includes a MOSFET transistor Q1 used for switching the primary current, a control circuit F1 to control the gate voltage of said transistor, a current measuring resistor R_s, a differential amplifier A1, a constant current supply I_c, a so-called "external" capacitor C_{ext}, a current path to discharge said capacitor including a resistor R_c and a switch S1, and a so-called additional circuit 10. The word "external" is used throughout this text simply to qualify the capacitor C_{ext} and it does not necessarily mean that said capacitor is physically located apart from the rest of the circuit. The additional circuit 10 connected to the additional winding 13 is a detector the task of which is to detect the demagnetization of transformer T1, or the moment at which the energy stored in the magnetic field during one ON cycle of transistor Q1 is completely transferred to the secondary of the power supply. The secondary of the power supply according to Fig. 2 comprises a diode D1, a relatively high-capacity capacitor C1 to stabilize output voltage variation in one cycle, and a relatively large shunt resistor R_o the purpose of which is to serve as a minimum load and to provide a discharge path for the charge stored in capacitor C1 upon switch-off.

The circuit depicted in Fig. 2 operates as follows: At the beginning of a cycle, the control circuit F1 switches the MOSFET transistor Q1 ON, i.e. into conductive state. An increasing primary current I_p starts to flow through the primary winding 11, MOSFET transistor Q1 and the current measuring resistor R_s. Affected by the inductance of winding 11, the primary current I_p increases linearly. The polarities of windings 11 and 12 and diode D1 are such that the magnetic field produced by the primary current I_p tries to induce in the secondary winding 12 a voltage in relation to which the diode D1 is reverse-biased. The diode prevents the flow of current in the secondary circuit, whereby energy is stored in the strengthening magnetic field. When the MOSFET transistor is switched OFF, the sign of the time derivative of the magnetic field is reversed and a current is induced in the secondary winding in relation to which the diode D1 is forward-biased. Part of the secondary current I_s produced is taken to the load as output current I_{OUT} and part of it charges the capacitor C1, which has maintained the output current I_{OUT} by partly discharging while the secondary current I_s was not flowing. When the energy in the magnetic field has been completely discharged, the secondary current I_s stops flowing and the additional circuit 10, which measures the small current I_a induced in the additional winding, detects the situation and informs the control circuit F1. The signal provided by the additional circuit affects the pulse ratio: the less time was used to discharge the magnetic energy, the longer the ON time in proportion to the OFF time that is needed in the next cycle and vice versa.

During the ON cycle of the MOSFET transistor Q1 the primary current I_p flows through a current measuring resistor R_s, as described above. A differential amplifier A1 compares the existing voltage loss of resistor R_s to a reference voltage U_{ext} between the terminals of the external capacitor C_{ext}. If the existing voltage loss of resistor R_s becomes greater than voltage U_{ext}, the differential amplifier A1 informs control circuit F1 that the primary current has reached its peak value, whereupon the MOSFET transistor Q1 is immediately switched OFF.

In addition to controlling the gate voltage of the MOSFET transistor Q1 the control circuit F1 controls the position of switch S1. Switch S1 should always be ON, i.e. conductive, when diode D1 is conductive, and correspondingly OFF when diode D1 is non-conductive. This is to keep the voltage U_{ext} between the terminals of capacitor C_{ext} correct by providing a current path, which comprises a switch S1 and a series resistor R_c, discharging the capacitor when switch S1 is ON. The control circuit F1 sets switch S1 ON when switching the MOSFET transistor Q1 OFF, and OFF when the additional circuit 10 informs that the transformer T1 has been demagnetized.

By using the demagnetizing information to control the pulse ratio and by preventing the primary current I_p from increasing too much the primary part of the switched-mode power supply shown in Fig. 2 controls the output current I_{OUT} of the device. When the output voltage U_{OUT} increases, e.g. when a battery connected

to the charger is being charged, the demagnetization time of transformer T1 and the conduction time of diode D1 become shorter. The power supply meets the growing demand for output current by increasing the pulse ratio on the basis that also the ON time of switch S1 is shortened, whereupon the voltage U_{ext} between the terminals of capacitor C_{ext} is increased. In the opposite case, slow demagnetization or very high primary current mean excessive output current, with switch S1 in conductive state for a long time during the cycle, which decreases the voltage U_{ext} between the terminals of capacitor C_{ext}, which in turn decreases the pulse ratio. As regards e.g. a battery charger like the one described above, the disadvantage of this known arrangement is that it includes no output voltage limiter.

Fig. 3a shows a known circuit used for estimating the output voltage of a flyback type switched-mode power supply. The circuit is intended to be used as part of the primary of the power supply, but for reasons of clarity the rest of the primary, with the exception of primary winding 11, are not shown. The voltage regulating circuit (as it will be called hereinafter) according to Fig. 3a comprises a rectifying diode D2, series resistor R2, resistors R3 and R4 for voltage division, capacitor C2 for stabilizing voltage variations at point A during one cycle, and as a load, a constant resistance R_a, which could be replaced by a constant current load the current I_a of which would be advantageously about 10 mA. The voltage regulating circuit also includes a voltage comparison stage which comprises a differential amplifier A2.

The voltage regulating circuit according to Fig. 3a is a kind of a mirror image of the secondary of the switched-mode power supply and indeed it is designed to produce a so-called image voltage U_a at point A in the same way that the secondary produces an output voltage U_{OUT} at the output terminals of the switched-mode power supply. The image voltage U_a is measured via a voltage divider comprising resistors R3 and R4 and compared to an accurate reference voltage U_{ref} by means of a differential amplifier A2. The output of the differential amplifier A2 is used to control the primary current switch (not shown) through a pulse width modulator and a control circuit (not shown). The component values are selected such that the power consumption in the voltage regulating circuit is as small as possible. Unfortunately this goal conflicts with the objective that the image voltage U_a should be a perfect image of the controlled output voltage U_{OUT}.

The fundamental flaw in the operation of the circuit is related to the magnetic properties of transformer T1. In a typical switched-mode power supply transformer that includes an additional winding, such as transformer T1 in Fig. 3a, there has to be an insulating layer between the primary 11 and secondary 12 windings. However, the additional winding 13 can be wound directly over or under the primary winding 11 or even interleaved with it. Therefore, the coupling coefficient between the primary winding 11 and the additional winding 13 is nearer to 1 than the coupling coefficient between the primary winding 11 and the secondary winding 12. In the case of the transformer shown in Fig. 3a, typical coupling coefficients can be about 0.99 between the primary and additional windings and about 0.98 between the primary and secondary windings. The difference of the coupling coefficients means that when the current through the primary winding 11 is shut off, the energy stored by its leak inductance cannot be transferred to the secondary winding 12, but part of it can be transferred to the additional winding 13, which results in a voltage peak across the additional winding. The height of the peak depends on the amount of energy stored in the leak inductance of the primary winding. If the output power, or output current, of the switched-mode power supply is high, a lot of energy is transferred in one cycle and, correspondingly, more energy is lost in the leak inductances than if the output power were low. A great amount of energy stored in the leak inductance means a high voltage peak across the additional winding 13. Capacitor C2 partly rounds off the effect of the voltage peak, but in any case it leads to a nearly linear dependence between the image voltage U_a and the output voltage, as seen in Fig. 4.

A solution to the problem described above would be to add an insulating layer between the primary 11 and additional 13 windings in transformer T1, whereby the coupling coefficient between them would be equal to that between the primary and secondary windings. A sandwich type transformer could also be used. However, the transformer is already the most expensive single component in a switched-mode power supply, so it is not preferable to make its construction more complex.

Another solution is to eliminate the voltage peak using any arrangement known to one skilled in the art. One such arrangement is shown in Fig. 3b where a low-pass type coupling consisting of a resistor R5 and a capacitor C3 is added to the arrangement shown in Fig. 3a. A rectifying diode D3 and a capacitor C4 are also added to the circuit. Resistors R3 and R4 comprise a voltage dividing coupling connected in series with diode D3, used for taking a voltage signal to the differential amplifier A2, said voltage signal being proportional to voltage U_b at point B, i.e. to the rectification result of the low-pass filtered image voltage. Voltage U_b is a better representation of the switched-mode power supply output voltage U_{OUT} as a function of the output current I_{OUT}, as can be seen from the curves in Fig. 4, but it still depends, and non-linearly depends, on the output current I_{OUT}.

The curves in Fig. 4 are the result of a laboratory measurement wherein the output voltage U_{OUT} of the switched-mode power supply was kept constant and image voltage alternatives U_a and U_b were studied as the function of the output current I_{OUT}. In a real switched-mode power supply using a voltage regulating circuit according to Fig. 3a or 3b, a differential amplifier A2 compares voltage U_a or U_b to an accurate and constant reference voltage U_{ref}, so it is implied that the

image voltage U_a or U_b, whichever is used, reflects the output voltage U_{OUT} realistically, being directly proportional to it and wholly independent of the output current I_{OUT}. Since this is not the case, the output voltage U_{OUT} of the switched-mode power supply becomes too high with a small output current I_{OUT}.

Several other ways to improve the output characteristics of a switched-mode power supply are known. A known arrangement includes a sampling circuit, which does not measure the shape of the whole voltage pulse induced in the additional winding, but takes a narrow sample from it, advantageously near the trailing edge of the pulse. The effect of the voltage peak mentioned above is at its smallest near the trailing edge of the pulse. The voltage sample is used to generate an image voltage, which is used in the same manner as image voltages U_a and U_b described above. The sampling circuit naturally adds to the complexity, manufacturing costs and power consumption of the arrangement. It is further known a solution in which a current integrator used for measuring the output voltage is added to the current limiting arrangement according to Fig. 2. The solutions described have not been able to correct the non-linear dependence between the output voltage and output current in a switched-mode power supply, which typically manifests itself in a sharp increase in the output voltage when the output current is small.

It is also known a method called burst mode control, where an image voltage (above, U_a and U_b) is measured and compared to a reference value. If the measured value is greater than the reference value indicating the allowed maximum, a Schmitt trigger circuit grounds the gate of the MOSFET transistor functioning as a primary current switch, i.e. switches the transistor OFF for a predetermined period of time the duration of which is determined by the component values. When the forced grounding of the transistor gate ceases, the cycle starts over again. The problem with this arrangement is that when the forced grounding of the switching transistor gate is ended, the switched-mode power supply immediately starts operating at a high power, pumping a great amount of magnetic energy into the transformer and causing sharp voltage peaks in the voltage across the additional winding. This has the same effect as the fact that the image voltages U_a and U_b mentioned above depend on the output current of the switched-mode power supply: the open circuit voltage, or the output voltage of the device increases when the output current is small.

The object of the invention is to provide a method and a circuit for controlling the output voltage and output current of a switched-mode power supply with couplings in its primary part partly avoiding and partly reducing the aforementioned disadvantages related to the prior art solutions.

The object of the invention is achieved by combining to the operation of a current measuring and regulating circuit a simultaneous operation of a voltage measuring and regulating circuit so that a compensating voltage is generated which compensates for the change that appears as a function of the output current of the switched-mode power supply in the operation of the voltage measuring and regulating circuit. Also, to achieve the object of the invention, a compensating coupling is provided from the voltage measuring and regulating circuit to the current measuring and regulating circuit to compensate for the variation of the reference voltage used in the current regulation as a function of the output current of the switched-mode power supply.

The method according to the invention, wherein a first reference voltage and a first voltage signal and switching pulses to switch the primary current switching element are generated on the primary side of a switched-mode power supply, is characterized in that also on the primary side

- a combination is produced of said first voltage signal and said first reference voltage, and
- said switching pulses for switching the primary current switching element are generated on the basis of said combination.

The circuit according to the invention, which includes a control circuit on the primary side to generate said switching pulses, is characterized in that it further includes on the primary side means for producing a combination of said first reference voltage and first voltage signal and for directing said combination to said control circuit to generate said switching pulses.

During the development work that led to the invention it was discovered that by combining the operation of a prior art current regulating circuit with the operation of a prior art voltage regulating circuit it is possible, with suitable couplings, to produce a voltage the behaviour of which as a function of the output current of the switched-mode power supply is particularly advantageous and which therefore may be used to compensate for a similar but opposite signed change in the voltage regulating circuit. Said voltage is produced between the terminals of an "external" capacitor belonging to a prior art current regulating circuit and its generation and value as a function of the output current of the switched-mode power supply will be discussed later.

Below, the invention is described in more detail using certain embodiments as illustrative examples and referring to the accompanying drawing, in which

Fig. 1 shows output current and output voltage limits in a typical known charging device designed for charging a series-connected battery comprising six NiCd cells,

Fig. 2 is a circuit diagram of a known current limiting circuit of a switched-mode power supply,

Fig. 3a is a circuit diagram of a known voltage limiting circuit of a switched-mode power supply,

Fig. 3b is a modified version of the coupling shown in Fig. 3a,

Fig. 4 graphically illustrates three measured voltages U_a, U_b and U_{OUT} as a function of the output current I_{OUT} in the switched-mode power supply according to the invention,

Fig. 5 graphically illustrates a measured and calculated reference voltage U_{ext} as a function of the output current I_{OUT} in the switched-mode power supply according to the invention,

Fig. 6 graphically illustrates two measured voltages U_{OUT} and U_{ext} as a function of the output current I_{OUT} in the switched-mode power supply according to the invention,

Fig. 7a is a circuit diagram of an embodiment of the invention,

Fig. 7b is a block diagram of part of Fig. 7a,

Fig. 8 is a block diagram of the whole embodiment shown in Fig. 7a,

Fig. 9 is an activity graph illustrating the flow of signals and information and the sequence of activities in the switched-mode power supply according to the invention, and

Fig. 10 is a circuit diagram of an embodiment of the invention where most of the necessary components are integrated in a single IC.

In all figures, like parts are denoted by like reference numbers.

A battery charging device will be described next in order to illustrate the ways in which the invention can be applied. However, the invention is not limited to the embodiments described, but it is clear to one skilled in the art that it can be used in all applications in which it is desired to limit the output voltage and output current of a switched-mode power supply by means of a circuit arrangement in the primary part.

The method and circuit according to the invention employ a known pulse width modulator controller designed for switched-mode power supplies; said controller will hereonafter be called a PWM circuit and as far as the structure of the invention is concerned, said circuit is thought to belong to the controller circuit of the power field-effect transistor serving as a primary current switch. A suitable PWM circuit is SGS-Thomson's LM3524 but other corresponding PWM circuits known to one skilled in the art can be used as well. The same functions can also be implemented using separate components. Parts and functions in the PWM circuit that are significant from the point of view of the invention are

- a differential amplifier for comparing a certain measured voltage to a certain reference voltage,
- a pulse generator, which on the basis of an output from said differential amplifier produces a pulse-width-modulated switching pulse sequence to control the primary current switch in the switched-mode power supply, and
- a clock pulse generator, which produces at a predetermined frequency the timing pulses needed for controlling the operation of the whole circuit arrangement, said predetermined frequency being advantageously 43 kHz, approximately, in the circuit and method according to the invention.

The method and circuit according to the invention employ a switched-mode power supply transformer which advantageously comprises three windings. A suitable transformer is e.g. the Salcomp FM3750, but other transformers can be used if the component values in the circuit arrangement are slightly changed.

Fig. 7a shows a circuit diagram illustrating an embodiment of the circuit according to the invention. The circuit according to the invention uses in a known manner a power FET Q1, hereonafter called a FET, to interrupt the primary voltage and current in a switched-mode power supply. The primary current I_p chopped by said FET Q1 flows through the primary winding 11 in transformer T1. A relatively low-resistance current measuring resistor R_s is connected in series with said FET Q1 to direct said primary current I_p also through said current measuring resistor R_s. A tuning resistor R6 can be connected in parallel with said current measuring resistor as in the embodiment illustrated by Fig. 7a, or other known methods can be used for accurately selecting a value for the current measuring resistance. The purpose of said current measuring resistor R_s is to determine the intensity of the primary current I_p by measuring the voltage loss across said current measuring resistor. For the measurement, a connection is provided to a differential amplifier A1 at a point between the FET Q1 and the current measuring resistor R_s. Advantageously the connection is made via a voltage dividing coupling consisting of resistors R7 to R10 so that the first end (R7) of said voltage dividing coupling is connected between said FET Q1 and said current measuring resistor R_s and the second end (R10) to the input voltage U_s of the switched-mode power supply. Connection from said voltage dividing coupling R7-R10 to the positive input of said differential amplifier A1 is advantageously made at a point between the first R7 and the second R8 resistor of the voltage dividing coupling. The purpose of the voltage dividing coupling R7-R10 is to compensate for disturbances occurring in the measurement, caused by variations in said input voltage U_s.

The negative input of said differential amplifier A1 is connected to a first reference voltage U_{ext} which is the voltage betweeen the terminals of an external capacitor C_{ext}. The purpose of said differential amplifier A1 is to compare a measured voltage proportional to the intensity of the primary current I_p to said first reference voltage. The output of the differential amplifier A1 is connected to a circuit F1 controlling the gate voltage of said FET Q1. If the voltage across the current measuring resistor R_s measured by the differential amplifier A1 is greater than said first reference voltage U_{ext}, the differential amplifier A1 sends to circuit F1 a signal on the basis of which circuit F1 switches FET Q1 OFF.

According to the embodiment shown in Fig. 7a, the circuit according to the invention can advantageously

include a second differential amplifier A3, and the same voltage proportional to the intensity of the primary current which was connected to the positive input of the differential amplifier A1 is connected to the positive input of said second differential amplifier A3. A second reference voltage U_{ref2}, which in the embodiment of Fig. 7a is generated with a voltage divider comprising resistors R24 and R25 at a point between +5V and the ground potential, is connected to the negative input of said second differential amplifier the purpose of which is to compare said voltage proportional to the intensity of the primary current to said second reference voltage U_{ref2}. If the voltage across the current measuring resistor R_s measured by differential amplifier A3 is greater than said second reference voltage U_{ref2}, differential amplifier A3 sends to circuit F1 a signal on the basis of which circuit F1 switches FET Q1 OFF. The purpose of this function is to improve the reliability of the circuit in a situation where the first reference voltage U_{ext} for some reason exceeds the fixed second reference voltage U_{ref2}.

Next, we will discuss the value of said first reference voltage U_{ref} and how it is determined. Said voltage is the voltage between the terminals of a so-called external capacitor C_{ext} and to affect the voltage the circuit according to the invention includes a controlled current path S1, R_c, which can be used to produce a discharging coupling between the terminals of said capacitor by making switch S1 conductive. The circuit according to the invention also includes a constant current supply 14 for continuously charging the external capacitor C_{ext} with a constant current I_C. From the point of view of the invention, it is essential that voltage U_{ext} is determined as a function of the output current I_{OUT} of the switched-mode power supply, and it can be theoretically calculated by assuming that the conduction time t_S of switch S1 is linearly dependent on the conduction time t_D of diode D1 in the secondary of the switched-mode power supply. Above in the description of the prior art, where a reference was made to Fig. 2, a similar connection was made between the conduction times t_S and t_D, where it was however assumed that as a result of the operation of an additional circuit 10 and controller circuit F1 the times t_S and t_D are the same. The linear dependence proposed here is a more realistic assumption.

According to a known induction law

$$U_{out} + U_D = L_S \frac{\hat{I}_S}{t_D}, \qquad (1)$$

where U_{OUT} is the output voltage of a switched-mode power supply, U_D is the voltage loss across diode D1, L_S is the inductance of the secondary winding, $\hat{I}_S$ is the peak value of the secondary current, and t_D is the conduction time of diode D1. Equation 1 is accurately true only if the constant current load I_a is zero. When calculating the connection between the peak current $\hat{I}_S$ and the output current I_{OUT} of the switched-mode power supply, an approximation can be made where the effect of a constant current load connected to the additional winding 13 is taken into account by adding to the output current term I_{OUT} a constant term

$$\frac{n_a}{n_S} I_a = \frac{34}{17} \cdot 10\,mA = 20\,mA, \qquad (2)$$

where n_a and n_S are the numbers of turns of the additional and secondary windings and I_a is the intensity of the constant current load, 10 mA in the embodiment of Fig. 7a. Now, the connection between the peak current $\hat{I}_S$ and the output current I_{OUT} of the switched-mode power supply is given by

$$\frac{1}{2} \hat{I}_S t_D = \left(I_{OUT} + \frac{n_a}{n_S} I_a + \frac{U_{out}}{R_o} \right) T, \qquad (3)$$

where R_o is the resistance of an output resistor (shunt resistor) R_o and T is the cycle time of the switched-mode power supply, or the inverse of the operating frequency, here assumed to be a constant. Also U_{OUT} and R_o are substantially constant, so in equation 2, time t_D depends only on the current I_{OUT}. By solving for the peak current $\hat{I}_S$ we get

$$\hat{I}_S = 2\left(I_{out} + \frac{n_a}{n_S} I_a + \frac{U_{out}}{R_o} \right) \frac{T}{t_D}, \qquad (4)$$

and by inserting this in equation 1 we get, after a little manipulation,

$$t_D = \sqrt{\frac{2L_s\left(I_{out} + \frac{n_a}{n_S} I_a + \frac{U_{out}}{R_o} \right) T}{U_{out} + U_D}} \qquad (5)$$

for the conduction time of diode D1. For the voltage between the terminals of the external capacitor we get

$$U_{ext} = R_C I_C \frac{T}{t_S}, \qquad (6)$$

where R_C and I_C are the discharge current path resistance and charging current according to Fig. 7a and t_S is the conduction time of switch S1. Above it was mentioned that a linear dependence is assumed between the conduction times t_S and t_D, or that

$$t_S = \kappa t_D + \tau, \qquad (7)$$

where κ and τ are constants. Combining the results of equations 5, 6 and 7, we get

$$U_{ext} = \frac{I_C R_C}{\kappa \sqrt{\frac{2L_S\left(I_{out} + \frac{n_a}{n_S} I_a + \frac{U_{out}}{R_o}\right)}{(U_{out} + U_D)T}} + \frac{\tau}{T}} \quad (8)$$

for the voltage U_{ext} between the terminals of the external capacitor C_{ext}. A laboratory measurement has been performed to determine the values of constants κ and τ, wherein the constant values were determined as

$$\kappa = 0.9900 \wedge \tau = 1.300\mu sec \quad (9)$$

at a probability of more than 99% in a series of more than 30 measurements. The behaviour of voltage U_{ext} as a function of the output current I_{OUT} of the switched-mode power supply, calculated on the basis of equation 8, is shown in Fig. 5 ("calc."). For the sake of comparison, the figure also shows a measured voltage U_{ext} ("meas.") for a real circuit according to the invention.

To control switch S1 in the manner described above the circuit according to the invention includes means to detect the moments of time at which the demagnetization of transformer T1 begins and ends during one cycle. Below it will be described the structure and operation of these means in the embodiment illustrated by Fig. 7a.

Demagnetization is started at the moment when FET Q1 is switched OFF. Information about this is brought to a demagnetization time simulation block 16 simply with a connection from the inverse of the gate voltage of FET Q1 generated in a control circuit F1. Detection of the end of demagnetization is more difficult, and therefore an additional winding 13 in the transformer in the embodiment of Fig. 7a produces a voltage the shape of which corresponds to the shape of the voltage of the secondary winding 12. When energy stored during a cycle in the magnetic field of the transformer has been discharged, diode D1 in the secondary stops conducting, which results in a drop in the induction voltage in all three windings 11, 12 and 13. Energy stored in the capacitances of the windings and in the internal capacitances of FET Q1 is discharged, which results in damped voltage oscillation in the windings. The first voltage swing is detected in the additional winding 13 as negative and it is taken to a detector, which in the embodiment of Fig. 7a is a differential amplifier coupling 15. On the basis of the detection it generates a signal which is taken to the demagnetization time simulation block 16.

On the basis of the start and end signals the demagnetization time simulation block generates the timing pulses that are needed for controlling switch S1 as described above. Then said first reference voltage U_{ext} is generated across capacitor C_{ext}.

Fig. 7b shows a partial block diagram of the embodiment of Fig. 7a, illustrating the generation of FET Q1 switching pulses in control circuit F1. The element that decides the length of the switching pulse is a logic NOR gate 20, shown in the middle of Fig. 7b, included in control circuit F1 in the embodiment of Fig. 7a. Its output is at logic level 0 if at least one of its three inputs is at logic level 1. The inputs are a pulse-width-modulated switching pulse train from a PWM circuit 3524, an inverted output $\overline{Q}$ from a flip-flop circuit F2 and an output from the demagnetization time simulation circuit 16, wherein logic level 1 corresponds to conduction time t_S of switch S1 (not shown in Fig. 7b). At the beginning of the cycle the rising edge of a clock pulse sets the value of the inverted output $\overline{Q}$ of the flip-flop circuit F2 to 0 and at the same time a 0-level pulse is started in the pulse-width-modulated switching pulse train. If the switched-mode power supply is operating normally and not transiting to continuous mode operation, switch S1 is non-conductive at the beginning of the cycle and, so, the level is 0 also at the output of the demagnetization time simulation circuit 16. As a result of the logic NOR function, gate 20 switches FET Q1 into conductive state through control circuit 21. When the pulse from PWM circuit 3524 rises to level 1 or when one of the current measuring amplifiers A1, A3 detects that primary current has reached its peak value and resets the flip-flop circuit F2, the logic NOR gate 20 receives one 1-level input and switches FET Q1 into non-conductive state through control circuit 21. So, the event that occurs first ends the conduction of FET Q1.

It is possible, particularly when the output voltage is relatively low, that a flyback type switched-mode power supply starts to operate in a so-called continuous mode. This can happen, for example, as a result of a short-circuit between output terminals or if a wholly discharged battery is connected to the charging device. Continuous mode operation means that the transformer T1 is not completely demagnetized when FET Q1 is switched back ON. In prior art systems, this may lead to very high primary and secondary currents and thus damage the components or conductors. Furthermore, in continuous mode operation, the current limiting algorithm described above will not function properly. By bringing an output from the demagnetization time simulation circuit 16, in which logic level 1 corresponds to conduction time t_S of switch S1, as an input to NOR gate 20 in the manner described above, it is possible to limit the continuous mode output current, but in order for the circuit according to the invention to completely prevent the switched-mode power supply from entering the continuous mode, it includes an anti-continuous mode block 17, hereinafter referred to as the ACM block. Next it will be described the structure and operation of this block in the embodiment illustrated by Figs. 7a and 8.

Start of cycle, i.e. switching of FET Q1 ON, occurs at the rising edge of the clock pulse controlling the operation of the system. In the embodiment of Figs. 7a to 8, the clock pulse is generated by an appropriate block in the PWM circuit 3524. If the power supply were operating in continuous mode, said rising edge of clock pulse would occur during the conduction time t_D of diode D1 in the secondary, which is the same as conduction time t_S

of switch S1, presuming that there is no delay between said conduction times. The ACM block 17 used in the circuit according to the invention includes a logic AND gate which in the embodiment of Fig. 7a comprises a PNP transistor pair 18 and resistors R20 to R23 and the inputs of which are said clock pulse controlling the operation of the system and the gate voltage of the switching transistor S1. A positive gate voltage naturally means that the switching transistor S1 is conductive. Said logic AND gate 18, R20-R23 issues an output signal "1", i.e. a positive voltage signal if the clock pulse is positive simultaneously with the positive gate voltage, or the conduction time t_S, of the switching transistor S1. The output of said logic AND gate is connected to switch S2, which is advantageously a transistor, as in the embodiment of Fig. 7a, in which case said output is connected so as to serve as its gate voltage. Between the gate of said transistor S2 and the ground potential there is a relatively high resistance so that a positive gate voltage pulse keeps said transistor conductive for a time of sufficient duration.

When said switch S2 is in conductive state, it provides a current path between the terminals of an external capacitor C_{ext}. This current path includes advantageously a series resistor, resistor R_{ACM} in Fig. 7a, the resistance value of which provides a means to control the capacitor discharging effect of the current path. If said logic AND gate 18, R20-R23 produces a positive signal, capacitor C_{ext} loses its charge through said current path S2, R_{ACM}, wherefore a differential amplifier A1 sends to control circuit F1 a signal which causes FET Q1 to be switched OFF according to the operating principle described above. The structure and operation of the ACM block 17 described above have the advantage that, in a way, the block is "ahead of the time", which means that it starts to limit the ON time of FET Q1 before the switched-mode power supply would enter the continuous mode. This is due to the fact that the signal taken as a second input to the ACM block 17 which represents the conduction time t_S of switch S1 and which is compared to the clock pulse marking the start of the next cycle, is slightly behind the conduction time t_D of diode D1, due to delays in the circuit.

Next it will be discussed the limitation of the output voltage of a switched-mode power supply in a method and circuit according to the invention. The additional winding 13 in transformer T1 is used also for this purpose. In the method and circuit according to the invention, an image voltage is generated for the output voltage U_{OUT} of the switched-mode power supply using a method shown in Fig. 3b, based on the obvious development of a known method described above in connection with the prior art. The image voltage is generated using a low-pass filter, which in the embodiment of Fig. 7a comprises a coupling of resistor R5 and capacitor C3 connected in series and a diode D3 connected to this coupling. The low-pass filter R5, C3 is connected in parallel with the additional winding 13 so as to eliminate the effect of sudden voltage spikes induced in the additional winding. The anode of diode D3 is connected in the middle of said low-pass filter, between resistor R5 and capacitor C3, and its cathode is connected via capacitor C4 to the ground potential. So, the cathode of diode D3, marked as B, shows an image voltage U_b the behaviour of which as a function of the output current I_{OUT} of the switched-mode power supply is shown graphically in Fig. 4.

However, in the method and circuit according to the invention, the image voltage U_b is not taken directly to the differential amplifier controlling the operation of the PWM circuit, as described above in connection with the discussion about the prior art and the obvious development related to it, referring to Fig. 3b. According to the invention, a linear combination is produced of said image voltage U_b and the aforementioned first reference voltage U_{ext} since these two voltages undergo a change that is substantially similar but of the opposite sign, as a function of the output current I_{OUT} of the switched-mode power supply. In the embodiment of Fig. 7a, said linear combination is produced using a two-input resistor network comprising resistors R11 to R14. Resistors R11 and R12 constitute a series connection which is the series resistance of the first input and through which the image voltage U_b is connected to said resistor network. Resistor R13 is the series resistance of the second input through which said first reference voltage U_{ext} is connected to said resistor network. Ends of the series resistances of said first input and second input are connected together at point C and resistor R14 is connected to the ground potential through this point. Voltage U_1 at point C is a linear combination of voltages U_{ext} and U_b, or

$$U_1 = mU_b + nU_{ext}, \qquad (10)$$

where constants m and n depend on the resistances of resistors R11 to R14. The embodiment of Fig. 7a also includes an amplifier A5, the amplification of which is advantageously 1 and the purpose of which is to prevent the voltage signals from being connected back from point C to the current regulating system which was described above and which is based on the voltage across the external capacitor C_{ext}. Voltage U_1 is taken to a differential amplifier A4 which controls the operation of the PWM circuit and which in the embodiment of Fig. 7a is included in PWM circuit 3524. Amplifier A4 compares voltage U_1 to a third reference voltage U_{ref3} which is generated by a voltage divider comprising resistors R15 and R16. PWM circuit 3524 uses the output signal of said differential amplifier to control the pulse ratio when generating FET Q1 switching pulses taken to control circuit F1. This is normal operation of a known, commercially available PWM circuit and therefore it is not described in further detail here.

In addition to the parts described above, the embodiment of the circuit according to the invention, illustrated in Fig. 7a, includes other parts which are known but the operation of which is related to the stabi-

lization of the output characteristics of the switched-mode power supply and which therefore will be described below. To limit said first reference voltage U_{ext} below a certain maximum value, a limiter circuit is used comprising a PNP transistor Q2 and resistors R17 and R18. Said resistors constitute a voltage dividing coupling between the +5V potential and ground potential, and there is a connection from a point between them to the base of said transistor Q2. The emitter of transistor Q2 is connected to the positive side of the external capacitor C_{ext}, and its collector is connected to the ground potential.

The embodiment of Fig. 7a also includes a relatively high-resistance compensating coupling R19 connected between point B (cathode of the image voltage rectifying diode, or the point at which image voltage U_b appears) and the positive side of the external capacitor C_{ext}. In the mathematical discussion of the first reference voltage U_{ext} above it was implied that there is no delay in the circuit between diode D1 of the secondary and the switching operation of switch S1. As a matter of fact, there is always a small delay between them, and therefore the conduction time t_S of switch S1 is a little too long with a high output voltage of the switched-mode power supply, which results in that the output current I_{OUT} increases when the output voltage U_{OUT} drops. If a voltage proportional to the output voltage U_{OUT} is used to produce a small additional charge in capacitor C_{ext}, it is possible to compensate for the capacitor overdischarge which is caused by the excessive conduction time of switch S1 with a high output voltage U_{OUT}. The image voltage U_b is suitably proportional to the output voltage, so by arranging a relatively high-resistance compensating coupling from it to the capacitor C_{ext} in the manner described above a desired stabilizing effect is achieved.

In above descriptions and especially in Fig. 7a the circuit according to the invention was regarded as a whole constituted by discrete components. However, there is a strong tendency in modem electronic equipment towards integration, with all applicable components realized within one integrated circuit, or IC. Fig. 10 shows an embodiment of the present invention in which most of the components and blocks that were shown discrete in Figs. 7a and 8 are realized as one application specific integrated circuit, or ASIC. For the sake of clarity, some of the lines describing connections have been left out in Fig. 10 and many of the component groups are shown only as functional blocks, but in principle the structure and operation of the coupling is the same as in the embodiment of Fig. 7a. In Fig. 10, components that are not included in the ASIC are either too big to fit in or intended to be easily replaceable so that the circuit characteristics can be altered according to the use. The embodiment shown in Fig. 10 only serves illustrative purposes and is by no means the only possible ASIC implementation of the method and circuit according to the invention. It is obvious to a person skilled in the art that many different ASIC applications can be realized within the scope of the claims set forth below.

Above it was described the use of the method and circuit according to the invention in a situation in which the transformer of the switched-mode power supply comprises three windings. However, the method and circuit according to the invention can with minor modifications be implemented using a two-coil transformer. Then the demagnetization information and generation of image voltage occur in a circuit connected directly in parallel with the primary winding. The two-coil solution requires certain safety measures to prevent the high primary power from being directly connected to the demagnetization information and image voltage circuits dimensioned for small signals. In an ASIC circuit this means that inside the circuit there must be a greater number of relatively wide isolation zones, which require space, and therefore the embodiment discussed above is considered better for the time being. In any case, it is possible to apply the method according to the invention to a switched-mode power supply employing a two-coil transformer.

Next it will be discussed only the method according to the invention to control the output characteristics of a switched-mode power supply with reference to Fig. 9 and without directly referring to any particular physical embodiment. The method comprises several operations applied simultaneously, so it is impossible to present an accurate temporal order.

The method according to the invention, illustrated by Fig. 9, realizes all the measures described above in connection with the descriptions of the physical embodiments. Rectangular blocks depict functional steps of the method and designations in oval frames clarify the type and meaning of information transferred in the form of signals or pulses or in other ways.

In the method according to the invention, output current limiting includes at least the following steps:

- current flowing through the primary current switching element, or power FET, is measured 100 and the measurement result is converted to a voltage value,
- a first reference voltage is generated 101 on the basis of information 102 about the beginning and end of demagnetization,
- said voltage value representing the current through the switching element is compared 103 to said first reference voltage, and
- the result from said comparison is used for dimensioning the primary current switch control pulses such that if said voltage value representing the current through the switching element indicates that the current exceeds a certain limit value, the control pulses will be shortened 104 in order to decrease the current.

In addition, output current limiting may include the following steps:

- said first reference voltage is compensated for with a small compensating signal 105 the size of which is proportional to an image voltage generated from the secondary voltage of the switched-mode power supply,
- said first reference voltage is further compensated for by altering its value so that if the simultaneousness of the clock pulse 110 and demagnetization time signal 102 indicates 111 that the switched-mode power supply is about to enter continuous mode operation, the value of the first reference voltage is changed 106 such that it causes the shortening of the switching pulses of the switching element,
- said first reference voltage is further compensated for with a limiter circuit which limits it below a certain maximum value (not shown in Fig. 9), and
- said voltage value representing the current through the switching element is compared to a fixed second reference voltage (not shown in Fig. 9) and the result from the comparison is used in the same way as the result from said first comparison.

In the method according to the invention, the switched-mode power supply output voltage control includes at least the following steps:

- an image voltage is generated 107 that corresponds to the voltage of the secondary winding in the switched-mode power supply,
- a combination is produced 108 of said image voltage and the first reference voltage mentioned above, and
- a pulse-width-modulated pulse train is produced 109 on the basis of said combination in order to switch the primary current switching element.

In the method according to the invention, the switched-mode power supply output voltage control may further include the following steps:

- said image voltage is compensated for by removing from it unwanted phenomena such as sudden voltage spikes, and
- said linear combination is compared to a third reference voltage in order to produce 109 a pulse-width-modulated pulse train.

The method and circuit according to the invention are suitable for producing a very stable switched-mode power supply output voltage U_{OUT} as a function of the output current I_{OUT}, as can be seen from Fig. 6, which for the sake of comparison also shows the first reference voltage U_{ext} across capacitor C_{ext}. The solution is very simple which means operational reliability, small manufacturing costs and good throughput in mass production. The method and circuit according to the invention eliminate the need for sandwich-type transformers or otherwise complex inductive elements, and the circuit has no need for opto-isolated connections between the primary and the secondary.

Claims

1. A circuit to control the output current and output voltage in a switched-mode power supply that comprises a transformer (T1) equipped with primary and secondary windings (11, 12, 13) through which power is transferred from the primary to the secondary, and a first switching element (Q1) on the primary side to interrupt the primary current (I_p) flowing through the primary winding (11) of said transformer, which circuit comprises on the primary side

   - a control circuit (F1) to regulate the output voltage of the power supply by means of pulse width modulation by adjusting the pulse ratio of the switching pulses of said first switching element (Q1),
   - means (14, S1, R_S, C_{ext}) for producing a first reference voltage (U_{ext}), and
   - means (D2, R2, C2, I_a, R5, D3, C3, C4) for producing a first voltage signal (U_b),

   characterized in that
   it further comprises on the primary side means (R11-R14) for producing a combination of said first reference voltage (U_{ext}) and first voltage signal (U_b) and for taking said combination to said control circuit (F1) in order to produce said switching pulses.

2. The circuit of claim 1, **characterized** in that to produce said combination it comprises a two-input resistor network (R11-R14) wherein said first reference voltage (U_{ext}) is substantially connected to the first input and said first voltage signal (U_b) is substantially connected to the second input.

3. The circuit of claim 1 or 2, **characterized** in that it comprises means (R_S; R7-R10) for measuring the current flowing through said first switching element (Q1) and for converting it to a second voltage signal.

4. The circuit of claim 3, **characterized** in that it comprises means (A1) for comparing said second voltage signal to said first reference voltage (U_{ext}) and for taking the signal representing the result from said comparison to said control circuit (F1).

5. The circuit of any one of the preceding claims, **characterized** in that it comprises means for producing an image voltage which represents the voltage of the secondary winding in said transformer (T1) and which substantially is said first voltage signal (U_b).

6. The circuit of claim 5, **characterized** in that in addition to a primary winding (11) and secondary winding (12) said transformer (T1) includes an additional winding (13) to produce said image voltage and first voltage signal (U_b).

7. The circuit of any one of the preceding claims, **characterized** in that it comprises means (17) for preventing continuous mode operation of the switched-mode power supply.

8. The circuit of claim 7, **characterized** in that it comprises on the secondary side a secondary diode (D1) and that said means (17) for preventing continuous mode operation of the switched-mode power supply comprises a comparison element (18) for comparing the signal, which indicates conduction of said secondary diode (D1), with the clock signal controlling the operation of said circuit.

9. The circuit of any one of the preceding claims, **characterized** in that it comprises means (R19) for conducting a compensating signal between said first voltage signal (U_b) and said first reference voltage (U_{ext}).

10. The circuit of any one of the preceding claims, **characterized** in that it comprises means (R24, R25, A3) for producing a second reference voltage (U_{ref2}) and for comparing said second voltage signal to said second reference voltage (U_{ref2}) and for taking the signal representing the result from said comparison to said control circuit (F1).

11. The circuit of any one of the preceding claims, **characterized** in that it comprises means (R7-R10) for eliminating disturbances caused by variations in the input voltage from the result of the measurement of the current (I_p) flowing through said first switching element (Q1).

12. The circuit of any one of the preceding claims, **characterized** in that it comprises means (A5) for preventing a back coupling from the part where said combination is generated to the part where said first reference voltage (U_{ext}) is generated.

13. The circuit of any one of the preceding claims, **characterized** in that it comprises means (Q2, R17, R18) for limiting said first reference voltage (U_{ext}) below a predetermined maximum value.

14. A method for controlling the output current and output voltage of a switched-mode power supply in which power is transferred by means of a transformer from the primary to the secondary, a switching element is switched on the primary side, and the output voltage is controlled by means of changing the pulse ratio of the switching pulses of said switching element, and wherein, on the primary side of the switched-mode power supply,

- a first reference voltage is produced and
- a first voltage signal is produced,

characterized in that also on the primary side

- a combination is produced of said first voltage signal and said first reference voltage and
- on the basis of said combination, said switching pulses are generated in order to switch the primary current switching element.

15. The method of claim 14, **characterized** in that said combination is compared to a third reference voltage in order to produce said switching pulses.

16. The method of claim 14, **characterized** in that said combination is a linear combination.

17. The method of any one of claims 14 to 16, **characterized** in that in it the primary current of the switched-mode power supply is measured, the measurement result is compared to said first reference voltage, and the result from said comparison is used for controlling said switching element.

18. The method of claim 17, **characterized** in that when said comparison indicates that said primary current is greater than a predetermined maximum value, the switching pulses of said switching element are shortened.

19. The method of claim 18, **characterized** in that the switching pulses are shortened with different components than those used to produce a pulse-width-modulated switching pulse train.

20. The method of any one of claims 14 to 19, **characterized** in that in it information is produced about the start and end times of demagnetization of the transformer in the switched-mode power supply and said first voltage signal is produced on the basis of said information and said first voltage signal represents the secondary voltage of the switched-mode power supply transformer.

21. The method of any one of claims 14 to 20, **characterized** in that if the switched-mode power supply is about to enter continuous mode operation, the value of said first reference voltage is changed such that it causes the switching pulses of the switching element to be shortened.

22. The method of any one of claims 14 to 21, **characterized** in that between the generation of said first voltage signal and the generation of said combination said first voltage signal is shaped in order to

produce better correspondence between it and said secondary voltage.

23. The method of claim 22, **characterized** in that said shaping is realized as low-pass filtering.

24. The method of any one of claims 20 to 23, **characterized** in that the information about the end of transformer demagnetization is produced by comparing the voltage across one winding of the transformer to a substantially constant voltage.

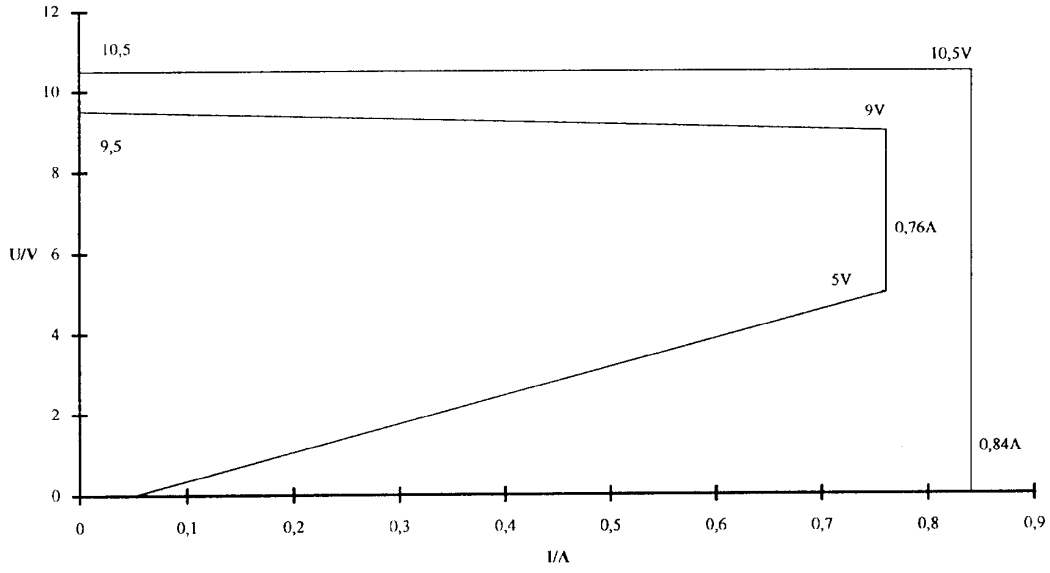
12
10
8
6
4
2
0
U/V
10,5
10,5V
9V
9,5
0,76A
5V
0,84A
0
0,1
0,2
0,3
0,4
0,5
0,6
0,7
0,8
0,9
I/A

Fig. 1

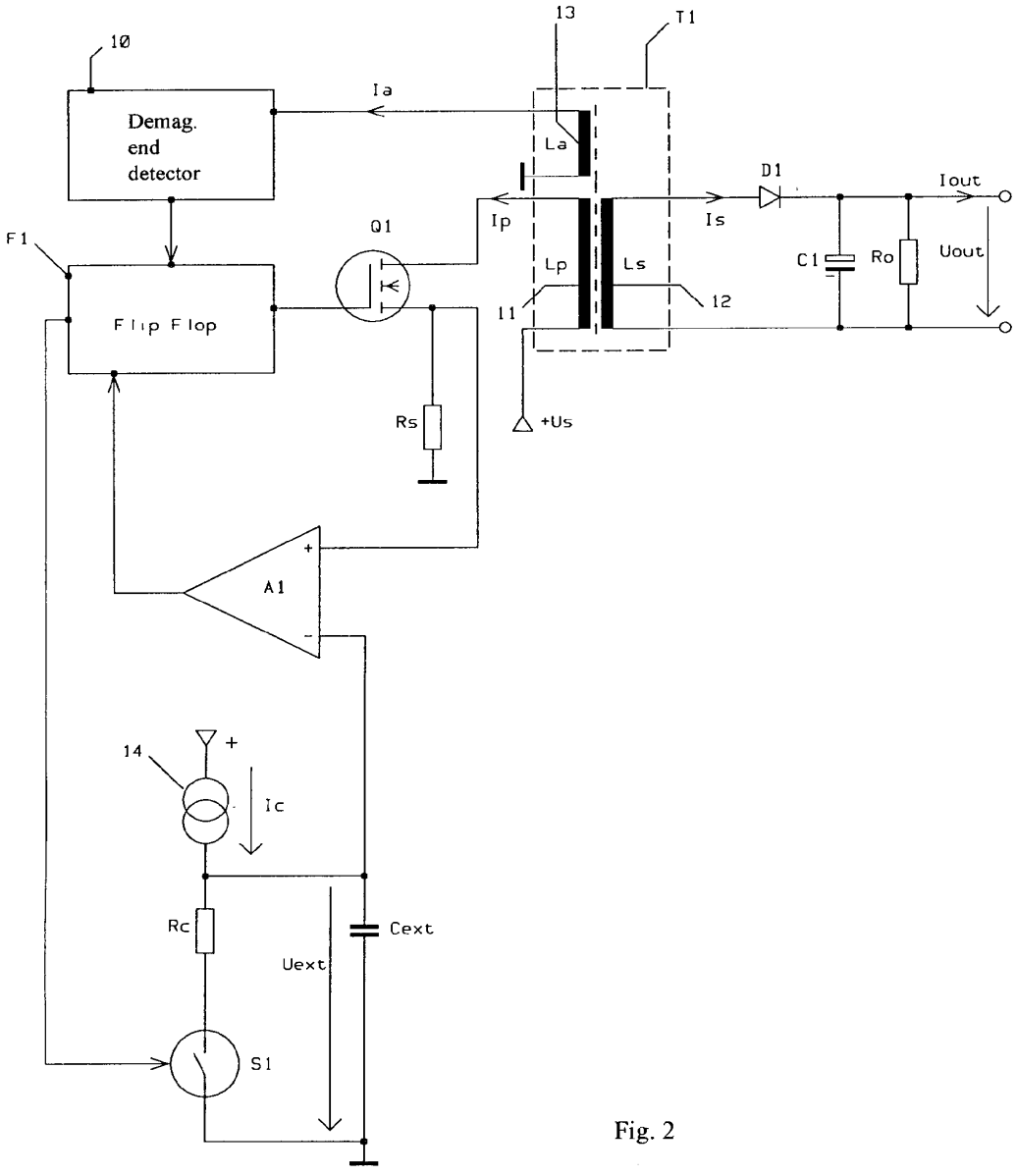
10
Demag.
end
detector
Ia
13
T1
La
D1
Iout
Ip
Is
Q1
F1
Flip Flop
Lp
Ls
C1
Ro
Uout
11
12
Rs
+Us
A1
14
Ic
Rc
Cext
Uext
S1

Fig. 2

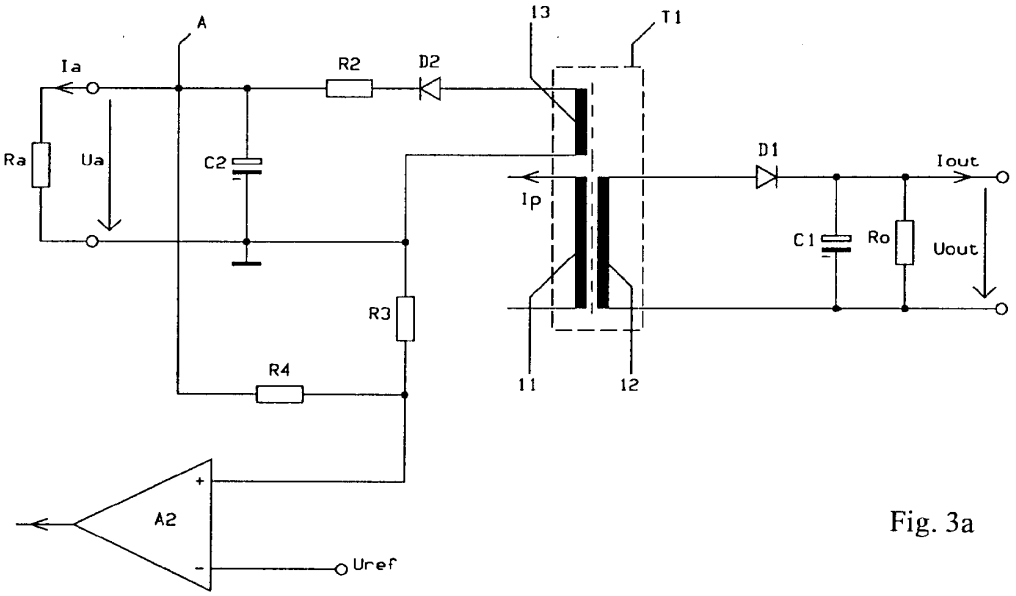
A
Ia
R2
D2
13
T1
Ra
Ua
C2
D1
Iout
Ip
C1
Ro
Uout
R3
R4
11
12
A2
Uref

Fig. 3a

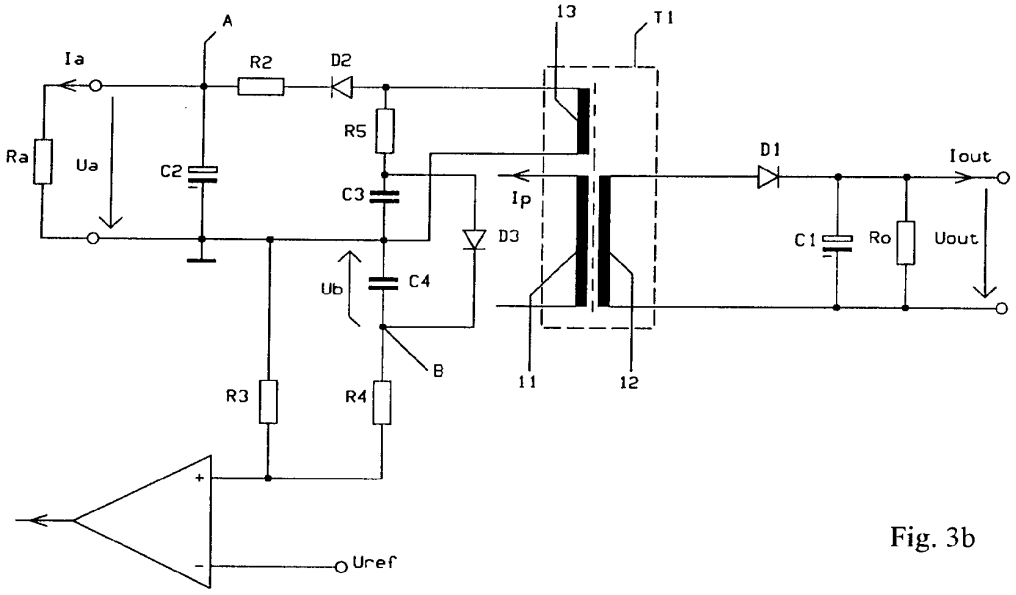
A
Ia
R2
D2
13
T1
R5
Ra
Ua
C2
C3
D1
Iout
Ip
D3
C1
Ro
Uout
Ub
C4
B
R3
R4
11
12
Uref

Fig. 3b

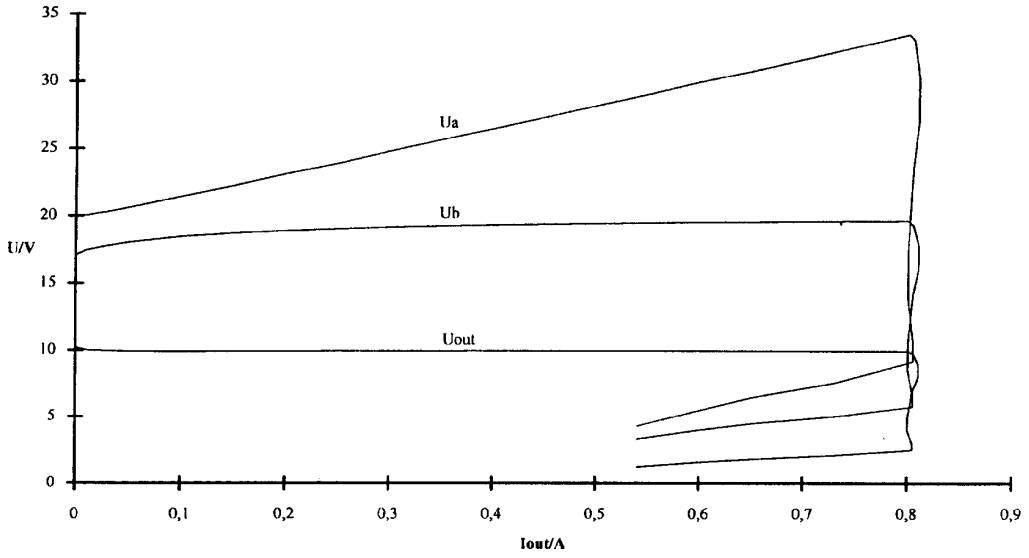

Fig. 4

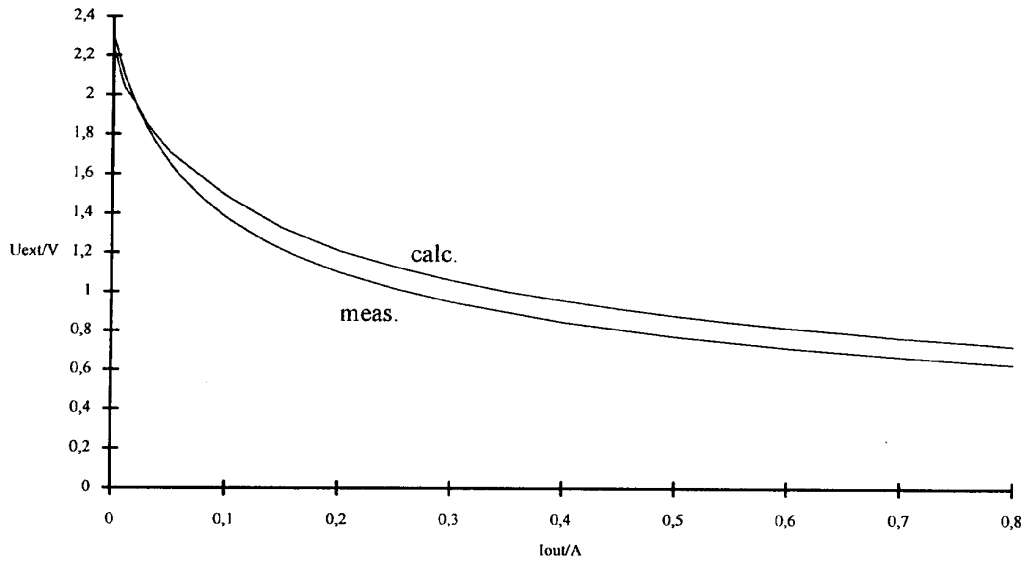
2,4
2,2
2
1,8
1,6
1,4
Uext/V 1,2
1
0,8
0,6
0,4
0,2
0
calc.
meas.
0
0,1
0,2
0,3
0,4
0,5
0,6
0,7
0,8
Iout/A

Fig. 5

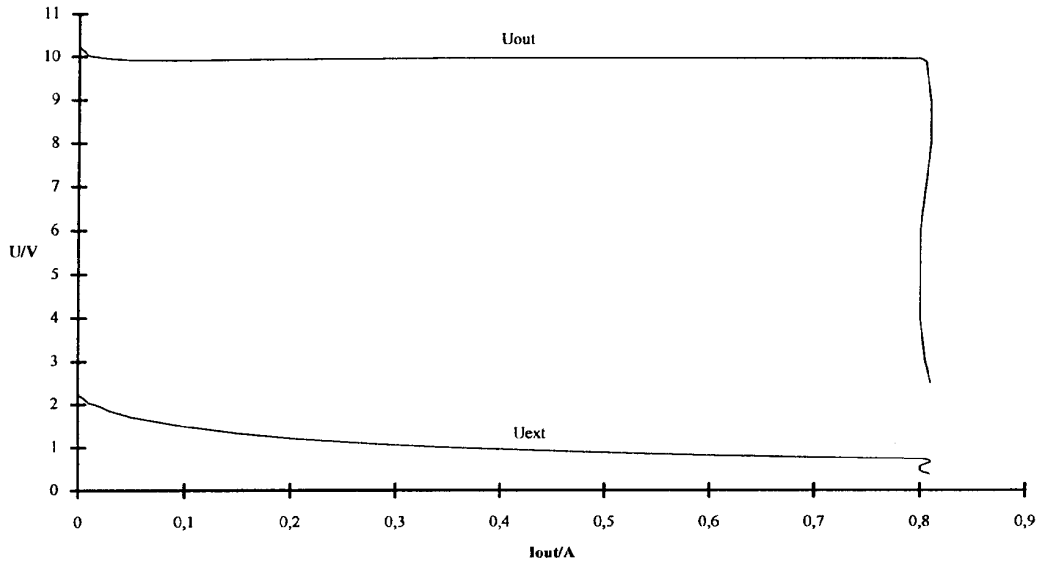

Fig. 6

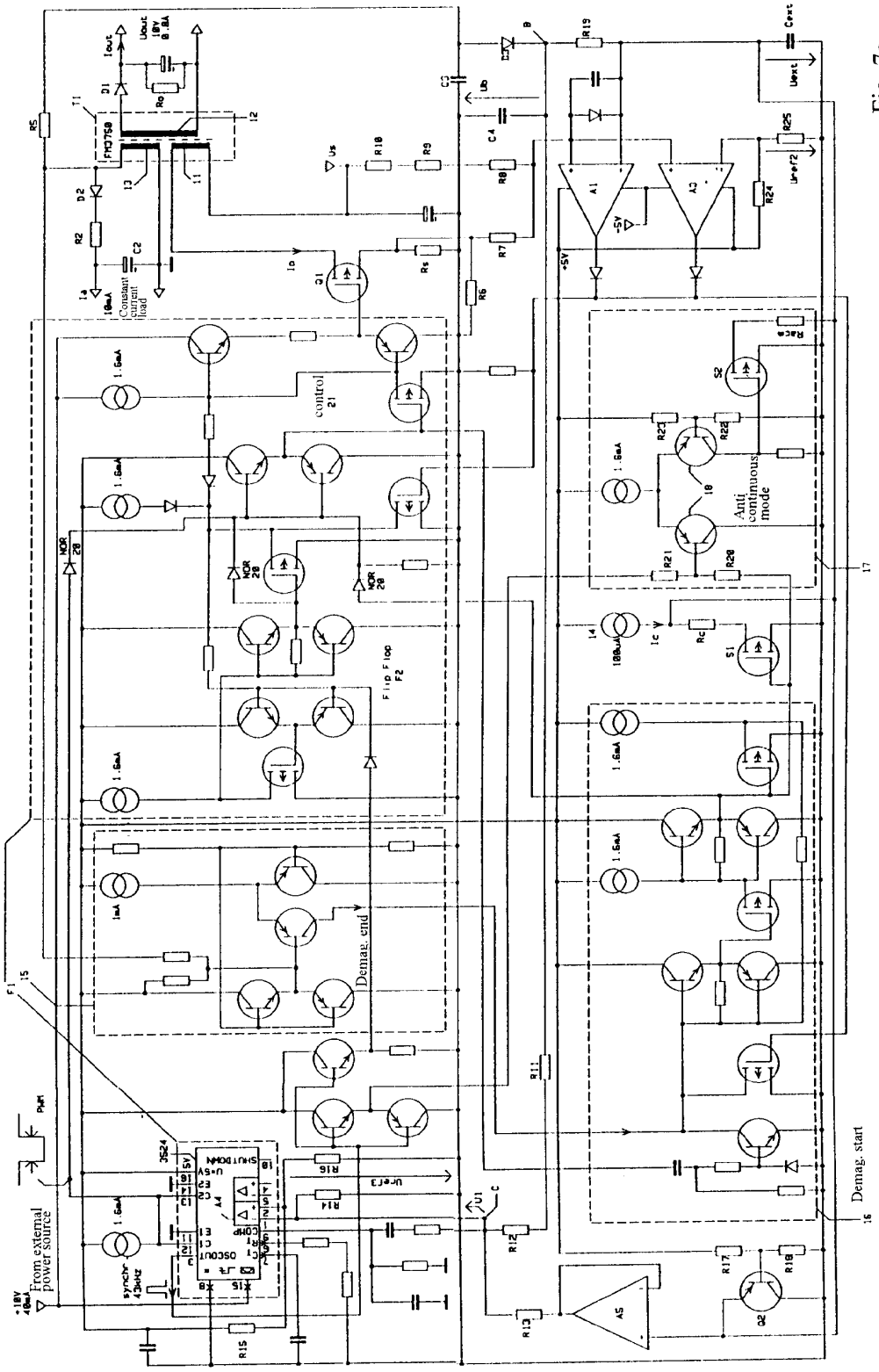
From external power source
control
21
Anti continuous mode
Demag. end
Demag. start
Constant current load
Flip Flop F2
SHUTDOWN
OSCOUT
COMP
synchr 43kHz
3524

Fig. 7a

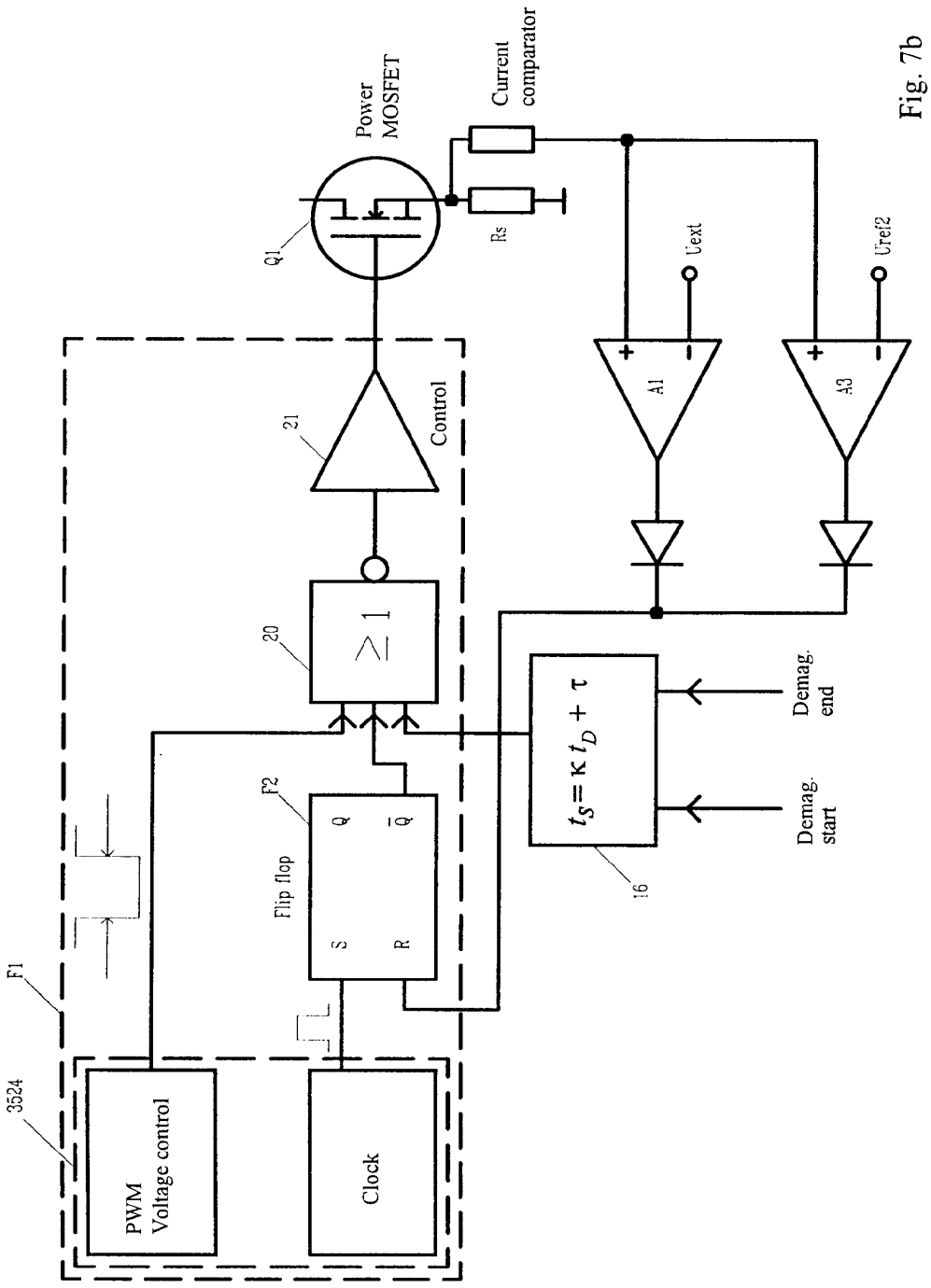
Power MOSFET
Current comparator
Q1
Rs
Uext
Uref2
A1
A3
21
Control
20
≥ 1
$t_S = \kappa t_D + \tau$
Demag. end
Demag. start
16
F2
Flip flop
Q
$\bar{Q}$
S
R
F1
3524
PWM Voltage control
Clock

Fig. 7b

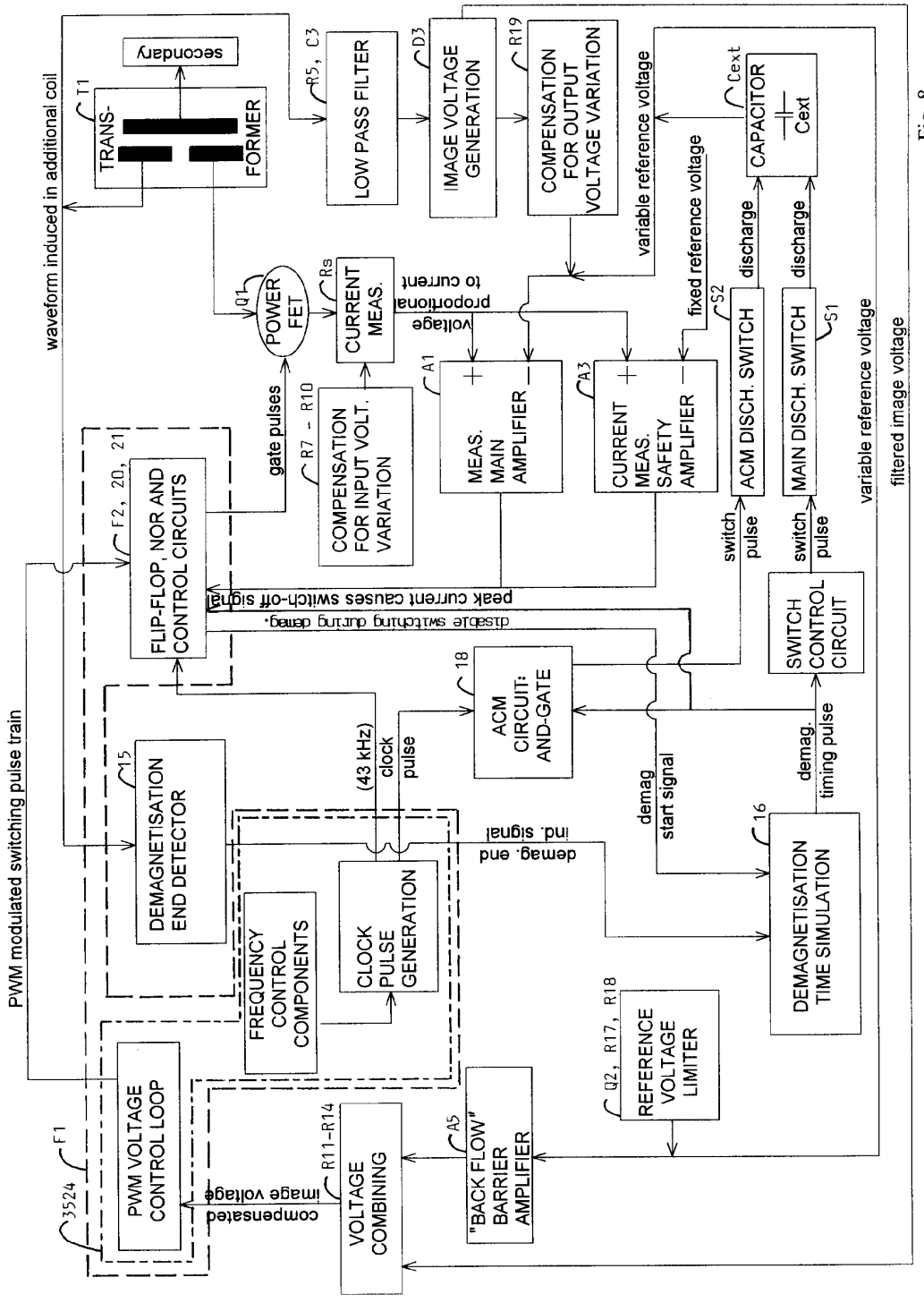
PWM modulated switching pulse train
waveform induced in additional coil
secondary
TRANS-
FORMER
T1
R5, C3
LOW PASS FILTER
D3
IMAGE VOLTAGE GENERATION
R19
COMPENSATION FOR OUTPUT VOLTAGE VARIATION
variable reference voltage
Cext
CAPACITOR
Cext
fixed reference voltage
discharge
discharge
S2
S1
Q1
POWER FET
Rs
CURRENT MEAS.
voltage proportional to current
A1
MEAS. MAIN AMPLIFIER
A3
CURRENT MEAS. SAFETY AMPLIFIER
ACM DISCH. SWITCH
MAIN DISCH. SWITCH
gate pulses
R7 - R10
COMPENSATION FOR INPUT VOLT. VARIATION
F2, 20, 21
FLIP-FLOP, NOR AND CONTROL CIRCUITS
peak current causes switch-off signal
disable switching during demag.
switch pulse
switch pulse
SWITCH CONTROL CIRCUIT
variable reference voltage
filtered image voltage
18
ACM CIRCUIT: AND-GATE
15
DEMAGNETISATION END DETECTOR
(43 kHz) clock pulse
demag start signal
demag. timing pulse
demag. end ind. signal
16
DEMAGNETISATION TIME SIMULATION
FREQUENCY CONTROL COMPONENTS
CLOCK PULSE GENERATION
Q2, R17, R18
REFERENCE VOLTAGE LIMITER
F1
3524
PWM VOLTAGE CONTROL LOOP
compensated image voltage
R11-R14
VOLTAGE COMBINING
A5
"BACK FLOW" BARRIER AMPLIFIER

Fig. 8

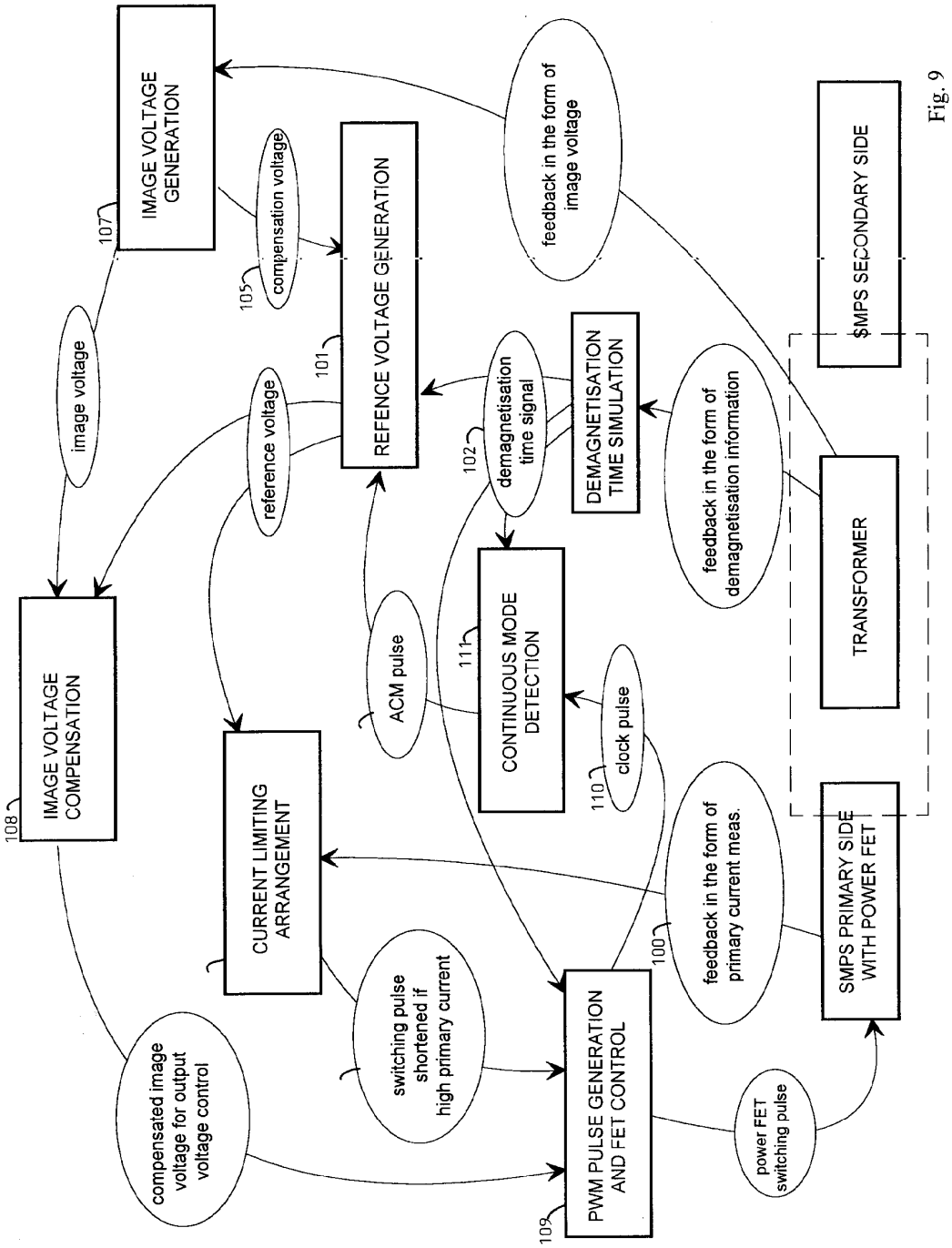
IMAGE VOLTAGE GENERATION
107
compensation voltage
105
REFENCE VOLTAGE GENERATION
101
feedback in the form of image voltage
SMPS SECONDARY SIDE
image voltage
reference voltage
demagnetisation time signal
102
DEMAGNETISATION TIME SIMULATION
feedback in the form of demagnetisation information
IMAGE VOLTAGE COMPENSATION
108
ACM pulse
CONTINUOUS MODE DETECTION
111
clock pulse
110
TRANSFORMER
CURRENT LIMITING ARRANGEMENT
feedback in the form of primary current meas.
100
SMPS PRIMARY SIDE WITH POWER FET
compensated image voltage for output voltage control
switching pulse shortened if high primary current
PWM PULSE GENERATION AND FET CONTROL
109
power FET switching pulse

Fig. 9

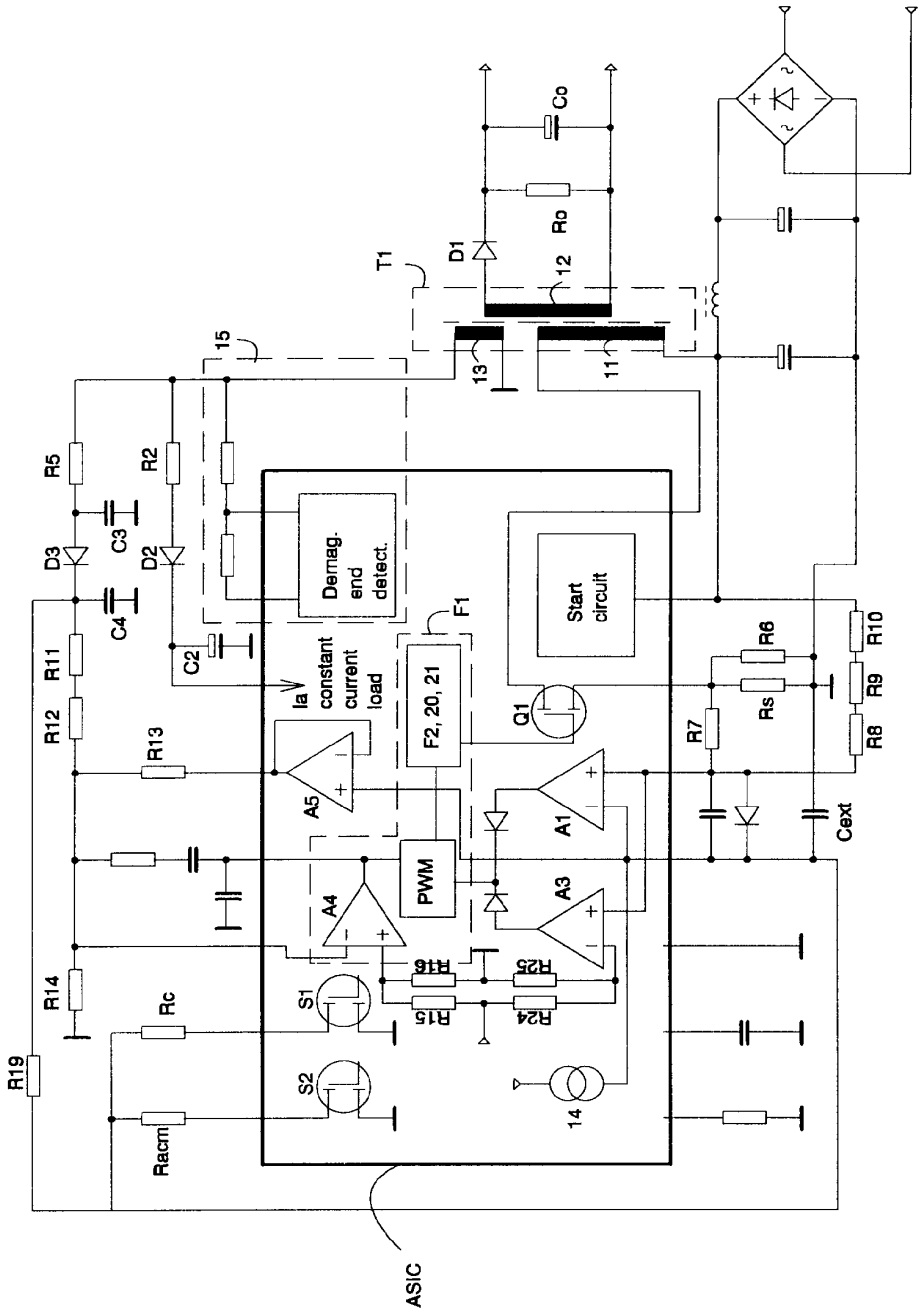
Co
Ro
D1
T1
12
15
13
11
R5
R2
C3
D3
D2
C4
C2
R11
R12
R13
R14
Rc
R19
Racm
S1
S2
Demag. end detect.
F1
F2, 20, 21
Start circuit
Ia
constant current load
A5
A1
A4
A3
PWM
R16
R25
R15
R24
Q1
R6
R10
R9
R8
R7
Rs
Cext
14
ASIC

Fig. 10

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 96 10 7637

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
Y	WO-A-95 09476 (SIEMENS) * page 3, line 25 - page 9, line 27; figures 1-7 *	1,3-6, 14-17, 20,24 2,19	H02M3/335
Y	DE-A-41 16 434 (CARL ZEISS JENA) * column 3, line 3 - column 4, line 45; figure 1 *	1,3-6, 14-17, 20,24	
A	DE-A-43 10 513 (KLÖCKNER-MOELLER) * column 2, line 61 - column 4, line 29; figures 1,2 *	1,4-8, 10,14-19	
A	EP-A-0 420 997 (SIEMENS) * column 4, line 9 - column 6, line 38; figures 1-5 *	1,5-7, 14,20-24	
A	DE-A-41 30 576 (SIEMENS) * column 1, line 41 - column 4, line 47; figure 1 *	1-6,11, 14-19, 22,23	TECHNICAL FIELDS SEARCHED (Int.Cl.6) H02M
A	INTERNATIONAL CONFERENCE ON CONSUMER ELECTRONICS IEEE1991, 5 - 7 June 1991, ROSEMONT,ILLINOIS, pages 58-59, XP000288206 KIEFFER ET AL: "switch mode power supply,new concept" * the whole document *	1-7, 10-19	

-/--

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	29 August 1996	Calarasanu, P

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
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T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

EPO FORM 1503 03.82 (P04C01)

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 96 10 7637

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
A	REVUE GENERALE DE L'ELECTRICITÉ, no. 5, May 1992, PARIS, pages 117-123, XP000290747 LHERMITE: "un controleur d'alimentation fly-back avec controle efficace des surcharges" * the whole document * ---	1,5-8, 14, 17-21,23	
A	EIGHTH ANNUAL APPLIED POWER ELECTRONICS CONFERENCE AND EXPOSITION, 7 - 11 May 1993, SAN DIEGO,CALIFORNIA, pages 527-532, XP000357938 GASS ET ALL: * the whole document * -----		
			TECHNICAL FIELDS SEARCHED (Int.Cl.6)

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
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L : document cited for other reasons

& : member of the same patent family, corresponding document

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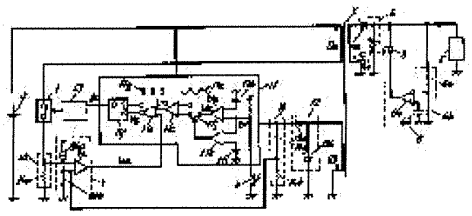
(54) SWITCHING POWER SUPPLY DEVICE

(57)Abstract:

PROBLEM TO BE SOLVED: To supply a switching power supply device with constant-current output characteristics for reducing cost and size by eliminating the need for a secondary output current error detection circuit and making equal output constant-current characteristics and eddy current protection characteristics.



SOLUTION: A switching element 1 and a current detection circuit 10 for converting current flowing through the switching element 1 and for outputting it are connected in series via a primary winding 2a of a transformer 2. Further, the output of the current detection circuit 10 is connected to the first input terminal of a comparator 9a and a serially-connected circuit of a diode and a capacitor is connected in parallel between the output of an output voltage monitoring circuit 14 for converting a voltage obtained by rectifying and smoothing a second primary winding 2b of the transformer 2 where a voltage

proportional to the secondary winding voltage 2c of the transformer 2 is generated and the primary winding 2b of the transformer 2 at the second input terminal of the above comparator 9a.

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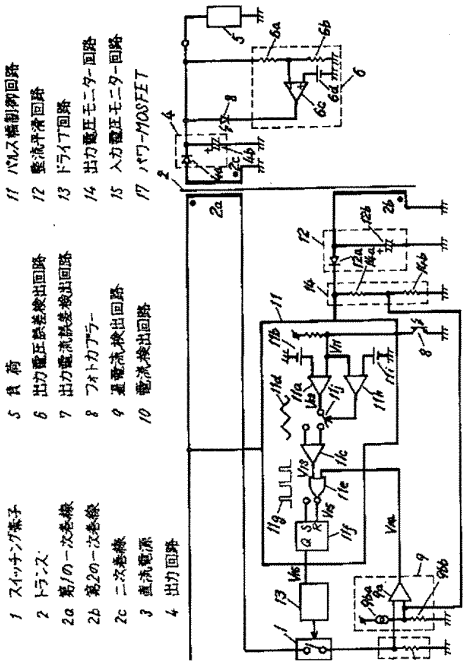
(54)【発明の名称】　スイッチング電源装置

(57)【要約】

【目的】　２次出力電流誤差検出回路が不要であり、出力定電流特性と過電流保護特性を同一特性にすることにより低コスト、小型化可能な定電流出力特性を具備するスイッチング電源装置を提供することを目的とする。

【構成】　トランス２の第１の一次巻線２ａを介してスイッチング素子１とスイッチング素子１を流れる電流を電圧信号に変換して出力する電流検出回路１０を直列に接続し、電流検出回路１０の出力を比較器９ａの第１の入力端子に接続し前比較器９ａの第２の入力端子にはトランス２の二次巻線電圧２ｃに比例した電圧が発生するトランス２の第２の一次巻線２ｂを整流平滑して得られる電圧を電流信号に変換する出力電圧モニター回路１４の出力とトランス２の第２の一次巻線２ｂ間にダイオードとコンデンサの直列接続回路を並列接続した構成からなる。



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【特許請求の範囲】

【請求項１】　トランスの第１の一次巻線を介してスイッチング素子と前記スイッチング素子を流れる電流を電圧信号に変換して出力する電流検出回路を直列に接続し、前記電流検出回路の出力を比較器の第１の入力端子に接続し前記比較器の第２の入力端子には前記トランスの二次巻線電圧に比例した電圧が発生する前記トランスの第２の一次巻線電圧を整流平滑して得られる電圧を電流信号に変換する手段の出力を接続し、前記比較器の出力は前記スイッチング素子のオン・オフを制御するパルス幅制御回路に接続されたスイッチング電源装置。

【請求項２】　トランスの第２の一次巻線間にダイオードとコンデンサの直列接続回路を並列接続した構成からなる前記トランスの第１の一次巻線に与えられる直流入力電圧に比例した電圧を電流信号に変換する手段の出力が比較器の第２の入力端子に接続された請求項１記載のスイッチング電源装置。

【請求項３】　スイッチング素子をＭＯＳＦＥＴとし前記ＭＯＳＦＥＴの単位セルの一部分を第２のソース電極とし前記第２のソース電極と電流検出回路を直列に接続した請求項１または請求項２記載のスイッチング電源装置。

【発明の詳細な説明】

【０００１】

【産業上の利用分野】本発明は出力に定電圧特性と定電流特性とを有するスイッチング電源装置に関するものである。

【０００２】

【従来の技術】近年、パソコンやビデオカメラ等のバッテリーを電源とする機器は低価格化とともに小型・軽量化が進みどこへでも持ち運びが可能となり普及している。これに伴いバッテリーを充電する出力特性すなわち定電流出力特性と機器に電力を供給する出力特性すなわち定電圧出力特性を備えたスイッチング電源装置に対しても低コスト化、小型・軽量化が求められている。

【０００３】以下図面を参照しながら従来のスイッチング電源装置の一例について説明する。

【０００４】図５は、従来のスイッチング電源装置の回路構成図である。図５において、１はバイポーラトランジスタあるいは電界効果トランジスタ等により構成されるスイッチング素子であり、２は電力変換用のトランスであり２ａは第１の一次巻線、２ｂは第２の一次巻線、２ｃは二次巻線であり、３は商用交流電源を整流平滑するなどして得られる直流電源であり、４は２次整流ダイオード４ａ、２次平滑コンデンサ４ｂからなる出力回路であり、５は負荷であり、直流電源３からトランス２の第１の一次巻線２ａを介して与えられる直流電力をスイッチング素子１によりスイッチングしそのスイッチング出力をトランス２の第１の一次巻線２ａから二次巻線２

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て整流平滑し、直流電力として負荷５に供給する。

【０００５】６は出力電圧誤差検出回路であり、負荷５に供給される出力電圧Ｖｏを抵抗６ａ、６ｂによって分圧し誤差増幅器６ｃの第１の入力端子に入力し、第２の入力端子に入力される基準電圧源６ｄとの誤差分を増幅しダイオード６ｅ、フォトカプラー８を介してパルス幅制御回路１１に出力する。

【０００６】７は出力電流誤差検出回路であり、負荷５に供給される出力電流Ｉｏを抵抗７ａにより電圧信号に変換し誤差増幅器７ｂの第１の入力端子に入力し、第２の入力端子に入力される基準電圧源７ｃとの誤差分を増幅しダイオード７ｄ、フォトカプラー８を介してパルス幅制御回路１１に出力する。

【０００７】９は過電流検出回路であり、スイッチング素子１に流れる電流を抵抗１０ａにより電圧信号に変換する電流検出回路１０の出力を比較器９ａの第１の入力端子に入力し、第２の入力端子に入力される基準電圧源９ｂと比較しその出力をパルス幅制御回路１１に出力する。

【０００８】パルス幅出力回路１１は、直流電源３または前記パルス幅制御回路１１が動作を開始すると前記トランス２の第２の一次巻線２ｂの電圧をダイオード１２ａ、コンデンサ１２ｂからなる整流平滑回路１２の出力を電源電圧とし、

（１）出力電流値Ｉｏ＜出力定電流値Ｉｏconstでは、

Io×R(7a)＜VREF(7c)

のため出力電流誤差検出回路７は動作しておらず、出力電圧誤差検出回路６のフォトカプラー８を介しての出力信号によりスイッチング素子１のオン・オフ時間を決定しその出力でドライブ回路１３を介してスイッチング素子１をスイッチングさせ出力電圧Ｖｏが一定となるすなわち定電圧出力特性となるようにスイッチング素子１のオン・オフ時間を制御する。

【０００９】但し、R(7a)は出力電流誤差検出回路７内の出力電流Ｉｏ検出用の抵抗７ａの抵抗値、VREF(7c)は出力電流誤差検出７内の誤差増幅器７ｂの第２の入力端子に接続される基準電圧源７ｃの電圧値である。

【００１０】図６は図５のスイッチング電源装置の出力特性である出力電流－出力電圧特性（以下Ｉ－Ｖ特性）を示し、この時は図中太線部Ａの特性となる。

【００１１】（２）次に、出力電流値Ｉｏ＝出力定電流値Ｉｏconstでは、

Io×R(7a)＝VREF(7c)

となり出力電流誤差検出回路７が動作を始めるため出力電圧Ｖｏが低下し出力電圧誤差検出回路６の動作が停止し、出力電流誤差検出回路７のフォトカプラー８を介しての出力信号によりスイッチング素子１のオン・オフ時間を決定しその出力でドライブ回路１３を介してスイッチ

ン・オフ時間を制御する。

【００１２】図６のＩ－Ｖ特性においては細線部Ｂの特性となる。

（３）又、スイッチング電源装置の異常時（例えば、図６においてトランス２の２次巻線２ｃの短絡又は出力電流誤差検出回路７の故障等）のスイッチング電源装置の保護及び負荷５に対する過電流保護はスイッチング素子１に直列に接続された前記スイッチング素子１を流れる電流を電圧信号に変換して出力する電流検出回路１０の出力Ｖ10が、

V10=R(10a)･I(1)limit

=V9REF

となると過電流検出回路９が動作し、過電流検出回路９の出力によりスイッチング素子１のオフを決定しドライブ回路１３を介してスイッチング素子１をオフする。

【００１３】但し、R(10a)は電流検出回路１０内の抵抗１０の抵抗値、I(1)limitは過電流検出回路９が動作する時のスイッチング素子１を流れる電流値、Ｖ9REFは過電流検出回路の比較器９ａの第２の入力端子に接続される基準電圧源９ｂの電圧値である。

【００１４】しかしながら、出力電力の最大時に必要なスイッチング素子１を流れる電流値をＩ(1)maxとすると、

Ｉ(1)limit＞Ｉ(1)max

であるため、図６においては点線部Ｃが出力過電流保護電流値Ｉolimit特性となる。

【００１５】

【発明が解決しようとする課題】前述のようにスイッチング電源装置の出力特性に定電圧特性と定電流特性を有するためには、

（１）出力電圧誤差検出回路６と出力電流誤差検出回路７とが必要であり誤差増幅器、基準電圧の比較的高価な部品が数多く必要となりそれに伴い誤差増幅器への入力手段を構成する部品数が多くなる。

（２）出力電流誤差検出回路７内に負荷５に供給される電流を検出するための手段として抵抗７ａが必要であり、このため抵抗７ａによる損失が大きく損失の低減がはかれない。

（３）さらに、スイッチング電源装置の過電流保護としてはスイッチング素子１を流れる電流が必ず、

Ｉ(1)limit＞Ｉ(1)max

となり図６のＩ－Ｖ特性の点線部Ｃの特性となるため、スイッチング素子１、２次整流ダイオード４ａ、トランス２等は出力過電流保護電流値Ｉolimitで設計しなければならず必要以上に大きな定格のものを使用することになる。

（４）熱設計に対しても前述の出力過電流保護電流値Ｉolimitで設計する必要があることからスイッチング電源装置として低コスト化、小型化が困難であるという課

【００１６】本発明は上記課題を解決するためのもので、出力電流誤差検出回路をなくし、出力電流値Ｉo＜出力過電流保護電流値Ｉolimitでは出力電圧誤差検出回路とパルス幅制御回路を用いて定電圧出力特性となるようにスイッチング素子のオン・オフを制御し、出力電流Ｉo＝出力過電流保護電流値Ｉolimitではトランスの二次巻線に比例する前記トランスの第２の一次巻線の電圧と過電流検出回路及びパルス幅制御回路を用いて、

出力電流値Ｉo＝出力定電流値Ｉoconst＝出力過電流保護電流値Ｉolimit

となる定電流出力特性になるようにスイッチング素子１のオン・オフを制御することにより、部品数の削減、損失の低減、使用部品定格の最適化、熱設計の最適化が行え、定電圧出力特性と定電流出力特性を有するスイッチング電源装置の低コスト化、小型化が可能となる。

【００１７】

【課題を解決するための手段】この目的を達成するために本発明は、トランスの第１の一次巻線を介してスイッチング素子と前記スイッチング素子を流れる電流を電圧信号に変換して出力する電流検出回路を直列に接続し、前記電流検出回路の出力を比較器の第１の入力端子に接続し前記比較器の第２の入力端子にはトランスの二次巻線電圧に比例した電圧が発生する前記トランスの第２の一次巻線を整流平滑して得られる電圧を電流信号に変換する手段の出力が接続し、前記比較器の出力は前記スイッチング素子のオン・オフを制御するパルス幅制御回路に接続された構成とする。

【００１８】また、トランスの第１の一次巻線を介してスイッチング素子と前記スイッチング素子を流れる電流を電圧信号に変換して出力する電流検出回路を直列に接続し、前記電流検出回路の出力を比較器の第１の入力端子に接続し前記比較器の第２の入力端子にはトランスの二次巻線電圧に比例した電圧が発生する前記トランスの第２の一次巻線を整流平滑して得られる電圧を電流信号に変換する手段の出力と前記トランスの第２の一次巻線間にダイオードとコンデンサの直列接続回路を並列接続した構成からなる前記トランスの第１の一次巻線に与えられる直流入力電圧に比例した電圧を電流信号に変換する手段の出力を接続し、前記比較器の出力は前記スイッチング素子のオン・オフを制御するパルス幅制御回路に接続された構成とする。

【００１９】さらに上記構成において前記スイッチング素子をＭＯＳＦＥＴとし前記ＭＯＳＦＥＴは大多数の単位セルが接続された第１のソース電極と単位セルの一部分が接続された第２のソース電極とを有し、前記第２のソース電極を電流検出回路に直列接続した構成とするものである。

【００２０】

【作用】この構成によって、出力電流誤差検出回路が不

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流を検出する出力電流検出抵抗が不要となるため損失の低減が図れるとともに、出力特性においては従来と同じ定電圧特性を有し定電流特性では、

出力電流Ｉo＝出力定電流値Ｉoconst＝出力過電流保護電流値Ｉolimit

とすることができ使用部品及び熱設計の最適化が行える。

【００２１】また、出力電流誤差検出回路をなくしてもトランスの第１の一次巻線に与えられる直流入力電圧に係らず出力の定電流特性においては

出力電流Ｉo＝出力定電流値Ｉoconst＝出力過電流保護電流値Ｉolimit

とすることができる。

【００２２】さらには、スイッチング素子を流れる電流を検出する電流検出回路内の抵抗の損失の低減が図れるとともにスイッチング素子と同一半導体基板上に数多くの回路が集積化できスイッチング電源装置の一次側部品数の削減ができるといったことからスイッチング電源装置として低コスト化、小型化を図ることができる。

【００２３】

【実施例】以下に本発明の一実施例を図１、図２を参考にしながら説明する。

【００２４】図１は本発明のスイッチング電源装置の回路構成図である。図１において図５と同じものについては同一の符合を記す。図１において１はバイポーラトランジスタあるいは電界効果トランジスタ等により構成されるスイッチング素子であり、２は電力変換用のトランスであり、２ａは第１の一次巻線、２ｂは第２の一次巻線、２ｃは二次巻線であり、３は商用交流電源を整流平滑するなどして得られる直流電源であり、４は２次整流ダイオード４ａと整流平滑コンデンサ４ｂからなる出力回路であり、５は負荷であり、直流電源３からトランス２の第１の一次巻線２ａを介して与えられる直流電力をスイッチング素子１によりスイッチングしそのスイッチング出力をトランス２の第１の一次巻線２ａから二次巻線２ｃに取出し二次巻線２ｃに接続された出力回路４によって整流平滑し、直流電力として負荷５に供給する。

【００２５】６は出力電圧誤差検出回路であり、負荷５に供給される出力電圧Voを抵抗６ａ、６ｂによって分圧し誤差増幅器６ｃの第１の入力端子に入力し、誤差増幅器６ｃの第２の入力端子に入力される基準電圧源６ｄとの誤差分を増幅しフォトカプラー８を介してパルス幅制御回路１１に出力する。

【００２６】９は過電流検出回路であり、スイッチング素子１に流れる電流を抵抗１０ａにより電圧信号に変換＊

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＊する電流検出回路１０の出力を比較器９ａの第１の入力端子に入力し、比較器９ａの第２の入力端子には定電流源９ｂａと抵抗９ｂｂからなる基準電圧源９ｂと前記トランス２の二次巻線２ｃに比例する前記トランス２の第２の一次巻線２ｂの電圧をダイオード１２ａ、コンデンサ１２ｂからなる整流平滑回路１２で整流平滑し、整流平滑回路１２に並列に接続された抵抗１４ａ、抵抗１４ｂからなる整流平滑回路１２の電圧を電流信号に変換する出力電圧モニター回路１４の出力とが入力され、比較器９ａは第１及び第２の入力端子に入力された信号を比較しその出力を出力信号Ｖ14としてパルス幅制御回路１１に出力する。

【００２７】パルス幅出力回路１１は、直流電源３または前記パルス幅制御回路１１が動作を開始すると前記トランス２の二次巻線２ｃに比例するトランス２の第２の一次巻線２ｂの電圧をダイオード１２ａ、コンデンサ１２ｂからなる整流平滑回路１２の出力を電源電圧とし、

（１）出力電流値Ｉo＜出力定電流値Ｉoconst＝出力過電流保護電流値Ｉolimit

では電圧誤差検出回路６によるフォトカプラー８を介しての出力により誤差増幅器１１ａの入力信号Ｖ11を変化させ誤差増幅器１１ａは基準電圧１１ｂと入力信号Ｖ11を比較し増幅してＰＷＭコンパレータ１１ｃに出力信号Ｖ12を出力しＰＷＭコンパレータ１１ｃは誤差増幅器１１ａの出力信号Ｖ12と三角波１１ｄを比較し出力信号Ｖ13をＮＯＲ回路１１ｅに出力し、ＮＯＲ回路１１ｅは過電流検出回路９の出力信号Ｖ14とＰＷＭコンパレータ１１ｃの出力信号Ｖ13とを論理演算し出力信号Ｖ15をＲ－Ｓフリップフロップ１１ｆのＲ端子に出力しＲ－Ｓフリップフロップ１１ｆはＳ端子に接続されるクロックパルス１１ｇとＮＯＲ回路１１ｅの出力信号Ｖ15により決定される出力信号Ｖ16をドライブ回路１３を介してスイッチング素子１に出力することにより出力電圧Voが一定となるようにスイッチング素子のオン･オフ時間を制御する。

【００２８】図２は図１のスイッチング電源装置の出力のＩ－Ｖ特性を示したものであり、この時のＩ－Ｖ特性は図２中の太線部Ａの特性となり定電圧特性となる。

（２）次に、負荷５のインピーダンスが低下し出力電流値Ｉoが大きくなり、

出力電流値Ｉo＝出力定電流値Ｉoconst＝出力過電流保護電流値Ｉolimit

となるとスイッチング素子１を流れる電流Ｉ（１）が大きくなり、

$$V10=I(1)\cdot R(10a)$$
$$=\{R(14a)\cdot(1/R(9bb)+1/R(14a)+1/R(14b))\}\cdot\{NB/NP\cdot Vo+Icc\cdot R(14a)\}$$
$$=V9REF\cdots\cdots(1)$$

とたると、過電流検出回路９が動作し出力信号Ｖ14をＮ　　出力信号Ｖ15をＲ－Ｓフリップフロップ１１ｆのＲ端子

されるクロックパルス１１ｇとＮＯＲ回路１１ｅの出力信号Ｖ15により決定される出力信号Ｖ16をドライブ回路１３を介してスイッチング素子１に出力するため出力電圧Voが低下し、これにより出力誤差検出回路６によるフォトカプラー８を介しての信号がなくなりフォトカプラー８電圧Ｖ11が基準電圧１１ｉより高くなるため比較器１１がスイッチ１１ｊをオフとしＰＷＭコンパレータの出力Ｖ13はロウレベルとなるためＮＯＲ回路１１ｅの出力Ｖ15は過電流検出回路９の出力信号Ｖ14で決されることになる。

【００２９】但し、V9REFは過電流検出回路９内の比較器９ａの第２の入力端子に入力される電圧値であり、上記式（１）において、R(10a)は、電流検出回路１０内の抵抗１０ａの抵抗値であり、R(14a)、R(14b)は、それぞれ出力電圧モニター回路１４内の抵抗１４ａ、１４ｂの抵抗値であり、R(9bb)は、過電流検出回路９内の抵抗９ｂｂの抵抗値であり、Iccは、過電流検出回路９内の定電流源９ｂａの定電流値であり、NPは、トランス２の第１の一次巻線２ａの巻線数であり、NBは、トランス２の第２の一次巻線２ｂの巻線数である。

【００３０】この時の出力電流Ｉoは、

$$Io=k\cdot Lp\cdot I(1)^2/Vo\cdot f$$
$$=k\cdot Lp\cdot\{V9REF/R(10a)\}^2/Vo\cdot f\cdots(2)$$
$$=I\,oconst$$

となる。

【００３１】但し、ｋは比例定数であり、Ｌｐはトランス２の第１の一次巻線のインダクタンス値であり、ｆはスイッチング素子１の発振周波数である。

【００３２】図２のＩ－Ｖ特性においてはＢ点となる。さらに、負荷５のインピーダンスが小さくなり出力電圧Voが低下しても

出力電流値Ｉo＝出力定電流値Ｉoconst＝出力過電流保護電流値Ｉolimit

となるように式（１）より設定された過電流検出回路９内の比較器９ａの第２の入力端子に入力される電圧値9REFが出力電圧Voにより低くなることで

出力電流値Ｉo＝出力定電流値Ｉoconst＝出力過電流保護電流値Ｉolimit

となる。

【００３３】又、前述の式（１）によりスイッチング素子１を流れる電流Ｉ（１）も小さくなる。出力電流Ｉoは前述の式（２）となる。

【００３４】図２のスイッチング電源装置の出力のＩ－Ｖ特性においてはＢ点からＣ点へとなる。

【００３５】さらに負荷５のインピーダンスが小さくなり出力電圧Voが低下すると

出力電流値Ｉo＝出力定電流値Ｉoconst＝出力過電流保護電流値Ｉolimit

となるように式（１）より設定された過電流検出回路９内の比較器９ａの第２の入力端子に入力される電圧値9REFが低くなることで

出力電流値Ｉo＝出力定電流値Ｉoconst＝出力過電流保護電流値Ｉolimit

となる。

【００３６】又、スイッチング素子１を流れる電流Ｉ（１）はさらに小さくなる。出力電流Ｉoは前述の式（２）となる。

【００３７】図２のスイッチング電源装置の出力のＩ－Ｖ特性はＣ点からＤ点へとなり、過電流検出回路９が動作を開始すると図２のＩ－Ｖ特性においては点線部の特性、すなわち出力定電流特性を得ることができる。図２の点線部の出力定電流特性部はパルス幅制御回路１１に入力される過電流検出回路９の出力によりスイッチング素子１のオン・オフが制御されているため、

出力電流値Ｉo＝出力定電流値Ｉoconst＝出力過電流保護電流値Ｉolimit

となる。

【００３８】図３に本発明の他の実施例を示す。図３は他の本発明のスイッチング電源装置の回路構成図である。図３において第１と同じものについては同一の符合を記す。１５はダイオード１５ａとコンデンサ１５ｂの直列回路からなる直流電源３の電圧値Ｅを検出する入力電圧モニター回路であり、前記トランス２の第２の一次巻線２ｂに並列接続され、出力は抵抗１６を介して過電流検出回路９内の比較器９ａの第２の入力端子に接続されている。図３のスイッチング電源装置の動作は図１に示すスイッチング電源装置の動作と同じため説明は省略する。

【００３９】但し、過電流検出回路９が動作し出力信号Ｖ14をＮＯＲ回路１１ｅに出力する時の電流検出回路の出力Ｖ10と過電流検出回路９内の比較器９ａの第２の入力端子の電圧V9REFは、

$$V10=I(1)\cdot R(10a)$$
$$=\{R(14a)\cdot(1/R(9bb)+1/R(14a)+1/R(14b)+I/R(16))\}\cdot\{NB/NP\cdot Vo+R(14a)/R(16)\cdot VBB+Icc\cdot R(14a)\}$$
$$=V9REF\cdots\cdots(3)$$

となる。

【００４０】但し、VBBは、入力電圧モニター回路１５の出力電圧Ｖで、VBB＝-NB/NP･Eであり、NBは、トランス２の第２の一次巻線２ｂの巻線数であり

NPは、トランス２の第１の一次巻線２ａの巻線数であり

Ｅは、直流電源３の電圧値であり、R(16)は、抵抗１６の抵抗値である。

【００４１】出力電流Ｉo、出力特性は図１の実施例と同じくそれぞれ式（２）、図２となり、

出力電流値Ｉo＝出力定電流値Ｉoconst＝出力過電流保護電流値Ｉolimit

とすることができる。

【００４２】図４に本発明のさらに他の実施例を示す

である。図４において図１と同じものについては同一の符合を記す。図４は図１のスイッチング素子１としてパワーＭＯＳＦＥＴ１７を用いた場合であり、パワーＭＯＳＦＥＴ１７は大多数の単位セルからなる第１のソース電極Ｓ１と少数の単位セルからなる第２のソース電極Ｓ２を有し第２のソース電極Ｓ２が電流検出回路１０に接続された構成である以外は図１と同じ構成であり、図１＊に示すスイッチング電源装置と動作は同じため説明は省略する。

【００４３】但し、過電流検出回路９が動作し出力信号Ｖ14をＮＯＲ回路１１ｅに出力する時の電流検出回路の出力Ｖ10と過電流検出回路９内の比較器９ａの第２の入力端子の電圧Ｖ9REFは、

$$
\begin{aligned}
V10 &= I(S2)\cdot R(10a)\\
&= n2/n1\cdot I(S1)\cdot R(10a)\\
&= n2/n1\cdot I(1)\cdot R(10a)\\
&= \{R(14a)\cdot(1/R(9bb)+1/R(14a)+1/R(14b))\}\cdot\{NB/NP\cdot Vo+Icc\cdot R(14a)\\
&= V9REF \qquad \cdots\cdots (4)
\end{aligned}
$$

となる。

【００４４】但し、ｎ１は、パワーＭＯＳＦＥＴ１７の第１のソース電極Ｓ１に接続されるパワーＭＯＳＦＥＴの単位セル数であり、ｎ２は、パワーＭＯＳＦＥＴ１７の第２のソース電極Ｓ２に接続されるパワーＭＯＳＦＥＴの単位セル数であり、I(S1)は、パワーＭＯＳＦＥＴ１７の第１のソース電極Ｓ１を流れる電流値であり、I(S2)は、パワーＭＯＳＦＥＴ１７の第２のソース電極Ｓ２を流れる電流値であり、

I(S2)=n2/n1･I(S1)

となる。

【００４５】n2/n1は通常約１～０．１％に設定されるため第１のスイッチング素子１を流れる電流Ｉ（１）とパワーＭＯＳＦＥＴ１７の第１のソース電極Ｓ１を流れる電流Ｉ（Ｓ１）はほぼ等しい。

【００４６】出力電流Ｉo、出力特性は図１の実施例と同じくそれぞれ式（２）、図２となり、

出力電流値Ｉo＝出力定電流値Ｉoconst＝出力過電流保護電流値Ｉolimit

とすることができる。

【００４７】さらに、式（４）から明らかなようにR(10a)をn1/n2倍又は、抵抗R(14a)、R(9b)、R(14b)をn1/n2倍に設定すれば図１の実施例の式（１）と同じことになるが図１の実施例に比べ、

・スイッチング素子１に流れる電流Ｉ（１）のn2/n1倍の極小さい電流で過電流検出回路９を動作させることができるため電流検出回路１０内の抵抗１０の損失の低減を図ることができスイッチング電源装置として小型化できる。

【００４８】・パワーＭＯＳＦＥＴ１７、電流検出回路１０、過電流検出回路９、パルス幅制御回路１１、出力電圧モニター回路１４を同一半導体基板上に集積化できる。以上の点から図１の実施例よりもさらに小型化、低コスト化を行うことができる。

【００４９】又、図３の実施例においても図４の実施例のようにスイッチング素子１をパワーＭＯＳＦＥＴの大多数の単位セルからなる第１のソース電極Ｓ１と少数の

ＭＯＳＦＥＴとしても動作、出力電流Ｉo及び出力特性は同じであり、入力電圧モニター回路１５、抵抗１６をも同一半導体基板上に集積化でき図４の実施例よりもさらに小型化、低コスト化を行うことができる。

【００５０】

【発明の効果】以上述べたように本発明は、

（１）トランスの第１の一次巻線を介してスイッチング素子と前記スイッチング素子を流れる電流を電圧信号に変換して出力する電流検出回路を直列に接続し、前記電流検出回路の出力を比較器の第１の入力端子に接続し前記比較器の第２の入力端子にはトランスの二次巻線電圧に比例した電圧が発生する前記トランスの第２の一次巻線を整流平滑して得られる電圧を電流信号に変換する手段の出力が接続され、前記比較器の出力は前記スイッチング素子のオン・オフを制御するパルス幅制御回路に接続された構成とする。

【００５１】（２）トランスの第１の一次巻線を介してスイッチング素子と前記スイッチング素子を流れる電流を電圧信号に変換して出力する電流検出回路を直列に接続し、前記電流検出回路の出力を比較器の第１の入力端子に接続し前記比較器の第２の入力端子にはトランスの二次巻線電圧に比例した電圧が発生する前記トランスの第２の一次巻線を整流平滑して得られる電圧を電流信号に変換する手段の出力と前記トランスの第２の一次巻線間にダイオードとコンデンサの直列接続回路を並列接続した構成からなる前記トランスの第１の一次巻線に与えられる直流入力電圧に比例した電圧を電流信号に変換する手段の出力を接続し、前記比較器の出力は前記スイッチング素子のオン・オフを制御するパルス幅制御回路に接続された構成とする。

【００５２】（３）上記（１）、（２）の構成において前記スイッチング素子をＭＯＳＦＥＴとし前記ＭＯＳＦＥＴは大多数の単位セルが接続された第１のソース電極と単位セルの一部分が接続された第２のソース電極とを有し、前記第２のソース電極を上記（１）、（２）の電流検出回路に接続した構成とするものであるから、

（１）出力電流誤差検出回路７が不要となり部品数の削

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電流検出抵抗７ａが不要となるため損失の低減が図れるとともに、出力特性においては従来と同じ定電圧特性を有し定電流特性では、出力電流値Ｉｏ＝出力定電流値Ｉｏconst＝出力過電流保護値Ｉolimitとすることができ使用部品及び熱設計の最適化が行える。

【００５３】（２）出力電流誤差検出回路７をなくしてもトランスの第１の一次巻線に与えられる直流入力電圧に係らず出力の定電流特性においては出力電流Ｉｏ＝出力定電流値Ｉoconst＝出力過電流保護電流値Ｉolimitとすることができる。

【００５４】（３）さらには、スイッチング素子１を流れる電流を検出する電流検出回路１０内の抵抗１０ａの損失の低減が図れるとともにスイッチング素子１と同一半導体基板上に数多くの回路が集積化できスイッチング電源装置の一次側部品数の削減ができる。といったことから低コスト化、小型化を図ることができる定電圧出力特性と定電流出力特性を有するスイッチング電源装置を提供することができる。

【図面の簡単な説明】

【図１】本発明の一実施例を示すスイッチング電源装置の回路構成図

【図２】本発明の一実施例におけるスイッチング電源装置の出力特性図

【図３】他の本発明の一実施例を示すスイッチング電源装置の回路構成図

【図４】他の本発明の一実施例を示すスイッチング電源装置の回路構成図

【図５】従来のスイッチング電源装置の回路構成図

【図６】従来のスイッチング電源装置の出力特性図

【符号の説明】

１　バイポーラトランジスタ或いは電界効果トランジスタにより構成されるスイッチング素子

２　トランス

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＊２ａ　トランス２の第１の一次巻線

２ｂ　トランス２の第２の一次巻線

２ｃ　トランス２の二次巻線

３　直流電源

４　出力回路

４ａ　２次整流ダイオード

４ｂ　２次平滑コンデンサ

５　負荷

６　出力電圧誤差検出回路

６ａ、６ｂ、７ａ、９ｂｂ、１０ａ、１４ａ、１４ｂ、１６　抵抗

６ｃ、７ｂ、１１ａ　誤差増幅器

６ｄ、７ｃ、９ｂ、１１ｂ、１１ｉ　基準電圧源

６ｅ、７ｄ、１２ａ、１５ａ　ダイオード

７　出力電流誤差検出回路

８　フォトカプラー

９　過電流検出回路

９ａ、１１ｈ　比較器

９ｂａ　定電流源

１０　電流検出回路

１１　パルス幅制御回路

１１ｃ　ＰＷＭコンパレータ

１１ｄ　三角波

１１ｅ　ＮＯＲ回路

１１ｆ　Ｒ－Ｓフリップフロップ

１１ｇ　クロックパルス

１１ｊ　スイッチ

１２　整流平滑回路

１２ｂ、１５ｂ　コンデンサ

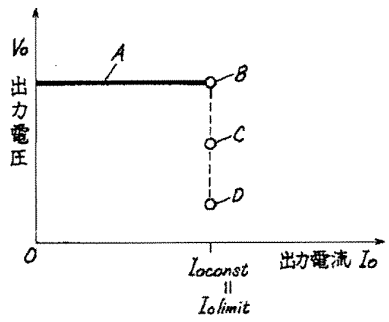
１３　ドライブ回路

１４　出力電圧モニター回路

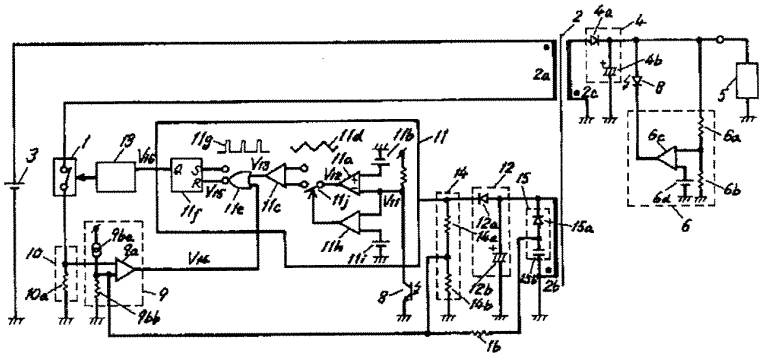
１５　入力電圧モニター回路

＊　１７　パワーＭＯＳＦＥＴ

【図２】



【図３】



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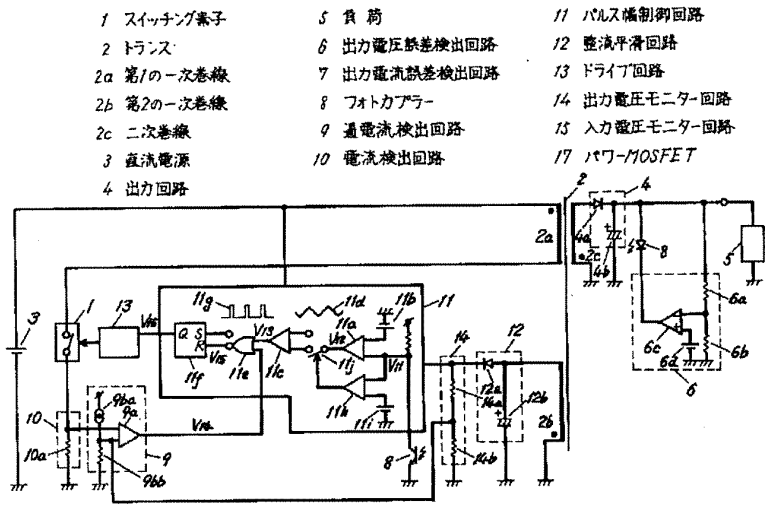
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4 出力回路
5 負荷
6 出力電圧誤差検出回路
7 出力電流誤差検出回路
8 フォトカプラー
9 過電流検出回路
10 電流検出回路
11 パルス幅制御回路
12 整流平滑回路
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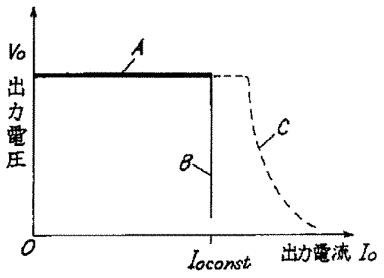
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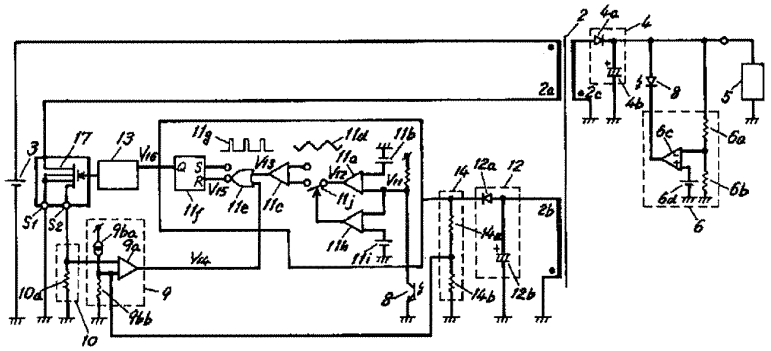

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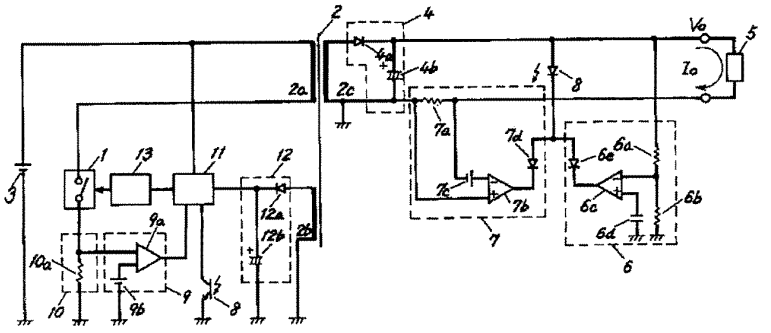

UNITED STATES PATENT APPLICATION

FOR

METHOD AND APPARATUS FOR MAINTAINING A CONSTANT LOAD CURRENT WITH LINE VOLTAGE IN A SWITCH MODE POWER SUPPLY

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METHOD AND APPARATUS FOR MAINTAINING A CONSTANT LOAD CURRENT WITH LINE VOLTAGE IN A SWITCH MODE POWER SUPPLY

RELATED APPLICATION

This application is a continuation of U.S. Application Serial No. 11/784,560, filed April 6, 2007, now pending, which is a continuation of U.S. Application Serial No. 11/397,524, filed April 3, 2006, now US 7,215,105 B2, which is a continuation of U.S. Application Serial No. 10/892,300, filed July 15, 2004, now US 7,110,270 B2, which is a continuation of U.S. Application Serial No. 10/253,307, filed September 23, 2002, now US 6,781,357 B2, which claims the benefit of and priority to U.S. provisional application serial no. 60/325,642, filed September 27, 2001, entitled "Method And Apparatus For Maintaining A Constant Load Current With Line Voltage In A Switch Mode Power Supply."

BACKGROUND OF THE INVENTION

Field of the Invention

This invention relates generally to power supplies and, more specifically, the present invention relates to a switched mode power supply.

Background Information

All electronic devices use power to operate. A form of power supply that is highly efficient and at the same time provides acceptable output regulation to supply power to electronic devices or other loads is the switched-mode power supply. In many electronic device applications, especially the low power off-line

adapter/charger market, during the normal operating load range of the power supply an approximately constant output voltage is required below an output current threshold. The current output is generally regulated below an output voltage in this region of approximately constant output voltage, hereafter referred to as the output voltage threshold.

In known switched mode power supplies without secondary current sensing circuitry, minimizing the variation of the output current at the output voltage threshold is performed with complex control schemes. Typically, these schemes include the measurement of input voltage, output diode conduction time and peak primary current limit. Some or all of this measured information is then used to control the regulator in order to reduce the variation of the output current at the output voltage threshold.

SUMMARY OF THE INVENTION

A power supply that maintains an approximately constant load current with line voltage below the output voltage threshold is disclosed. In one embodiment, a regulation circuit includes a semiconductor switch and current sense circuitry to sense the current in the semiconductor switch. The current sense circuitry has a current limit threshold. The regulation circuit current limit threshold is varied from a first level to a second level during the time when the semiconductor switch is on. In one embodiment, the regulation circuit is used in a power supply having an output characteristic having an approximately constant output voltage below an output current threshold and an approximately constant output current below an output voltage threshold. In another embodiment, a power supply is described, which includes a power supply input and a power supply output and that maintains an approximately constant load current with line voltage below the output voltage threshold. In one embodiment, the power supply has an output characteristic having an approximately constant output voltage below an output current threshold and an approximately constant output current below an output voltage threshold. A regulation circuit is coupled between the power supply input and the power supply output. The regulation circuit includes a semiconductor switch and current sense circuitry to sense the current in the semiconductor switch. The current sense circuitry has a current limit threshold. The regulation circuit current limit threshold is varied from a first level to a second level during the time when the semiconductor switch is on. In another

aspect, the current limit threshold being reached coincides with the power supply output characteristic transitioning from providing an approximately constant output voltage to supplying an approximately constant output current. In yet another aspect, the semiconductor switch is a MOSFET. Additional features and benefits of the present invention will become apparent from the detailed description and figures set forth below.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention detailed illustrated by way of example and not limitation in the accompanying figures.

Figure 1 is a schematic of one embodiment of a switched mode power supply regulator in accordance with the teachings of the present invention.

Figure 2 is a diagram illustrating one embodiment of sawtooth, duty cycle and intrinsic current limit waveforms in accordance with the teachings of the present invention.

Figure 3 shows one embodiment of a power supply that has an approximately constant voltage and constant current characteristic in accordance with the teachings of the present invention.

Figure 4 shows one embodiment of a power supply that has an approximately constant voltage and constant current characteristic in accordance with the teachings of the present invention.

Figure 5 is a diagram illustrating the typical relationship between the output current and output voltage of one embodiment of a power supply in accordance with the teachings of the present invention.

DETAILED DESCRIPTION

Embodiments of methods and apparatuses for maintaining a power supply output current substantially constant independent of input voltage at the point where the power supply output characteristic transitions from providing an approximately constant output voltage to supplying an approximately constant output current are disclosed. In the following description, numerous specific details are set forth in order to provide a thorough understanding of the present invention. It will be apparent, however, to one having ordinary skill in the art that the specific detail need not be employed to practice the present invention. In other instances, well-known materials or methods have not been described in detail in order to avoid obscuring the present invention.

Reference throughout this specification to "one embodiment" or "an embodiment" means that a particular feature, structure or characteristic described in connection with the embodiment is included in at least one embodiment of the present invention. Thus, the appearances of the phrases "in one embodiment" or "in an embodiment" in various places throughout this specification are not necessarily all referring to the same embodiment. Furthermore, the particular features, structures or characteristics may be combined in any suitable manner in one or more embodiments.

In one embodiment here, a switched mode power supply is described in which the output current below the output voltage threshold, is regulated to be approximately constant. This provides an approximate constant voltage/constant

current output characteristic. The output current level at the output voltage threshold in known power supplies sensed at the output of the power supply to provide feedback to a regulator circuit coupled to the primary winding of the power supply. If however, the approximate constant current functionality is achieved without feedback from the secondary winding side of the power supply, the output current at the output voltage threshold is a function of a peak current limit of the primary regulator.

Embodiments of the present invention reduce the variation of the output current at the output voltage threshold by reducing the peak current limit variation with changing input voltage. In general, the intrinsic peak current limit is set by internal circuitry in the regulator to be constant. In one embodiment, once the drain current reaches a current limit threshold, the switching cycle should, in theory, terminate immediately. However, a fixed delay is inherent from the time the threshold is reached until the power metal oxide semiconductor field effect transistor (MOSFET) is finally disabled. During this delay, the drain current continues to ramp up at a rate equal to the direct current (DC) input voltage divided by the primary inductance of the transformer (drain current ramp rate). Therefore, the actual current limit is the sum of the intrinsic current limit threshold and a ramp-rate dependent component (the overshoot), which is the drain current ramp rate multiplied by the fixed delay. Thus, at higher DC input voltages, the actual current limit ramps to a higher level above the intrinsic current limit level than at low DC input voltages. This can result in variations in

the output current delivered to the load at the output voltage threshold over a range of input line voltages.

The actual current limit is the sum of the intrinsic current limit and the ramp-rate dependent component (the overshoot). The goal is to maintain a constant actual current limit over DC input voltage variations. Since the ramp-rate component (the overshoot) increases with respect to the DC input voltage, the only way to maintain a relatively constant current limit would be to reduce the intrinsic current limit threshold when the DC input voltage rises.

In discontinuous power supply designs, the point in time during the switching cycle in which the current limit is reached is dependent on the DC input voltage. In fact, the time it takes from the beginning of the cycle to the point where current limit is inversely proportional to the DC input voltage. Thus, the time elapsed from the beginning of the cycle can be used to gauge the DC input voltage.

Therefore, in order to create an intrinsic current limit which decreases relative to the DC input voltage, the time elapsed can be used. It is simply necessary to increase the intrinsic current limit as a function of the time elapsed during the cycle. A first approximation for increasing the intrinsic current limit with time can be obtained by using the Equation 1 below:

$$I_{LIM\text{-}INTRINSIC} = K_1 + K_2 * t_{elapsed,} \qquad \text{(Equation 1)}$$

where is $I_{LIM\text{-}INTRINSIC}$ the intrinsic current limit, K_1 and K_2 are constants and $t_{elapsed}$ is the time elapsed.

In one embodiment, the time elapsed can be detected by the internal oscillator output waveform. In one embodiment, this waveform is a triangular one. It starts at its minimum at the beginning of the cycle. It gradually ramps until it reaches the point of maximum duty cycle.

In one embodiment, he ramp is substantially linear with time. In another embodiment, the ramp can also be nonlinear depending on the requirements of the power supply in which the regulator is used. The intrinsic current limit threshold is basically proportional to the voltage seen at the input of the current limit comparator. This bias voltage is the product of the resistor value and the current delivered to this resistor. One way to increase the intrinsic current limit linearly as a function of the elapsed time would then be to derive a linearly increasing (with elapsed time) current source and deliver this current to the resistor. This linearly increasing (with elapsed time) current source can thus be derived from the oscillator.

Figure 1 shows a schematic of one embodiment of a switched mode power supply in accordance with the teachings of the present invention. All of the circuitry shown in this schematic is used to control the switching of the power MOSFET 2. The timing of the switching is controlled by oscillator 5. Oscillator 5 generates three signals: Clock 10, DMAX (Maximum duty cycle) 15, and Sawtooth 20. The rising edge of Clock signal 10 determines the beginning of the switching cycle. As shown in the illustrated embodiment, when Clock signal 10 is high, output latch 90 is set, which results in a control signal output from output

latch 90 to enable power MOSFET 2 to begin conducting. The maximum conducting time is determined by DMAX 15 signal being high. When DMAX 15 signal goes low, latch 90 is reset, thus causing the control signal output from latch 90 to disable power MOSFET 2 from conducting.

The intrinsic current limit is, to the first order proportional to the voltage on node 22. As stated earlier, the goal of the invention is to generate an intrinsic current limit proportional to the time elapsed in the switching cycle. The saw tooth waveform 20 can be used to perform this task. As the base voltage of NPN transistor 30 rises, the emitter voltage also rises at the same rate. Thus, the current through resistor 25 is linearly increasing with time elapsed during the switching cycle. After mirroring this current through current mirror 40, the linearly increasing (with elapsed time) current source 27 is derived. The current limit threshold 22 is thus proportional to the product of the combination of linearly increasing current source 27 and constant current source 50 with the resistor 17. The voltage on node 37 is proportional to the power MOSFET drain voltage because of the voltage divider network formed by resistors 55 and 60. The drain current is proportional to the drain voltage. As the drain current 7 ramps up during the switching cycle, the voltage on node 37 rises proportionately. After the voltage on node 37 exceeds the voltage on current limit threshold node 22, comparator 70 disables the power MOSFET by ultimately resetting latch 90.

PWM Comparator 32 modulates the duty cycle based on the feedback signal coming from the output of the power supply. The higher the feedback voltage, the higher the duty cycle will be.

Figure 2 shows an embodiment of three waveforms: sawtooth 20, duty cycle max 15, and intrinsic current limit 22. The sawtooth waveform 20 and the duty cycle max waveform 15 are generated by the oscillator 5. The duty cycle max 15 signal determines the maximum duration of a power MOSFET switching cycle, when it is high. The sawtooth waveform 20 starts increasing at the low point when the duty cycle max waveform 15 goes high. This signals the beginning of the power MOSFET switching cycle. The high point of the sawtooth 20 is reached at the end of the cycle, at the same time the duty cycle max signal 15 goes low. The intrinsic current limit 22 signal starts at the low point at the beginning of the cycle and then linearly increases with elapsed time throughout the cycle. At a time elapsed of zero, the intrinsic current limit is at K_1. As time elapsed increases, the current limit increases by a factor of $K_2 * t_{elapsed.}$ As can be seen in Figure 2 therefore, the intrinsic current limit ($I_{LIM-INTRINSIC}$) is the sum of K_1 and $K_2 * t_{elapsed.}$

Figure 3 shows one embodiment of a power supply that has an approximately constant voltage and constant current characteristic in accordance with the teachings of the present invention. An energy transfer element 220 is coupled between DC output 200 and HV DC input 255. In one embodiment, energy transfer element is a transformer including an input winding 225 and an

output winding 215. Regulation circuit 250 is coupled between HV DC input 255 and energy transfer element 220 to regulate DC output 200. In the illustrated embodiment, feedback information responsive to DC output 200 is provided to the regulator 250 at its control pin. The current at the control pin is proportional to the voltage across resistor 235, which in turn is related to the output voltage at DC output 200.

In operation, the regulator circuit reduces the duty cycle of the power MOSFET when the voltage across resistor 235 increases above a threshold. In this section, the output is in approximately constant voltage mode. The regulator circuit reduces the current limit of the power MOSFET when the voltage across resistor 235 decreases below a threshold. The current limit is reduced as a function of the voltage across resistor 235 to keep the output load current constant. Thus, the load current is proportional to the current limit of the power MOSFET in regulator 250. By keeping the current limit invariant to line voltage, the output load current would remain constant at all line voltages.

Figure 4 shows one embodiment of a power supply that has an approximately constant voltage and constant current characteristic in accordance with the teachings of the present invention. The feedback information is provided to the regulator 350 at its control pin. The current at the control pin is proportional to the voltage across resistor 335, which in turn is related to the output voltage. The regulator circuit reduces the duty cycle of the power MOSFET when the voltage across resistor 335 increases above a threshold. In

this section, the output is in approximately constant voltage mode. The regulator circuit reduces the current limit of the power MOSFET when the voltage across resistor 335 decreases below a threshold. The current limit is reduced as a function of the voltage across resistor 335 to keep the output load current approximately constant. Thus, the load current is proportional to the current limit of the power MOSFET in regulator 350. By keeping the current limit substantially constant with line voltage, the output load current would remain substantially constant at all line voltages.

Figure 5 is a diagram illustrating the typical relationship between the output current and output voltage of one embodiment of a power supply in accordance with the teachings of the present invention. As can be seen in curve 400, the power supply utilizing the invention exhibits an approximately constant output current and constant output voltage characteristic. That is, as output current increases, the output voltage remains approximately constant until the output current reaches an output current threshold. As the output current approaches the output current threshold, the output voltage decreases as the output current remains approximately constant over the drop in output voltage until a lower output voltage threshold is reached when the output current can reduce further as shown by the range of characteristics. It is appreciated that the constant output voltage and constant output current characteristics of the present invention are suitable for battery charger applications or the like.

In the foregoing detailed description, the method and apparatus of the

present invention has been described with reference to specific exemplary embodiments thereof. It will, however, be evident that various modifications and changes may be made thereto without departing from the broader spirit and scope of the present invention. The present specification and figures are accordingly to be regarded as illustrative rather than restrictive.

CLAIMS

What is claimed is:

1. A power supply regulator, comprising:

a comparator having a first input coupled to sense a voltage representative of a current flowing through a switch during an on time of the switch, the comparator having a second input coupled to receive a variable current limit threshold that increases during the on time of the switch;

a feedback circuit coupled to receive a feedback signal representative of an output voltage at an output of a power supply; and

a control circuit coupled to generate a control signal in response to an output of the comparator and in response to an output of the feedback circuit, the control signal to be coupled to a control terminal of the switch to control switching of the switch.

2. The power supply regulator of claim 1 further comprising an oscillator having a first output to generate a sawtooth waveform, wherein the variable current limit threshold is generated in response to the sawtooth waveform.

3. The power supply regulator of claim 2 wherein the feedback circuit is coupled to receive the sawtooth waveform.

4. The power supply regulator of claim 2 wherein the oscillator further has a second output to generate a maximum duty cycle signal, wherein the control circuit is coupled to generate the control signal further in response to the maximum duty cycle signal.

5. The power supply regulator of claim 2 wherein the control circuit includes a latch to provide the control signal, wherein the latch includes a reset input coupled to the output of the comparator.

6. The power supply regulator of claim 5 wherein the latch further includes a set input coupled to be responsive to a clock signal generated from a third output of the oscillator.

7. The power supply regulator of claim 5 wherein the reset input of the latch is further coupled to be responsive to a maximum duty cycle signal from a second output of the oscillator.

8. The power supply regulator of claim 5 wherein the feedback circuit comprises a feedback comparator coupled to receive the feedback signal and the sawtooth waveform, wherein the reset input of the latch is coupled to be responsive to an output of the feedback comparator.

9. The power supply regulator of claim 1 wherein a duty cycle of the control signal is modulated in response to an output of the feedback circuit.

10. The power supply of regulator of claim 2 further comprising a current mirror coupled to the oscillator to receive the sawtooth waveform, wherein the variable current limit threshold is generated in response to the current mirror.

11. The power supply regulator of claim 1 wherein the switching of the switch provides at the output of the power supply an output characteristic having an approximately constant output current below an output voltage threshold.

12. The power supply regulator of claim 11 wherein the approximately constant output current remains substantially constant at all line voltages.

ABSTRACT OF THE DISCLOSURE

A power supply regulator including a variable current limit threshold that increases during an on time of a switch. In one aspect, a power supply regulator includes a comparator that has a first input coupled to sense a voltage representative of a current flowing through a switch during an on time of the switch. The comparator has a second input coupled to receive a variable current limit threshold that increases during the on time of the switch. A feedback circuit is coupled to receive a feedback signal representative of an output voltage at an output of a power supply. A control circuit is coupled to generate a control signal in response to an output of the comparator and in response to an output of the feedback circuit. The control signal is to be coupled to a control terminal of the switch to control switching of the switch.

Electronic Patent Application Fee Transmittal	
Application Number:	
Filing Date:	
Title of Invention:	METHOD AND APPARATUS FOR MAINTAINING A CONSTANT LOAD CURRENT WITH LINE VOLTAGE IN A SWITCH MODE POWER SUPPLY
First Named Inventor/Applicant Name:	Balu Balakrishnan
Filer:	James Go
Attorney Docket Number:	5510P064C4
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Utility application filing	1011	1	330	330
Utility Search Fee	1111	1	540	540
Utility Examination Fee	1311	1	220	220
Pages:				
Claims:				
Miscellaneous-Filing:				
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Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
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Extension-of-Time:				
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First Named Inventor/Applicant Name:	Balu Balakrishnan
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File Listing:

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Information:					
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2	Drawings-only black and white line drawings	5510P064C4_Figures_101609.pdf	335276 3f1549fe62b00e20fff6bb7b6c92870a86ab4f53	no	5
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	Specification	1	15
	Claims	16	18
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If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Electronic Acknowledgement Receipt	
EFS ID:	6280016
Application Number:	12581054
International Application Number:	
Confirmation Number:	1732
Title of Invention:	METHOD AND APPARATUS FOR MAINTAINING A CONSTANT LOAD CURRENT WITH LINE VOLTAGE IN A SWITCH MODE POWER SUPPLY
First Named Inventor/Applicant Name:	Balu Balakrishnan
Customer Number:	08791
Filer:	James Go/Kristy Marvel
Filer Authorized By:	James Go
Attorney Docket Number:	5510P064C4
Receipt Date:	16-OCT-2009
Filing Date:	
Time Stamp:	19:40:07
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	$1090
RAM confirmation Number	4561
Deposit Account	022666
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees) Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)	

Charge any Additional Fees required under 37 C.F.R. Section 1.19 (Document supply fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.20 (Post Issuance fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Application Data Sheet	5510P064C4_ADS_101609.pdf	64408 fa4cdfe649068f3062d671b1e4feb4be4a903292	no	6
Warnings:					
Information:					
This is not an USPTO supplied ADS fillable form					
2	Drawings-only black and white line drawings	5510P064C4_Figures_101609.pdf	335276 3f1549fe62b00e20fff6bb7b6c92870a86ab4f53	no	5
Warnings:					
Information:					
3	Oath or Declaration filed	5510P064C4_Declaration_101609.pdf	751308 fb9b21e9e64144cab21d80cbb8a33cef9bce18a6	no	5
Warnings:					
Information:					
4	Miscellaneous Incoming Letter	5510P064C4_Reqst37CFR1_101609.pdf	25056 d605ba4c5ae31852b8b9688f4b30641a7f48f89a	no	2
Warnings:					
Information:					
5	Transmittal Letter	5510P064C4_IDS_101609.pdf	25405 cb96e36c7959da49bb70888d124b684782ff23c4	no	2
Warnings:					
Information:					
6	Information Disclosure Statement (IDS) Filed (SB/08)	5510P064C4_1449_101609.pdf	103707 841397c5a47c744b73ae721b1660ffcd4312ece7	no	4
Warnings:					
Information:					
This is not an USPTO supplied IDS fillable form					
7	Foreign Reference	5510P064C4_Foreign1_101609.pdf	1330972 8492c6cc599107c145579d21c4c2d4a53b0eb8ff	no	26
Warnings:					
Information:					

8	Foreign Reference	5510P064C4_Foreign2_101609.pdf	1083940 8162d58114996ef19b34336ff428017a611cff6f	no	10
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Information:					
9	NPL Documents	5510P064C4_NPL1_101609.pdf	762357 06fe85f7b4f6760c699cbef5784531323738 6b98	no	16
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10	NPL Documents	5510P064C4_NPL2_101609.PDF	95974 1e0204e2948c8b8389b1837b02341470e9d83633	no	2
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11	NPL Documents	5510P064C4_NPL4_101609.PDF	1747228 fb2379d9e36d1d38c66f45fbe95461beb5d64368	no	29
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13	NPL Documents	5510P064C4_NPL6_101609.PDF	1720013 03f0d257165c4d4c6eeb8287ba29f9e7a4c2413c	no	15
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Information:					

17	NPL Documents	5510P064C4_NPL12_101609.PDF	948676 a9d8637bd0a67bdf9ddf6ad48a3867079af1e297	no	12
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18	NPL Documents	5510P064C4_NPL13_101609.pdf	444225 f4df75b540dec3a700b0824b65026b36932 1ae35	no	15
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Information:					
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22		5510P064C4_Application_101609.pdf	62125 8232ec2baf5bf850ed0692539a572176640 b1728	yes	19

Multipart Description/PDF files in .zip description

Document Description	Start	End
Specification	1	15
Claims	16	18
Abstract	19	19

Warnings:					
Information:					
23	Fee Worksheet (PTO-875)	fee-info.pdf	33142 3cb4db0cab4cecd326f435c0577b5997b33 df7b6	no	2
Warnings:					
Information:					
			Total Files Size (in bytes):	23245641	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
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PTO/SB/14 (07-07)
Approved for use through 06/30/2010. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	5510P064C4
	Application Number	
Title of Invention	METHOD AND APPARATUS FOR MAINTAINING A CONSTANT LOAD CURRENT WITH LINE VOLTAGE IN A SWITCH MODE POWER SUPPLY	

The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.
This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.

Secrecy Order 37 CFR 5.2

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Applicant Information:

Applicant 1

Applicant Authority ◉ Inventor ○ Legal Representative under 35 U.S.C. 117 ○ Party of Interest under 35 U.S.C. 118

Prefix	Given Name	Middle Name	Family Name	Suffix
	Balu		Balakrishnan	

Residence Information (Select One) ◉ US Residency ○ Non US Residency ○ Active US Military Service

City	Saratoga	State/Province	CA	Country of Residence	US

Citizenship under 37 CFR 1.41(b) US

Mailing Address of Applicant:

Address 1	21789 Villa Oaks Lane
Address 2	

City	Saratoga	State/Province	CA
Postal Code	95070	Country	US

Applicant 2

Applicant Authority ◉ Inventor ○ Legal Representative under 35 U.S.C. 117 ○ Party of Interest under 35 U.S.C. 118

Prefix	Given Name	Middle Name	Family Name	Suffix
	Alex	B.	Djenguerian	

Residence Information (Select One) ◉ US Residency ○ Non US Residency ○ Active US Military Service

City	Saratoga	State/Province	CA	Country of Residence	US

Citizenship under 37 CFR 1.41(b) US

Mailing Address of Applicant:

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Address 2	

City	Saratoga	State/Province	CA
Postal Code	95070	Country	US

Applicant 3

Applicant Authority ◉ Inventor ○ Legal Representative under 35 U.S.C. 117 ○ Party of Interest under 35 U.S.C. 118

Prefix	Given Name	Middle Name	Family Name	Suffix
	Kent		Wong	

Residence Information (Select One) ◉ US Residency ○ Non US Residency ○ Active US Military Service

City	Fremont	State/Province	CA	Country of Residence	US

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	5510P064C4
	Application Number	
Title of Invention	METHOD AND APPARATUS FOR MAINTAINING A CONSTANT LOAD CURRENT WITH LINE VOLTAGE IN A SWITCH MODE POWER SUPPLY	

Citizenship under 37 CFR 1.41(b)	US				
Mailing Address of Applicant:					
Address 1	34347 Enea Terrace				
Address 2					
City	Fremont	**State/Province**	CA		
Postal Code	94555	**Country**	US		

Applicant 4

Applicant Authority ◉ Inventor	○ Legal Representative under 35 U.S.C. 117	○ Party of Interest under 35 U.S.C. 118		
Prefix	**Given Name**	**Middle Name**	**Family Name**	**Suffix**
	David	Michael Hugh	Matthews	

Residence Information (Select One)	○ US Residency	◉ Non US Residency	○ Active US Military Service		
City	Windsor	**Country Of Residence**	GB		
Citizenship under 37 CFR 1.41(b)	GB				
Mailing Address of Applicant:					
Address 1	36A Clarence Rd				
Address 2					
City	Windsor	**State/Province**			
Postal Code	SL4 5AU	**Country**	GB		

All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the **Add** button. Add

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below.
For further information see 37 CFR 1.33(a).

☐ **An Address is being provided for the correspondence Information of this application.**

Customer Number	08791		
Email Address		Add Email	Remove Email

Application Information:

Title of the Invention	METHOD AND APPARATUS FOR MAINTAINING A CONSTANT LOAD CURRENT WITH LINE VOLTAGE IN A SWITCH MODE POWER SUPPLY		
Attorney Docket Number	5510P064C4	**Small Entity Status Claimed**	☐
Application Type	Nonprovisional		
Subject Matter	Utility		
Suggested Class (if any)		**Sub Class (if any)**	
Suggested Technology Center (if any)			
Total Number of Drawing Sheets (if any)	5	**Suggested Figure for Publication (if any)**	

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	5510P064C4
	Application Number	
Title of Invention	METHOD AND APPARATUS FOR MAINTAINING A CONSTANT LOAD CURRENT WITH LINE VOLTAGE IN A SWITCH MODE POWER SUPPLY	

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

☐ **Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S. C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32).
Enter either Customer Number or complete the Representative Name section below. If both sections are completed the Customer Number will be used for the Representative Information during processing.

Please Select One:	◉ Customer Number	○ US Patent Practitioner	○ Limited Recognition (37 CFR 11.9)
Customer Number	08791		

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, or 365(c) or indicate National Stage entry from a PCT application. Providing this information in the application data sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78(a)(2) or CFR 1.78(a)(4), and need not otherwise be made part of the specification.

Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
11784560	Continuation of	11397524	2007-04-06

Prior Application Status	Patented				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
11397524	Continuation of	10892300	2006-04-03	7215105	2007-05-08

Prior Application Status	Patented				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
10892300	Continuation of	10253307	2004-07-15	7110270	2006-09-19

Prior Application Status	Patented				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
10253307	Continuation of	60325642	2002-09-23	6781357	2004-08-24

Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
60325642			2001-09-27

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	5510P064C4
	Application Number	
Title of Invention	METHOD AND APPARATUS FOR MAINTAINING A CONSTANT LOAD CURRENT WITH LINE VOLTAGE IN A SWITCH MODE POWER SUPPLY	

Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the **Add** button.

Foreign Priority Information:

This section allows for the applicant to claim benefit of foreign priority and to identify any prior foreign application for which priority is not claimed. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55(a).

Remove

Application Number	Country[i]	Parent Filing Date (YYYY-MM-DD)	Priority Claimed
			○ Yes ◉ No

Additional Foreign Priority Data may be generated within this form by selecting the **Add** button.

Assignee Information:

Providing this information in the application data sheet does not substitute for compliance with any requirement of part 3 of Title 37 of the CFR to have an assignment recorded in the Office.

Assignee 1

If the Assignee is an Organization check here. ☒

Organization Name	Power Integrations, Inc.		
Mailing Address Information:			
Address 1	5245 Hellyer Avenue		
Address 2			
City	San Jose	**State/Province**	CA
Country[i]	US	Postal Code	95138
Phone Number		Fax Number	
Email Address			

Additional Assignee Data may be generated within this form by selecting the **Add** button.

Signature:

A signature of the applicant or representative is required in accordance with 37 CFR 1.33 and 10.18. Please see 37 CFR 1.4(d) for the form of the signature.

Signature	/James Y. Go/			Date (YYYY-MM-DD)	2009-10-16
First Name	James Y.	Last Name	Go	Registration Number	40621

PTO/SB/14 (07-07)
Approved for use through 06/30/2010. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	5510P064C4
	Application Number	
Title of Invention	METHOD AND APPARATUS FOR MAINTAINING A CONSTANT LOAD CURRENT WITH LINE VOLTAGE IN A SWITCH MODE POWER SUPPLY	

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

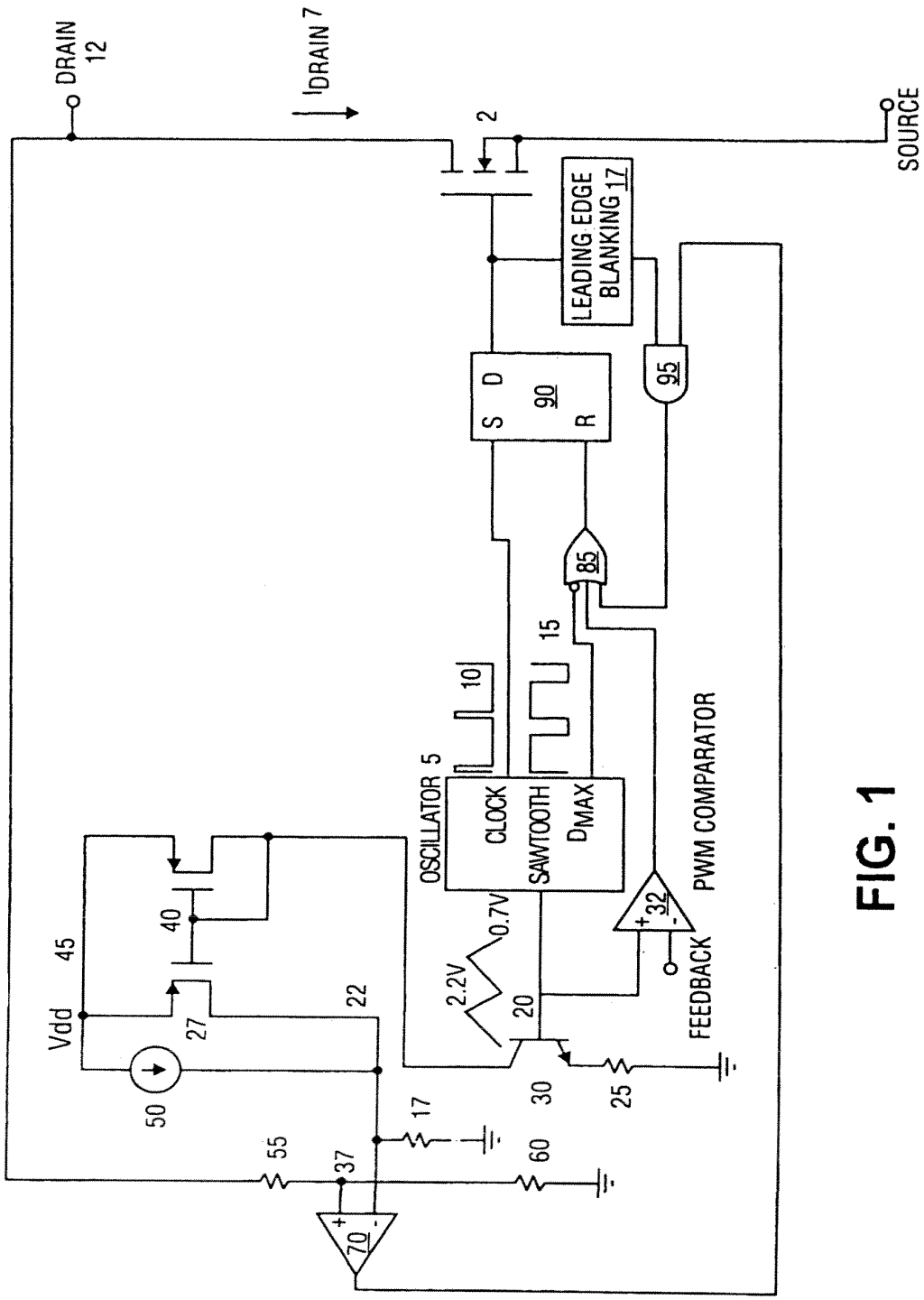
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.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DMAX
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2.2V
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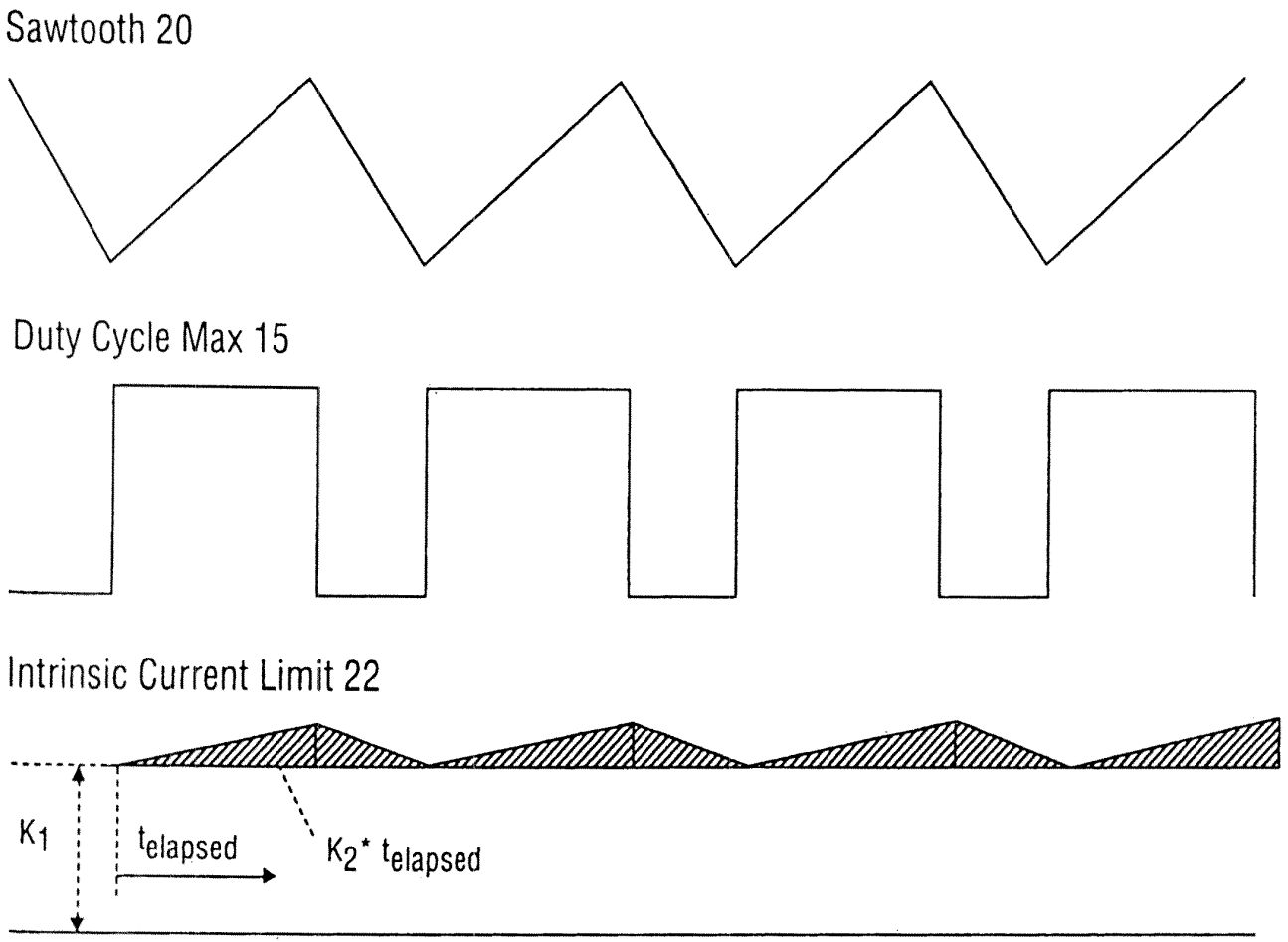
FIG. 1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K2* telapsed

FIG. 2

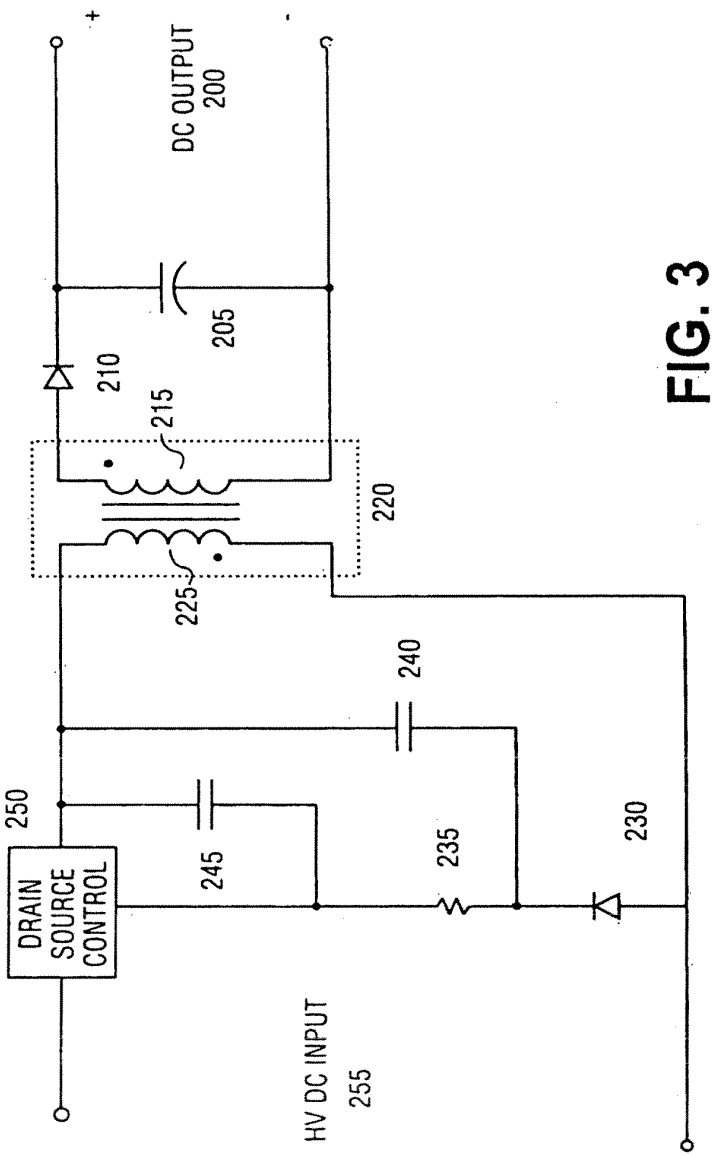
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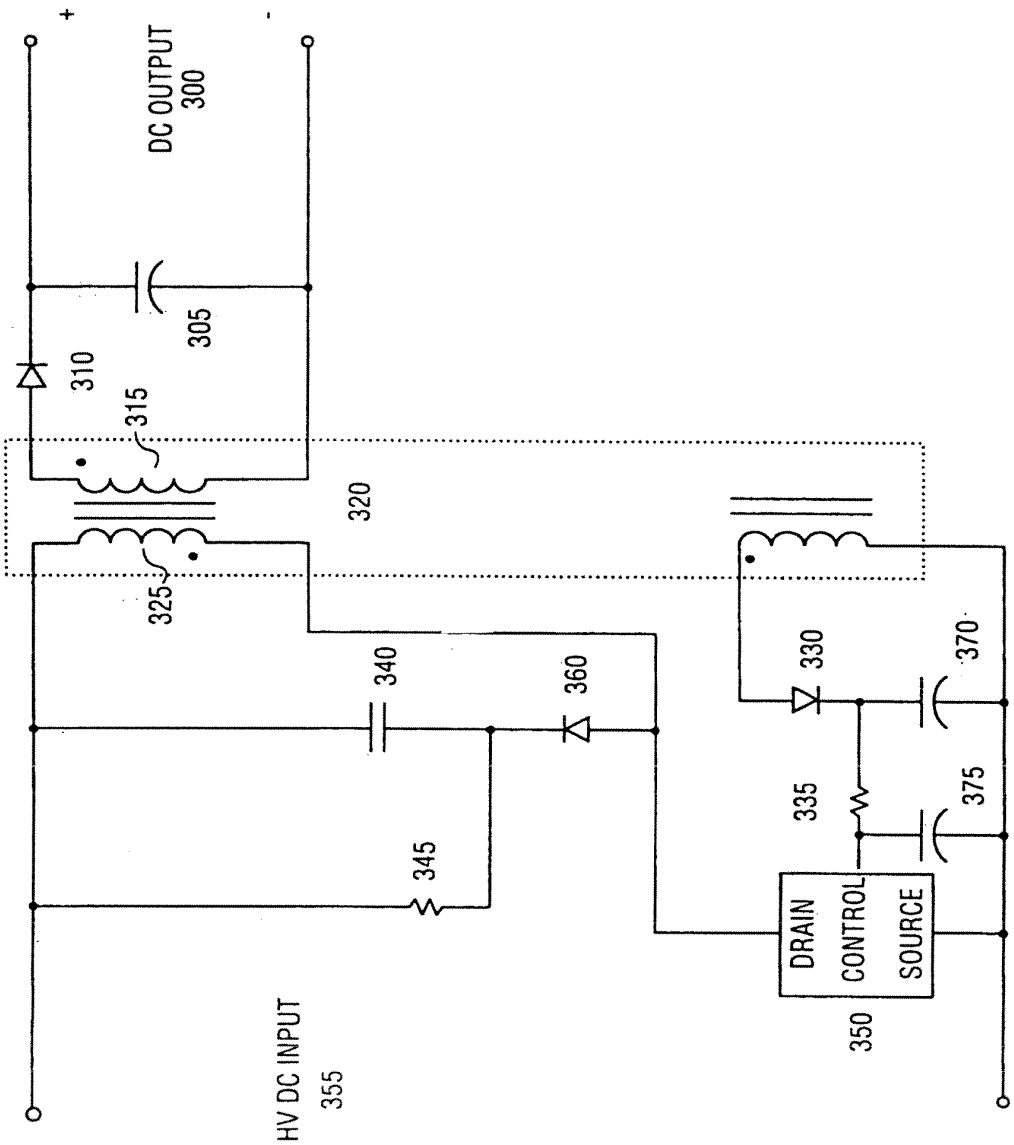
FIG. 3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350
HV DC INPUT
355

FIG. 4

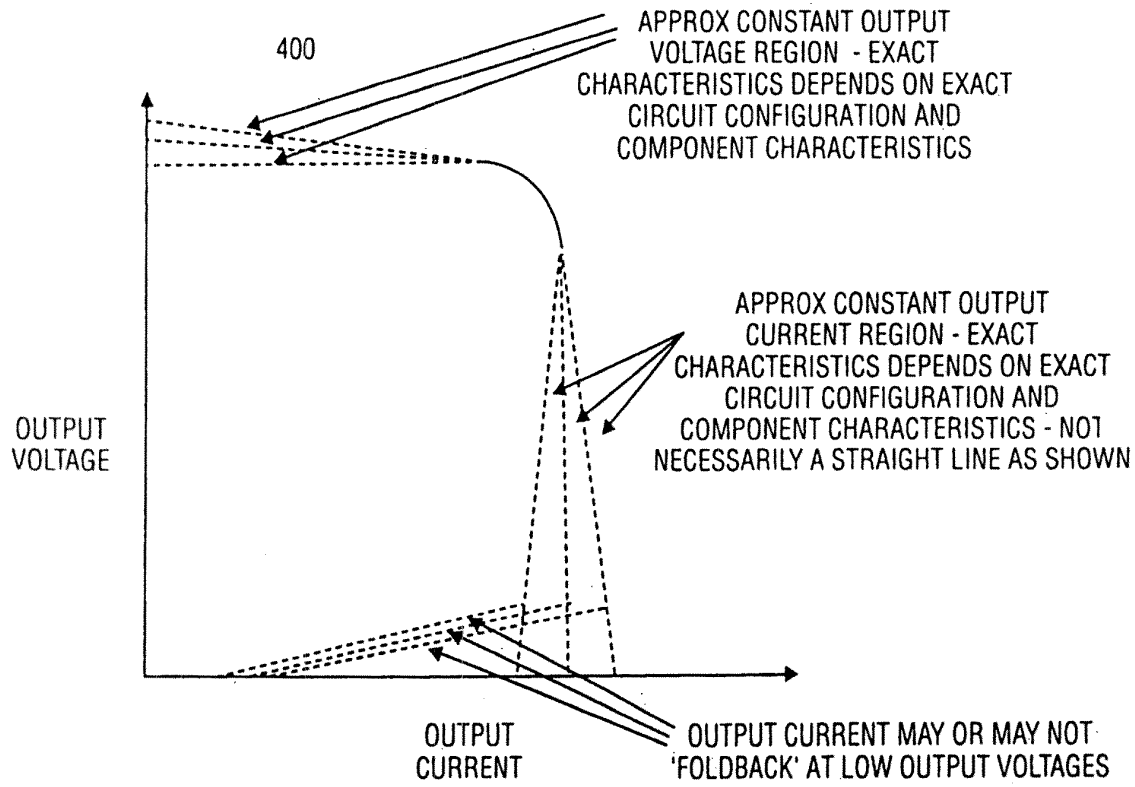
400
APPROX CONSTANT OUTPUT VOLTAGE REGION - EXACT CHARACTERISTICS DEPENDS ON EXACT CIRCUIT CONFIGURATION AND COMPONENT CHARACTERISTICS
APPROX CONSTANT OUTPUT CURRENT REGION - EXACT CHARACTERISTICS DEPENDS ON EXACT CIRCUIT CONFIGURATION AND COMPONENT CHARACTERISTICS - NOT NECESSARILY A STRAIGHT LINE AS SHOWN
OUTPUT VOLTAGE
OUTPUT CURRENT
OUTPUT CURRENT MAY OR MAY NOT 'FOLDBACK' AT LOW OUTPUT VOLTAGES

FIG. 5

Attorney's Docket No.: 005510.P064 PATENT

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below, next to my name.

I believe I am the original, first, and sole inventor (if only one name is listed below) or an original, first, and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

METHOD AND APPARATUS FOR MAINTAINING A CONSTANT LOAD CURRENT WITH LINE VOLTAGE IN A SWITCH MODE POWER SUPPLY

the specification of which

___ is attached hereto.
_X_ was filed on (MM/DD/YYYY) September 23, 2002 as
United States Application Number 10/253,307
or PCT International Application Number ____
and was amended on (MM/DD/YYYY) ____ (if applicable).

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claim(s), as amended by any amendment referred to above.

I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, Section 119(a)-(d), of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s)			Priority Claimed	
Number	Country	(Foreign Filing Date - MM/DD/YYYY)	Yes	No
Number	Country	(Foreign Filing Date - MM/DD/YYYY)	Yes	No
Number	Country	(Foreign Filing Date - MM/DD/YYYY)	Yes	No

I hereby claim the benefit under Title 35, United States Code, Section 119(e) of any United States provisional application(s) listed below:

60/325,642	September 27, 2001
Application Number	(Filing Date – MM/DD/YYYY)
Application Number	(Filing Date – MM/DD/YYYY)

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application:

Application Number	(Filing Date – MM/DD/YYYY)	Status – patented, pending, abandoned

I hereby appoint the persons listed on Appendix A hereto (which is incorporated by reference and a part of this document) as my respective patent attorneys and patent agents, with full power of substitution and revocation, to prosecute this application and to transact all business in the Patent and Trademark Office connected herewith.

Send correspondence to James Y. Go **(Name of Attorney or Agent)**, **BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP, 12400 Wilshire Boulevard 7th Floor, Los Angeles, California 90025 and direct telephone calls to** James Y. Go **(Name of Attorney or Agent)**, **(408) 720-8300.**

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full Name of Sole/First Inventor Balu Balakrishnan

Inventor's Signature Balu Balakrishnan Date 12-6-2002

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Inventor's Signature Alex B. Djenguerian Date 12-11-02

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Full Name of Third/Joint Inventor Kent Wong

Inventor's Signature [signature] Date 12/5/2002

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Full Name of Fourth/Joint Inventor David Michael Hugh Matthews

Inventor's Signature [signature] Date 5th Dec 2002

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Full Name of Fifth/Joint Inventor _____

Inventor's Signature _____ Date _____

Residence _____ (City, State) Citizenship _____ (Country)

Post Office Address _____

Full Name of Sixth/Joint Inventor _____

Inventor's Signature _____ Date _____

Residence _____ (City, State) Citizenship _____ (Country)

Post Office Address _____

Full Name of Seventh/Joint Inventor _____

Inventor's Signature _____ Date _____

Residence _____ (City, State) Citizenship _____ (Country)

Post Office Address _____

APPENDIX A

Ramin Aghevli, Reg. No. 43,462; William E. Alford, Reg. No. 37,764; Farzad E. Amini, Reg. No. 42,261; W. Thomas Babbitt, Reg. No. 39,591; Jordan M. Becker, Reg. No. 39,602; Todd M. Becker, Reg. No. 43,487; Michael A. Bernadicou, Reg. No. 35,934; Roger W. Blakely, Jr., Reg. No. 25,831; R. Alan Burnett, Reg. No. 46,149; Gregory D. Caldwell, Reg. No. 39,926; Thomas M. Coester, Reg. No. 39,637; Robert P. Cogan, Reg. No. 25,049; Florin A. Corie, Reg. No. 46,244; Mimi D. Dao, Reg. No. 45,628; Stephen M. De Klerk, Reg. No. 46,503; Daniel M. De Vos, Reg. No. 37,813; Sanjeet Dutta, Reg. No. 46,145; Tarek N. Fahmi, Reg. No. 41,402; Thomas S. Ferrill, Reg. No. 42,532; George L. Fountain, Reg. No. 37,374; Angelo J. Gaz, Reg. No. 45,907; Andre M. Gibbs, Reg. No. 47,593; James Y. Go, Reg. No. 40,621; Mark A. Goldstein, Reg. No. 50,759; Michael D. Graham, Reg. No. 51,751; Melissa A. Haapala, Reg. No. 47,622; Alan E. Heimlich, Reg. No. 48,808; James A. Henry, Reg. No. 41,064; William E. Hickman, Reg. No. 46,771; Willmore F. Holbrow III, Reg. No. 41,845; Sheryl Sue Holloway, Reg. No. 37,850; George W Hoover II, Reg. No. 32,992; Libby H. Hope, Reg. No. 46,774; Eric S. Hyman, Reg. No. 30,139; William W. Kidd, Reg. No. 31,772; Walter T. Kim, Reg. No. 42,731; Eric T. King, Reg. No. 44,188; Steve Laut, Reg. No. 47,736; Suk S. Lee, Reg. No. 47,745; Gordon R. Lindeen III, Reg. No. 33,192; Jan C. Little, Reg. No. 41,181; Julio Loza, Reg. No. 47,758; Joseph Lutz, Reg. No. 43,765; Lawrence E. Lycke, Reg. No. 38,540; Michael J. Mallie, Reg. No. 36,591; Andre L. Marais, Reg. No. 48,095; Raul D. Martinez, Reg. No. 46,904; Paul A. Mendonsa, Reg. No. 42,879; Jonathan S. Miller, Reg. No. 48,534; Richard A. Nakashima, Reg. No. 42,023; Thien T. Nguyen, Reg. No. 43,835; Thinh V. Nguyen, Reg. No. 42,034; Robert B. O'Rourke, Reg. No. 46,972; Daniel E. Ovanezian, Reg. No. 41,236; Gregg A. Peacock, Reg. No. 45,001; Philip A. Pedigo, Reg. No. P-52,107; Marina Portnova, Reg. No. 45,750; Michael A. Proksch, Reg. No. 43,021; Joseph A. Pugh, Reg. No. P-52,137; James H. Salter, Reg. No. 35,668; William W. Schaal, Reg. No. 39,018; James C. Scheller, Reg. No. 31,195; Saina S. Shamilov, Reg. No. 48,266; Kevin G. Shao, Reg. No. 45,095; Stanley W. Sokoloff, Reg. No. 25,128; Judith A. Szepesi, Reg. No. 39,393; Edwin H. Taylor, Reg. No. 25,129; Lisa Tom, Reg. No. P-52,291; John F. Travis, Reg. No. 43,203; Thomas J. Treutler, Reg. No. 51,126; Kerry D. Tweet, Reg. No. 45,959; Mark C. Van Ness, Reg. No. 39,865; Thomas A. Van Zandt, Reg. No. 43,219; Lester J. Vincent, Reg. No. 31,460; Glenn E. Von Tersch, Reg. No. 41,364; John P. Ward, Reg. No. 40,216; Mark L. Watson, Reg. No. 46,322; Thomas C. Webster, Reg. No. 46,154; and Norman Zafman, Reg. No. 26,250; my patent attorneys, and Brent E. Vecchia, Reg. No. 48,011, and Lehua Wang, Reg. No. 48,023; my patent agents, of BLAKELY SOKOLOFF TAYLOR & ZAFMAN LLP, with offices located at 12400 Wilshire Boulevard, 7th Floor, Los Angeles, California 90025, telephone (310) 207-3800, and James R. Thein, Reg. No. 31,710, my patent attorney with full power of substitution and revocation, to prosecute this application and to transact all business in the Patent and Trademark Office connected herewith.

APPENDIX B

Title 37, Code of Federal Regulations, Section 1.56
Duty to Disclose Information Material to Patentability

(a) A patent by its very nature is affected with a public interest. The public interest is best served, and the most effective patent examination occurs when, at the time an application is being examined, the Office is aware of and evaluates the teachings of all information material to patentability. Each individual associated with the filing and prosecution of a patent application has a duty of candor and good faith in dealing with the Office, which includes a duty to disclose to the Office all information known to that individual to be material to patentability as defined in this section. The duty to disclose information exists with respect to each pending claim until the claim is cancelled or withdrawn from consideration, or the application becomes abandoned. Information material to the patentability of a claim that is cancelled or withdrawn from consideration need not be submitted if the information is not material to the patentability of any claim remaining under consideration in the application. There is no duty to submit information which is not material to the patentability of any existing claim. The duty to disclose all information known to be material to patentability is deemed to be satisfied if all information known to be material to patentability of any claim issued in a patent was cited by the Office or submitted to the Office in the manner prescribed by §§1.97(b)-(d) and 1.98. However, no patent will be granted on an application in connection with which fraud on the Office was practiced or attempted or the duty of disclosure was violated through bad faith or intentional misconduct. The Office encourages applicants to carefully examine:

(1) Prior art cited in search reports of a foreign patent office in a counterpart application, and

(2) The closest information over which individuals associated with the filing or prosecution of a patent application believe any pending claim patentably defines, to make sure that any material information contained therein is disclosed to the Office.

(b) Under this section, information is material to patentability when it is not cumulative to information already of record or being made of record in the application, and

(1) It establishes, by itself or in combination with other information, a prima facie case of unpatentability of a claim; or

(2) It refutes, or is inconsistent with, a position the applicant takes in:

(i) Opposing an argument of unpatentability relied on by the Office, or

(ii) Asserting an argument of patentability.

A prima facie case of unpatentability is established when the information compels a conclusion that a claim is unpatentable under the preponderance of evidence, burden-of-proof standard, giving each term in the claim its broadest reasonable construction consistent with the specification, and before any consideration is given to evidence which may be submitted in an attempt to establish a contrary conclusion of patentability.

(c) Individuals associated with the filing or prosecution of a patent application within the meaning of this section are:

(1) Each inventor named in the application;

(2) Each attorney or agent who prepares or prosecutes the application; and

(3) Every other person who is substantively involved in the preparation or prosecution of the application and who is associated with the inventor, with the assignee or with anyone to whom there is an obligation to assign the application.

(d) Individuals other than the attorney, agent or inventor may comply with this section by disclosing information to the attorney, agent, or inventor.

(e) *In any continuation-in-part application, the duty under this section includes the duty to disclose to the* Office all information known to the person to be material to patentability, as defined in paragraph (b) of this section, which became available between the filing date of the prior application and the national or PCT international filing date of the continuation-in-part application.

Attorney's Docket No. 5510P064C4 PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of:	
Balu Balakrishnan et al.	Examiner: *Not Yet Assigned*
Application No.: *New Patent Application*	Art Unit: *Not Yet Assigned*
Filed: *Concurrently Herewith*	Confirmation No.: *Not Yet Assigned*
For: METHOD AND APPARATUS FOR MAINTAINING A CONSTANT LOAD CURRENT WITH LINE VOLTAGE IN A SWITCH MODE POWER SUPPLY	

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

REQUEST UNDER 37 C.F.R. § 1.32(c)(3) FOR RECOGNITION OF A MAXIMUM OF TEN PRACTITIONERS FROM THOSE NAMED IN DECLARATION AND POWER OF ATTORNEY

Dear Sir/Madam:

Accompanying this Request is a Declaration and Power of Attorney that names more than ten patent practitioners. In accordance with 37 C.F.R. § 1.32(c)(3), applicant(s) hereby request that the following patent practitioners (maximum of ten) from those named in that Declaration and Power of Attorney be recognized by the U.S. Patent and Trademark Office as being of record for the patent application to which the Declaration and Power of Attorney is directed:

Attorney	Reg. No.	Attorney	Reg. No.
James Y. Go	40,621	William W. Shaal	39,018
Edwin H. Taylor	25,129	Gregory D. Caldwell	39,926
Eric S. Hyman	30,139	Mark L. Watson	46,322
Jan Little-Washington	41,181	Michael A. Bernadicou	35,934
Michael J. Mallie	36,591	Todd M. Becker	43,487

If there are any additional charges, please charge Deposit Account No. 02-2666.

Respectfully submitted,

BLAKELY SOKOLOFF TAYLOR & ZAFMAN LLP

Dated: October 16, 2009 /James Y. Go/
James Y. Go
Reg. No. 40,621

1279 Oakmead Parkway
Sunnyvale, CA 94085-4040
(206) 292-8600

CERTIFICATE OF MAILING/TRANSMISSION
I hereby certify that this correspondence is being submitted electronically via EFS Web on the date shown below.

/Kristy A. Marvel/ October 16, 2009

Kristy A. Marvel ***Date***

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:	)	
	)	
Balu Balakrishnan et al.	)	Examiner: *Not yet assigned*
	)	
Application No.: *New Patent Application*	)	Art Unit: *Not yet assigned*
	)	
Filed: *Concurrently Herewith*	)	Confirmation No.: *Not yet assigned*
	)	
For: METHOD AND APPARATUS FOR MAINTAINING A CONSTANT LOAD CURRENT WITH LINE VOLTAGE IN A SWITCH MODE POWER SUPPLY	)	

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Dear Sir:

Enclosed is a copy of Information Disclosure Citation Form PTO-1449 or PTO/SB/08 together with copies of the documents cited on that form. It is respectfully requested that the cited documents be considered and that the enclosed copy of Information Disclosure Citation Form PTO-1449 or PTO/SB/08 be initialed by the Examiner to indicate such consideration and a copy thereof returned to applicant(s).

Pursuant to 37 C.F.R. § 1.97, the submission of this Information Disclosure Statement is not to be construed as a representation that a search has been made and is not to be construed as an admission that the information cited in this statement is material to patentability.

Pursuant to 37 C.F.R. § 1.97, this Information Disclosure Statement is being submitted under one of the following (as indicated by an "X" to the left of the appropriate paragraph):

__X__ 37 C.F.R. §1.97(b).

_____ 37 C.F.R. §1.97(c). If so, then with this Information Disclosure Statement please note the following:

____ Statement pursuant to 37 C.F.R. §1.97(e) or

____ Please charge our deposit account no. 02-2666 for $180.00 for the fee under 37 C.F.R. §1.17(p).

_____ 37 C.F.R. §1.97(d). If so, then enclosed with this Information Disclosure Statement are the following:

(1) A statement pursuant to 37 C.F.R. §1.97(e); and

(2) A check for $_____ for the fee under 37 C.F.R. §1.17(p) for submission of the Information Disclosure Statement.

If there are any additional charges, please charge Deposit Account No. 02-2666.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Date: October 16, 2009

/James Y. Go/
James Y. Go
Reg. No. 40,621

1279 Oakmead Parkway
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CERTIFICATE OF MAILING/TRANSMISSION
I hereby certify that this correspondence is being submitted electronically via EFS Web on the date shown below.

/Kristy A. Marvel/ October 16, 2009

Kristy A. Marvel ***Date***

PTO/SB/06 (12-04)

Filing Date: 10/16/09

Approved for use through 7/31/2006. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 12/581,054

APPLICATION AS FILED – PART I

	(Column 1)	(Column 2)	SMALL ENTITY		OR	OTHER THAN SMALL ENTITY	
FOR	NUMBER FILED	NUMBER EXTRA	RATE ($)	FEE ($)		RATE ($)	FEE ($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	**330**
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	**540**
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	**220**
TOTAL CLAIMS (37 CFR 1.16(i))	**12** minus 20 =		x$26		OR	x$52	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	**1** 2	*	x$110			x$220	
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $270 ($135 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR						
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))			195			390	
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	**1090**

APPLICATION AS AMENDED – PART II

		(Column 1)		(Column 2)	(Column 3)	SMALL ENTITY		OR	OTHER THAN SMALL ENTITY	
		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE ($)	ADDI-TIONAL FEE ($)		RATE ($)	ADDI-TIONAL FEE ($)
AMENDMENT A	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))							OR		
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))					N/A		OR	N/A	
						TOTAL ADD'T FEE		OR	TOTAL ADD'T FEE	

		(Column 1)		(Column 2)	(Column 3)			OR		
		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE ($)	ADDI-TIONAL FEE ($)		RATE ($)	ADDI-TIONAL FEE ($)
AMENDMENT B	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))							OR		
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))					N/A		OR	N/A	
						TOTAL ADD'T FEE		OR	TOTAL ADD'T FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.