[54] **DATA COMMUNICATION SYSTEM WITH RANDOM AND BURST ERROR PROTECTION AND CORRECTION**

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[51] Int. Cl.$^2$ ............................................. G06F 11/12
[52] U.S. Cl. ........................................ **340/146.1 AL**
[58] **Field of Search** .................. 340/146.1, 146.1 AL, 340/146.1 D, 146.1 AG, 146.1 C; 325/163, 41

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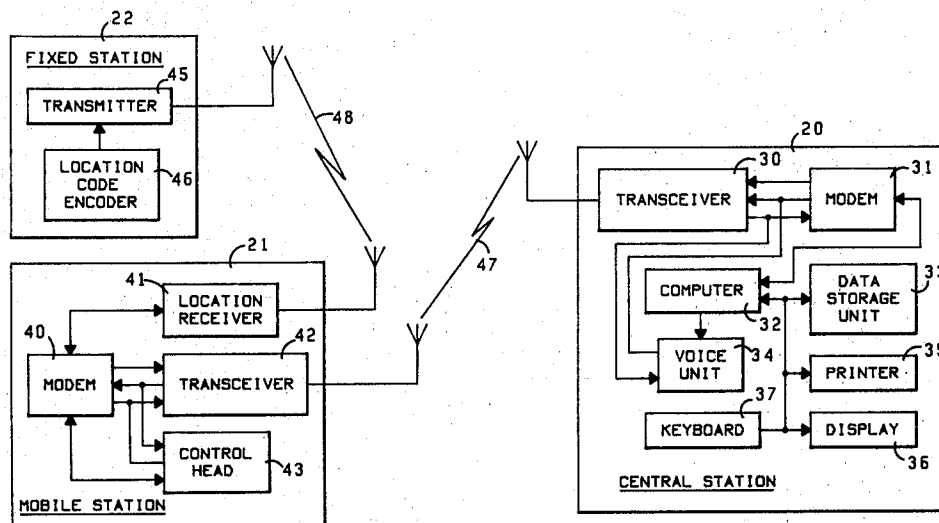
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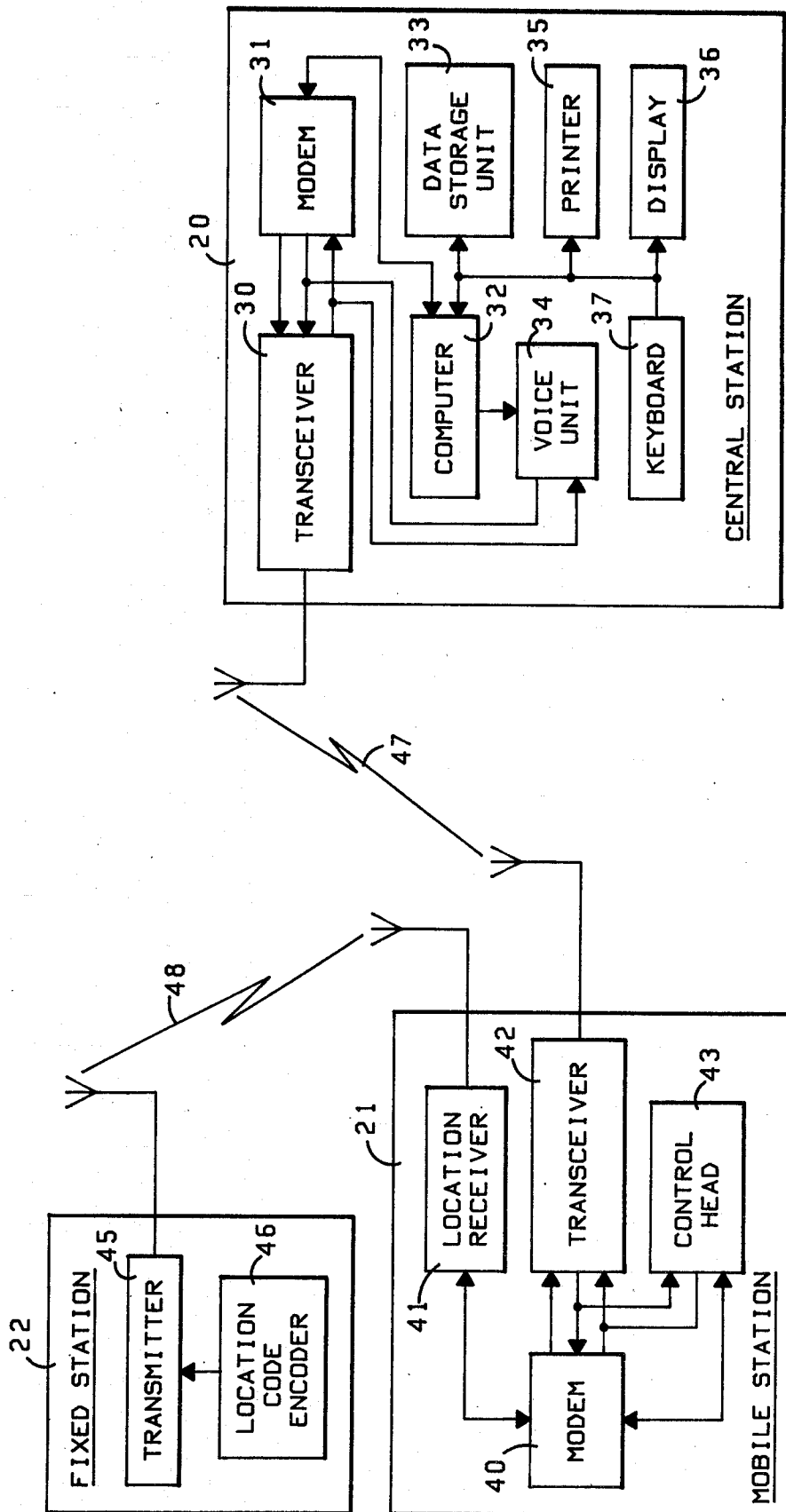
*Primary Examiner*—Charles E. Atkinson
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[57] **ABSTRACT**

A data communication system for use in the control and monitoring of mobile stations, for example, in a bus monitoring system, from a central station over a communication channel carrying both data and voice information. Information is encoded into digital messages having a start code followed by one or more data blocks. The start code identifies the beginning of the data block that follows and enables synchronization of clock circuitry to the received data frequency. The data blocks have N digital words with M binary bits where one word is a parity word and N-1 words are data words. Each of the data words has a data portion and parity portion coded for correction of at least one error. Reliability is enhanced by a data detector which discriminates between data and noise or voice to provide an indication of the presence of data. In transmitting the digital messages, the bits of the N words in each data block are interleaved to provide protection against error bursts.
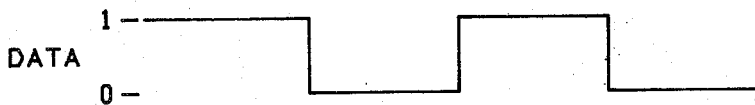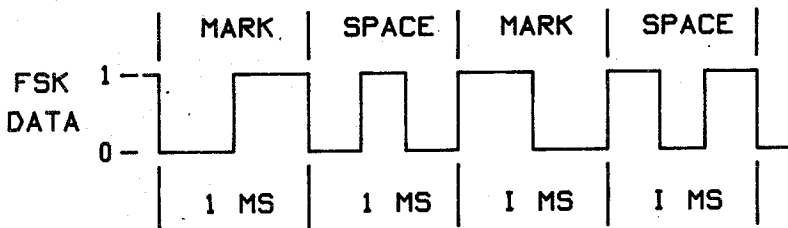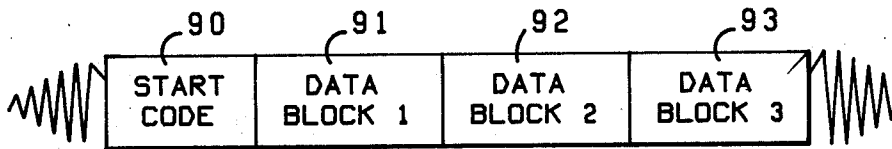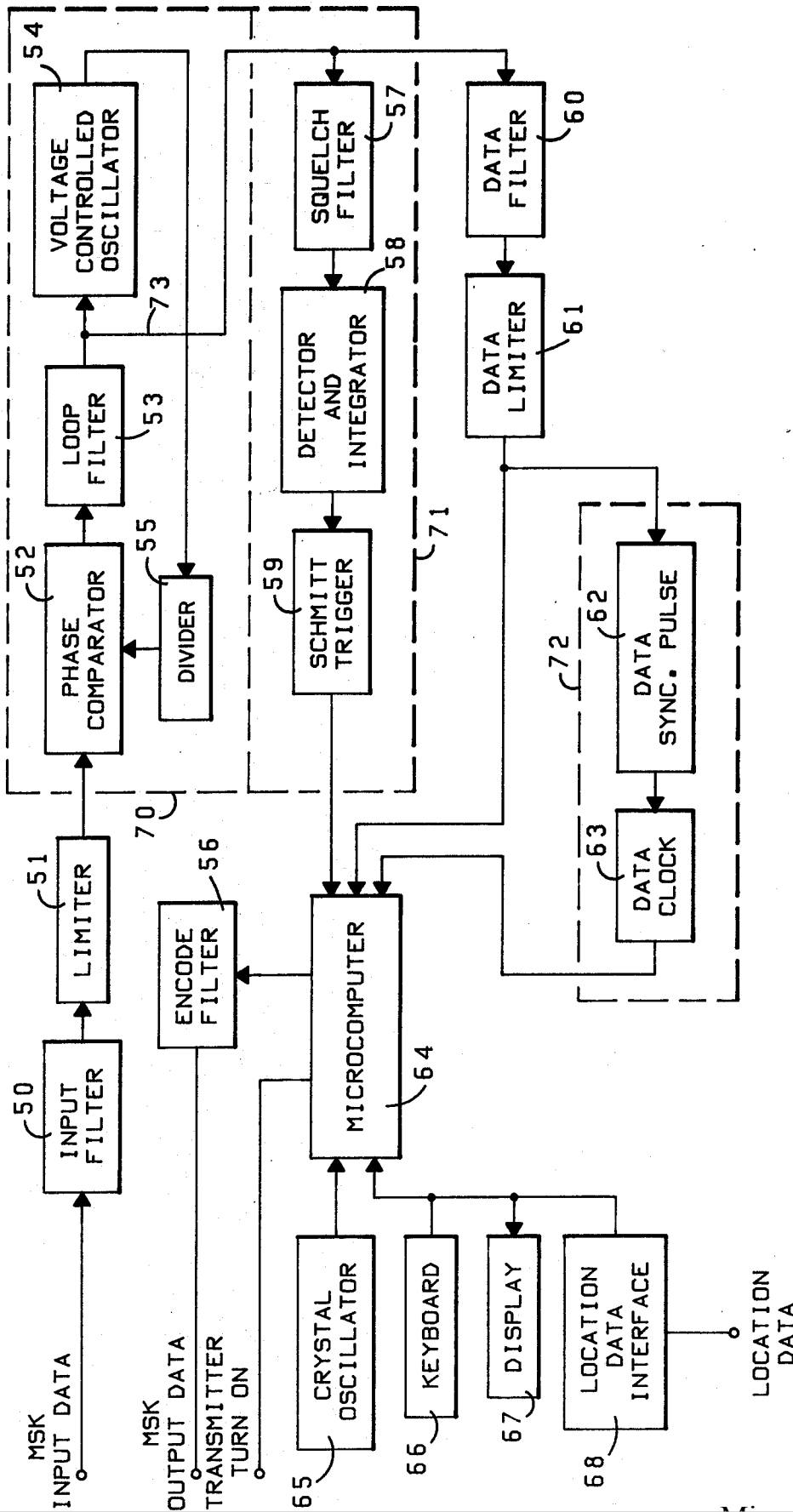
**8 Claims, 12 Drawing Figures**

FIG. 1

CENTRAL STATION

20

30 TRANSCEIVER
31 MODEM
33 DATA STORAGE UNIT
35 PRINTER
36 DISPLAY
32 COMPUTER
34 VOICE UNIT
37 KEYBOARD

47

48

FIXED STATION

22

45 TRANSMITTER
46 LOCATION CODE ENCODER

MOBILE STATION

21

42 LOCATION RECEIVER
TRANSCEIVER
43 CONTROL HEAD
41
40 MODEM

| D1 | D2 | D3 | D4 | P1 | P2 | P3 |
|-----|-----|-----|-----|-----|-----|-----|
| D5 | D6 | D7 | D8 | P4 | P5 | P6 |
| D9 | D10 | D11 | D12 | P7 | P8 | P9 |
| D13 | D14 | D15 | D16 | P10 | P11 | P12 |
| D17 | D18 | D19 | D20 | P13 | P14 | P15 |
| D21 | D22 | D23 | D24 | P16 | P17 | P18 |
| VP1 | VP2 | VP3 | VP4 | VP5 | VP6 | VP7 |

~80

Fig. 3

| START CODE | DATA BLOCK 1 | DATA BLOCK 2 | DATA BLOCK 3 |
|-----|-----|-----|-----|
| 90 | 91 | 92 | 93 |

Fig. 2

MARK | SPACE | MARK | SPACE

FSK DATA

1 MS | 1 MS | I MS | I MS

Fig. 4A

DATA

Fig. 4B

Fig. 5

AMPLITUDE

121

120

0    500    1000    1500    2000

FREQUENCY

Fig. 6

PLL
ERROR
VOLTAGE

71

57    +5V    58    +9V    59

SQUELCH
OUTPUT

Fig. 7

72

RECOVERED
INPUT DATA

62    63    +9V

154

152

150

151

155

156

DATA
CLOCK

Fig. 8
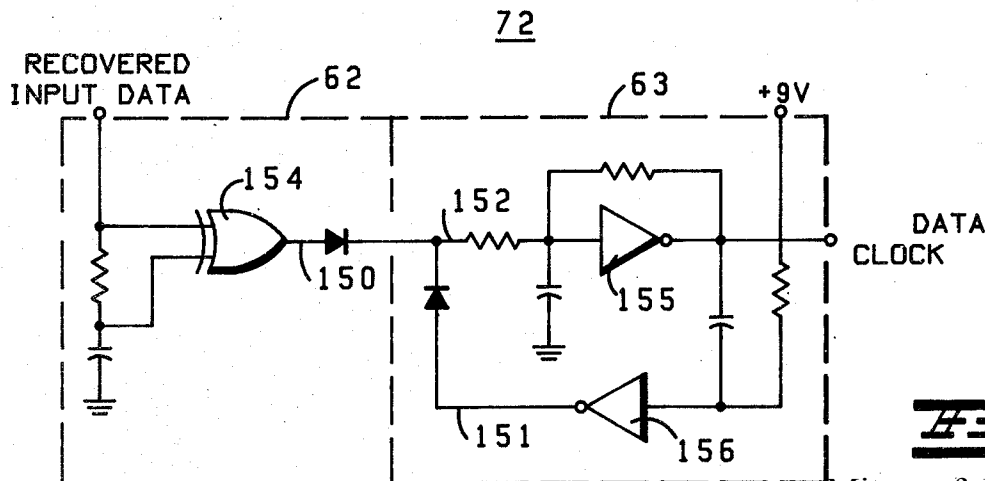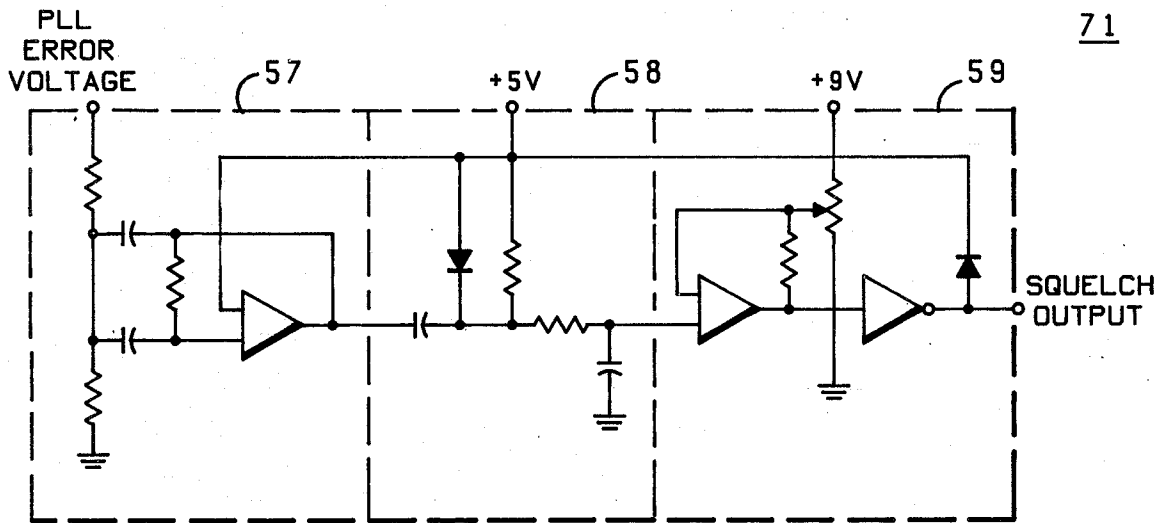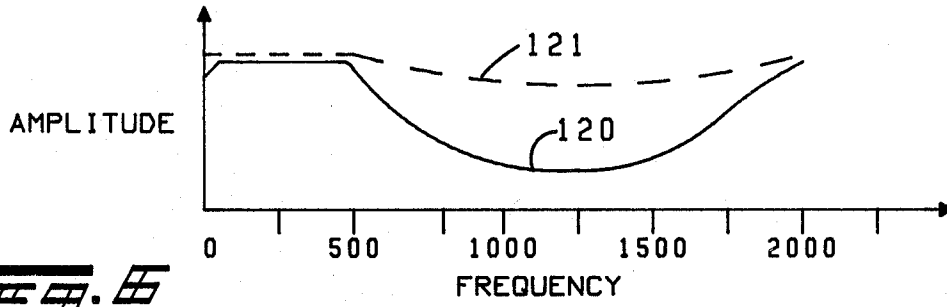
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