UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

APPLE INC.,
Petitioner,

v.

LIMESTONE MEMORY SYSTEMS LLC,
Patent Owner.

Case IPR2016-01567
Patent No. 5,894,441

PETITION FOR *INTER PARTES* REVIEW

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Patent Trial and Appeal Board
U.S. Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450
Submitted Electronically via the Patent Review Processing System

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TABLE OF EXHIBITS

Exhibit #	Exhibit Description
1001	Declaration of Dr. Pinaki Mazumder
1002	Curriculum Vitae of Dr. Pinaki Mazumder
1003	U.S. Patent No. 5,894,441
1004	File History for U.S. Patent No. 5,894,441
1005	U.S. Patent No. 5,265,055 to Horiguchi
1006	U.S. Patent No. 5,126,973 to Gallia
1007	*Inter Partes* Review No. IPR2016-00094, Petition for *Inter Partes* Review filed October 27, 2015 (without exhibits)
1008	U.S. Patent No. 5,270,975 to McAdams
1009	Japanese Patent Appl. No. H06-052696 to Minami
1010	*Inter Partes* Review No. IPR2016-00094, Patent Owner's Preliminary Response filed January 27, 2016
1011	*Inter Partes* Review No. IPR2016-00094, Decision Denying Institution filed April 12, 2016
1012	U.S. Patent No. 5,956,285 to Watanabe
1013	Masashi Horiguchi et al., *A Flexible Redundancy Technique for High-Density DRAMs*, IEEE JOURNAL OF SOLID-STATE CIRCUITS, Vol. 26, No. 1, Jan. 1991, at 12-17
1014	U.S. Patent No. 5,267,214 to Fujishima
1015	U.S. Patent No. 5,349,556 to Lee
1016	U.S. Patent No. 5,355,339 to Oh
1017	U.S. Patent No. 5,359,560 to Suh

1018	U.S. Patent No. 5,798,974 to Yamagata
1019	U.S. Patent No. 5,808,948 to Kim
1020	Masashi Horiguchi, *Redundancy Techniques for High-Density DRAMs*, INNOVATIVE SYSTEMS IN SILICON CONFERENCE, Oct. 1997, at 22-29
1021	Masashi Horiguchi et al., NANOSCALE MEMORY REPAIR (Springer 2011)
1022	Robert T. Smith et al., *Laser Programmable Redundancy and Yield Improvement in a 64 K DRAM*, IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. SC-16, NO. 5, Oct. 1981, at 506-14

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