Redundancy Techniques for High-Density DRAMs

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Abstract

This paper describes the redundancy techniques for high-density DRAMs to solve the following two problems arisen with the increase in memory capacity: (1) the increase in memory-array division reduces the replacement flexibility between defective lines and spare lines; (2) the defects causing DC-characteristics faults, especially excessive standby current faults cannot be repaired with the conventional redundancy techniques. First, two approaches to solve the first problem are discussed: enhancing the replacement flexibility within the limits of intra-subarray replacement, and the introduction of inter-subarray replacement. Next, the recent proposals to solve the second problem are reported. The DC-characteristics faults are repaired through the modification of bitline precharge circuit or the subarray-replacement redundancy

1. Introduction

Redundancy techniques have been widely used as effective methods of enhancing the production yield and reducing cost-per-bit of DRAMs since 64 - 256-kbit generations [1] - [5]. The currently used technique replaces defective memory elements (usually wordlines and/or bitlines (datalines)) by on-chip spare elements as shown in Fig. 1. However, with the increase in memory capacity, the following two problems have arisen.

One is the increase in memory-array division shown in Fig. 2. The number of subarrays doubled each generation before 64-Mbit. This is mainly due to the bitline division for the signal/noise ratio enhancement and the charging/discharging current reduction [6], [7]. The number of divisions even quadrupled each generation after the introduction of hierarchical wordline architecture [8], [9]. The boundaries between subarrays work as barriers to the defective-element replacement, and reduces the replacement flexibility, resulting in yield degradation.

The other problem is the defects causing DC-characteristics faults, especially excessive standby current (I_{SB}) faults. An example of an I_{SB} fault is shown in Fig. 3 [10]. A short circuit between a wordline (electrically connected to the ground in the standby state) and a bitline (connected to the bitline precharge voltage, $V_{DD}/2$) creates an

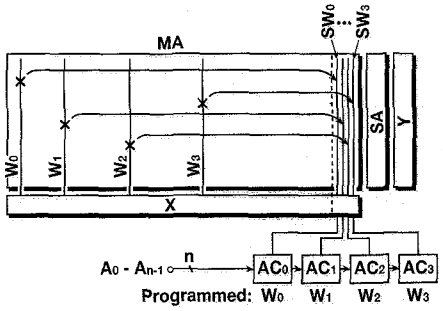

Fig. 1 Conventional redundancy technique applied to a DRAM.

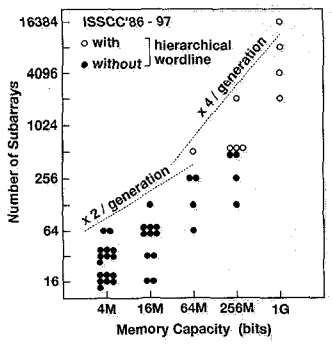

Fig. 2 Trend of memory-array division.

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illegal DC current path from $V_{DD}/2$ to ground. Replacing the wordline (bitline) by a spare wordline (spare bitline) inhibits the defective line from being accessed, but the current path still remains. Thus, the fault is not repaired by the conventional redundancy technique.

This paper describes the redundancy techniques to solve these problems. First, the flexibility enhancement within the limits of intra-subarray replacement is discussed in Section 2. Second, the inter-subarray replacement techniques are described in Section 3. The recent proposals to repair the DC-characteristics faults are reported in Section 4.

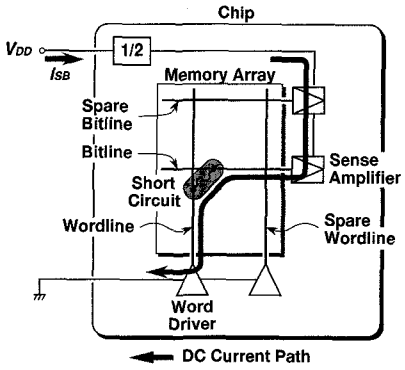


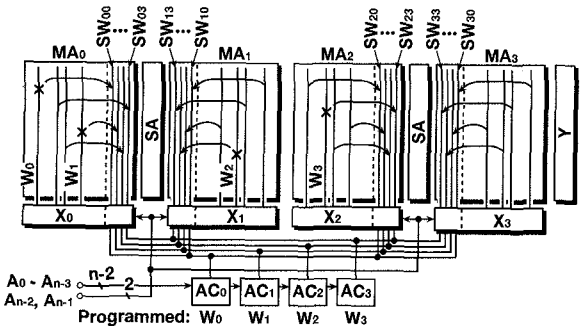
Fig. 3 *ISB* fault model.

2. Intra-subarray replacement redundancy

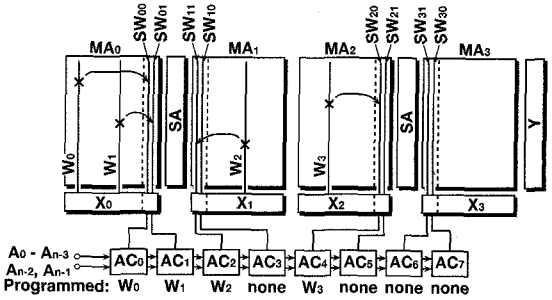
Fig. 1 shows the well-known redundancy technique [3], [5] applied to a DRAM without memory-array division. Redundant bitlines are omitted here for simplicity. The memory has L (here, $L = 4$) spare wordlines SW0 - SW3 and as many address comparators AC0 - AC3. Defective word addresses are programmed (usually by fuses) in the address comparators and compared with the input address. Thus, at most L defective normal wordlines can be repaired. In this example, defective normal wordlines W0 - W3 are replaced by spare wordlines SW0 - SW3, respectively, as shown by the arrows in the figure.

Now let us consider dividing the memory array into subarrays. Two approaches within the limits of intra-subarray replacement are shown in Fig. 4(a) and (b). Here the memory array MA in Fig. 1 is divided into four subarrays, MA0 - MA3, only one of which is selected.

In the simultaneous replacement (Fig. 4(a)), the



(a) simultaneous replacement



(b) individual replacement

Fig. 4 Conventional intra-subarray replacement redundancy techniques applied to a DRAM with memory-array division.

number of address comparators equals L, the number of spare wordlines in a subarray. Each address comparator compares only the intra-subarray address signals (here, A0 - An-3), and the output is commonly supplied to all the subarrays. The inter-subarray address signals (here, An-2 and An-1) in turn select one of the four spare wordlines. As many defective wordlines can be repaired as are shown in Fig. 1, if L is the same as that of Fig. 1. In this approach four normal lines are replaced simultaneously by spare lines. That is, to replace one defective normal line, three other normal lines with the same intra-subarray address are also replaced even if they are not defective. This causes the following problems. First, the usage efficiency of spare lines is lower, and the number of spare lines should be larger, which results in chip-area increase. Second, the probability of unsuccessful repair due to defects in the spare lines that replaced normal lines is higher, which results in yield degradation.

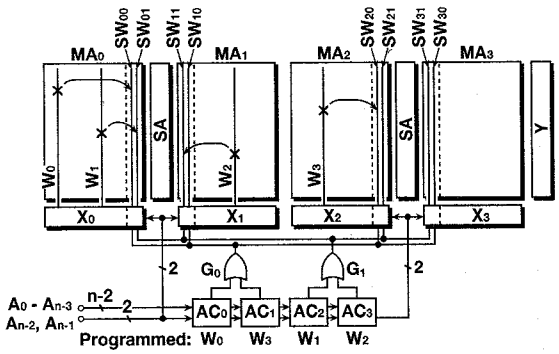
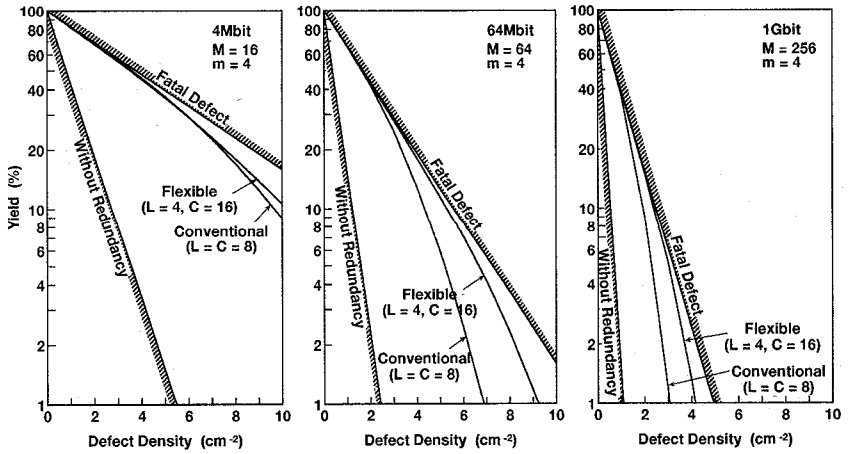


Fig. 5 Flexible intra-subarray replacement redundancy technique applied to a DRAM with memory-array division.

In the individual replacement (Fig. 4(b)), every spare line in every subarray has its own address comparator. The number of address comparators is therefore $L*M$, where M (= 4) is the number of subarrays. Each address comparator compares both intra- and inter-subarray address signals. This approach has the following advantages over the simultaneous replacement. First, a smaller L is statistically required (here, $L = 2$) to repair as many defects. This is because the probability of clustered defects in a particular subarray is small under random defect distribution. Second, since only one normal line is at a time replaced by a spare line, the probability of a defect in the spare line is lower. This approach, however, has the



(a) 4-Mbit DRAM (b) 64-Mbit DRAM (c) 1-Gbit DRAM

Fig. 6 Calculated DRAM yield with conventional and flexible intra-subarray replacement redundancy techniques.

disadvantage of lower usage efficiency of address comparators, resulting in an increase in the area of address comparators.

Fig. 5 shows the flexible intra-subarray replacement scheme [11] proposed to overcome the problems described above. The spare lines and address comparators are not connected directly, but through the OR gates G0 and G1. Each address comparators compares both intra- and inter-subarray address signals. This connection provides a flexible relationship between spare lines and address comparators. In the architecture shown in Fig. 4, this relationship is fixed so that a spare line can be activated only by a particular address comparator. However in Fig. 5, a spare line can be activated by one of several address comparators. Another advantage of this architecture is that more flexible selection of the number of address comparators C. as well as the relationship $L \leq C \leq L*M/m$ stands, where m is the number of subarrays in which defective normal lines are simultaneously replaced by spare lines.

The calculated yield through the conventional (Fig. 4(a)) and flexible (Fig. 5) intra-subarray replacement redundancy techniques is shown in Fig. 6. The yield improvement factors through the both techniques are almost the same in a 4-Mbit DRAM. The advantage of the flexible technique becomes apparent in 64-Mbit and 1-Gbit DRAMs, especially for a large defect density, that is, in the early stages of production. For a 1-Gbit DRAM, however, the yield is determined mainly by fatal defects, such as those causing excessive standby current.

When the flexible intra-subarray replacement is applied to bitline redundancy, the problem of a 'global' defect (a defect over two or more subarrays) arises. A defect on a sense-amplifier or a column selection line (CSL) in a DRAM using the multidivided bitline architecture [6], [7] causes two or more bitlines to fail simultaneously as shown in Fig. 7. Thus these types of defects are 'global' and require more than one address comparators to be repaired. To solve this problem, programming "don't-care" values in address comparators was proposed [11]. Table I shows the number of address comparators required to repair the various defects with and without "don't-care" programming.

The access-time penalty due to redundancy is the delay time required for the address comparison. Fig. 8

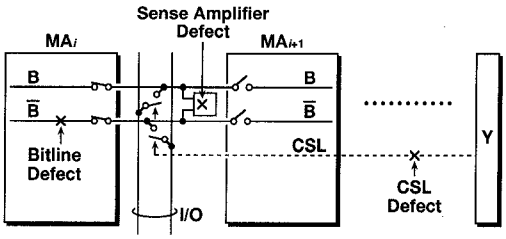


Fig. 7 Defect modes in memory array using multidivided bitline architecture.

Table I Number of address comparators required to repair defects.

Defect mode	Number of address comparators	
	with "don't-care" programming	without "don't-care" programming
Bitline	1	1
Sense amp.	1	2
CSL	1	n*

*n: number of subarrays connected to a CSL

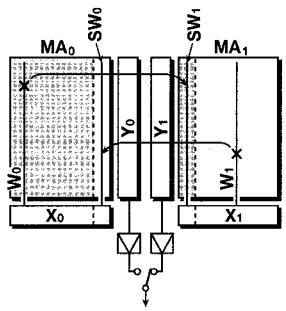


Fig. 8 No access-penalty intra-subarray replacement redundancy technique [12] (simultaneous activation of normal and spare lines).

shows a technique to eliminate this delay time for a high-speed SRAM [12]. In this technique, a defective line in a subarray is replaced by a spare line in the adjacent subarray. The two subarrays are activated simultaneously and one of the data from them is selected according to the result of address comparison. This technique is difficult to be applied to wordline redundancy of a DRAM because of the doubling of the bitline charging/discharging current. However, it can be applied to bitline redundancy [13]. Note that this technique is *not* inter-subarray replacement. This will be clear if the hatched areas in Fig. 8 are assumed to be a subarray and the white areas are assumed to be another subarray.

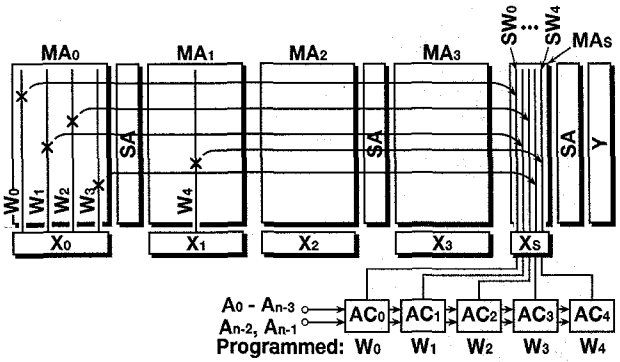
3. Inter-subarray replacement redundancy

With the further increase in memory-array division, the probability of clustered defects in a particular subarray becomes no more negligible. In the intra-subarray replacement, the number of spare lines in a subarray, L, must be larger or equal to the maximum number of defective lines in a subarray to repair clustered defects. This causes the increase in L and chip-area penalty.

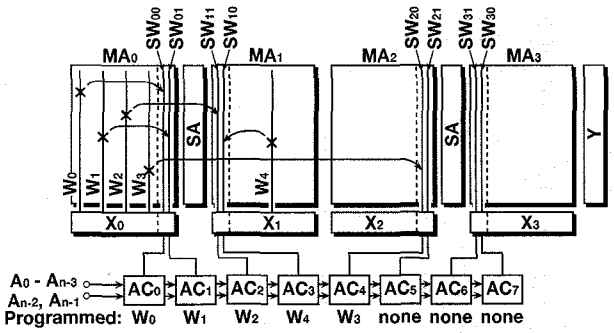
To solve this problem, inter-subarray replacement redundancy techniques [14] - [16] were proposed, which permit a defective line to be replaced by a spare line in any subarray. They are classified into two categories as shown in Fig. 9.

In the distributed-spare-line approach [14] shown in Fig. 9(a), each subarray has its own spare lines like the intra-subarray replacement. Each spare line, however, can replace any defective normal line not only in the same subarray but also in another subarray. Therefore at most $L*M$ defects clustered in a particular subarray can be repaired, where M is the number of subarrays. In this example, four clustered defective normal wordlines W0 - W3 are replaced by the spare wordlines in subarrays MA0, MA1 and MA2. It is sufficient for successful repair that the number L is the average number of defective lines in a subarray and is smaller than that of intra-subarray replacement. The number of address comparators C is equal to $L*M$ in this case. The number, however, can be reduced through the similar technique shown in Fig. 5.

In the concentrated-spare-line approach [15], [16] shown in Fig. 9(b), each subarray has no spare lines. There is a spare subarray MAS, instead, composed of L' (here, $L' = 5$) spare lines. Each spare line can replace a defective normal line in any subarray. Therefore at most



(a) distributed spare lines



(b) concentrated spare lines

Fig.9 Inter-subarray replacement redundancy techniques.

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