[54] ROW REDUNDANCY CIRCUIT OF A SEMICONDUCTOR MEMORY DEVICE

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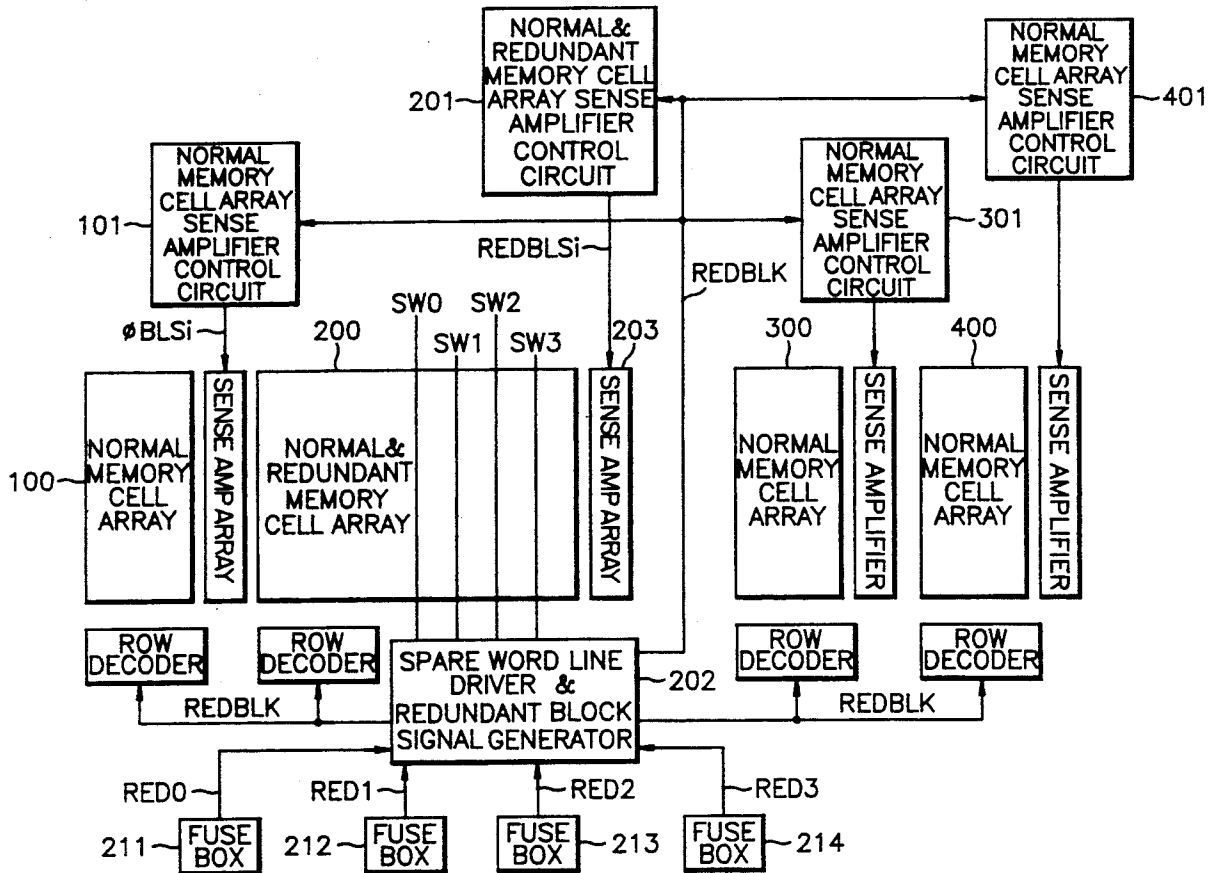Primary Examiner—Eugene R. LaRoche
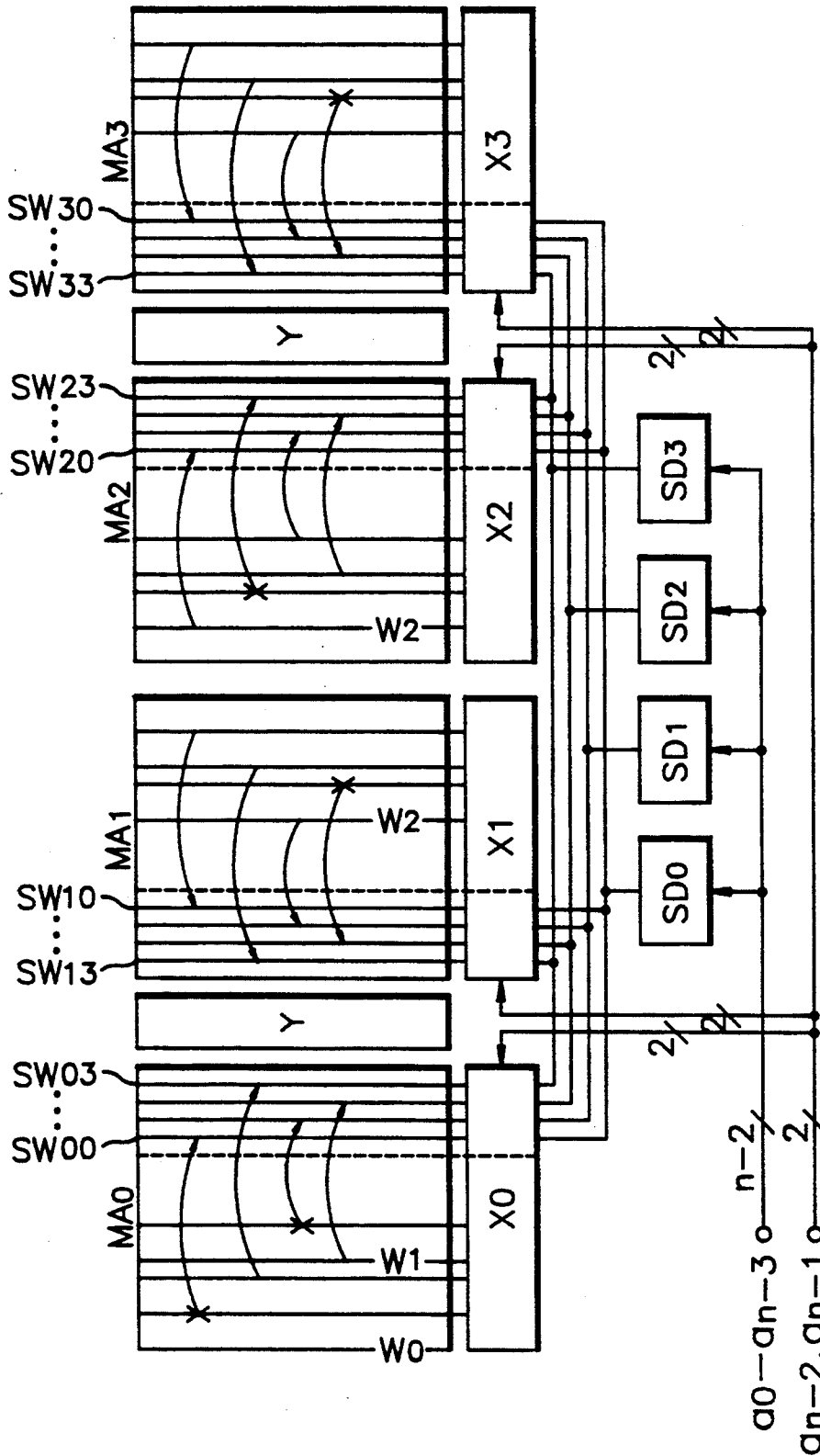Assistant Examiner—Son Dinh
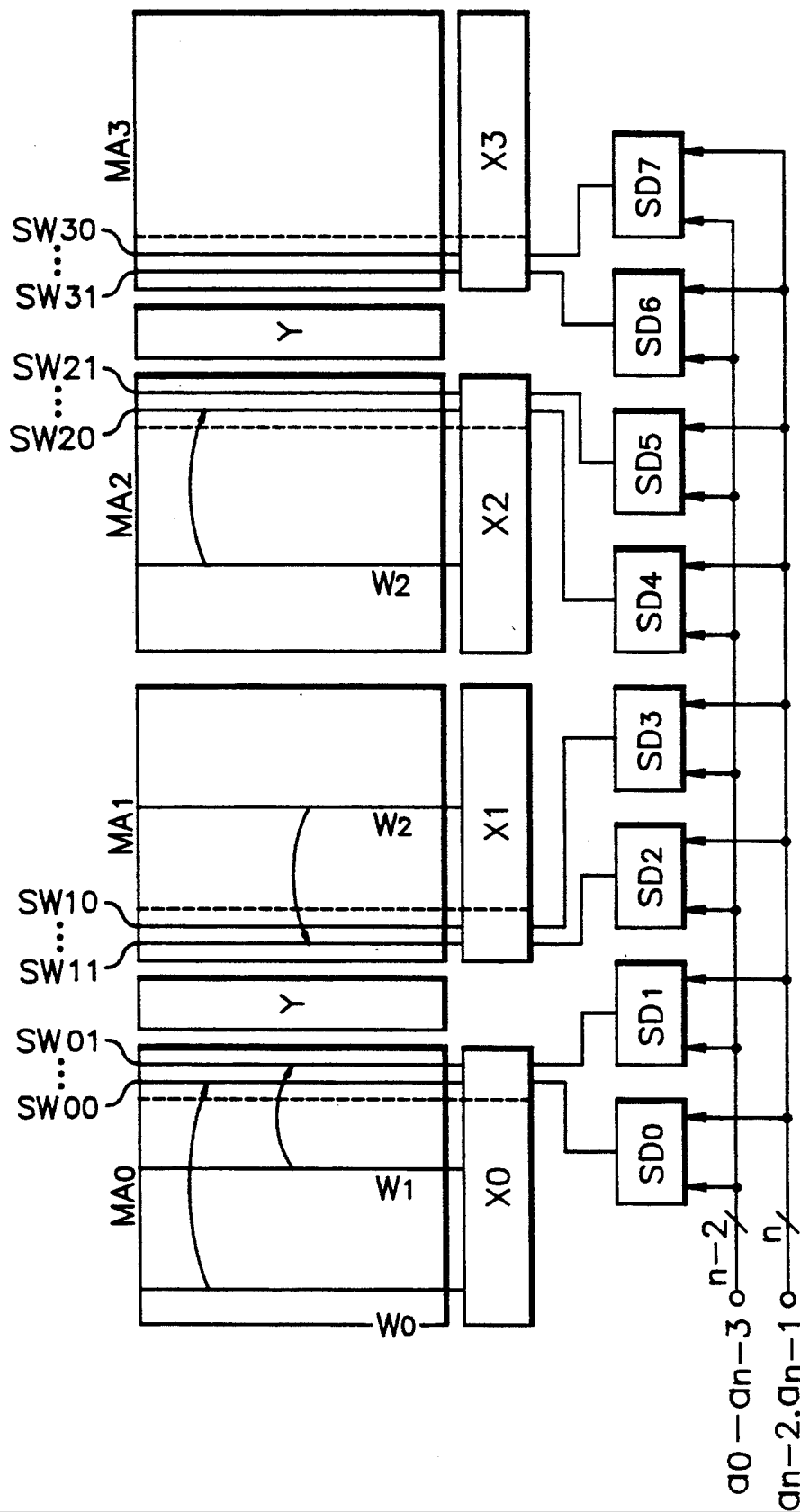Attorney, Agent, or Firm—Cushman, Darby & Cushman

[57] ABSTRACT

Disclosed is a semiconductor device with redundancy for replacing a memory cell with a predetermined defect with additional spare cells. In a semiconductor memory device having a plurality of normal submemory arrays, the present invention discloses a redundancy technique that allows any redundant address decoder to be used with any of the submemory arrays. This maximizes efficiency in redundant repairs as well as maximizes the use of the chip area.
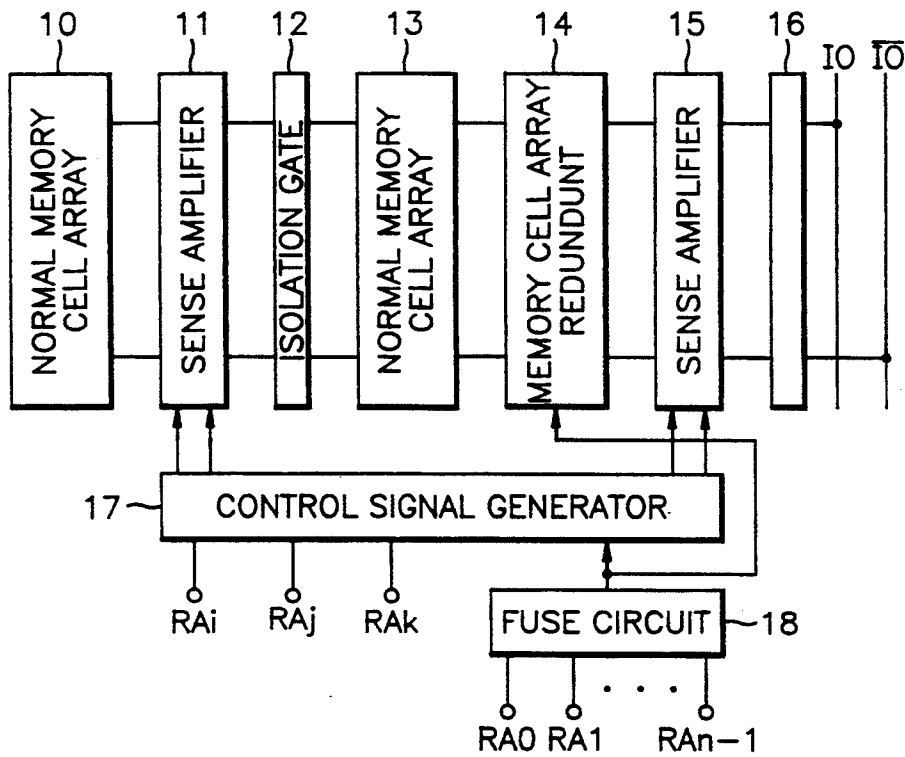
11 Claims, 10 Drawing Sheets
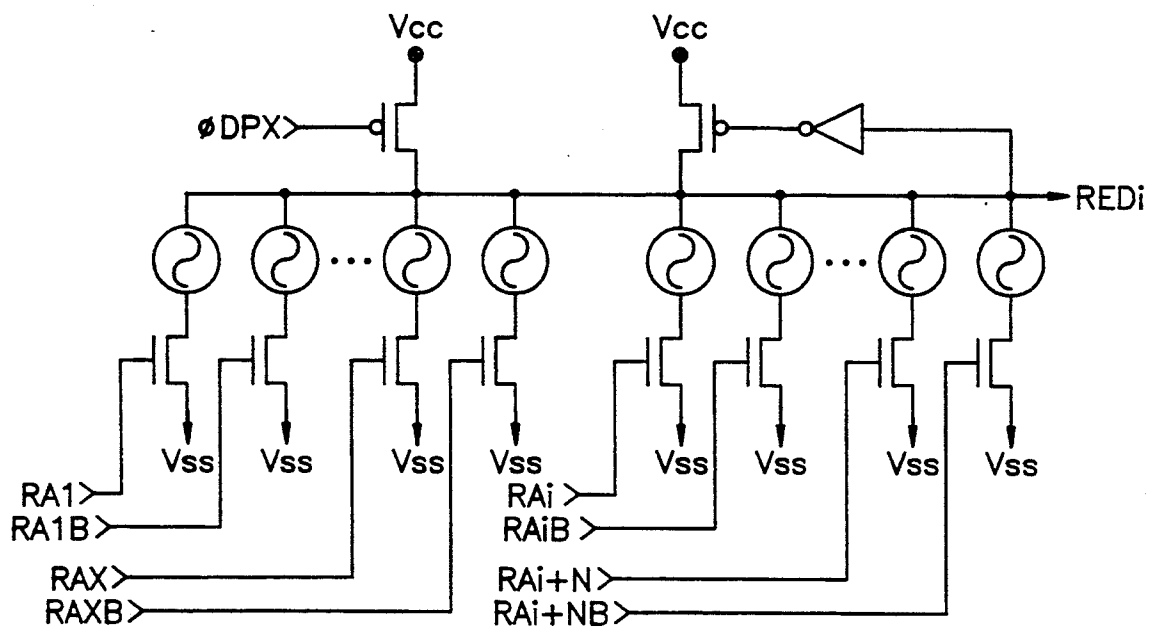
(PRIOR ART)
FIG. 1

(PRIOR ART)
FIG. 2

(PRIOR ART)

FIG. 3

FIG. 5

FIG. 4

DOCKET ALARM
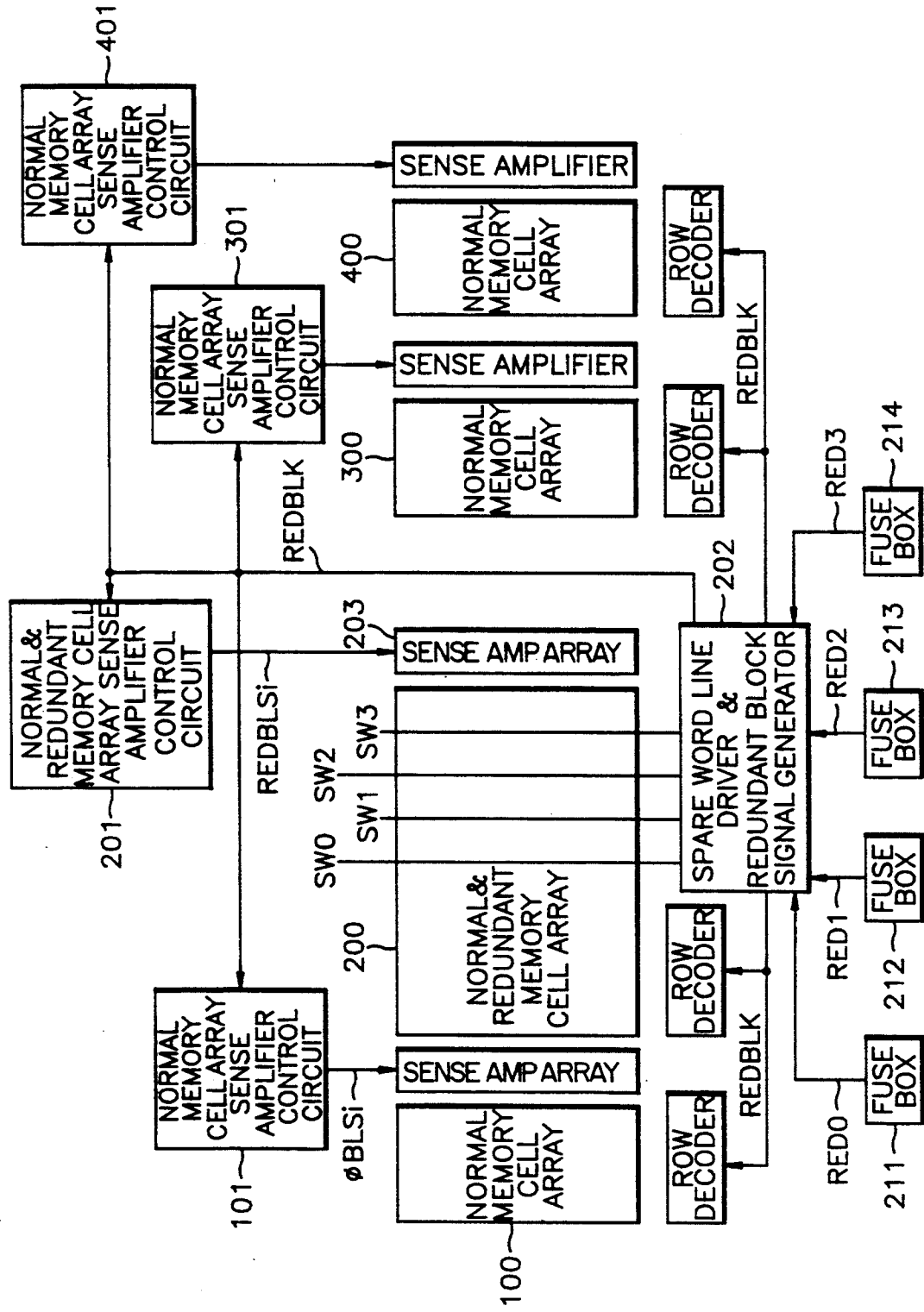
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