



[54] SYNCHRONOUS SEMICONDUCTOR MEMORY DEVICE WITH MULTI-BANK CONFIGURATION

5,621,693 4/1997 Nakase ..... 365/190

FOREIGN PATENT DOCUMENTS

6-243674 9/1994 Japan .

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[57] ABSTRACT

[21] Appl. No.: 08/798,953

Memory blocks provided to share a sense amplifier bank, a global IO (GIOB) bus provided in common to the memory blocks for transferring internal data, and local IO bus lines provided corresponding to the memory blocks are connected-controlled based on signals related to a column select operation. Driving memory blocks independently from each other permits each memory block to be used as a bank, and if one memory block is accessed during activation of another memory block, data can be prevented from colliding on the global IO bus. A main memory with high page hit rate is implemented using a semiconductor memory device with a shared-sense amplifier configuration. When a memory block sharing a sense amplifier coupled to another memory block is addressed, the another memory block is inactivated and then addressed memory block is accessed, when a valid data is output, such valid data outputting is signaled by a data valid signal.

[22] Filed: Feb. 11, 1997

[30] Foreign Application Priority Data

Apr. 22, 1996 [JP] Japan ..... 8-100122

[51] Int. Cl.<sup>6</sup> ..... G11C 8/00

[52] U.S. Cl. .... 365/230.03; 365/196

[58] Field of Search ..... 365/230.03, 196, 365/191, 190

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9 Claims, 18 Drawing Sheets

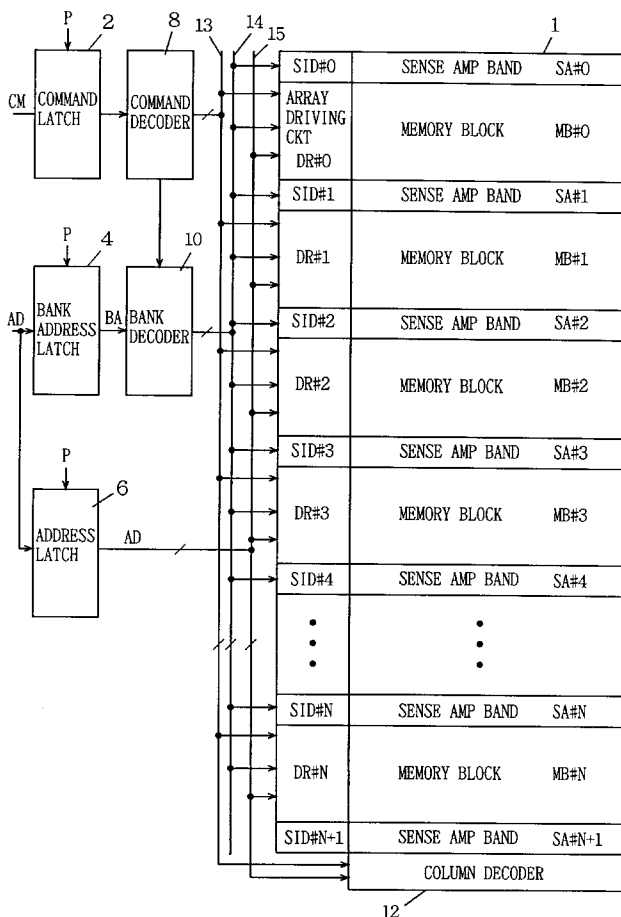


FIG. 1

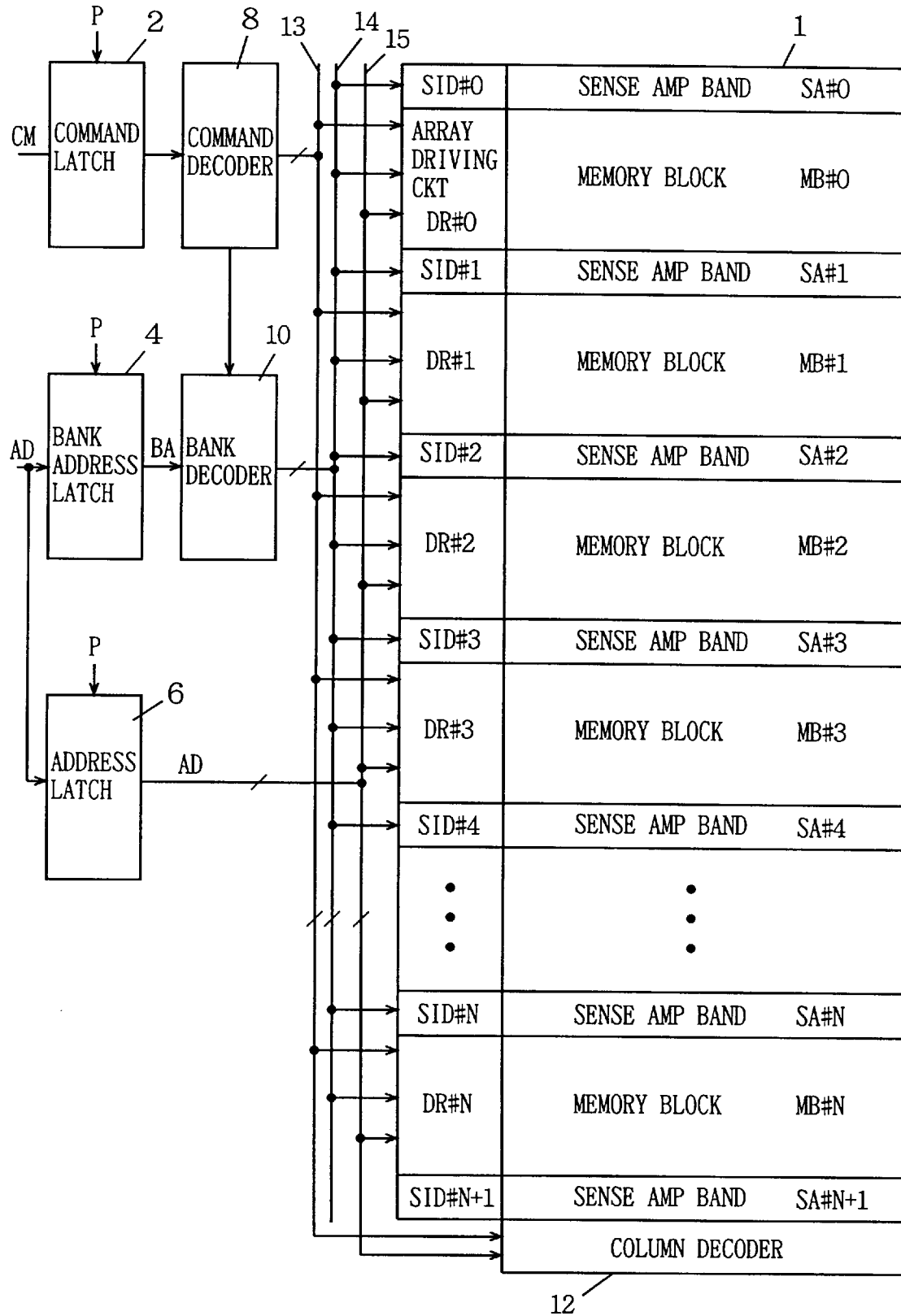


FIG. 2

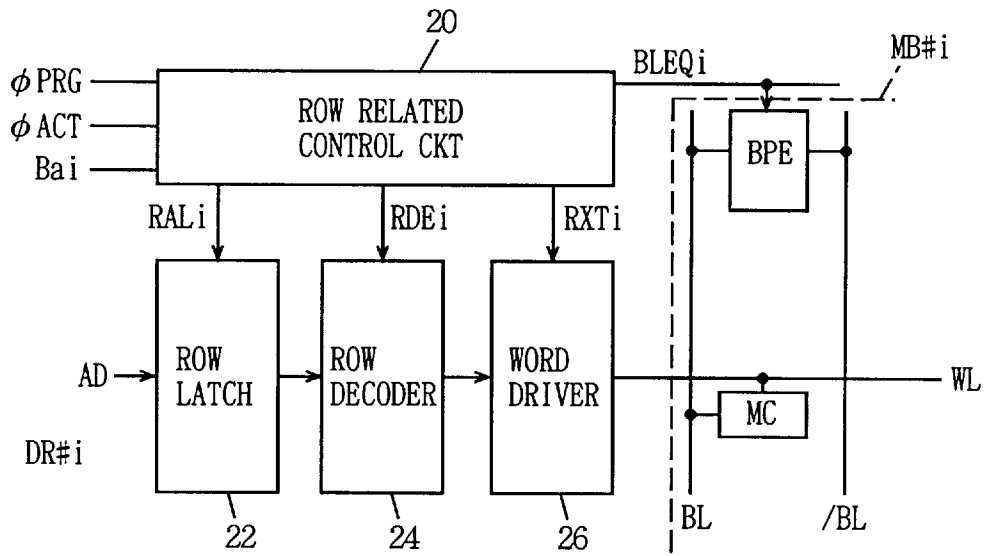


FIG. 3

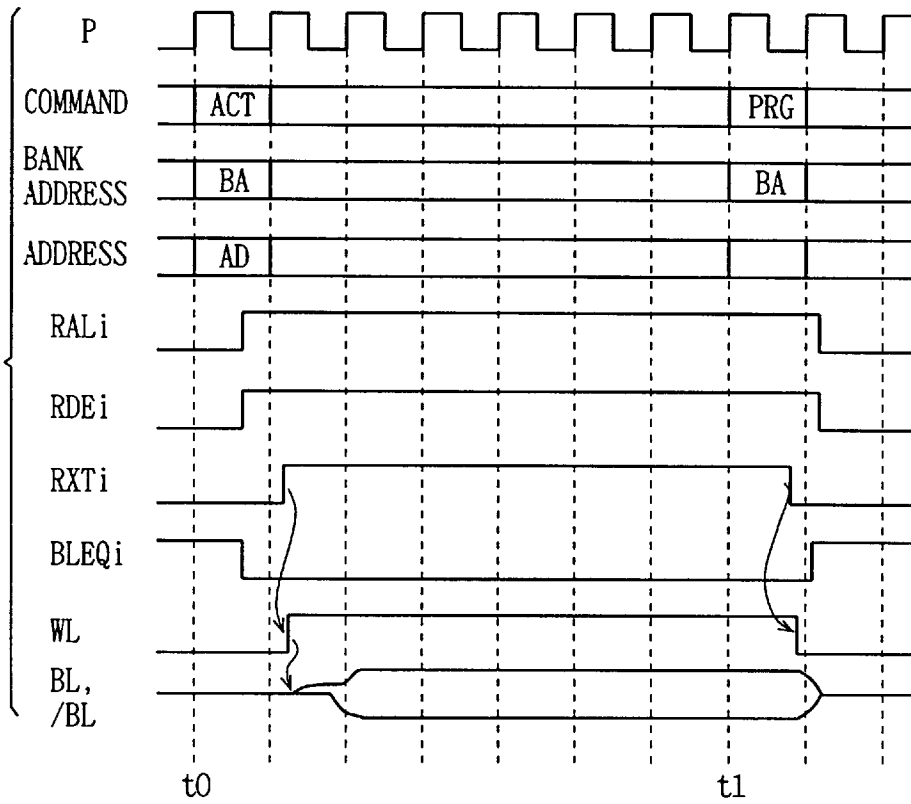


FIG. 4

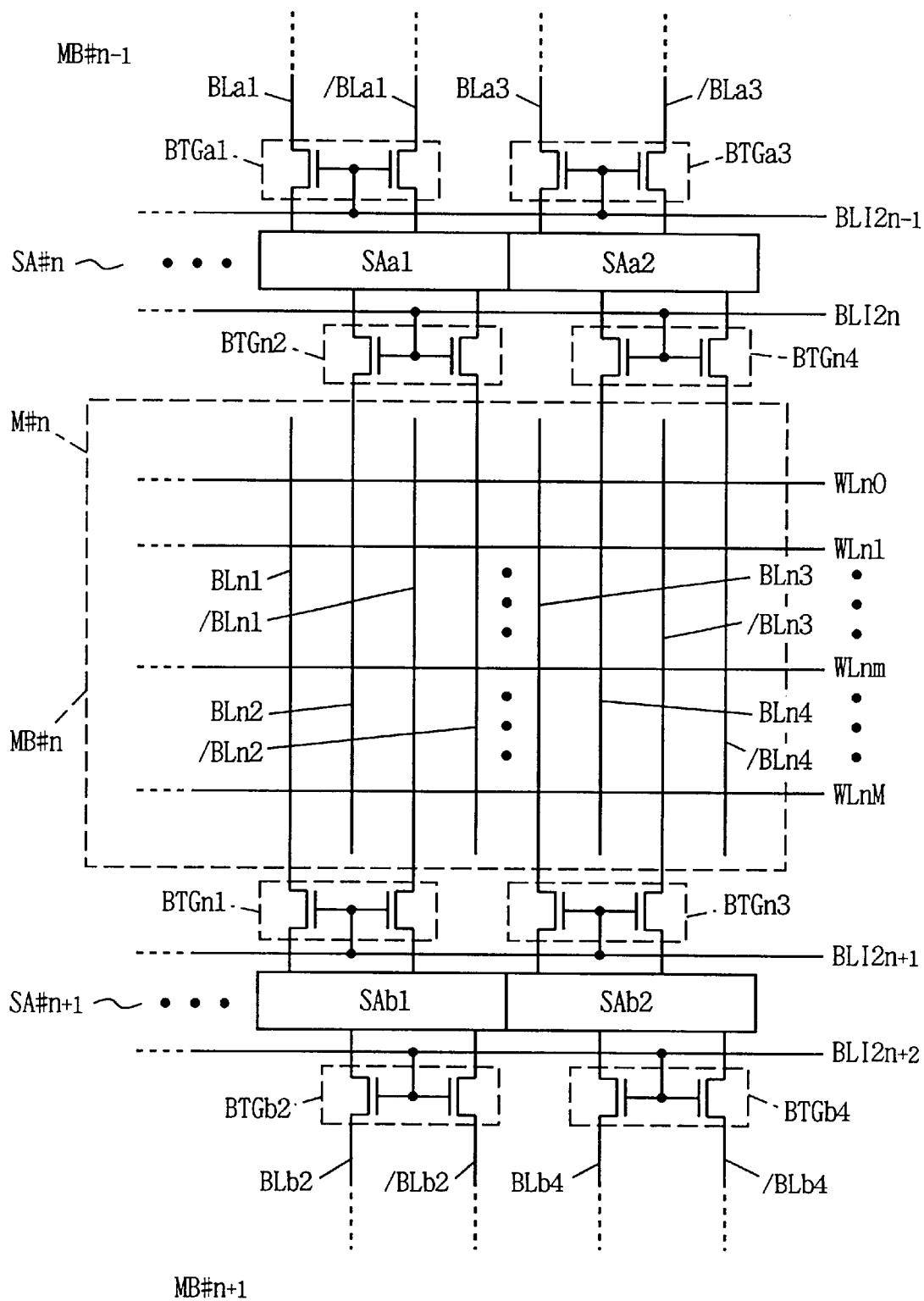
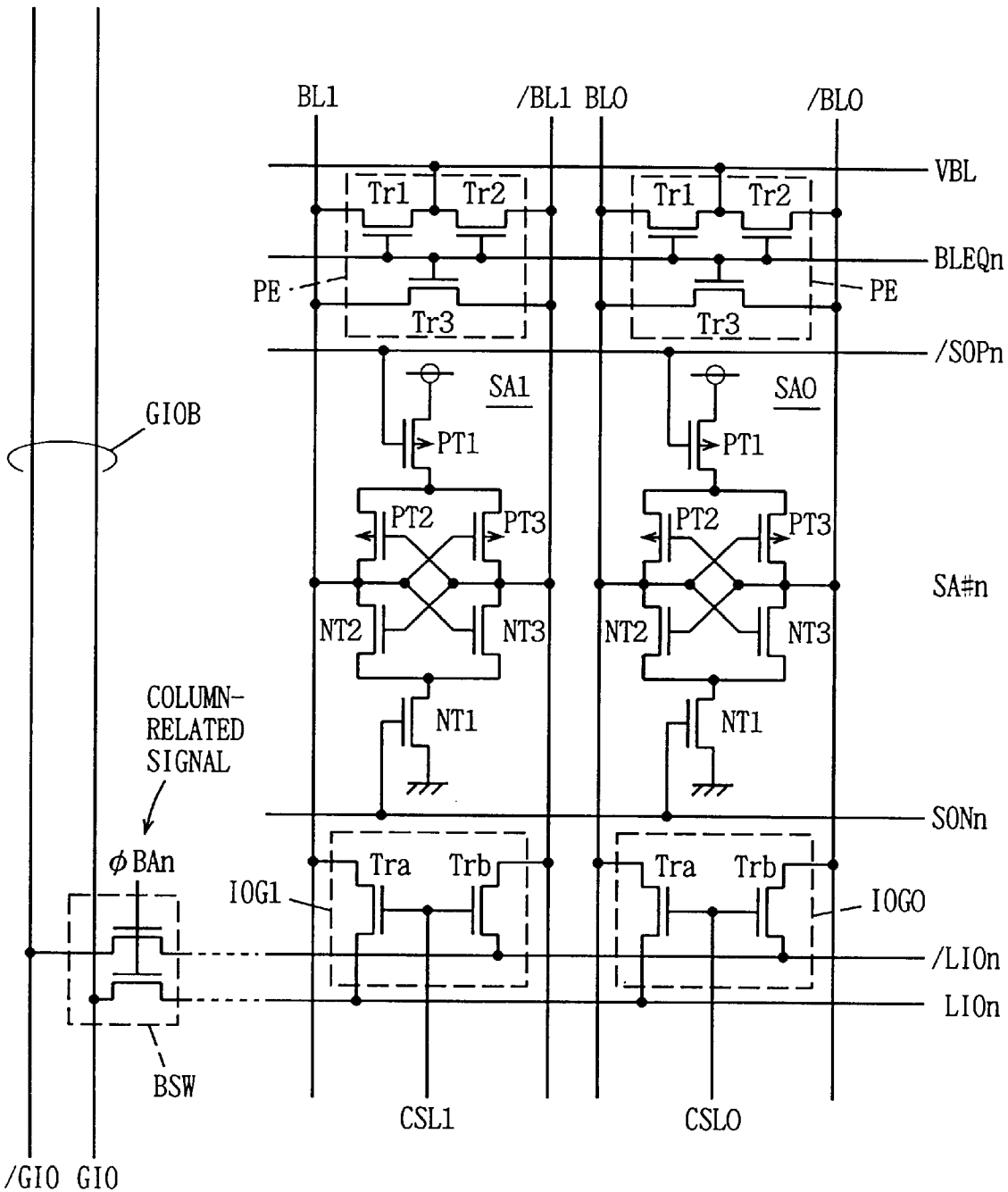


FIG. 5



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