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Paper No. 8
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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner,

v.

LIMESTONE MEMORY SYSTEMS LLC,
Patent Owner.

Case IPR2016-00094
Patent 5,894,441

Before BART A. GERSTENBLITH, BARBARA A. PARVIS, and ROBERT J. WEINSCHENK, *Administrative Patent Judges*.

PARVIS, *Administrative Patent Judge*.

DECISION
Denying Institution of *Inter Partes* Review
37 C.F.R. § 42.108

I. INTRODUCTION

A. Background

Micron Technology, Inc. ("Petitioner") filed a Petition (Paper 1, "Pet.") requesting institution of *inter partes* review of claims 1–3 and 5–15 of U.S. Patent No. 5,894,441 (Ex. 1001, "the '441 patent"). Limestone

Memory Systems LLC ("Patent Owner") filed a Preliminary Response (Paper 7, "Prelim. Resp.").

In its Preliminary Response, Patent Owner indicates that it has disclaimed claims 1–3 and 5 under 35 U.S.C. § 253(a). Prelim. Resp. 10. As evidence of that disclaimer, Patent Owner filed an Acknowledgement Receipt. Ex. 2001. 37 C.F.R. § 42.107(e) provides: "The patent owner may file a statutory disclaimer under 35 U.S.C. 253 (a) in compliance with § 1.321(a) of this chapter, disclaiming one or more claims in the patent." Patent Owner's disclaimer is in compliance with 37 C.F.R. § 1.321(a). Accordingly, we decline to institute an *inter partes* review as to claims 1–3 and 5.

Furthermore, upon consideration of the Petition, and applying the standard set forth in 35 U.S.C. § 314(a), which requires demonstration of a reasonable likelihood that Petitioner would prevail with respect to at least one challenged claim, we deny the Petition and decline to institute an *inter partes* review of claims 6–15 of the '441 patent.

B. Related Proceedings

The parties indicate that the '441 patent is asserted against Petitioner in *Limestone Memory Sys. LLC v. Micron Tech., Inc.*, No. 8:15-cv-00278 (C.D. Cal.). Pet. 2; Paper 6, 2. The parties indicate that other proceedings may be related. Pet. 2–3; Paper 6, 2–3.

C. Real Parties-in-Interest

The Petition identifies Micron Technology, Inc. as the real party-in-interest. Pet. 2. Patent Owner identifies Limestone Memory Systems LLC and Acacia Research Group LLC as the real parties-in-interest. Paper 6, 1.

D. The References

Petitioner relies on the following references:

U.S. Patent No. 5,270,975, issued December 14, 1993 (Ex. 1005, "McAdams"); and

Japanese Patent Application No. H06-052696, published February 25, 1994 (Ex. 1006, "Minami").[1]

E. The Asserted Grounds of Unpatentability

Petitioner challenges the patentability of claims 6–15 of the '441 patent on the ground that they are unpatentable, under 35 U.S.C. § 103(a), over McAdams and Minami. Pet. 4. Petitioner supports its challenge with a declaration executed by Dr. R. Jacob Baker on October 22, 2015 (Ex. 1003).

F. The '441 patent

The '441 patent is directed to a "SEMICONDUCTOR MEMORY DEVICE WITH REDUNDANCY CIRCUIT." Ex. 1001, [54]. The '441 patent explains:

> The semiconductor memory device according to this invention comprises a plurality of column selection lines, at least one redundant column selection line, a column decoder which activates one line out of the plurality of column selection lines in response to a column address a first circuit which generates a detection signal when the column address of a defect-related column selection line is supplied, and a second circuit which receives at least a part of a row address and activates the redundant column selection line in response to at least a part of the row address and the detection signal. With this arrangement, when a defect occurs in one bit, instead of replacing all of the

[1] Unless otherwise noted, citations are to the certified English-language translation, submitted as part of Exhibit 1006.

many bit lines included in the column selection line to which the defective bit line belongs, it is possible to relieve a larger number of defective bit lines using a single redundant column selection line by replacing only a part of these bit lines.

Id. at 2:13–28.

G. Illustrative Claim

Claim 6 is the remaining independent claim challenged in this proceeding. Claims 7–15 depend, directly or indirectly, from claim 6. Independent claim 6 is illustrative of the claimed subject matter and is reproduced below with emphasis on the element that is the focus of our analysis.

6. A semiconductor memory device comprising:

a plurality of word lines including at least first and second word lines;

a plurality of bit lines including at least first and second bit lines;

a plurality of redundant bit lines including at least first and second redundant bit lines;

a plurality of memory cells each of which is disposed on intersections of said word lines and bit lines;

a plurality of redundant memory cells each of which is disposed on intersections of said word lines and redundant bit lines;

a plurality of column selection lines including at least a first column selection line; said first and second bit lines being selected when said first column selection line is activated;

a redundant column selection line; said first and second redundant bit lines being selected when said redundant column selection line is activated;

a column decoder activating said first column selection line in response to a first column address when said first word line is activated; and

a column redundancy decoder activating said redundant column selection line in response to said first column address when said second word line is activated.[2]

Ex. 1001, 13:55–14:13 (emphasis added).

II. CLAIM CONSTRUCTION

A. Legal Standard

Petitioner proposes that we construe the claim term "transfer gate" to mean "logic that transfers the logic value of a signal." Pet. 10. For the purposes of this Decision, we are not persuaded that "transfer gate" requires express construction, because even if we were to adopt Petitioner's proffered construction, Petitioner has not established that it is reasonably likely to succeed in showing that the challenged claims are unpatentable. *See Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999) ("[O]nly those terms need be construed that are in controversy, and only to the extent necessary to resolve the controversy.").

III. ANALYSIS

A. Obviousness of Claim 6 over McAdams and Minami

Petitioner asserts that a combination of the teachings of McAdams and Minami would have rendered the subject matter of claim 6 obvious to one of ordinary skill in the art at the time of the invention. Pet. 26–44. The Petition includes discussion identifying where McAdams and Minami allegedly teach or suggest the elements of each challenged claim. *Id.*

[2] We refer to this limitation as "the column redundancy decoder limitation."

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