



[54] REDUNDANCY SCHEME FOR ELIMINATING DEFECTS IN A MEMORY DEVICE

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[52] U.S. Cl. 365/200; 365/230.03; 365/230.06

[58] Field of Search 365/200, 230.03, 230.06; 371/10.3, 11.1, 8

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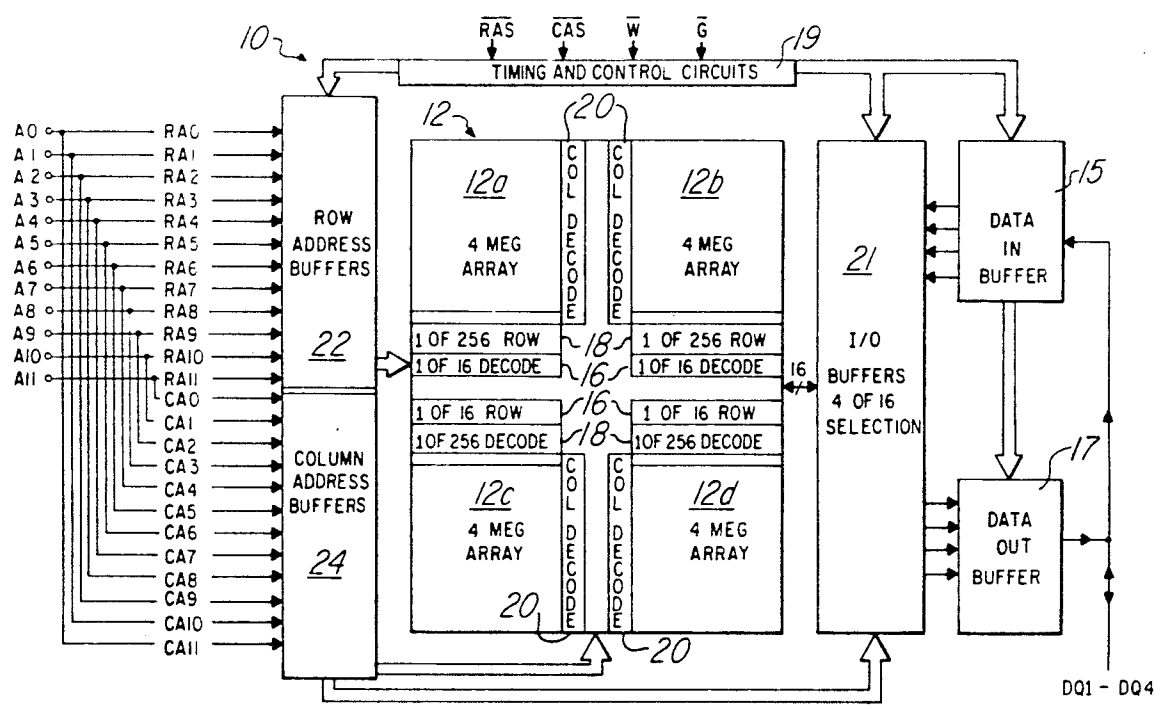
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[57] ABSTRACT

A redundancy scheme for a memory device, as well as a method for developing a redundancy scheme, resulting in improved reparability for given space constraints. A memory device is formed with a plurality of data blocks having individual input/output paths. Each block comprises an array of memory cells arranged in addressable rows and columns along row lines and column lines. The array is configured in sub-blocks each comprising a plurality of the memory cells. The device includes row address circuitry for selecting a row of the memory cells, column address circuitry for selecting a column of the memory cells and address repair circuitry. The address repair circuitry is configurable to render a first portion of a first of the columns of cells responsive to the address of a portion of a second of the columns of cells. There is also provided a method for eliminating a defect in a memory device having a logical data block formed with addressable rows and columns of memory cells. A defect associated with a first column of cells is eliminated by programming a portion of a second column of cells to be responsive to the addresses of a portion of the cells in the first column.

4 Claims, 10 Drawing Sheets



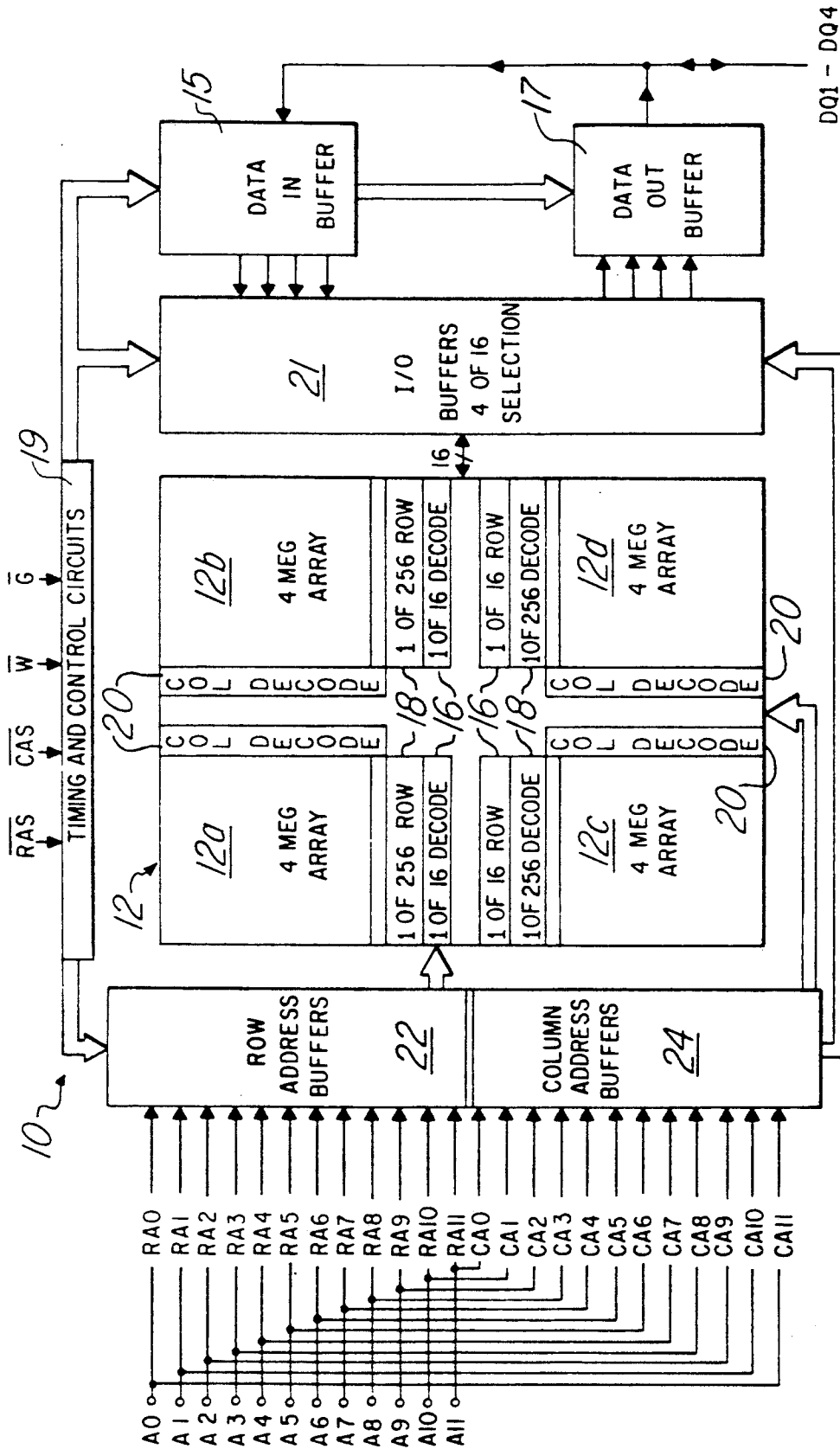


FIG. 1

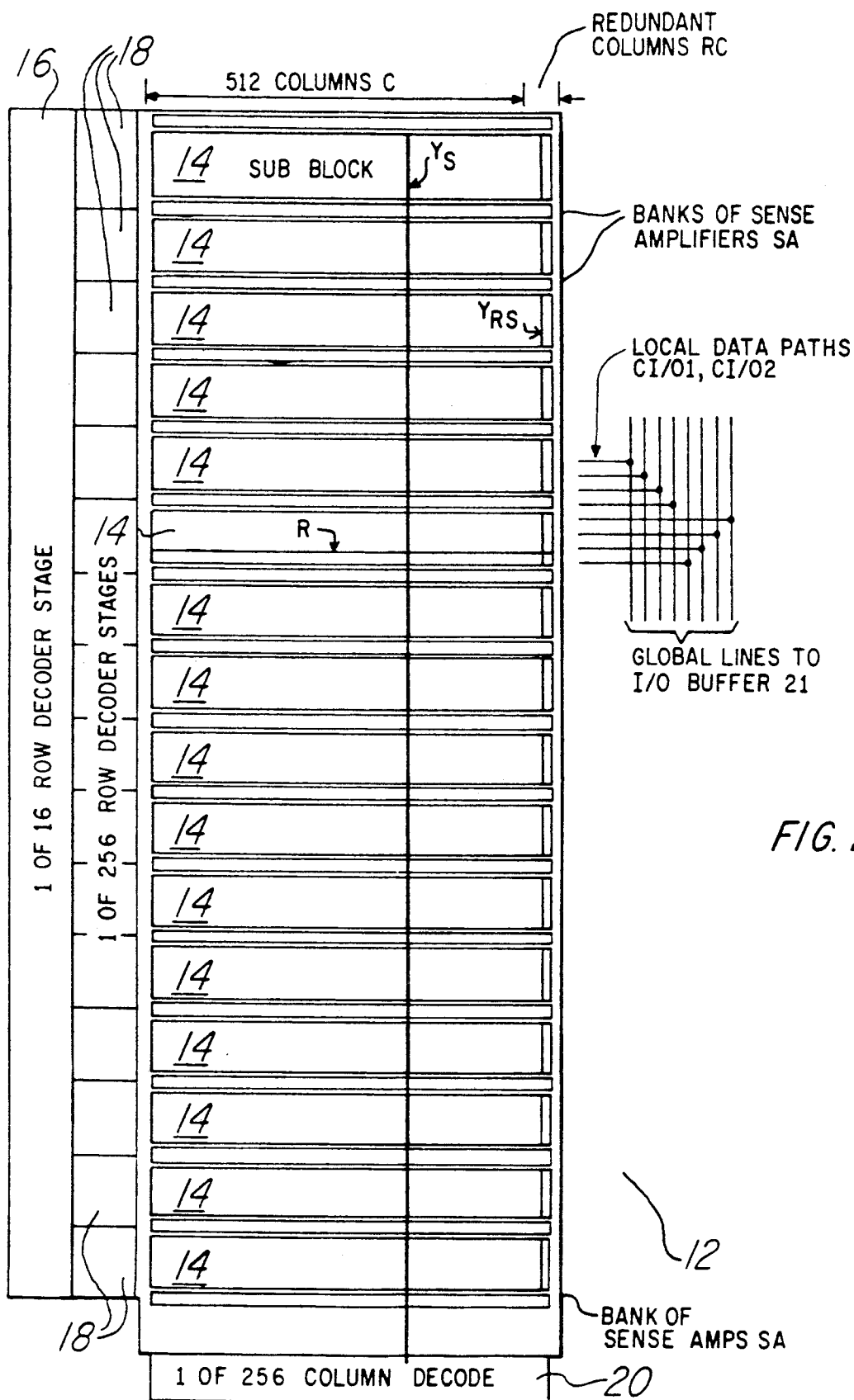


FIG. 2

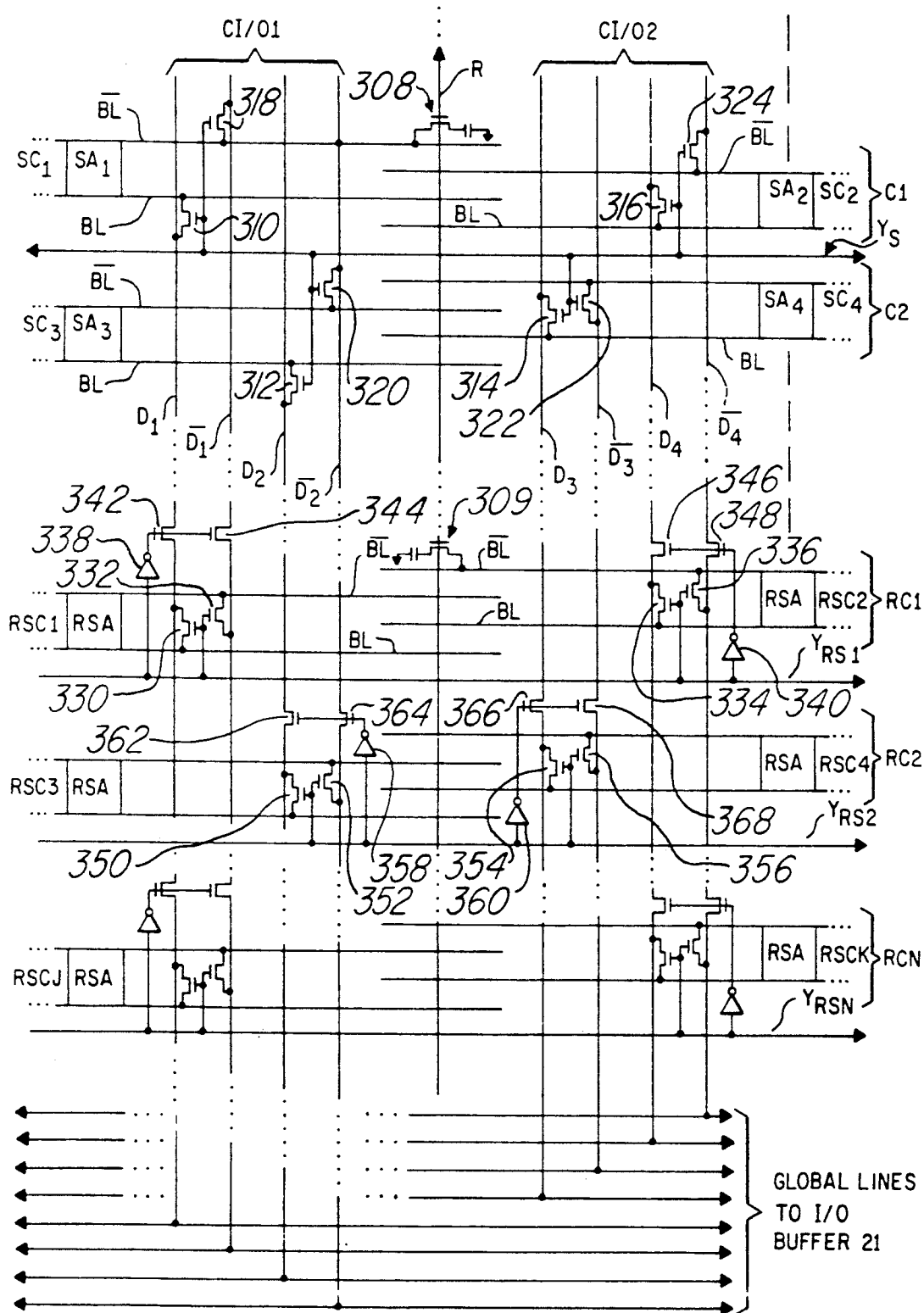


FIG. 3

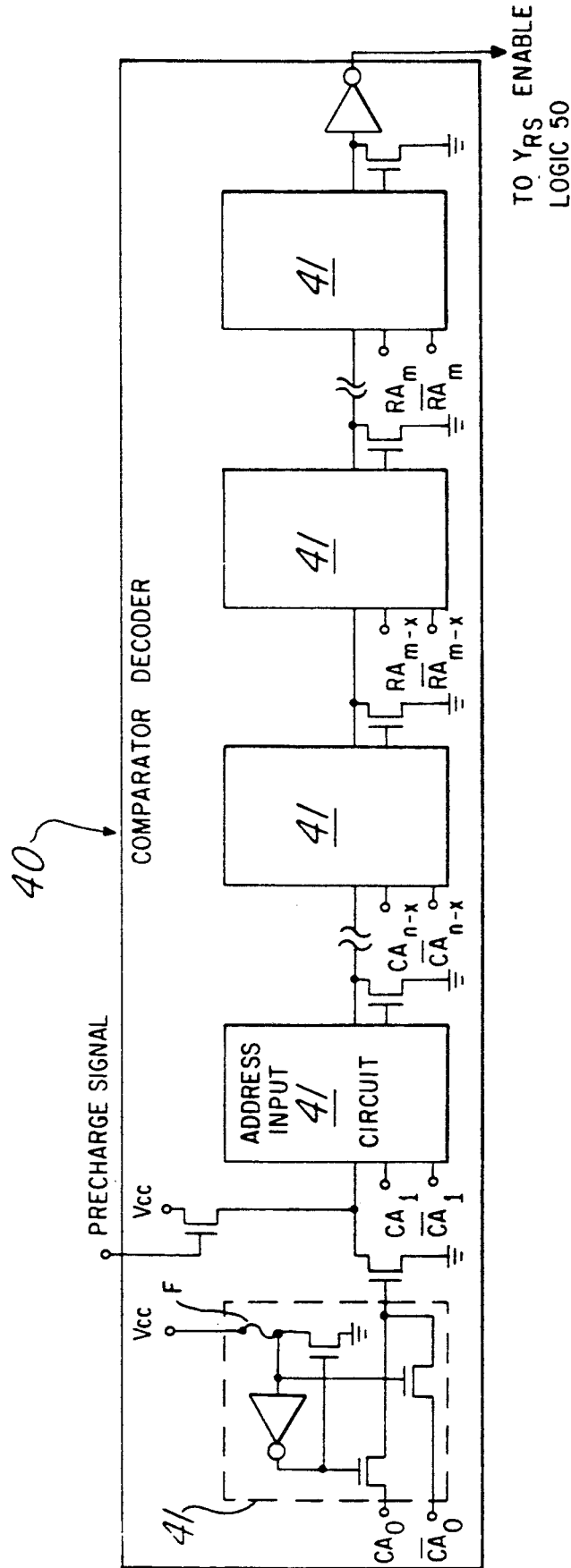


FIG. 4

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