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Horiguchi et al.

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[54] SEMICONDUCTOR MEMORY HAVING REDUNDANCY CIRCUIT

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[21] Appl. No.: **818,434**

[22] Filed: **Dec. 27, 1991**

Related U.S. Application Data

[63] Continuation of Ser. No. 419,399, Oct. 10, 1989, abandoned.

[30] Foreign Application Priority Data

Oct. 7, 1988 [JP] Japan 63-252028
Oct. 31, 1988 [JP] Japan 63-275375

[51] Int. Cl.⁵ **G11C 29/00; G11C 7/00**

[52] U.S. Cl. **365/200; 365/230.03; 371/10.2; 371/10.3**

[58] Field of Search **365/200, 230.01, 230.03, 365/230.04, 230.06; 371/8.1, 10.1, 10.2, 10.3**

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[57] ABSTRACT

A redundancy technique is introduced for a semiconductor memory and, more particularly a redundancy technique for a dynamic random access memory (DRAM) having a storage capacity of 16 mega bits or more. In such a DRAM, the efficiency of the redundancy technique is reduced, since a memory array is divided into a large number of memory mats. According to the present redundancy technique, in a semiconductor memory including a memory array which has a plurality of word lines, a plurality of bit lines arranged so that two-level crossings are formed between the word lines and the bit lines, and memory cells disposed at desired ones of the two-level crossings, there is provided, furthermore, a plurality of spare word (or bit) lines, address comparing circuits for storing therein a defective address existing in the memory array, to compare an address to be accessed with the defective address, and selection circuitry for replacing a word or bit line including a defective memory cell by a spare word (or bit) line in accordance with the result of the comparison. The memory array of the semiconductor memory is divided into M memory mats (where $M \geq 2$), the number m of word or bit lines which are simultaneously replaced by spare word (or bit) lines, is less than the number M and equal to a divisor thereof, and the number L of spare word (or bit) lines per one memory mat and the number R of address comparing circuits satisfy a relation $L < R \leq LM/m$ and, preferably, $L < R < LM/m$.

12 Claims, 34 Drawing Sheets

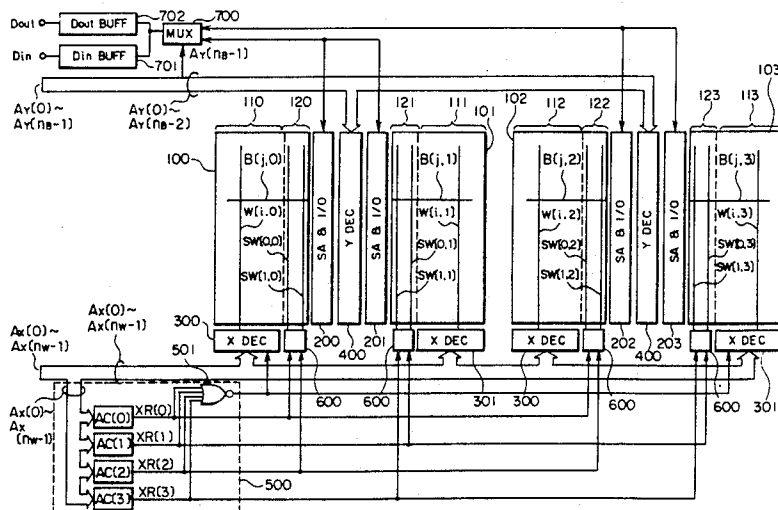


FIG. 1A
PRIOR ART

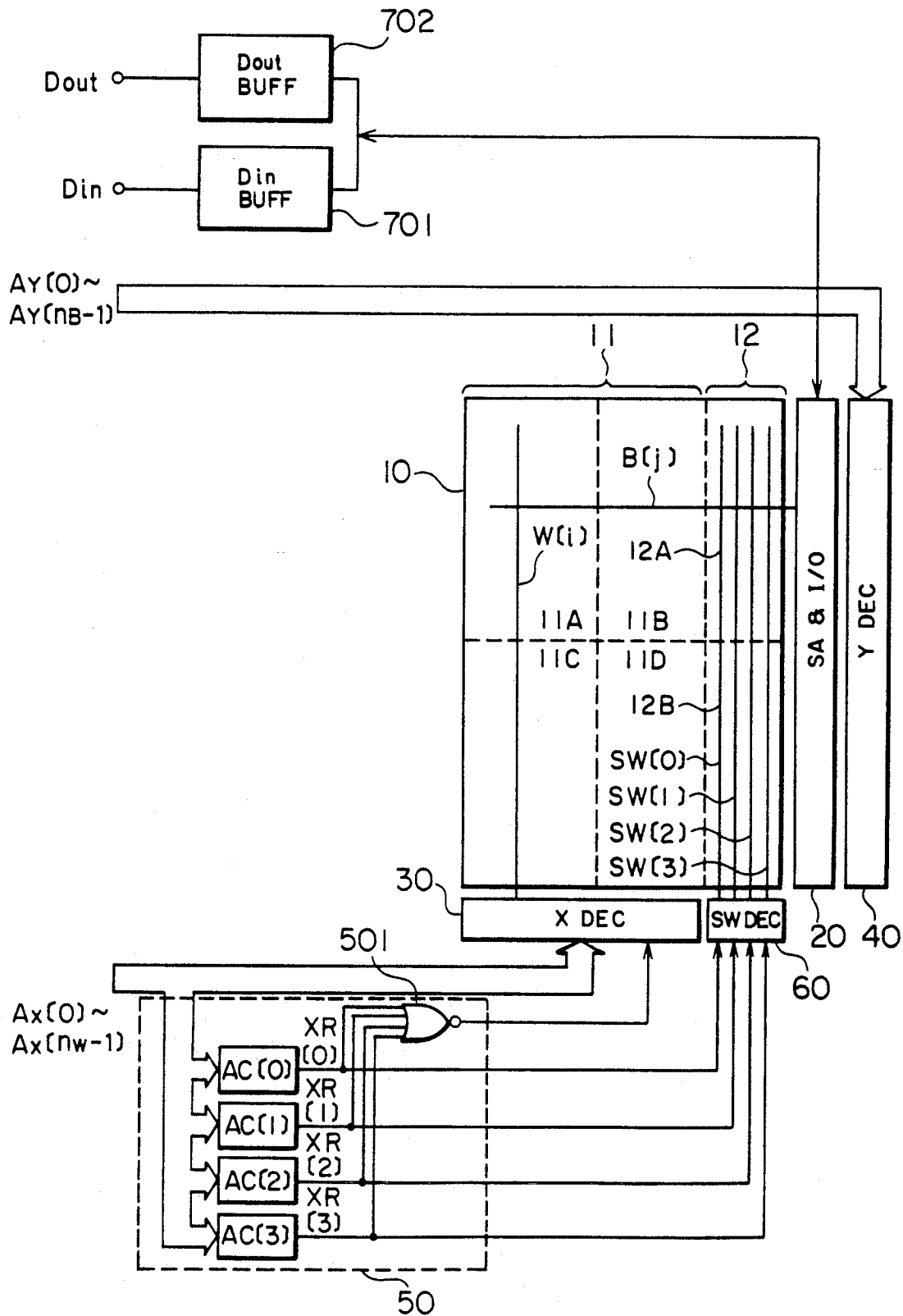


FIG. 1B
PRIOR ART

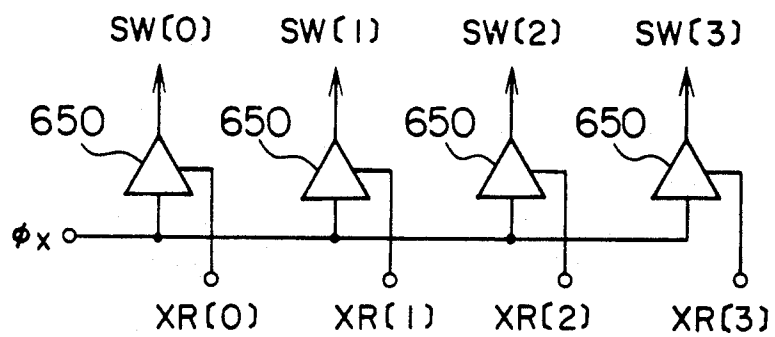


FIG. 2A
PRIOR ART

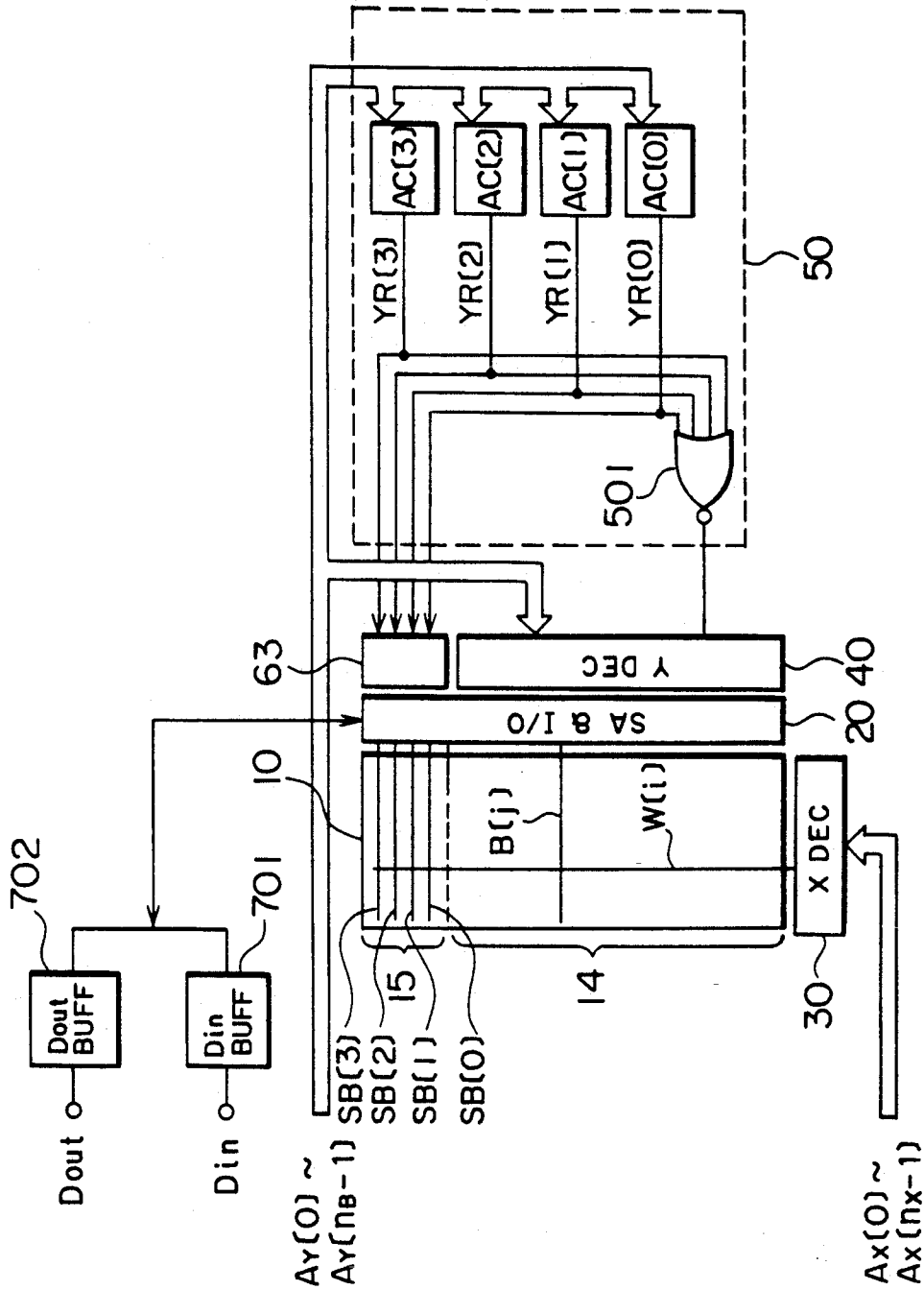
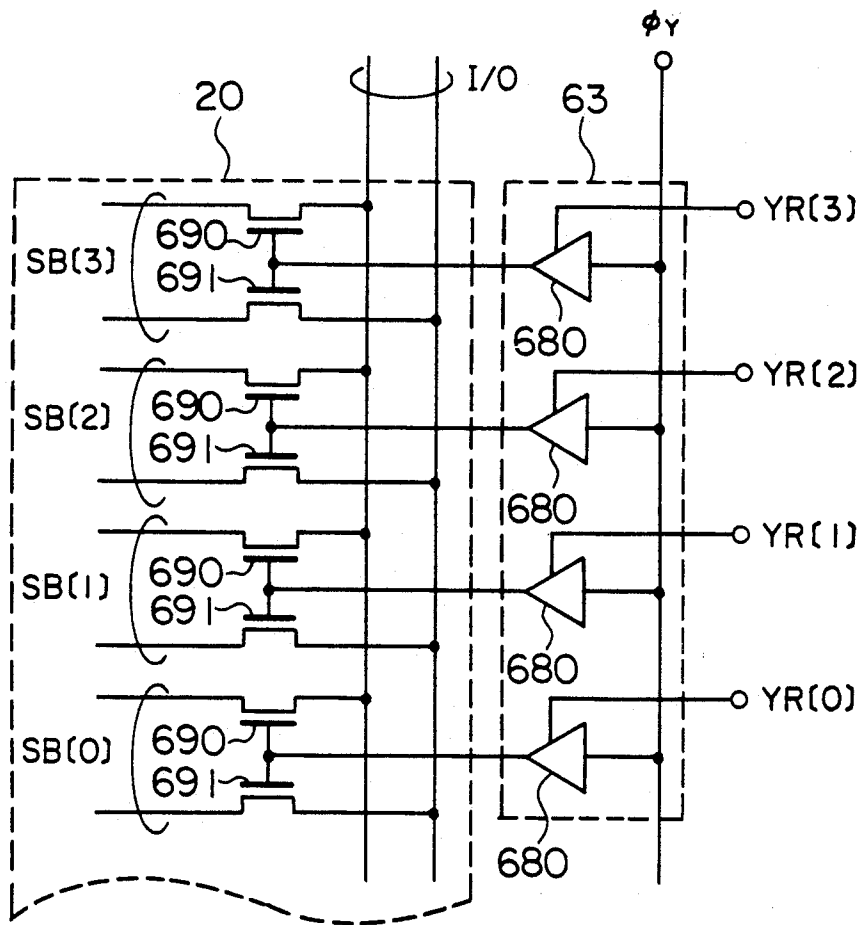


FIG. 2B
PRIOR ART



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