

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

APPLE INC.,
Petitioner,

v.

LIMESTONE MEMORY SYSTEMS LLC,
Patent Owner.

Case IPR2016-01567
Patent 5,894,441

Before BART A. GERSTENBLITH, BARBARA A. PARVIS, and
ROBERT J. WEINSCHENK, *Administrative Patent Judges*.

PARVIS, *Administrative Patent Judge*.

DECISION

Denying Petitioner's Request for Rehearing
37 C.F.R. § 42.71

I. INTRODUCTION

Apple Inc. ("Petitioner") filed a Request for Rehearing (Paper 12, "Req. Reh'g") of the Decision Denying Institution of *Inter Partes* Review of U.S. Patent No. 5,894,441 (Ex. 1003, "the '441 patent") (Paper 11, "Dec."). Petitioner requests reconsideration of the denial of institution and contends

that we misapprehended and overlooked disclosure of Horiguchi, U.S. Patent No. 5,265,055 (Ex. 1005). Req. Reh'g 2.

II. STANDARD OF REVIEW

Under 37 C.F.R. § 42.71(c), “[w]hen rehearing a decision on petition, a panel will review the decision for an abuse of discretion.” An abuse of discretion occurs when a “decision was based on an erroneous conclusion of law or clearly erroneous factual findings, or . . . a clear error of judgment.” *PPG Indus., Inc. v. Celanese Polymer Specialties Co.*, 840 F.2d 1565, 1567 (Fed. Cir. 1988) (citations omitted). The request must identify, specifically, all matters the party believes the Board misapprehended or overlooked, and the place where each matter was addressed previously in a motion, opposition, or reply. 37 C.F.R. § 42.71(d).

III. DISCUSSION

In our Decision Denying Institution, we determined that Petitioner had not shown sufficiently that Horiguchi discloses “a plurality of column selection lines including at least a first column selection line; said first and second bit lines being selected when said first column selection line is activated,” as recited in claim 6. Dec. 9. In its Request for Rehearing, Petitioner contends that (1) we failed to appreciate or overlooked Dr. Mazumder’s testimony (Req. Reh’g 3–9) and (2) Horiguchi must disclose multiple column selection lines (*id.* at 9–11).

We turn to Petitioner’s contentions that we failed to appreciate or overlooked Dr. Mazumder’s testimony. Petitioner first points to Dr. Mazumder’s testimony regarding the background of the technology (*see, e.g., id.* at 4 (citing Ex. 1001 ¶¶ 31, 33–35)) and contends that a person of

ordinary skill in the art would have known of multiple column selection lines. Petitioner relies on Dr. Mazumder's testimony pertaining to a figure and teachings that are not found in Horiguchi. *Id.* The ground presented in the Petition, however, is anticipation by Horiguchi. Pet. 4.

Petitioner also points to its previous contentions in the Petition (Paper 1, "Pet.") and contends that "there are multiple column selection lines disclosed in Horiguchi, one for each value of 'j.'" Req. Reh'g 6 (citing Pet. 30–31). More specifically, Petitioner contends that "Dr. Mazumder explained the connection between each column selection line and the bit lines" and "how the iterative notation of YS[j] (a commonly used variable notation) represents separate column selection lines for different values of j." *Id.* at 7 (citing Ex. 1003 ¶¶ 152–53).

As we explained in the Decision Denying Institution, we considered Dr. Mazumder's testimony and determined that he did not offer persuasive evidence to remedy the deficiencies in the Petition. Dec. 8–9. For instance, Dr. Mazumder testifies that "[f]or each value of 'j', column selection line YS[j] selects bit line B[j,n] in each of the sub-arrays." Ex. 1001 ¶ 152. Dr. Mazumder also testifies regarding an example, "YS[0] selects at least bit lines B[0,0] in sub-array 130 and B[0,1] in sub-array 131." *Id.* ¶ 153. Claim 6 requires "a plurality of column selection lines including at least a first column selection line; said first and second bit lines being selected when said first column selection line is activated." Dr. Mazumder's testimony identified in Petitioner's Request for Rehearing pertains to "said first and second bit lines being selected when said first column selection line is activated."

As we explained in the Decision Denying Institution, however, the Petition does not address sufficiently Petitioner's basis for contending that Horiguchi discloses the first portion of the recitation, i.e., "a plurality of column selection lines." Dec. 7–9. In this regard, Dr. Mazumder's testimony identified by Petitioner (Pet. 30–31; Req. Reh'g 7–8) is the same as the contentions in the Petition (*compare, e.g.,* Ex. 1003 ¶ 152 *with* Pet. 30), and both were discussed in the Decision Denying Institution (Dec. 7–9).

In its Request for Rehearing, Petitioner acknowledges part of our analysis in the Decision Denying Institution and contends that the single column selection line shown in Figure 26 is exemplary. Req. Reh'g 8–9 (citing Dec. 8–9; Ex. 1006, 5:10–20). Petitioner, for the first time, relies on Gallia (U.S. Patent No. 5,126,973, Ex. 1006) as support for this contention. *Id.* The ground presented in the Petition, however, is anticipation by Horiguchi. Pet. 4. In addition to this deficiency, Petitioner's contention is newly presented in its Request for Rehearing and, therefore, we cannot have misapprehended or overlooked it.

In Petitioner's contentions regarding Dr. Mazumder's testimony, Petitioner also points to a new portion of Horiguchi not identified previously in the Petition. *Id.* at 5 (citing Ex. 1005, 22:18–22). Again, we cannot have misapprehended or overlooked newly made arguments. Additionally, the newly identified sentence is followed by a description of replacing bit defects, for example, using a spare bit line (*see, e.g.,* Ex. 1005, 22:22–42). Petitioner has not provided sufficient argument or evidence to persuade us that the use of "output lines" (Req. Reh'g 5) refers to anything other than bit

lines and, therefore, we are not persuaded that this disclosure remedies the aforementioned deficiencies.

We now turn to Petitioner’s contention that Horiguchi must disclose multiple column selection lines (*id.* at 9–11). Petitioner, for example, contends “[g]iven that there are multiple bit lines in each memory array, there *must be* multiple column selection lines in order to access all of the memory cells in the array.” Req. Reh’g 11 (citing Ex. 1001 ¶¶ 33–35, 117–18; Ex. 1005, 21:58–65); *see also id.* at 5 (“The multiple output lines from the Y-decoder *are necessary* to access all of the bit lines”) (citing Ex. 1001 ¶¶ 117–18; Pet. 12–13) (emphasis added). Petitioner points to Dr. Mazumder’s testimony in support of its contention. *Id.*

As an initial matter, this also is a new contention not made in the Petition (*see* Pet. 30–31) and, therefore, we cannot have misapprehended or overlooked it. Additionally, contrary to Petitioner’s contention, Dr. Mazumder does not testify that multiple output lines from the Y-decoder are necessary. Ex. 1001 ¶¶ 117–18. Instead, Dr. Mazumder testifies that “the four sub-arrays share *a single* column address decoder (40), to activate *a* column selection *line* YS[j].” *Id.* ¶ 118 (citing Ex. 1005, 22:6–10, Fig. 26) (emphases added).

For the foregoing reasons, we determine that our Decision Denying Institution was not “based on an erroneous conclusion of law or clearly erroneous factual findings, or . . . a clear error of judgment.” *PPG Indus., Inc.*, 840 F.2d at 1567 (citations omitted).

IV. ORDER

For the foregoing reasons, it is:

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