UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

APPLE INC.,
Petitioner,

v.

LIMESTONE MEMORY SYSTEMS LLC,
Patent Owner.

Case IPR2016-01567
Patent No. 5,894,441

PETITIONER'S REQUEST FOR REHEARING UNDER 37 C.F.R. § 42.71(d)

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I. INTRODUCTION

On January 18, 2017, the Board issued a Decision denying institution of *inter partes* review of U.S. Patent No. 5,894,441 ("the '441 patent") on Petitioner's Ground 1. Paper No. 11 ("Decision") at 9. In Ground 1, Petitioner contends that claims 6-12, 14 and 15 of the '441 patent are invalid under (pre-AIA) 35 U.S.C. § 102(b) because they are anticipated by U.S. Patent No. 5,265,055 ("Horiguchi"). Paper No. 1 ("Petition") at 4 & 26-51. In denying institution, the Board erroneously concluded that Horiguchi did not teach the "plurality of column selection lines" limitation of the semiconductor memory device described in independent claim 6. Decision, 9. Petitioner requests rehearing seeking reconsideration of Ground 1.

Horiguchi discloses multiple column selection lines, explicitly in its specification and by using a well-known variable notation in its figures to represent multiple lines. This disclosure is well understood by a person of ordinary skill in the art because multiple column selection lines are required for even the most basic dynamic random access memory ("DRAM") devices to function. This is confirmed by the unrebutted testimony of Dr. Pinaki Mazumder. Petitioner respectfully submits that the Board overlooked this basic fact of DRAM architecture in misapprehending the teachings of and contentions regarding Horiguchi set forth in the Petition. As a result, the Board clearly erred in finding

that Horiguchi discloses only a single column selection line and abused its discretion in denying institution of the Petition.

II. LEGAL STANDARD

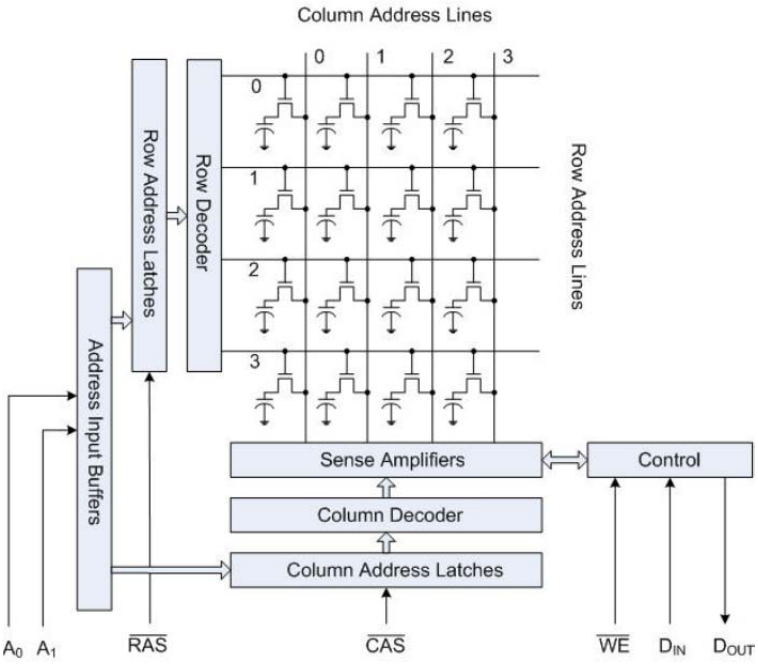
Under 37 C.F.R. § 42.71(d), a petitioner may request rehearing on a decision denying institution of *inter partes* review. A request for rehearing "must specifically identify all matters the party believes the Board misapprehended or overlooked, and the place where each matter was previously addressed in a motion, an opposition, or a reply." 37 C.F.R. § 42.71(d). When evaluating a request for rehearing on a decision, the Board will review the decision for an abuse of discretion. 37 C.F.R. § 42.71(c). An abuse of discretion occurs when a decision is based on an "erroneous conclusion of law or clearly erroneous factual findings, or . . . a clear error of judgment." *PPG Indus. Inc. v. Celanese Polymer Specialties Co.*, 840 F.2d 1565, 1567 (Fed. Cir. 1988); *see, e.g.*, *Facebook, Inc. v. Software Rights Archive, LLC*, IPR2013-00478, Paper No. 31 (Apr. 14, 2014).

III. ARGUMENT

A. The Board failed to appreciate or overlooked the testimony from Dr. Mazumder regarding basic DRAM architecture.

The '441 patent is directed to semiconductor memory with redundant circuitry. Horiguchi discloses a semiconductor memory device "and, more particularly a redundancy technique for a dynamic random access memory (DRAM) having a storage capacity of 16 mega bits or more." Petition, 26 (citing

Horiguchi). As discussed in the technology background of Dr. Mazumder's Declaration, DRAM cells are compact memory cells, with each cell comprising one transistor and one capacitor. Ex. 1001 ("Mazumder Decl.") at ¶ 31. Dr. Mazumder explained the basic structure of DRAM by referencing an exemplary 4x4 memory cell array along with its peripheral components. *Id.* at ¶ 33, Fig. 2.



Each DRAM cell is located at the intersection of a word line and bit line, each cell having its own unique address. *Id.* at ¶ 34. In the exemplary figure above, the row (word line) addresses 0-3 and column (bit line) addresses 0-3 are marked for each distinct row and column. *Id.* at ¶ 33, Fig. 2. Each memory cell in the array is accessed by activating the respective Row Address Line (word line) and Column Address Line (Column Selection Line) (bit line) in order to, for example, read the value stored in the cell. *Id.* at ¶¶ 34-35. As depicted in the

figure, there are two address bits, A0 and A1, used to identify the location of a particular memory cell, and there are four column selection lines, one for each column of memory cells, that enable access to all memory cells in the array. *Id.* at Fig. 2. Put mildly, the necessary existence of multiple column selection lines in DRAM is well-known. *Id.* at ¶¶ 33-35, 76-77; *see, e.g.*, Ex. 1006, 5:10-20.

Claim 6 of the '441 patent recites these well-known structures of DRAM, including the limitation "a plurality of column selection lines including at least a first column selection line." With respect to this claim limitation, the Petition explains that Horiguchi (Ex. 1005, 22:7-10) in fact discloses multiple column selection lines YS[j]: "[a]n output YS[j] of the Y-decoder is applied to each memory mat through a wiring conductor which is indicated by a dot-dash line in FIG. 26." Petition, 30-31. Each memory mat includes an array of memory cells disposed at the crossings of word lines and bit lines. Ex. 1005, 21:51-22:3; Mazumder Decl., ¶¶ 117-118; Petition, 12-13. Horiguchi further explains, with reference to Fig. 26 (shown below), that "[t]he present invention is specifically effective for a semiconductor memory, in which a plurality of memory mats use circuit means (for example, **a Y-decoder and output lines thereof**) in common, such as the present embodiment." Ex. 1005, 22:18-22 (emphasis added). The multiple output lines from the Y-decoder are necessary to access all of the bit lines,

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