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Paper No. 11
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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

APPLE INC.,
Petitioner,

v.

LIMESTONE MEMORY SYSTEMS LLC,
Patent Owner.

Case IPR2016-01567
Patent 5,894,441

Before BART A. GERSTENBLITH, BARBARA A. PARVIS, and ROBERT J. WEINSCHENK, *Administrative Patent Judges*.

PARVIS, *Administrative Patent Judge*.

DECISION
Denying Institution of *Inter Partes* Review
37 C.F.R. § 42.108

I. INTRODUCTION

A. Background

Apple Inc. ("Petitioner") filed a Petition (Paper 1, "Pet.") requesting institution of *inter partes* review of claims 6–12, 14, and 15 ("challenged claims") of U.S. Patent No. 5,894,441 (Ex. 1003, "the '441 Patent").

Limestone Memory Systems LLC ("Patent Owner") filed a Preliminary Response (Paper 8, "Prelim. Resp.").

For the reasons set forth below, on behalf of the Director (*see* 37 C.F.R. § 42.4(a)), we decline to institute an *inter partes* review of the challenged claims of the '441 Patent.

B. Related Proceedings

The parties indicate that the '441 Patent is asserted against Petitioner in *Limestone Memory Sys. LLC v. Apple Inc.*, No. 8:15-cv-01274 (C.D. Cal.). Pet. 1; Paper 4, 5. The parties indicate that other proceedings may be related. Pet. 1–2; Paper 4, 1–5.

C. Real Parties-in-Interest

The Petition identifies Apple Inc. as the real party-in-interest. Pet. 1. Patent Owner identifies Limestone Memory Systems LLC and Acacia Research Group LLC as the real parties-in-interest. Paper 4, 1.

D. The References

Petitioner relies on the following references:

U.S. Patent No. 5,265,055, issued November 23, 1993 (Ex. 1005, "Horiguchi"); and

U.S. Patent No. 5,126,973, issued on June 30, 1992 (Ex. 1006, "Gallia").

E. The Asserted Grounds of Unpatentability

Petitioner asserts the following grounds of unpatentability (Pet. 4):

Challenged Claims	Basis	Reference(s)
6–12, 14, and 15	§ 102(b)	Horiguchi
6, 7, 9, 11, 12, 14, and 15	§ 102(b)	Gallia
8 and 10	§ 103(a)	Gallia and Horiguchi

Petitioner supports its challenge with a declaration executed by Dr. Pinaki Mazumder on August 12, 2016 (Ex. 1001).

F. The '441 Patent

The '441 Patent is directed to a "SEMICONDUCTOR MEMORY DEVICE WITH REDUNDANCY CIRCUIT." Ex. 1003, [54]. The '441 Patent explains:

> The semiconductor memory device according to this invention comprises a plurality of column selection lines, at least one redundant column selection line, a column decoder which activates one line out of the plurality of column selection lines in response to a column address, a first circuit which generates a detection signal when the column address of a defect-related column selection line is supplied, and a second circuit which receives at least a part of a row address and activates the redundant column selection line in response to at least a part of the row address and the detection signal. With this arrangement, when a defect occurs in one bit, instead of replacing all of the many bit lines included in the column selection line to which the defective bit line belongs, it is possible to relieve a larger number of defective bit lines using a single redundant column selection line by replacing only a part of these bit lines.

Id. at 2:13–28.

G. Illustrative Claim

Claim 6 is the only independent claim challenged in this proceeding. Claims 7–12, 14, and 15 depend, directly or indirectly, from claim 6. Independent claim 6 is illustrative of the claimed subject matter and is reproduced below.

> 6. A semiconductor memory device comprising:
>
> a plurality of word lines including at least first and second word lines;
>
> a plurality of bit lines including at least first and second bit lines;
>
> a plurality of redundant bit lines including at least first and second redundant bit lines;
>
> a plurality of memory cells each of which is disposed on intersections of said word lines and bit lines;
>
> a plurality of redundant memory cells each of which is disposed on intersections of said word lines and redundant bit lines;
>
> a plurality of column selection lines including at least a first column selection line; said first and second bit lines being selected when said first column selection line is activated;
>
> a redundant column selection line; said first and second redundant bit lines being selected when said redundant column selection line is activated;
>
> a column decoder activating said first column selection line in response to a first column address when said first word line is activated; and
>
> a column redundancy decoder activating said redundant column selection line in response to said first column address when said second word line is activated.

Ex. 1003, 13:55–14:13.

II. CLAIM CONSTRUCTION

A. Legal Standard

Petitioner contends "[t]he claim terms of the '441 patent should be construed to have their plain and ordinary meaning in view of the

specification." Pet. 5. Petitioner does not propose that we construe any specific claim terms. *Id*. at 4–5. Patent Owner responds that it "agrees for purposes of this preliminary response that no construction is necessary to analyze whether trial should be instituted." Prelim. Resp. 25.

Only terms that are in controversy need to be construed, and only to the extent necessary to resolve the controversy. *Wellman, Inc. v. Eastman Chem. Co.*, 642 F.3d 1355, 1361 (Fed. Cir. 2011); *Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc*., 200 F.3d 795, 803 (Fed. Cir. 1999). We determine that no express construction of a claim term is needed to resolve a dispute in this proceeding.

III. ANALYSIS

A. Independent Claim 6

Petitioner asserts that claim 6 is anticipated by either Horiguchi or Gallia. Pet. 26–36, 51–62. The Petition includes discussion identifying where each of Horiguchi and Gallia allegedly describes the elements of claim 6. *Id.*

1. Principles of Law

Anticipation, under 35 U.S.C. § 102, requires a lack of novelty. *Karsten Mfg. Corp. v. Cleveland Golf Co.*, 242 F.3d 1376, 1383 (Fed. Cir. 2001). To establish anticipation, each and every element in a claim, arranged as is recited in the claim, must be found in a single prior art reference. *Id.*

2. Horiguchi

Horiguchi is directed to a semiconductor memory and in particular to "a technique for repairing a semiconductor memory in such a manner that

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