

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.
Petitioner

v.

LIMESTONE MEMORY SYSTEMS LLC
Patent Owner

Case IPR. No. Unassigned
U.S. Patent No. 6,233,181
Title: SEMICONDUCTOR MEMORY DEVICE
WITH IMPROVED FLEXIBLE REDUNDANCY SCHEME

**Petition For *Inter Partes* Review of U.S. Patent No. 6,233,181 Under
35 U.S.C §§ 311-319 and 37 C.F.R. §§ 42.1-.80, 42.100-.123**

***Mail Stop* “PATENT BOARD”**
Patent Trial and Appeal Board
U.S. Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450

TABLE OF CONTENTS

	Page
1. INTRODUCTION	1
2. REQUIREMENTS FOR PETITION FOR INTER PARTES REVIEW	1
2.1. Grounds for Standing (37 C.F.R. § 42.104(a))	1
2.2. Notice of Lead and Backup Counsel and Service Information.....	1
2.3. Notice of Real-Parties-in-Interest (37 C.F.R. § 42.8(b)(1)).....	2
2.4. Notice of Related Matters (37 C.F.R. § 42.8(b)(2)).....	2
2.5. Fee for <i>Inter Partes</i> Review	4
2.6. Proof of Service.....	4
3. IDENTIFICATION OF CLAIMS BEING CHALLENGED (§ 42.104(B))	4
4. OVERVIEW OF THE 181 PATENT.....	6
5. 181 PATENT PROSECUTION HISTORY	9
6. CLAIM CONSTRUCTION	11
6.1. Applicable Law	11
6.2. Construction of Claim Terms	12
6.2.1. “word lines” (claims 1-7).....	12
6.2.2. “spare memory cells” (claims 1-7)	13
6.2.3. “sense amplifier bands” (claims 3 and 5)	14
7. PERSON HAVING ORDINARY SKILL IN THE ART	15
8. DESCRIPTION OF THE PRIOR ART	16
8.1. U.S. Patent No. 5,487,040 (“Sukegawa”).....	16
8.2. U.S. Patent No. 4,967,397 (“Walck”)	19

8.3.	Betty Prince, <i>Semiconductor Memories</i> (2d ed. 1992)	20
8.4.	U.S. Patent No. 5,355,339 (“Oh”).....	20
9.	GROUND #1: CLAIMS 1-2 AND 6 OF THE 181 PATENT ARE UNPATENTABLE AS OBVIOUS OVER SUKEGAWA.....	21
9.1.	Claim 1 is obvious over Sukegawa	21
9.1.1.	[1.P] A semiconductor memory device, comprising:	22
9.1.2.	[1.1a] a plurality of first memory blocks	22
9.1.3.	[1.1b] each having a plurality of first normal memory cells arranged in a matrix of rows and columns,	24
9.1.4.	[1.1c] each of said plurality of first memory blocks including word lines provided corresponding to said rows, respectively,.....	28
9.1.5.	[1.1d] and the first memory blocks aligned in the column direction; and.....	28
9.1.6.	[1.2a] a plurality of first spare memory cells arranged in a matrix of rows and columns in a particular one of said plurality of first memory blocks,	30
9.1.7.	[1.2b] each row of said plurality of first spare memory cells being capable of replacing a defective row including a defective first normal memory cell in said plurality of first memory blocks.	31
9.2.	Claim 2 is obvious over Sukegawa	32
9.2.1.	[2.P] The semiconductor memory device as recited in claim 1, further comprising:.....	32
9.2.2.	[2.1a] a plurality of second memory blocks arranged alternatively with said plurality of first memory blocks along the column direction,.....	32
9.2.3.	[2.1b] the second memory blocks each having a plurality of second normal memory cells arranged in a matrix of rows and columns; and.....	33

9.2.4. [2.2a] a plurality of second spare memory cells arranged in a matrix of rows and columns in a particular one of said plurality of second memory blocks,	34
9.2.5. [2.2b] each row of said plurality of second spare memory cells being capable of replacing a defective row including a defective second normal memory cell in said plurality of second memory blocks.	35
9.3. Claim 6 is obvious over Sukegawa	36
9.3.1. [6.P] The semiconductor memory device as recited in claim 1, wherein.....	36
9.3.2. [6.1] the first normal memory cells and the first spare memory cells are arranged alignedly in the column direction.	36
10. GROUND #2: CLAIM 3 OF THE 181 PATENT IS UNPATENTABLE AS OBVIOUS OVER SUKEGAWA IN VIEW OF PRINCE	39
10.1. [3.P] The semiconductor memory device as recited in claim 2, further comprising	39
10.1. [3.1] a plurality of sense amplifier bands provided between each of said plurality of first memory blocks and each of said second memory blocks,	39
10.2. [3.2] and shared by adjacent memory blocks in the column direction for sensing and amplifying data in each column of the adjacent memory block including a selected memory cell when activated.....	42
10.3. Motivation to Combine Prince and Sukegawa.....	43
11. GROUND #3: CLAIM 4 OF THE 181 PATENT IS UNPATENTABLE AS OBVIOUS OVER SUKEGAWA IN VIEW OF PRINCE	44
11.1. [4.P] The semiconductor memory device as recited in claim 2, wherein	44

11.2.	[4.1] the first memory blocks and the second memory blocks share a circuit related to a memory cell selection operation.	44
11.3.	Motivation to Combine Prince and Sukegawa.....	46
12.	GROUND #4: CLAIM 5 OF THE 181 PATENT IS UNPATENTABLE AS OBVIOUS OVER SUKEGAWA IN VIEW OF WALCK.....	47
12.1.	[5.P] The semiconductor memory device as recited in claim 3, wherein	47
12.2.	[5.1] said plurality of first memory blocks, said plurality of second memory blocks and said plurality of sense amplifier bands form a first memory array, and	47
12.3.	[5.2] said semiconductor memory device further comprises: a second memory array having a same arrangement as the first memory array; and.....	48
12.4.	[5.3a] control circuitry for driving one memory block from the first and second memory arrays into a selected state in a normal operation mode,	49
12.5.	[5.3b] and for simultaneously driving a prescribed number of memory blocks from each of said first and second memory arrays into a selected state in a particular operation mode.	50
12.6.	Motivation to Combine Sukegawa and Walck	51
13.	GROUND #5: CLAIM 7 OF THE 181 PATENT IS UNPATENTABLE AS OBVIOUS OVER SUKEGAWA IN VIEW OF OH.....	52
13.1.	[7.P] The semiconductor memory device as recited in claim 1, wherein	53
13.2.	[7.1] the first memory blocks other than said particular one has no first spare memory cells.	53
13.3.	Motivation to Combine Sukegawa and Oh	56
14.	CONCLUSION.....	56

Explore Litigation Insights

Docket Alarm provides insights to develop a more informed litigation strategy and the peace of mind of knowing you're on top of things.

Real-Time Litigation Alerts



Keep your litigation team up-to-date with **real-time alerts** and advanced team management tools built for the enterprise, all while greatly reducing PACER spend.

Our comprehensive service means we can handle Federal, State, and Administrative courts across the country.

Advanced Docket Research



With over 230 million records, Docket Alarm's cloud-native docket research platform finds what other services can't. Coverage includes Federal, State, plus PTAB, TTAB, ITC and NLRB decisions, all in one place.

Identify arguments that have been successful in the past with full text, pinpoint searching. Link to case law cited within any court document via Fastcase.

Analytics At Your Fingertips



Learn what happened the last time a particular judge, opposing counsel or company faced cases similar to yours.

Advanced out-of-the-box PTAB and TTAB analytics are always at your fingertips.

API

Docket Alarm offers a powerful API (application programming interface) to developers that want to integrate case filings into their apps.

LAW FIRMS

Build custom dashboards for your attorneys and clients with live data direct from the court.

Automate many repetitive legal tasks like conflict checks, document management, and marketing.

FINANCIAL INSTITUTIONS

Litigation and bankruptcy checks for companies and debtors.

E-DISCOVERY AND LEGAL VENDORS

Sync your system to PACER to automate legal marketing.