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Yamauchi et al.

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[54] SEMICONDUCTOR MEMORY DEVICE ALLOWING REPAIR OF A DEFECTIVE MEMORY CELL WITH A REDUNDANT CIRCUIT IN A MULTIBIT TEST MODE

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[73] Assignee: Mitsubishi Denki Kabushiki Kaisha, Tokyo, Japan

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[21] Appl. No.: 08/781,387

[22] Filed: Jan. 13, 1997

Primary Examiner—Robert W. Beausoliel, Jr.
Assistant Examiner—Nadeem Iqbal
Attorney, Agent, or Firm—McDermott, Will & Emery

[30] Foreign Application Priority Data

May 30, 1996 [JP] Japan 8-136935

[57] ABSTRACT

[51] Int. Cl.⁶ G06F 11/00

[52] U.S. Cl. 714/711; 365/201

[58] Field of Search 371/10.3, 10.2, 371/21.2, 21.1, 20.4, 22.5, 27.5, 40.2; 395/183.01, 183.06, 182.04, 182.05, 183.18, 185.01, 185.07; 365/201, 200, 189.01, 189.07; 324/73.1

In a predetermined multibit test mode, a multibit test circuit 114 issues determination result data pairs RDM0 and /RDM0 to RDM3 and /RDM3, each of which corresponds to match/mismatch of logics of data read from memory cells selected by one column select line in corresponding one of memory cell plane blocks. In each memory cell plane block, memory cell columns selected by one single column select line can be replaced as a unit. The unit of memory cell columns containing a defective memory cell is replaced in accordance with determination result data RDM0 and /RDM0 to RDM3 and /RDM3.

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24 Claims, 16 Drawing Sheets

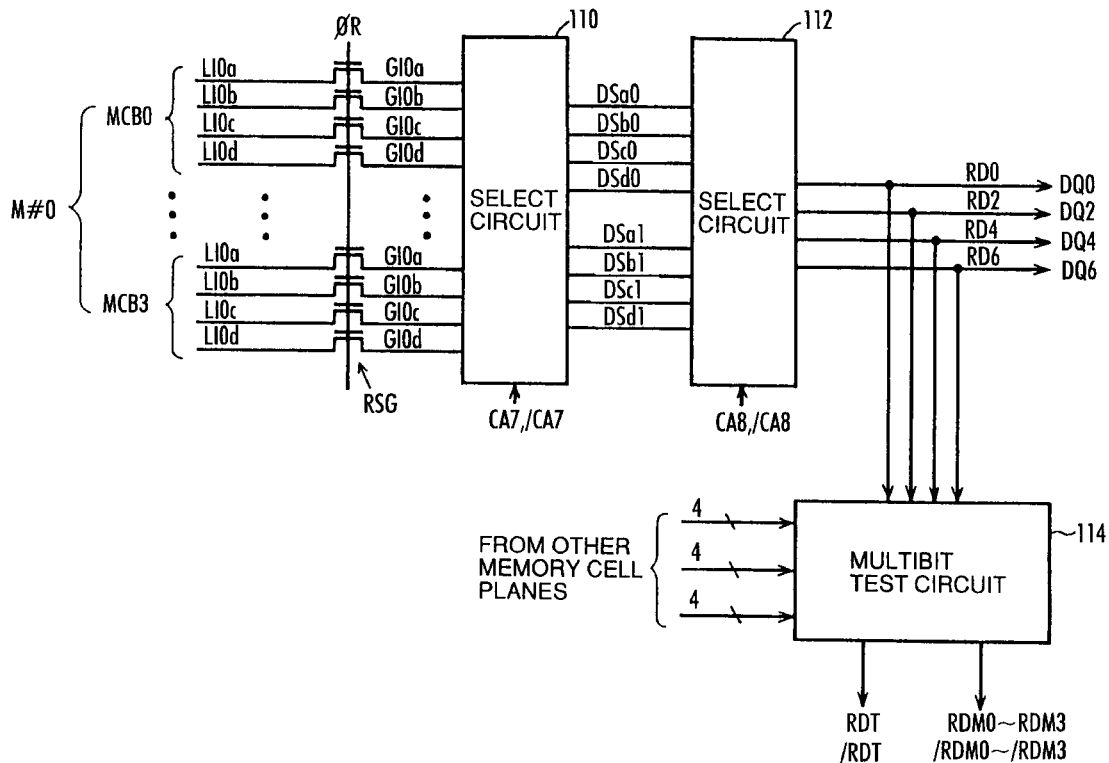


FIG. 1

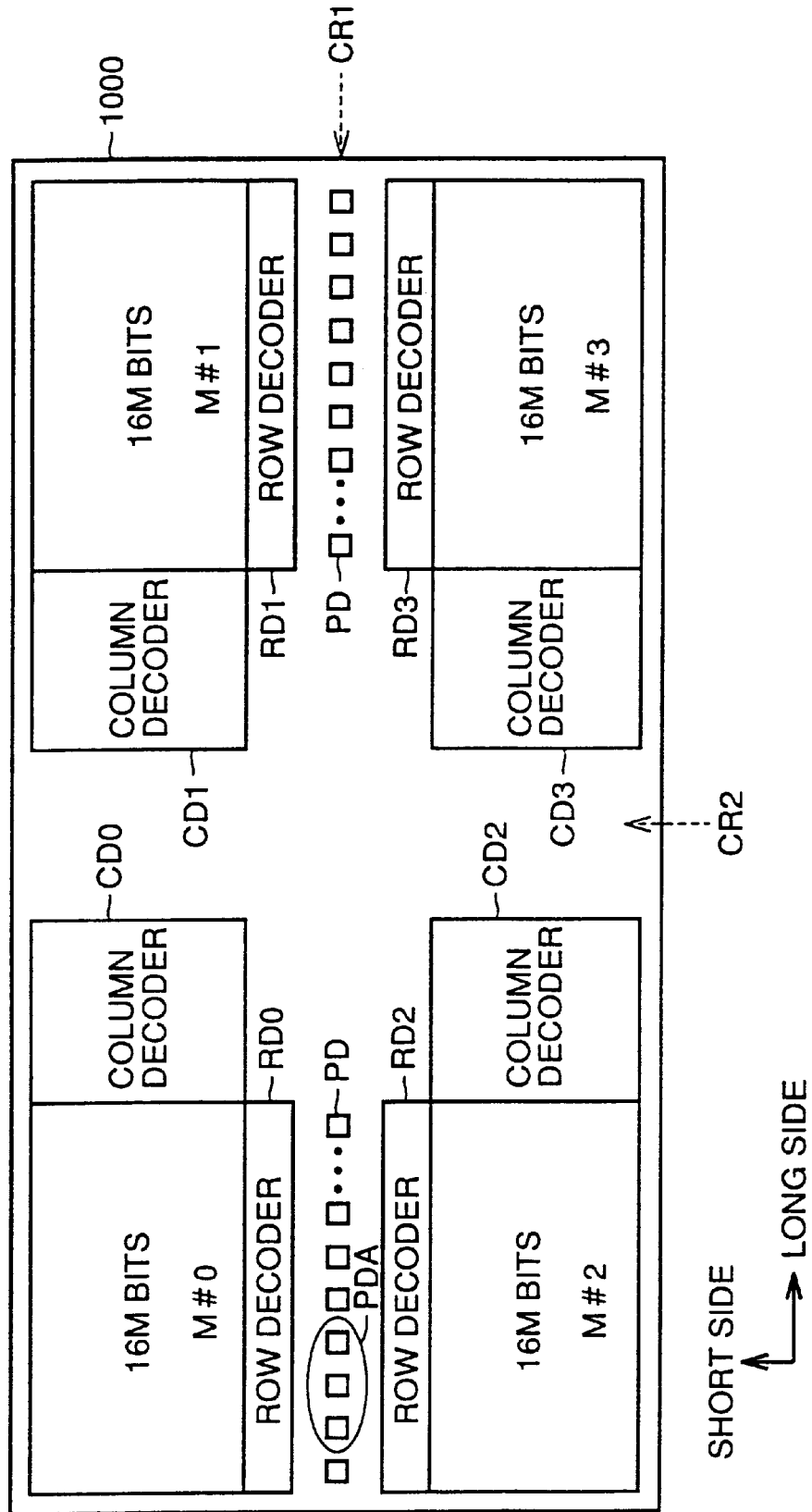


FIG. 2

CD	ROW DECODER							RD	
	COLUMN DECODER	SENSE AMPLIFIER BAND	512K ROW BLOCK	SENSE AMPLIFIER BAND	512K ROW BLOCK	SENSE AMPLIFIER BAND	512K ROW BLOCK	SENSE AMPLIFIER BAND	M#
		SAB0	MRB0	SAB1	MRB1	SAB31	MRB31	SAB32	
					•••				
	SPARE COLUMN DECODER				SPARE COLUMN				

FIG. 3

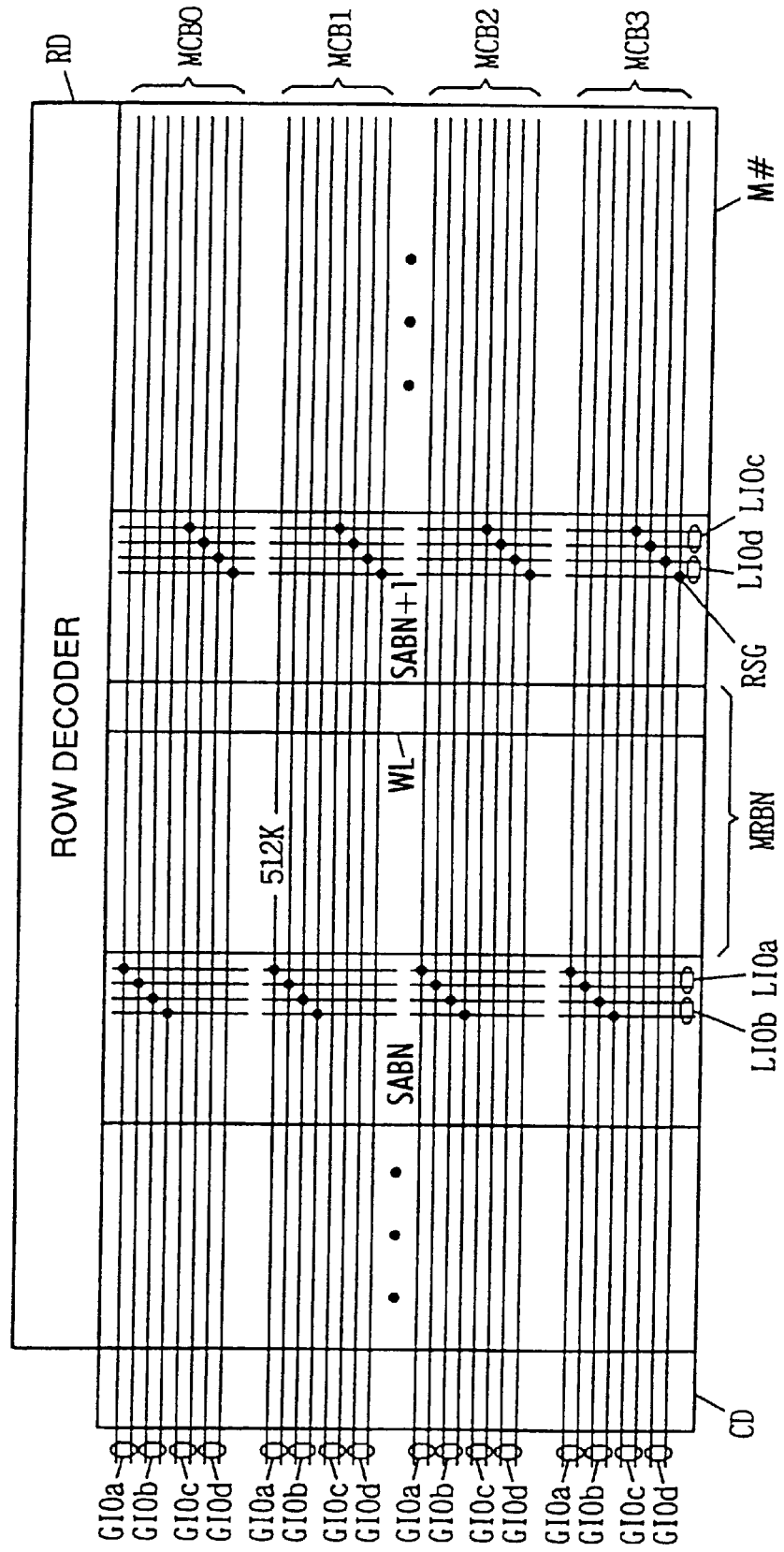
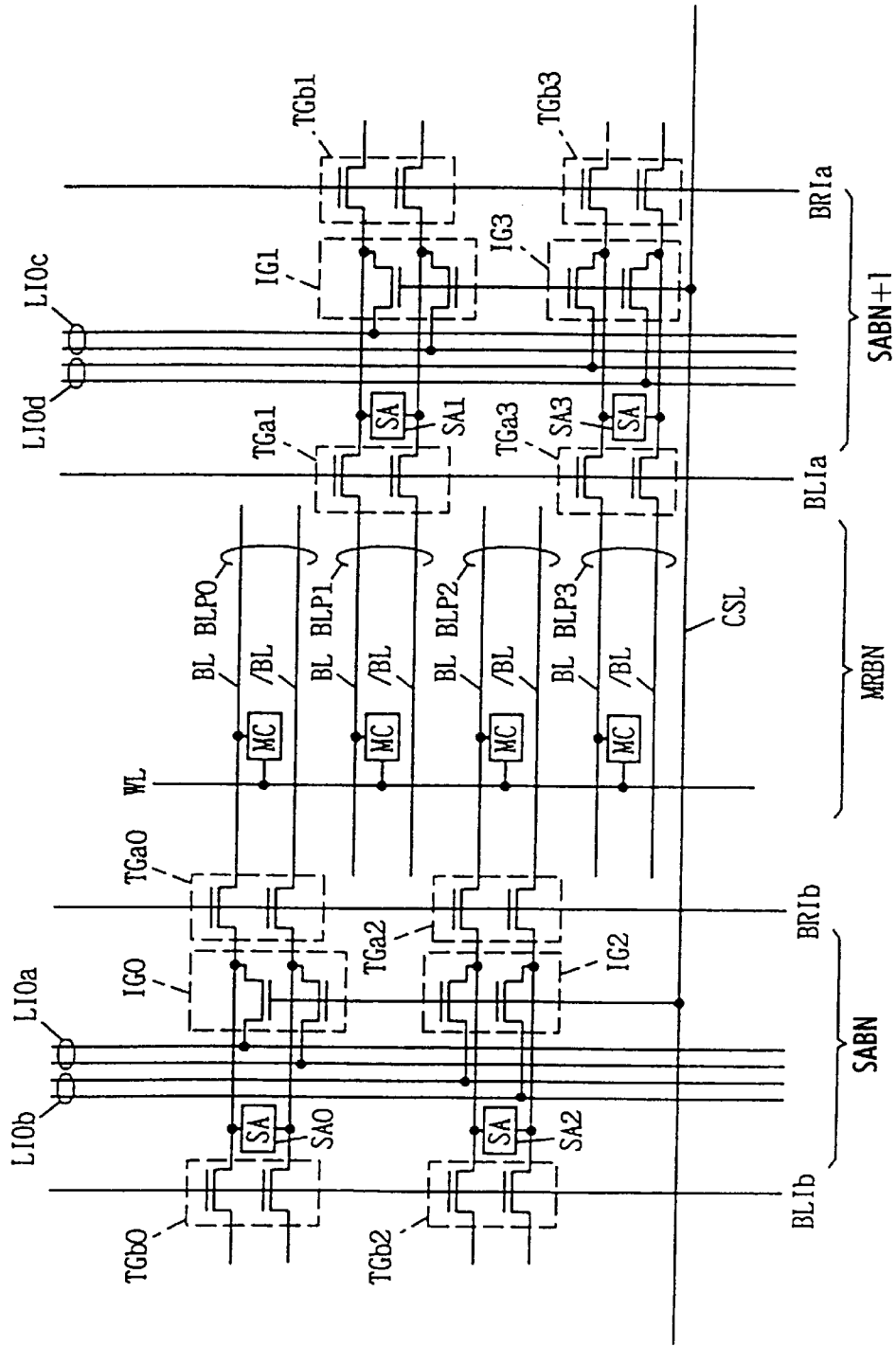


FIG. 4



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