



[54] SEMICONDUCTOR MEMORY DEVICE

FOREIGN PATENT DOCUMENTS

[75] Inventors: **Hideto Hidaka; Mikio Asakura; Kazuyasu Fujishima; Tsukasa Ooishi; Kazutami Arimoto; Shigeki Tomishima; Masaki Tsukude**, all of Hyogo, Japan

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[73] Assignee: **Mitsubishi Denki Kabushiki Kaisha**, Tokyo, Japan

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*Primary Examiner*—Do Hyun Yoo  
*Attorney, Agent, or Firm*—Lowe, Price, LeBlanc & Becker

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Jan. 10, 1994 [JP] Japan ..... 6-001017  
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[57] ABSTRACT

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Drains of first and second transistors are connected to a low level line of an internal circuitry such as a sense amplifier related to determination of a potential in a memory cell. The first transistor has its gate diode-connected to a sense drive line and its source grounded. The second transistor receives at its gate an internally generated signal, and its source is grounded. In the standby state, the potential of the sense drive line is set higher than low level of said word lines by the threshold voltage  $V_{thn}$  of the first transistor and used as dummy GND potential  $V_{ss}'$ , and in the active state, the second transistor is rendered conductive so as to prevent floating of the sense drive line from the dummy GND potential  $V_{ss}'$ .

[52] U.S. Cl. .... 365/189.09; 365/174; 365/189.01; 365/189.11; 365/2.01; 365/226; 365/230.06

[58] Field of Search ..... 365/189.01, 226, 365/189.11, 189.09, 230.06, 174, 201

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42 Claims, 57 Drawing Sheets

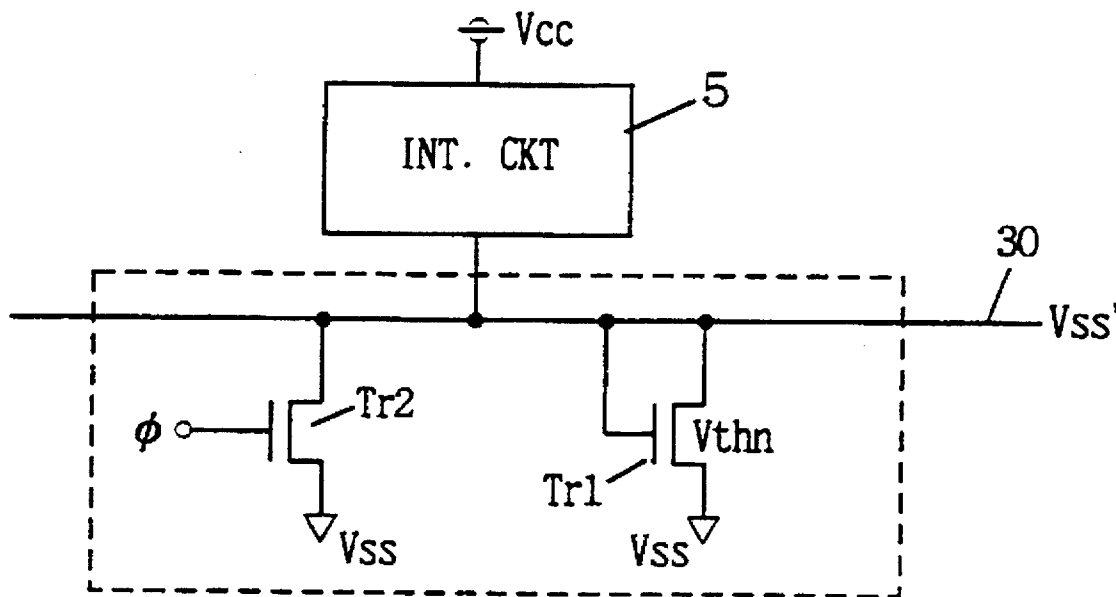


FIG. 1B

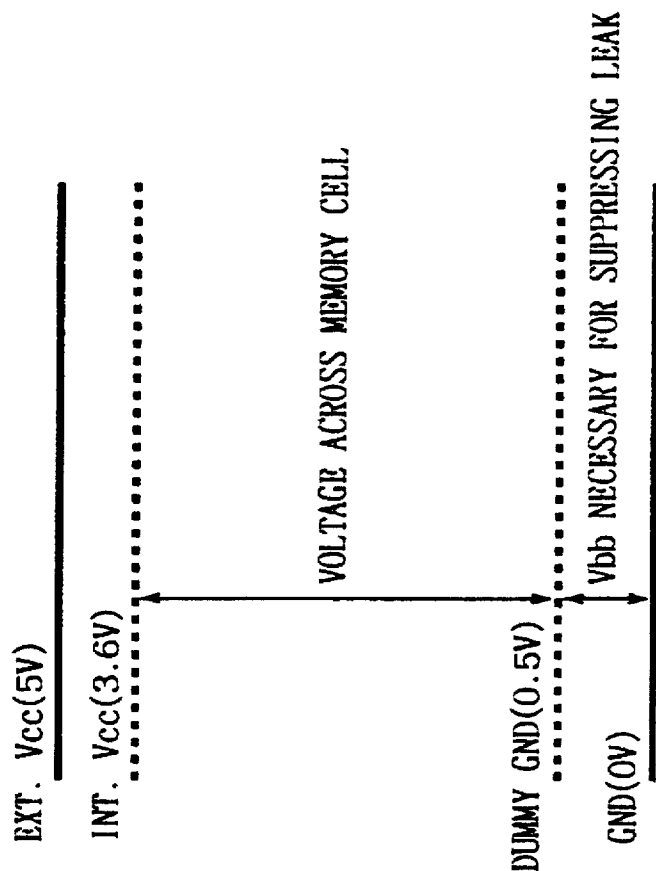


FIG. 1A

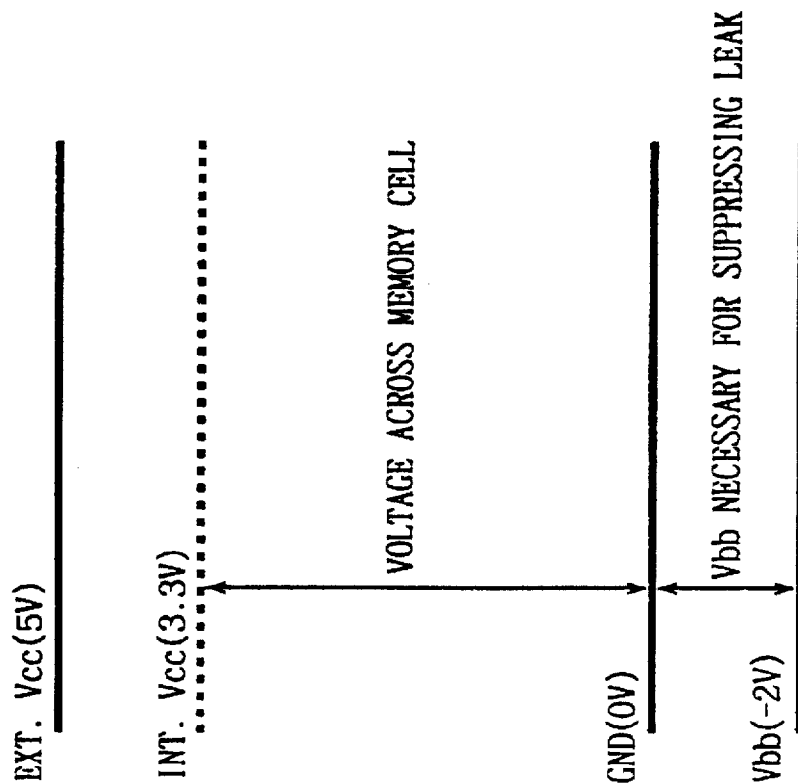


FIG. 2

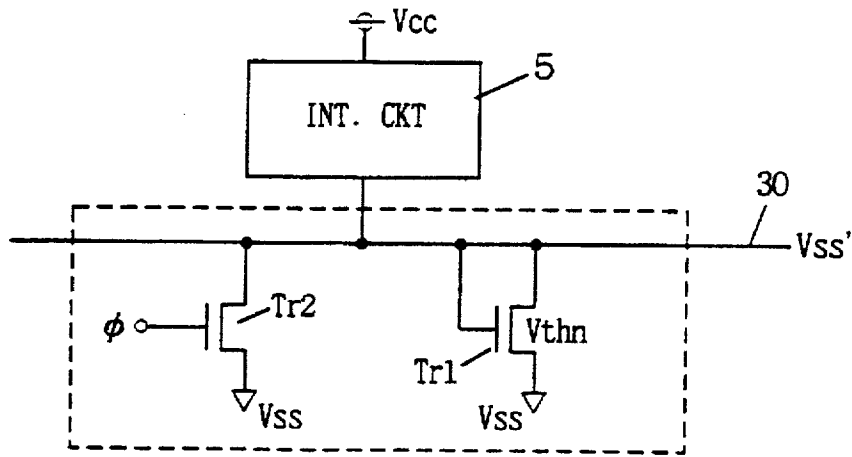


FIG. 3

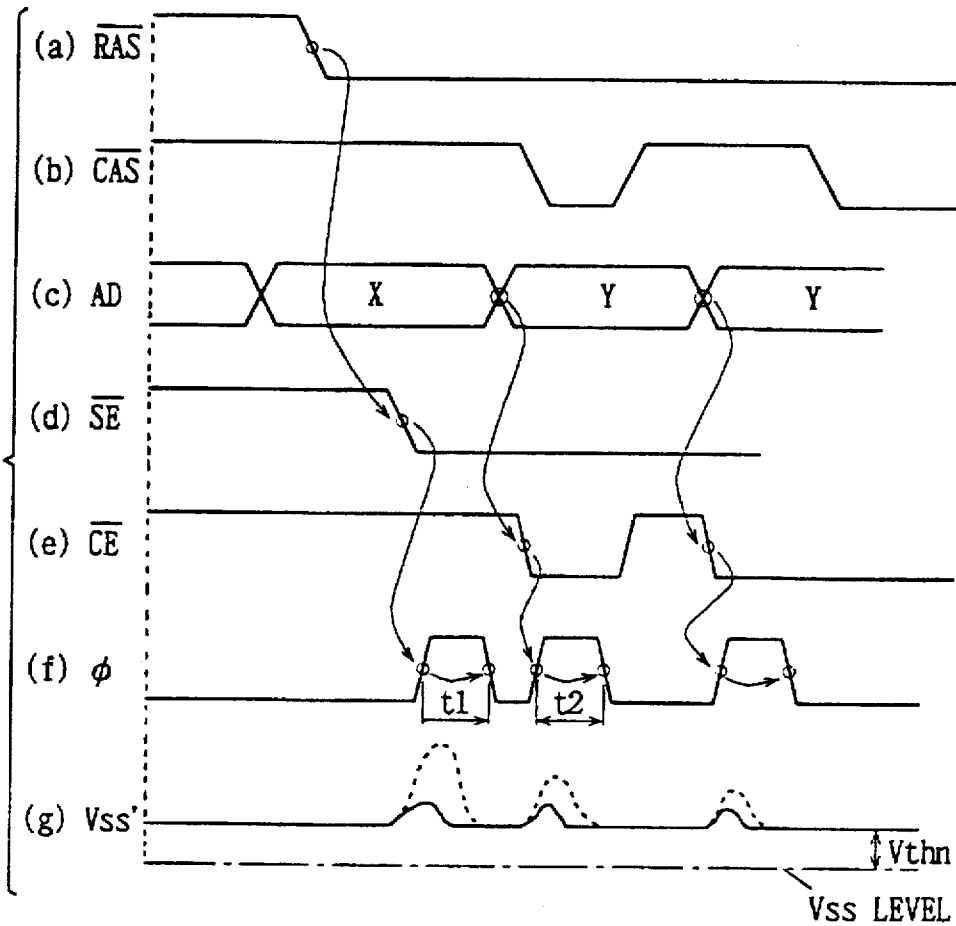


FIG. 4

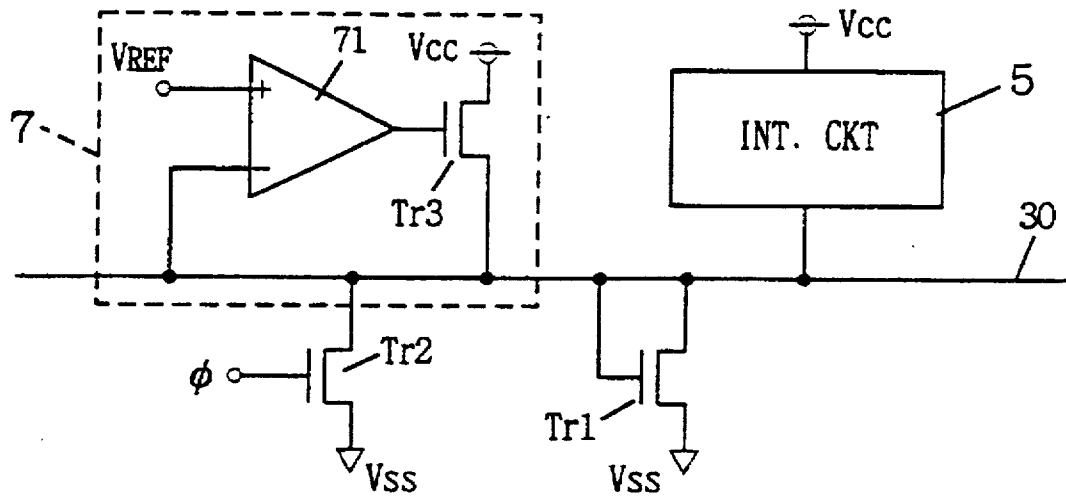


FIG. 5

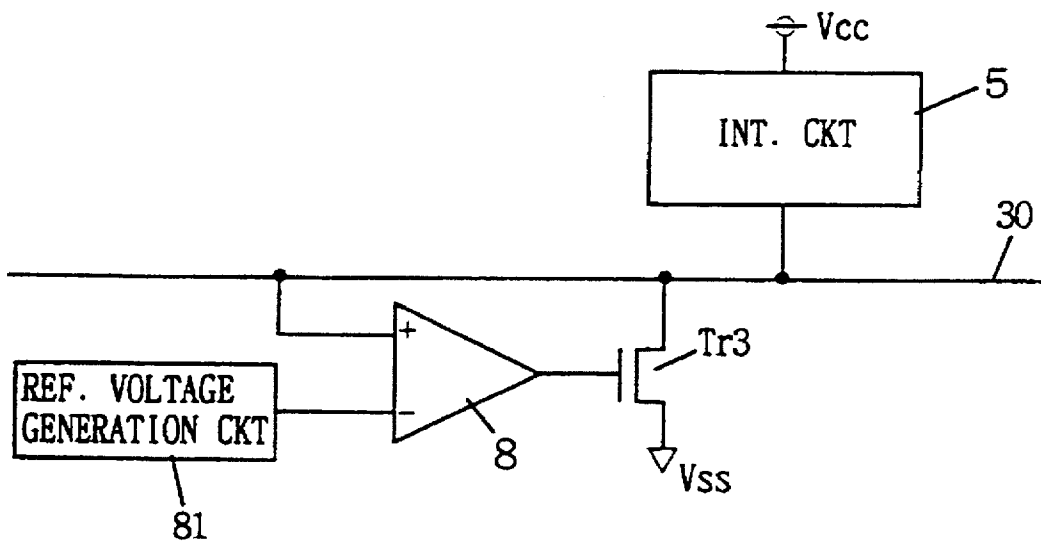


FIG. 6

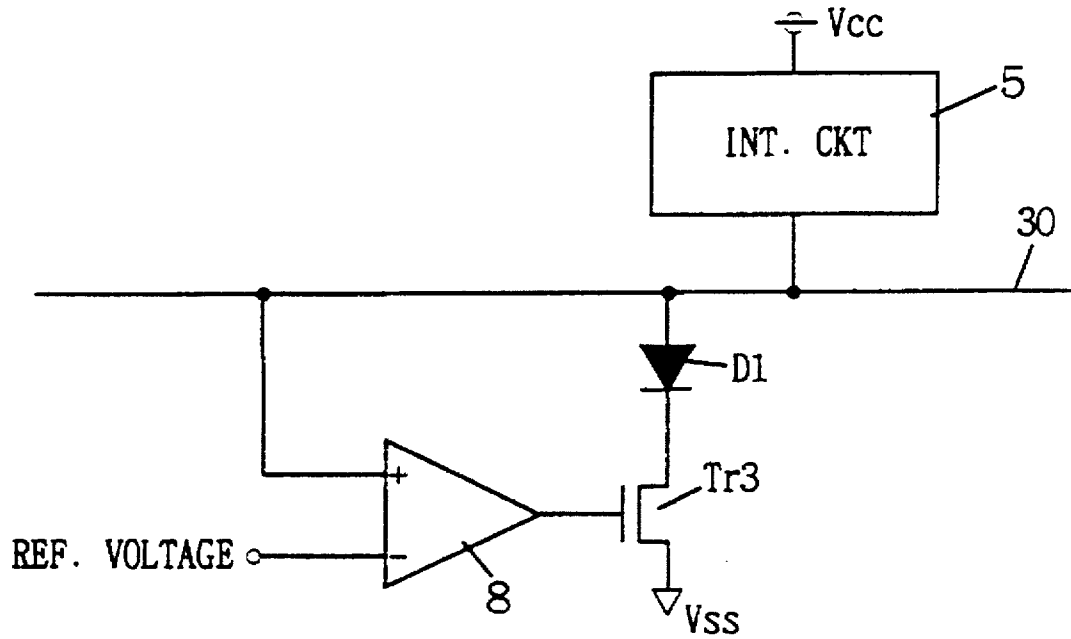
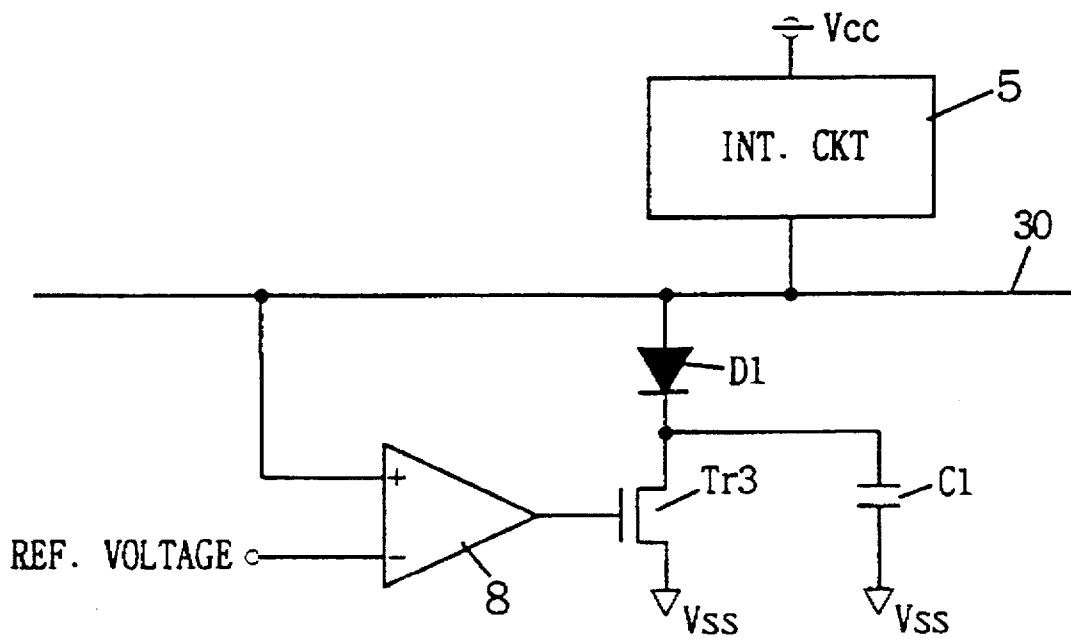


FIG. 7



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