United States Patent [19]

Watanabe et al.

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[54] **SYNCHRONOUS SEMICONDUCTOR MEMORY DEVICE WITH MULTI-BANK CONFIGURATION**

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[30] **Foreign Application Priority Data**

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[51] **Int. Cl.^{6}** **G11C 8/00**

[52] **U.S. Cl.** **365/230.03**; 365/196

[58] **Field of Search** 365/230.03, 196, 365/191, 190

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Attorney, Agent, or Firm—McDermott, Will & Emery

[57] **ABSTRACT**

Memory blocks provided to share a sense amplifier bank, a global IO (GIOB) bus provided in common to the memory blocks for transferring internal data, and local IO bus lines provided corresponding to the memory blocks are connected-controlled based on signals related to a column select operation. Driving memory blocks independently from each other permits each memory block to be used as a bank, and if one memory block is accessed during activation of another memory block, data can be prevented from colliding on the global IO bus. A main memory with high page hit rate is implemented using a semiconductor memory device with a shared-sense amplifier configuration. When a memory block sharing a sense amplifier coupled to another memory block is addressed, the another memory block is inactivated and then addressed memory block is accessed, when a valid data is output, such valid data outputting is signaled by a data valid signal.
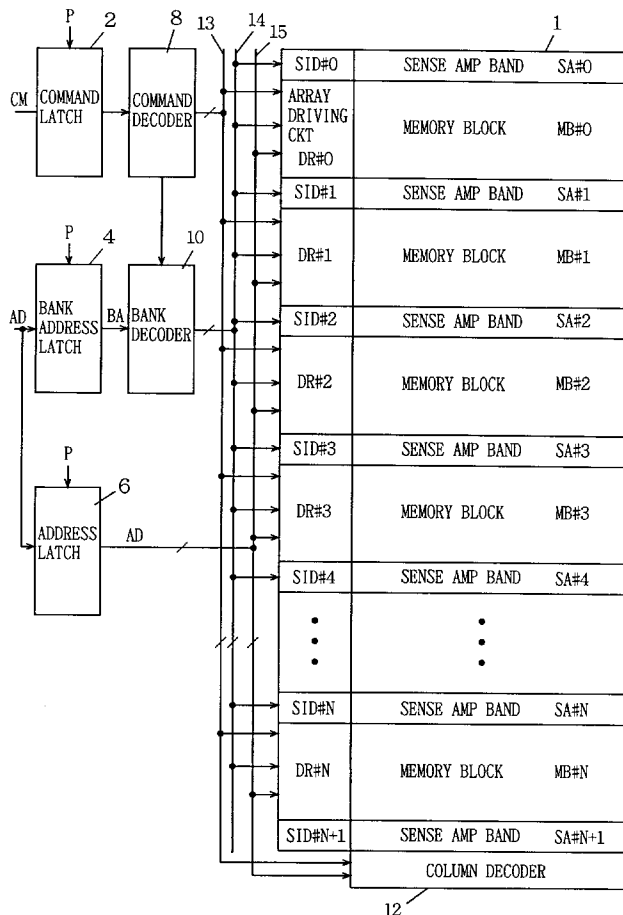
9 Claims, 18 Drawing Sheets

FIG. 1

FIG. 2

FIG. 3

F I G. 4

MB#n-1

BLa1 /BLa1 BLa3 /BLa3

BTGa1 BTGa3

BLI2n-1

SA#n • • • SAa1 SAa2

BLI2n

BTGn2 BTGn4

M#n

WLn0

WLn1

BLn1 BLn3
/BLn1 /BLn3

WLnm

BLn2 BLn4
/BLn2 /BLn4

MB#n

WLnM

BTGn1 BTGn3

BLI2n+1

SA#n+1 • • • SAb1 SAb2
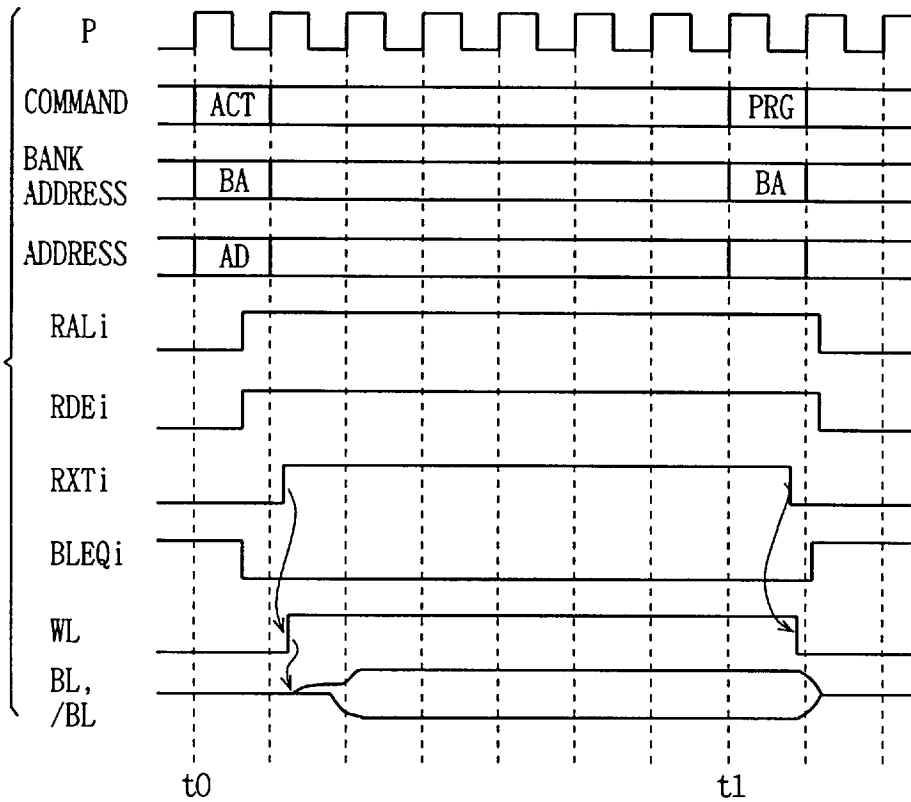
BLI2n+2

BTGb2 BTGb4
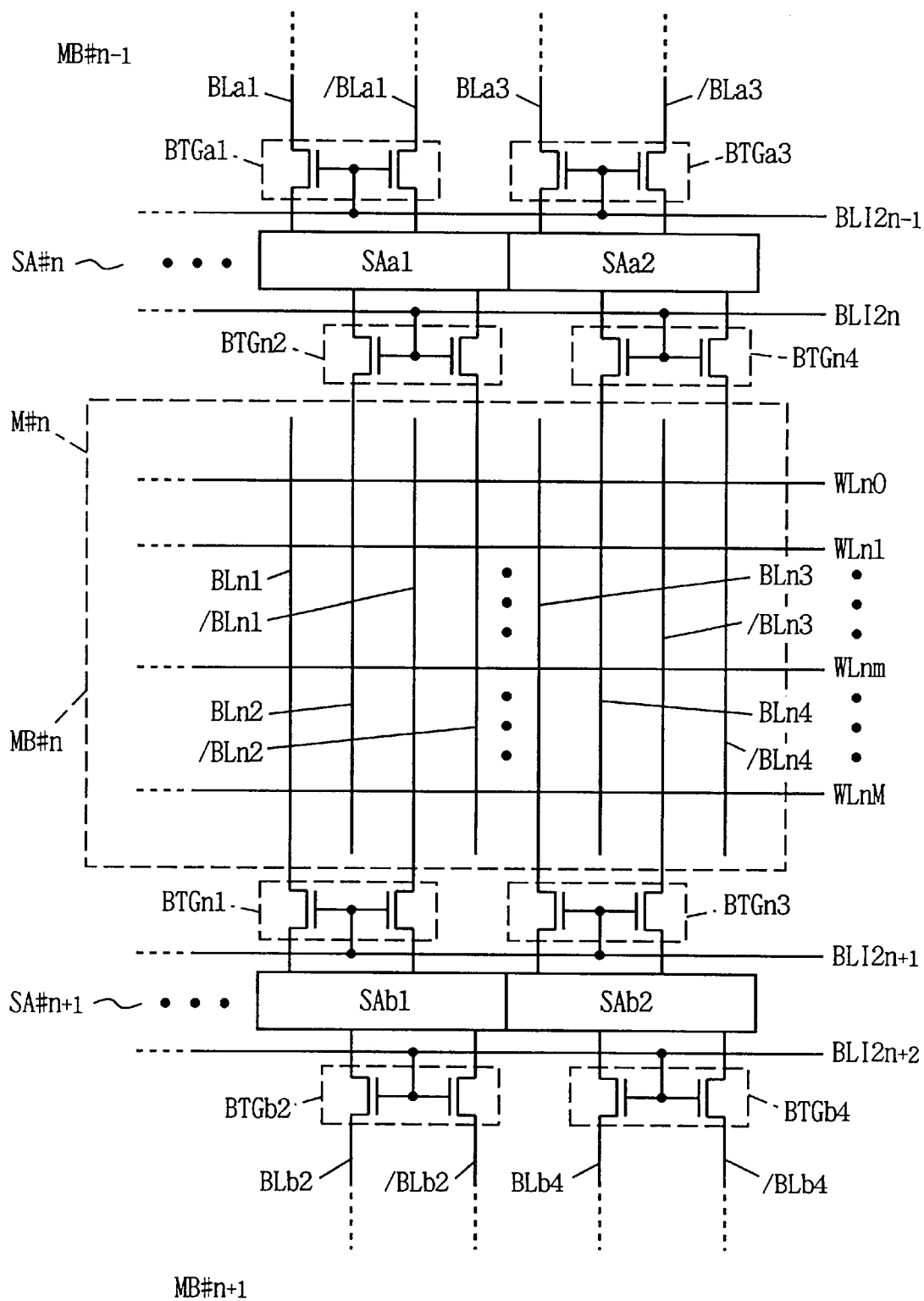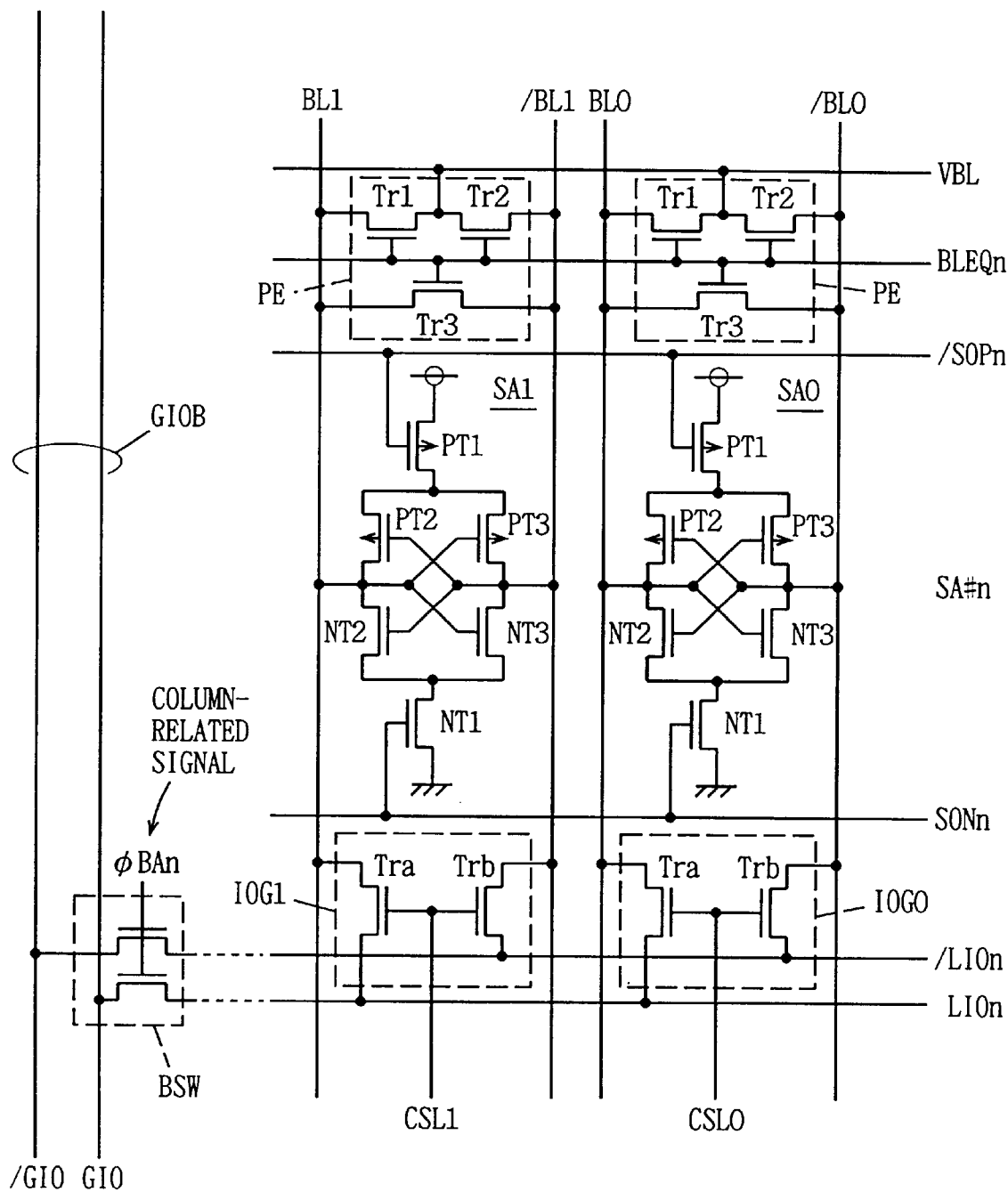
BLb2 /BLb2 BLb4 /BLb4

MB#n+1
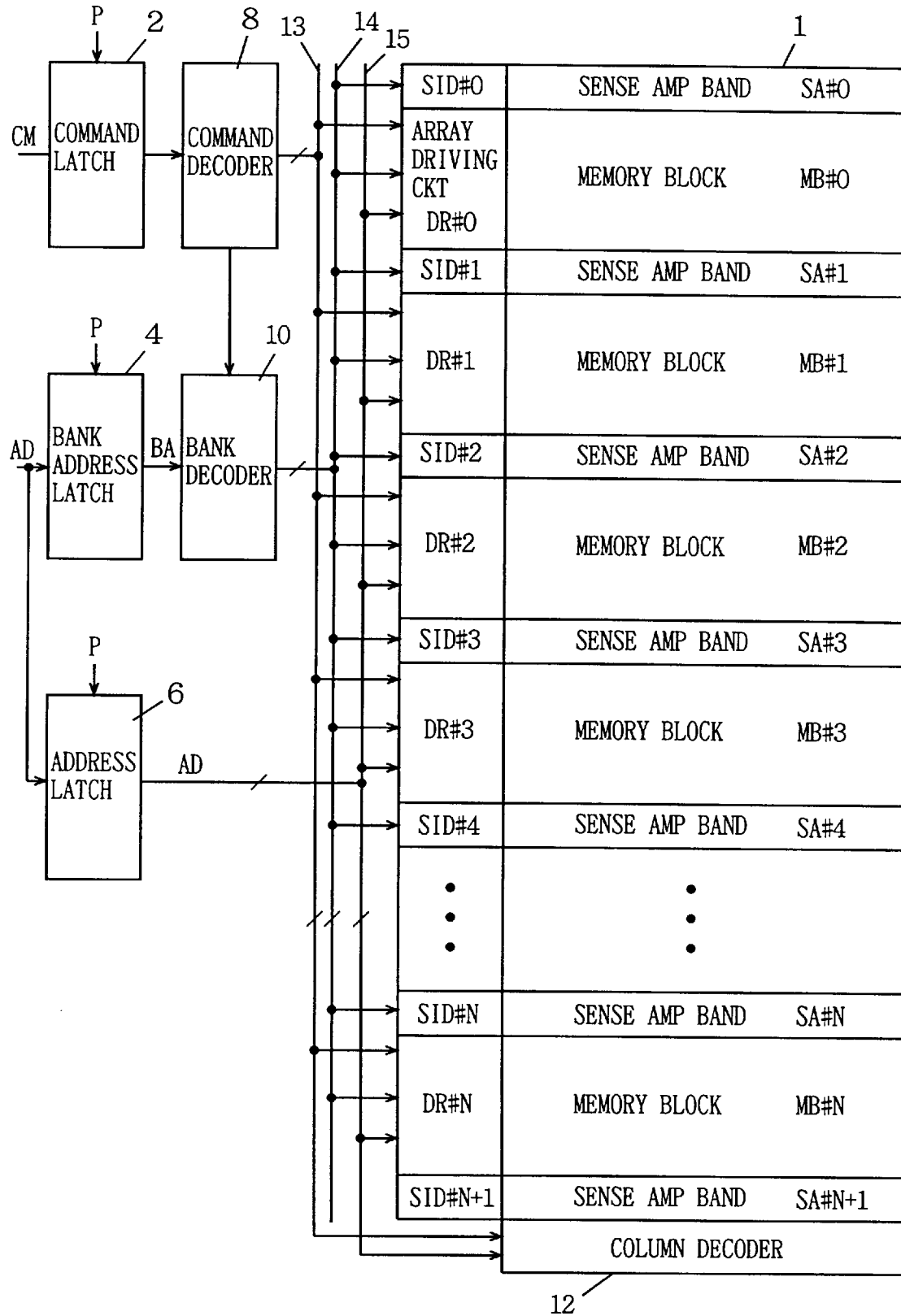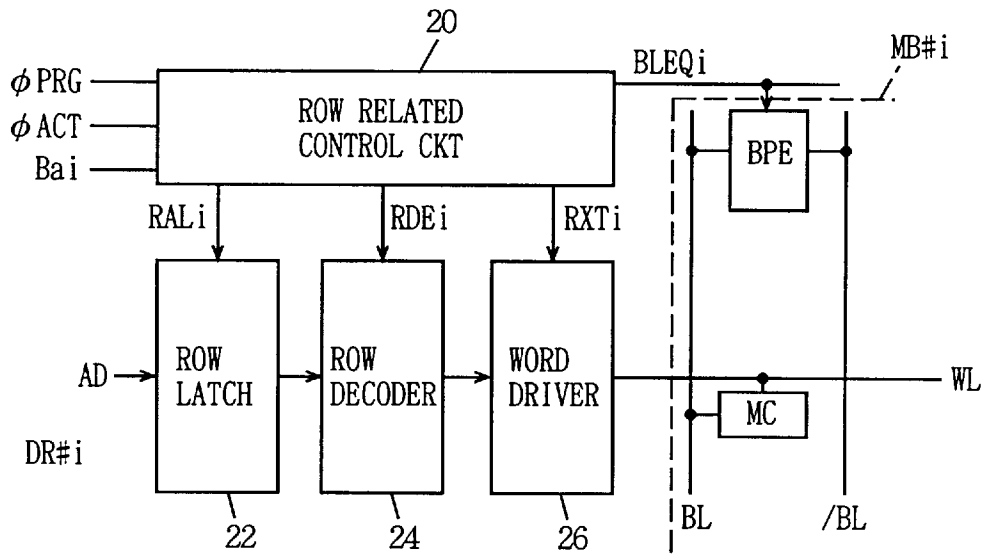
F I G. 5

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