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United States Patent [19]

[11] Patent Number: **5,267,214**

Fujishima et al.

[45] Date of Patent: **Nov. 30, 1993**

[54] **SHARED-SENSE AMPLIFIER CONTROL SIGNAL GENERATING CIRCUIT IN DYNAMIC TYPE SEMICONDUCTOR MEMORY DEVICE AND OPERATING METHOD THEREFOR**

FOREIGN PATENT DOCUMENTS

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[57] ABSTRACT

[21] Appl. No.: **616,264**

A dynamic random access memory amplifier arrangement includes a sense amplifier band shared between two different memory blocks. In this memory, only sense amplifiers related to a selected memory block are activated. The memory comprises a circuit for boosting a control signal voltage to a switching unit for connecting the selected memory block to the sense amplifiers up to a level higher than a power supply voltage V_{cc} during the activation of the sense amplifiers, and a circuit for separating a memory block paired with the selected memory block from the activated sense amplifiers during the sensing operation. The memory further comprises a circuit for generating a control signal of the power supply voltage V_{cc} and connecting all the memory blocks to the corresponding sense amplifiers in a stand-by state wherein a row address strobe signal is inactive. With this arrangement, a highly reliable memory consuming less power can be achieved which ensures data writing and/or rewriting at a full V_{cc} level.

[22] Filed: **Nov. 20, 1990**

[30] **Foreign Application Priority Data**

Feb. 16, 1990 [JP] Japan 2-36666

[51] Int. Cl.⁵ **G11C 11/34**

[52] U.S. Cl. **365/230.03; 365/230.06; 365/149; 365/208**

[58] Field of Search **365/230.03, 207, 208, 365/230.06, 149, 189.11**

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9 Claims, 15 Drawing Sheets

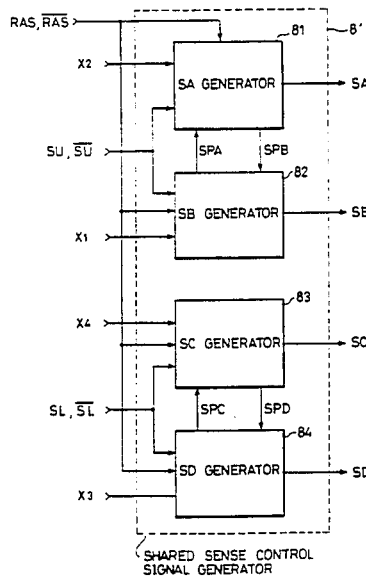
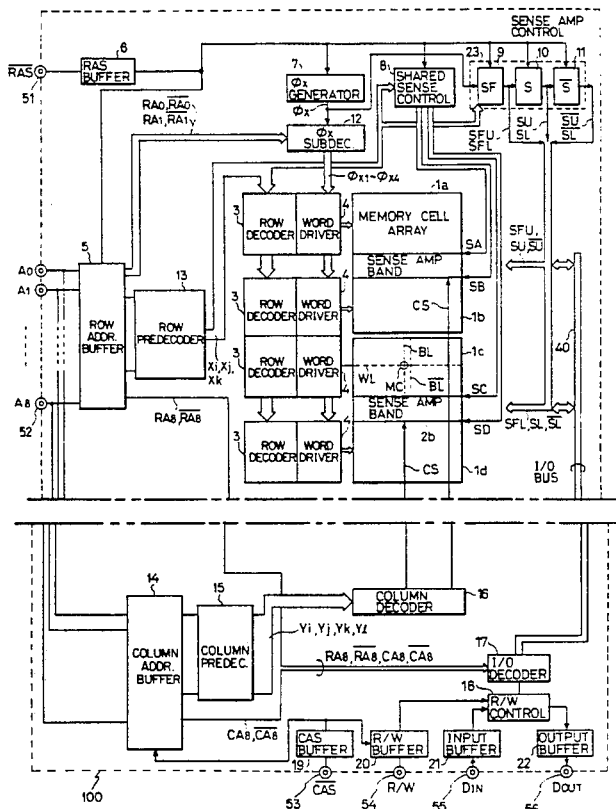


FIG. 1B
PRIOR ART

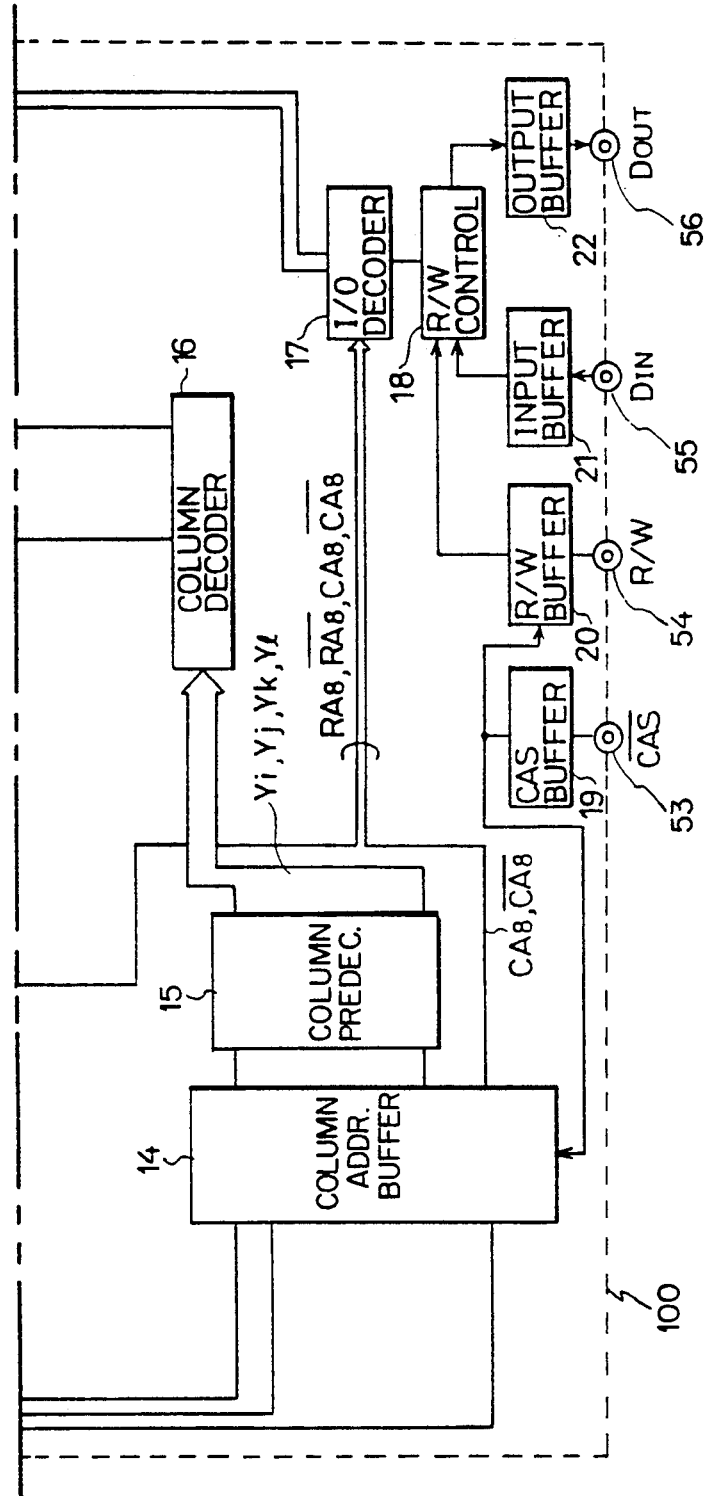


FIG.2 PRIOR ART

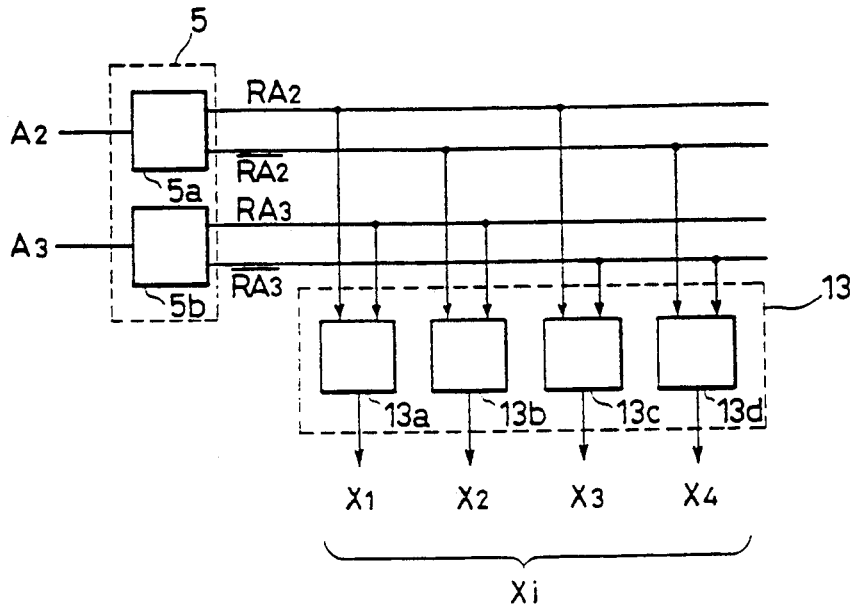
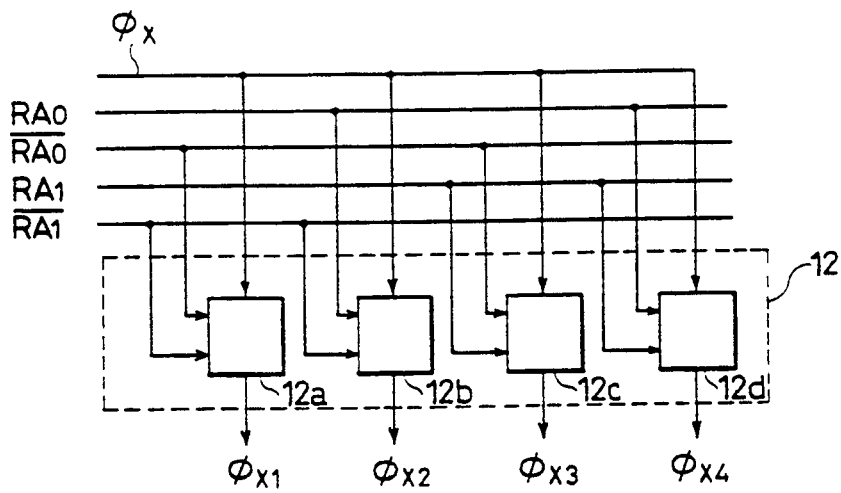
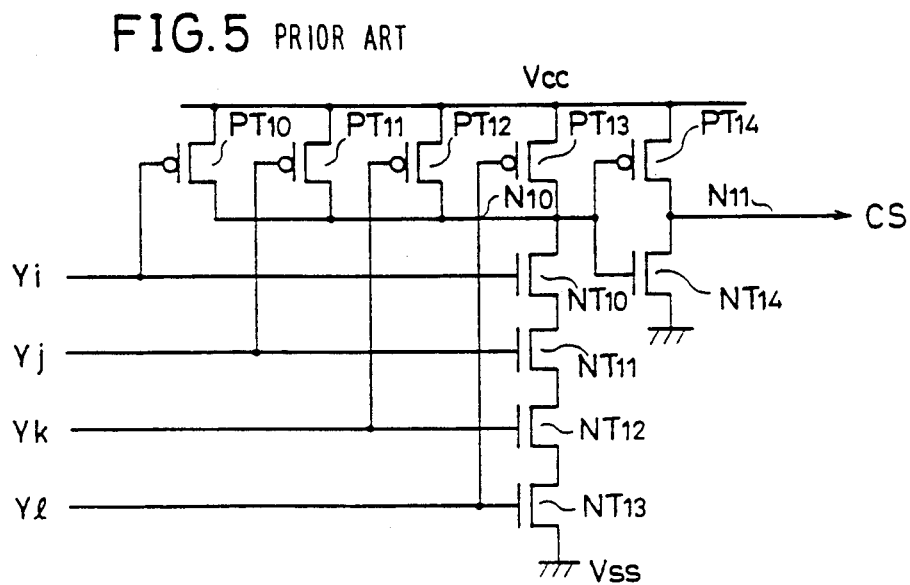
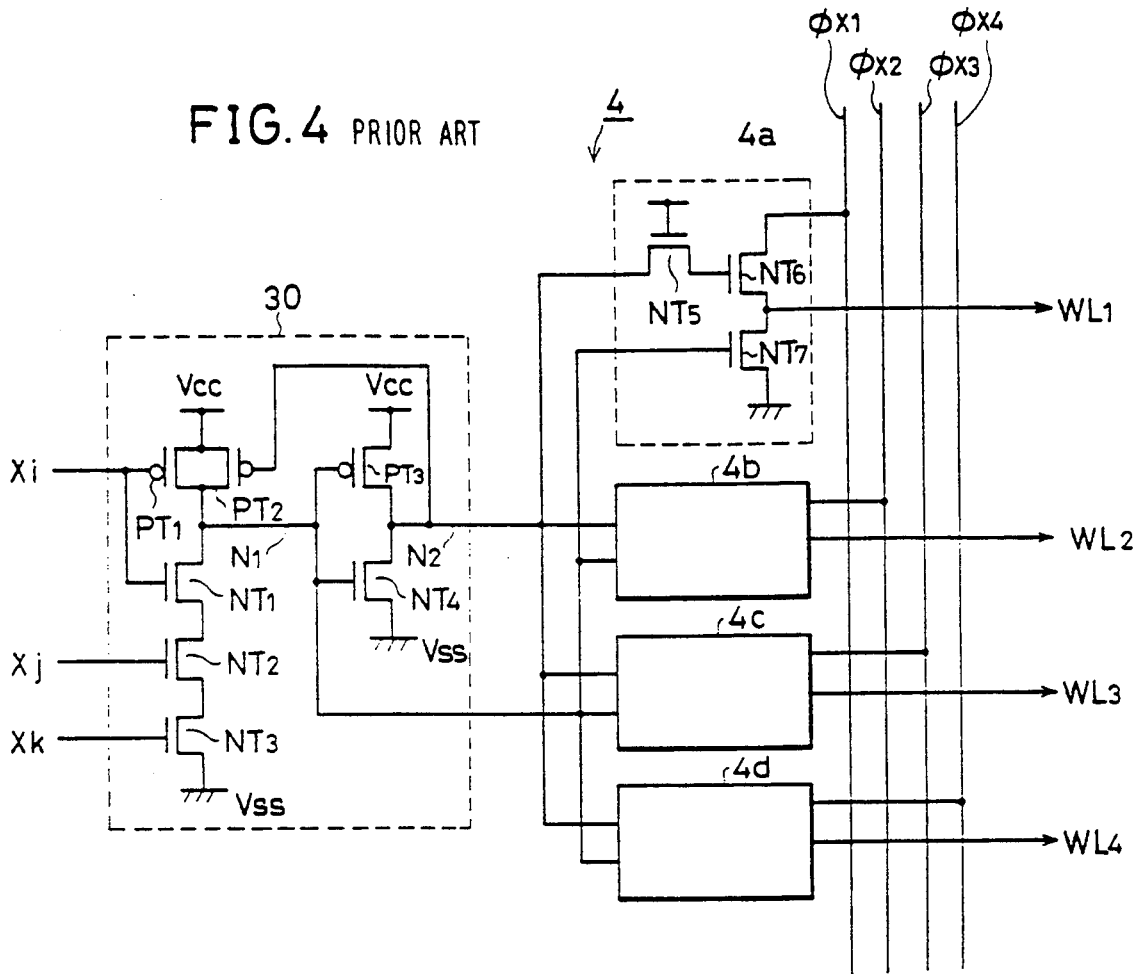


FIG.3 PRIOR ART





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