(54) **High efficiency row redundancy for dynamic ram.**

(57) A row redundancy scheme is disclosed which allows the enablement of a redundant array (4-RED.WARDS) of memory before the disablement of a defective and usual array (0-31) of memory. Each redundant array is capable of serving numberous usual arrays in the function of replacing rows of usual memory arrays. Consequently, considerable space saving and memory operating speed are realized by the row redundancy scheme.
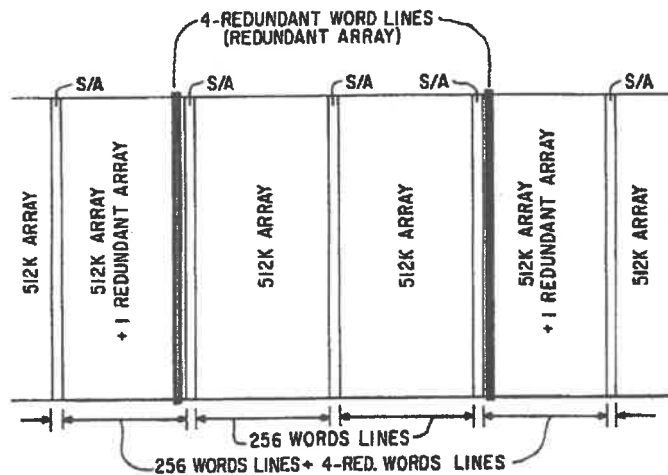
FIG. 5b

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## Field of the Invention

The invention is in the field of integrated circuits and more specifically, in the field of integrated circuit memory devices.

## Background of the Invention

Electronic devices and systems such as printers, copiers, electronic storage devices (memories), high definition television, enhanced definition television and computational devices (e.g. calculators and computers including personal computers, minicomputers, personal work stations and microcomputers) requiring electronic storage devices, often provide data storage on a semiconductor integrated circuit chip. Because these devices often require large amounts of storage space for many applications, these storage devices are embodied in a dynamic random access memory.

As the demand has grown for increased memory space, the density of dynamic random access memories, DRAMs, has correspondingly increased. However, with increased memory density, increased memory operating speed is also demanded. Consequently, the complexity of the DRAM has likewise increased with these demands.

Defects in fabrication discovered in earlier generations of DRAMs resulted in disposal of the DRAM. This practice became too expensive and wasteful. Therefore, conventional memories often provide redundant structures (i.e. redundant word lines along with associated redundant memory cells) on the memory chip to act in place of the word line and its associated memory with which a defect is attributable. As a consequence of the redundancy, an integrated memory chip can be salvageable regardless of the defect.

Goals of increased density and speed in the development of DRAMS has resulted in the additional criterion of optimized use of chip real estate within the constraints of the desired memory density.

Prior art DRAMS have been developed for memory densities up to 16 megabits. Memories, such as the 16 megabit memory are often organized as a plurality of memory arrays with each array having a predetermined density. Such memories place a predetermined number, i.e. 4, of redundant word lines and their associated memory cells within each memory array. Generally, there are as many redundant word lines (and associated redundant memory cells) as there are memory arrays. Along with the redundant word lines and cells, row decoders for decoding word lines and the rows of redundant memory are required. Conceivably, with an increasing memory density, this redundancy scheme can result in many unused and therefore wasted redundancy word lines and associated redundancy memory cells since the number and decoding capacity of the row redundancy decoders is much smaller than the number of redundant word lines. An additional drawback of conventional redundancy schemes is that even though a large number of redundant word lines exist on a memory chip, only defects associated with a word line or a memory cell up to the number of redundant word lines in an array can be corrected in an array. For instance, if the redundancy scheme for the 16 megabit DRAM were incorporated for use in a 64 megabit memory, perhaps it could be arranged such that there are 128 arrays of approximately 512,000 (512k) rows of memory. If 4 redundant word lines exist in each array, then approximately 512 total redundant word lines (and associated circuitry) would exist on the 64 megabit chip. Thus, even though there are 512 redundant word lines on the chip, only four defective word lines are replaceable in each array. The average number of defects in conventionally sized DRAMs is 10. However, the average number of defects in a 64 megabit DRAM will probably be close to 50. Since the 16 megabit DRAM redundancy scheme requires the same number of redundant word lines as the number of memory arrays, the 16 megabit redundancy scheme incorporated into a 64 megabit memory would occupy a large amount of chip real estate.

A further drawback of conventional redundancy schemes such as a redundancy scheme for 16 megabit DRAMs is that since the defect is replaced by a redundant word line (and associated circuitry) in the same array in which the defect exists, the defective word line must be disabled before the redundant word line can be activated, otherwise a bit error may result. Consequently, this requirement slows the speed of the memory.

Until now a need has existed for a new and improved memory since conventional schemes are unacceptable, as explained above, for memory densities of 64 megabits and greater.

## OBJECTS OF THE INVENTION

It is an object of the invention to provide a new and improved redundancy scheme for a memory.

It is another object of the invention to provide anew and improved row redundancy scheme for a memory.

It is a further object of the invention to provide a row redundancy scheme for a memory which dose not require the disablement of a usual array before activation of an associated redundant array.

These and other objects of the invention, together with the features and advantages thereof, will become apparent from the following detailed

specification when read together with the accompanying drawings in which applicable reference numerals, letters, and symbols have been carried forward.

## SUMMARY OF THE INVENTION

The foregoing objects of the invention are accomplished by a row redundancy scheme which activates a redundant array prior to disabling an associated usual array.

The scheme can be implemented in a memory architecture comprising a plurality of memory arrays in which a predetermined number of arrays each include a redundancy array. Each time a row of memory from a redundant array is chosen to replace a defective row of memory cells in a memory array, the redundant array lies outside of the array in which the defective row exists.

## BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1a illustrates a plan view of the architecture of the hierarchical multi-data lines memory.

Figure 1b illustrates a block diagram illustrating the flow of data to the wide data path circuit.

Figures 1c through 1e illustrate logic diagrams of possible logic accomplished in the wide data path.

Figure 2 illustrates a read/write data bus scheme which includes a schematic drawing of a wide data path circuit.

Figure 3a illustrates a plan view of another embodiment of the memory architecture.

Figure 3b illustrates a plan view of the preferred embodiment of the memory architecture.

Figure 4 illustrates one 512,00 bit memory cell array and its associated circuitry.

Figure 5a illustrates a plan view of one quadrant of the invention's memory architecture.

Figure 5b illustrates a more detailed plan view of the invention's memory architecture.

Figure 6 illustrates a logic diagram relating to the activation or disablement of a redundant array.

Figure 7 illustrates a schematic drawing of the invention's row redundancy decoder circuit.

Figure 8a illustrates a schematic drawing of a usual memory array and its associated sense amps.

Figure 8b illustrates a timing diagram for the operation of that illustrated in figure 8a.

Figure 8c illustrates a schematic drawing of a usual memory array, an associated redundant array, and associated circuitry.

Figure 8d illustrates a timing diagram for the operation of that illustrated in figure 8c.

Figure 9 illustrates a plan view of on quadrant of an alternative embodiment of the memory architecture.

Figure 10 illustrates an alternative embodiment of the invention's row redundancy decoder circuit for use in the memory architecture shown in figure 8.

## ADVANTAGES OF THE INVENTION

A primary advantage of the invention is its ability to allow selection of redundant memory before disablement of the usual memory, thereby resulting in increased memory operation.

Another primary advantage of the invention lies its versatility in the replacement of a defective word line by redundant word lines.

Still another primary advantage of the invention is its compact size which results in part by its not having to provide dedicated redundant word lines for each memory array.

## Detailed Description of the Invention

The invention provides a new and improved redundancy scheme suitable for high density memories, i.e. memories of the size 16 megabit, 64 megabit and greater.

The invention's redundancy scheme is most adaptable for DRAM architectures which have local input/output (I/O) lines generally running in the same direction as the memory bit lines. Such a memory architecture shall be explained below with regard to a memory size of about 64 megabits.

Figure 1a illustrates a plan view of the architecture of the hierarchical multi-data lines memory. Such a memory is ideally suited for memory sizes of 64 megabits and greater. As shown, two columns of a plurality of 512k memory arrays (for ease of illustration only one 512k array is specifically labeled) are shown with the memory arrays divided into sets of 8. Each set of eight 512k memory arrays comprise a 4 megabit block. Note that the terms 512k and 4 megabit as used herein throughout in many instances only approximate the number of memory cells. Each column of memory arrays is spaced apart from one another along a line interposed between the columns of arrays. Bond pads substantially line up along this line. A Y decoder is substantially centered in the middle of a column of memory arrays. Wide data path circuits which can operate on multiple data simultaneously are interspersed in a column between memory arrays after every eighth 512k memory array. Physically data travels on the path of local input/output lines which are shared by arrays on each side of the wide data circuit. The wide data path comprises the local input/output lines between memory arrays and the physical space therebetween. As shown in figure 1b (a block diagram

illustrating the flow of data to the wide data path circuit) and figures 1c through 1e (logic diagrams illustrating possible logic accomplished in the wide data path) data travelling on said wide data path which originates from either of two memory arrays or a location external the arrays is operated upon by logic connected to the local input/output lines in the wide data path. The logic operation may comprise ANDing, ORing, SHIFTING, complements of the foregoing and combinations thereof.

An explanation of the wide data path circuit follows with reference to figure 2. Figure 2 illustrates a read/write data bus scheme which includes a schematic drawing of a wide data path circuit. A wide data path circuit is a circuit for implementing a read/write data bus scheme for a high speed DRAM such as a 64 megabit DRAM. Main input/output (I/O) lines are interposed between cell arrays. Each cell array 20 (note that only one cell array is shown in detail) contains a plurality of sense amps S/A. Selection of a sense amplifier S/A is governed by a signal from a sense amp select line S/A SEL. Line S/A SEL selects a particular sense amp S/A by delivering a high signal to the gate of a n-channel transistor 122 (Note that for illustrative purposes, only two transistors 122 are shown for one sense amplifier even though others are present). A logic high signal on section select line SEC SEL turns on transistor 21 to allow the delivery of information to and from sense amps through local differential amplifier 124 comprised on n-channel transistors 28 and 30 arranged in the symmetrical fashion shown and connected to p-channel load transistors 34. READ operations are accomplished by sending a signal form column decoder YDEC along line YREAD. Local I/O line and (a line carrying its complement) line local I/O__ are precharged high by circuitry not shown. A high S/A signal allows passage of data form a memory cell (not specifically shown) through a selected sense amp and onto a sub I/O line pair, one line carrying a true signal and the other carrying its complement signal. A differential signal from the sub I/O pair output on the gates of each transistor 28 of local differential amplifier 124 in connection with n-channel transistor 19 turning on as a result of a logic high voltage level on line YREAD creates a differential signal on a pair of local I/O lines, line I/O carrying a true signal and line I/O__ carrying its complement. Differential signals on the local I/O lines are transferred to a pair of main I/O lines through transistors 32. In connection with a WRITE operation on a memory cell, column decoder YDEC places a high signal on the gates of transistors 30 after energizing line YWRITE. Data is transferred in through n-channel transistors 46 through a pair of main I/O lines onto local lines I/O and I/O__. A drain/source connection of transistors 230 to a local

line (I/O or I/O__) allows differential amplifier 124 to place data on a selected memory cell (not shown) through transistors 122 after selection by S/A SEL from a chosen sense amplifier.

With reference back to figure 1a, row decoders generally indicated at 40, lie alongside the columns of memory arrays and lie on an inner edge next to bond pads which provide bonds to the outside environment for functions such as address, control, and input/output. A row decoder is provided for each tow 4 megabit blocks of memory as shown. In connection with a signal from a Y decoder, information from/to a sense amplifier (not shown) goes from/to the wide data path circuits which connect to main input/output lines of the memory chip. A channel for placement of the main input/output lines is shown along an edge of the row decoders. The provision of a plurality of wide data path circuits to the extent of 8 per set of 512K memory arrays allows parallel processing and thus increased speed.

Figure 3a illustrates a plan view of another embodiment of the memory architecture. This embodiment is similar to the embodiment shown in figure 1a except that the wide data path circuits, now shown associated with four 4 megabit memory blocks, are located at each end of the columns of memory. A signal traveling from a Y decoder for sense amp selection allows selection of a sense amp and the import or export of data without back travel across the chip.

Figure 3b illustrates a plan view of the preferred embodiment of the memory architecture. In this embodiment note that two wide data path circuits are centered substantially between a Y decoder and an edge of the memory chip. Signals coming from the Y decoder travelling to the farthest most sense amp only require the sense amp to send or receive a signal half the distance as compared with the previous memory architecture embodiment since the wide data path circuit is at mid point between the Y decoder and the farthest most sense amp. Consequently, signals travelling between the Y decoder and the wide data path circuit provide service faster in the architecture shown in figure 3b than that of the embodiment shown in figure 3a. Further, the memory architecture of figure 3b is less complex than that shown in figure 1a since half as many wide data path circuits are needed in the architecture of figure 3b as compared with the architecture of figure 1a.

Figure 4a illustrates one 512,00 bit memory cell array and its associated circuitry being generally referenced at 2. One section of the array, being generally referenced at 4, is shown enlarged to facilitate discussion. The 512k array is associated with a pair of 1024 sense amplifiers grouped in sets of 4 sense amplifiers each or rather 256-

pair sets of 4 sense amplifiers. One set of a pair of sense amplifiers is included within enlarged section 4 with each sense amplifier (also called sense amp) being labeled S/A. The remaining pairs of 1020 sense amplifiers are generally labeled 1k S/A. Each vertical row (indicated along the directions of arrows v) of sense amplifiers can service two 512k arrays of memory. Bit lines, generally indicated at 6, are of te twisted type and connect to two sense amplifiers form each 512k array. Therefore, each sense amplifier is connected to 4 bit lines. However, note that since only one 512k array is shown, a pair of bit line connections for each sense amplifier is truncated along an outer edge for the other 512k arrays. For operation upon a memory cell, Y decoder 8, the column decoder, selects the column of memory cells and row decoder 10 selects the row of memory cells. The transmission media from row decoder 10 are word lines. As shown, one extended arrow labeled word line and representing the same indicates word lines selection by row decoder 10. An extended arrow labeled Y select represents a column and indicates column selection by Y decoder 8. Note that the vicinity of the intersection of a word line and a column can be equated to the location of a memory cell in the 512k array. Thus, extended arrow Y SELECT could have been shown at other locations along Y decoder 8 and likewise extended arrow WORD LINE could have been shown at other locations along row decoder 10. In conjunction with row decoder 10 of the 512k array shown and Y decoder 8, sense amplifier selection is accomplished such that access to the sense amplifier is determined by sense amp selection circuitry 12 which selects the proper sense amp pair corresponding to the selected column. Sense amp selection circuitry 12 comprises transistor pairs 14, one of the transistors form pair 14 acting as a pass transistor to carry a true signal and the other transistor from the pair serving as a pass transistor to carry the complement of the true signal. Note, however, that a single transistor 14 symbol represents a pair of transistors, shown here as n-type, although p-type and bipolar transistors of the n-p-n or p-n-p variety could be used. Transistor pairs 14 are connected to an associated sub input/output line of a sub input/output pair 16. The transistor for passing the true signal is therefore connected to a sub input/output line for transmission of the true signal and the transistor for passing the complement of the true signal is connected to the other sub input/output line from the pair which serves to transmit the complement of the true signal. Note that a pair of the sense amp circuitry 12 can service an entire 512k array. A pair of pass transistors 18 are associated with each of the 256 sets of 4 sense amplifier pairs. As with transistor pair 14,

transistor symbol 18 represents a pair of transistors, shown here as n-type transistors. Note, however, that p-type or bipolar transistors of the n-p-n or p-n-p variety could have been used. In connection with the selection of a particular sense amplifier S/A, determination thereof dictated in part by sense amplifier selection circuitry 12 and row decoder 10, a selected transistor pair 14 turns on. Pass transistor pair 18, associated with one of the 256 sets of sense amplifiers turns on so as to provide access to a local input/output pair 20 of lines. Like the sub input/output pair 16 and transistor pair 14 relationship, a pass transistor from pair 18 for passing a true signal connects to a local input/output line from pair 20, for transmission of a true signal. Similarly, a pass transistor from pair 18 for passing a complemented signal connects to the other local input/output line from local input/output pair 20. A local input/output pair 20 for each set of the 256 sets of sense amplifier pairs is coupled to wide data path circuitry 22. Selection determined by decoder 8 places data from selected pairs of the 256 local input/output pairs onto pairs of main input/output lines 24, the pairs comprising the true and complemented signals of the selected signals. For the particular case shown in figure 3a, 8 pairs of local input/output pair 20 are chosen from the 256 pairs of local input/output lines for placement of data onto or from the main input/output pair 24. However, fewer or more main input/output lines and consequently fewer or more local input/output pairs could have been chosen for selection and operation thereupon. 128 of the 512k memory arrays described above are used to create the 64 megabit memory. Y decoder 8 turns on selected transistors 18 for coupling data from a sub input/output line to a local input/output line. Selected transistors are located along arrow z. Sense amplifier select circuitry 12 determines which group of sense amplifiers and consequently, data from which 512k array gets placed on a sub input/output pair. For instance, if 127 512k arrays and their associated circuitry were located along arrow z, then a signal form Y decoder 8 would turn on transistors 18 for the same set of sense amplifiers in each 512k array. The same signal determines the column of a selected memory cell. Sense amplifier selection circuitry 12 exists for each 512k array in the z direction as does a row decoder 10 for each 512k array. Therefore, sense amplifier select circuitry determines which set of sense amplifiers are coupled to a sub input/output pair of lines. Note that the sense amplifier selection circuitry would couple the same sense amplifiers to sub input/output pairs in each of the 256 sets of sense amplifiers that exist along arrows v. However, Y decoder 8 determines which set out of the 256 sets gets selected so that through a transistor 18 a sub input/output pair is

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