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(APD/19760101->19980609 AND (DRAM AND "redundant memory")): 390 patents.
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PAT. NO.	Title
1 7,705,383	Integrated circuitry for semiconductor memory
2 7,447,069	Flash EEprom system
3 6,967,369	Semiconductor memory circuitry
4 6,598,171	Integrated circuit I/O using a high performance bus interface
5 6,570,790	Highly compact EPROM and flash EEPROM devices
6 6,460,110	Semiconductor memory
7 6,392,948	Semiconductor device with self refresh test mode
8 6,373,747	Flash EEprom system
9 6,317,370	Timing fuse option for row repair
10 6,307,273	High contrast, low noise alignment mark for laser trimming of redundant memory arrays
11 6,288,421	Semiconductor memory circuitry including die sites for 16M to 17M memory cells in an 8" wafer
12 6,272,577	Data processing system with master and slave devices and asymmetric signal swing bus
13 6,266,753	Memory manager for multi-media apparatus and method therefor
14 6,252,281	Semiconductor device having an SOI substrate
15 6,243,829	Memory controller supporting redundant synchronous memories
16 6,223,248	Circuits systems and methods for re-mapping memory row redundancy during two cycle cache access

17 6,208,567 Semiconductor device capable of cutting off a leakage current in a defective array section

18 6,208,545 Three dimensional structure memory

19 6,205,514 Synchronous SRAM having global write enable

20 6,194,738 Method and apparatus for storage of test results within an integrated circuit

21 6,182,257 BIST memory test system

22 6,178,549 Memory writer with deflective memory-cell handling capability

23 6,154,851 Memory repair

24 6,149,316 Flash EEprom system

25 6,141,768 Self-corrective memory system and method

26 6,134,681 Semiconductor memory device with spare memory cell

27 6,133,640 Three-dimensional structure memory

28 6,130,837 Storage device employing a flash memory

29 6,130,468 Fuse, memory incorporating same and method

30 6,130,442 Memory chip containing a non-volatile memory register for permanently storing information about the quality of the device and test method therefor

31 6,122,213 Device and method for repairing a memory array by storing each bit in multiple memory cells in the array

32 6,115,828 Method of replacing failed memory cells in semiconductor memory device

33 6,115,299 Device and method for repairing a memory array by storing each bit in multiple memory cells in the array

34 6,105,152 Devices and methods for testing cell margin of memory devices

35 6,104,645 High speed global row redundancy system

36 6,097,643 Semiconductor storage apparatus and method of manufacturing of the same

37 6,093,933 Method and apparatus for fabricating electronic device

38 6,081,463 Semiconductor memory remapping

39 6,078,534 Semiconductor memory having redundancy circuit

40 6,073,258 Method and device for performing two dimensional redundancy calculations on embedded memories avoiding fail data collection

41 6,073,251 Fault-tolerant computer system with online recovery and reintegration of redundant components

42 6,069,064 Method for forming a junctionless antifuse

43 6,066,886 Semiconductor wafer in which redundant memory portion is shared by two neighboring semiconductor memory portions and is connected to the semiconductor memory portions

44 6,066,539 Honeycomb capacitor and method of fabrication

45 6,055,611 Method and apparatus for enabling redundant memory

46 6,055,204 Circuits, systems, and methods for re-mapping memory column redundancy

47 6,055,196 Semiconductor device with increased replacement efficiency by redundant memory cell arrays

48 6,049,505 Method and apparatus for generating memory addresses for testing memory devices

49 6,046,945 DRAM repair apparatus and method

50 6,044,029 **T** Device and method for repairing a memory array by storing each bit in multiple memory cells in the array

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