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Paper 11
Entered: February 7, 2017

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

APPLE INC.,
Petitioner,

v.

LIMESTONE MEMORY SYSTEMS LLC,
Patent Owner.

Case IPR2016-01561
Patent 6,233,181 B1

Before BART A. GERSTENBLITH, BARBARA A. PARVIS, and ROBERT J. WEINSCHENK, *Administrative Patent Judges*.

WEINSCHENK, *Administrative Patent Judge*.

DECISION
Institution of *Inter Partes* Review
37 C.F.R. § 42.108

I. INTRODUCTION

Apple Inc. ("Petitioner") filed a Petition (Paper 1, "Pet.") requesting an *inter partes* review of claims 3 and 5 of U.S. Patent No. 6,233,181 B1 (Ex. 1003, "the '181 patent"). Limestone Memory Systems LLC ("Patent Owner") filed a Preliminary Response (Paper 10, "Prelim. Resp.") to the Petition. An *inter partes* review may not be instituted "unless . . . there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition." 35 U.S.C. § 314(a).

For the reasons set forth below, Petitioner demonstrates a reasonable likelihood of prevailing in showing the unpatentability of claims 3 and 5 of the '181 patent. Accordingly, we institute an *inter partes* review as to claims 3 and 5 of the '181 patent on the grounds specified below.

A. *Related Proceedings*

The parties indicate that the '181 patent is the subject of several cases in the United States District Court for the Central District of California. Pet. 1–2; Paper 4, 4–6. The parties also indicate that the following petitions for *inter partes* review may be related to this case:

Case No.	**Involved U.S. Patent No.**
IPR2016-00093	U.S. Patent No. 5,805,504
IPR2016-00094	U.S. Patent No. 5,894,441
IPR2016-00095	U.S. Patent No. 5,943,260
IPR2016-00096	U.S. Patent No. 6,233,181
IPR2016-00097	U.S. Patent No. 6,697,296
IPR2016-01567	U.S. Patent No. 5,894,441

Pet. 2; Paper 4, 2–3.

B. *The '181 Patent*

The '181 patent relates to repairing defective memory cells in a semiconductor memory device. Ex. 1003, col. 1, ll. 9–13. The '181 patent

explains that, when a memory cell becomes defective, it can be replaced with a spare memory cell. *Id.* at col. 1, ll. 15–18. According to the '181 patent, prior semiconductor memory devices contained an array of spare memory cells for each memory block in the device, and, as a result, the spare memory cells were not used efficiently. *Id.* at col. 3, l. 58–col. 4, l. 8. To address this problem, the '181 patent describes a semiconductor memory device with an array of spare memory cells that can be shared among a plurality of memory blocks. *Id.* at col. 16, ll. 31–39.

C. *Illustrative Claim*

Claim 3 depends from claims 1 and 2. Claims 1, 2, and 3 are reproduced below.

> 1. A semiconductor memory device, comprising:
>
> a plurality of first memory blocks each having a plurality of first normal memory cells arranged in a matrix of rows and columns, each of said plurality of first memory blocks including word lines provided corresponding to said rows, respectively, and the first memory blocks aligned in the column direction; and
>
> a plurality of first spare memory cells arranged in a matrix of rows and columns in a particular one of said plurality of first memory blocks, each row of said plurality of first spare memory cells being capable of replacing a defective row including a defective first normal memory cell in said plurality of first memory blocks.
>
> 2. The semiconductor memory device as recited in claim 1, further comprising:
>
> a plurality of second memory blocks arranged alternatively with said plurality of first memory blocks along the column direction, the second memory blocks each having a plurality of second normal memory cells arranged in a matrix of rows and columns; and

> a plurality of second spare memory cells arranged in a matrix of rows and columns in a particular one of said plurality of second memory blocks, each row of said plurality of second spare memory cells being capable of replacing a defective row including a defective second normal memory cell in said plurality of second memory blocks.
>
> 3. The semiconductor memory device as recited in claim 2, further comprising a plurality of sense amplifier bands provided between each of said plurality of first memory blocks and each of said second memory blocks, and shared by adjacent memory blocks in the column direction for sensing and amplifying data in each column of the adjacent memory block including a selected memory cell when activated.

Ex. 1003, col. 45, l. 55–col. 46, l. 31.

D. *Evidence of Record*

Petitioner relies on the following references and declaration (Pet. 4):

Reference or Declaration	**Exhibit No.**
Declaration of Dr. Pinaki Mazumder ("Mazumder Declaration")	Ex. 1001
Sukegawa et al., U.S. Patent No. 5,487,040 (issued Jan. 23, 1996) ("Sukegawa")	Ex. 1005
Fujishima et al., U.S. Patent No. 5,267,214 (issued Nov. 30, 1993) ("Fujishima")	Ex. 1006
Walck, U.S. Patent No. 4,967,397 (issued Oct. 30, 1990) ("Walck")	Ex. 1007

E. *Asserted Grounds of Unpatentability*

Petitioner asserts that the challenged claims are unpatentable on the following grounds (Pet. 5):

Claim	**Basis**	**References**
3	35 U.S.C. § 103(a)	Sukegawa and Fujishima
5	35 U.S.C. § 103(a)	Sukegawa, Fujishima, and Walck

II. ANALYSIS

A. *Claim Construction*

The claims of an unexpired patent are interpreted using the broadest reasonable interpretation in light of the specification of the patent in which they appear. 37 C.F.R. § 42.100(b); *Cuozzo Speed Techs., LLC v. Lee*, 136 S. Ct. 2131, 2144–46 (2016). The parties agree that no claim construction is necessary at this stage of the proceeding. Pet. 6; Prelim. Resp. 18–19. Therefore, on this record and for purposes of this decision, we determine that no claim terms require express construction. *See Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999) ("[O]nly those terms need be construed that are in controversy, and only to the extent necessary to resolve the controversy.").

B. *Asserted Grounds of Unpatentability*

1. *Obviousness of Claim 3 over Sukegawa and Fujishima*

Petitioner argues that claim 3 would have been obvious over Sukegawa and Fujishima. Pet. 5. We have reviewed the parties' assertions and supporting evidence. For the reasons discussed below, Petitioner demonstrates a reasonable likelihood of prevailing in showing that claim 3 would have been obvious over Sukegawa and Fujishima.

Claim 3 depends from claims 1 and 2. Ex. 1003, col. 45, l. 55–col. 46, l. 31. Petitioner identifies evidence indicating that Sukegawa teaches the limitations in claims 1 and 2. Pet. 39–52. Patent Owner does not raise any specific disputes with respect to the limitations in claims 1 and

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