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(54) **Thermal CVD/PECVD reactor and use for thermal chemical vapor deposition of silicon dioxide and in-situ multi-step planarized process.**

(57) A high pressure, high throughput, single wafer, semiconductor processing reactor (10) is disclosed which is capable of thermal CVD, plasma-enhanced CVD, plasma-assisted etchback, plasma self-cleaning, and deposition topography modification by sputtering, either separately or as part of in-situ multiple step processing. The reactor includes cooperating arrays of interdigitated susceptor (16) and wafer fin-

gers (20) which collectively remove the wafer (15) from a robot transfer blade (24) and position the wafer with variable, controlled, close parallel spacing between the wafer and the chamber gas inlet manifold (26) then return the wafer to the blade. A combined RF/gas feed-through device (36) protects against process gas leaks and applies RF energy to the gas inlet manifold without internal breakdown or deposition of the gas. The gas inlet manifold (26) is adapted for providing uniform gas flow over the wafer. Temperature-controlled internal and external manifold surfaces suppress condensation, premature reactions and decomposition and deposition on the external surfaces. The reactor also incorporates a uniform radial pumping gas system which enables uniform reactant gas flow across the wafer and directs purge gas flow downwardly and upwardly toward the periphery of the wafer for sweeping exhaust fases radially away from the wafer to prevent deposition outside the wafer and keep the chamber clean. The reactor provides uniform processing over a wide range of pressure including very high pressures. A low temperature CVD process for forming a highly conformal layer of silicon dioxide is also disclosed. The process uses very high chamber pressure and low temperature, and TEOS and ozone reactants. The low temperature CVD silicon dioxide deposition step is particularly useful for planarizing underlying stepped dielectric layers, either alone on in conjunction with a subsequent isotropic etch. A preferred in-situ multiple-step process for forming a planarized silicon dioxide layer uses (1) high rate silicon dioxide deposition at a low temperature and high pressure followed by (2) the deposition of the conformal silicon dioxide layer also at high pressure and low temperature, followed by (3) a high rate isotropic etch, preferably at low temperature and high pressure in the same reactor used for the two oxide deposition steps. Various combinations of the steps are disclosed for different applications, as is a preferred reactor self-cleaning step.

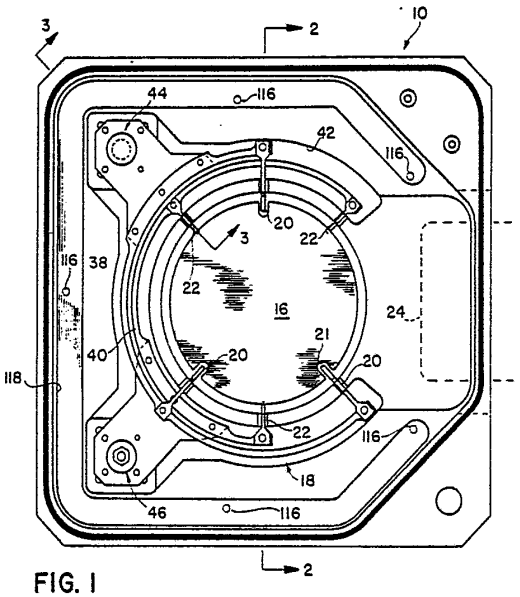
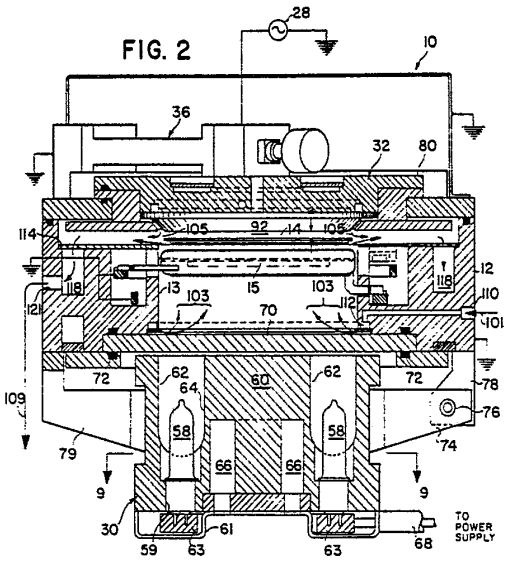


FIG. 1

FIG. 2



THERMAL CVD/PECVD REACTOR AND USE FOR THERMAL CHEMICAL VAPOR DEPOSITION OF SILICON DIOXIDE AND IN-SITU MULTI-STEP PLANARIZED PROCESS

Background of the Invention

The present invention relates to a reactor and methods for performing single and in-situ multiple integrated circuit processing steps, including thermal CVD, plasma-enhanced chemical vapor deposition (PECVD), reactor self-cleaning, film etchback, and modification of profile or other film property by sputtering. The present invention also relates to a process for forming conformal, planar dielectric layers on integrated circuit wafers and to an in-situ multi-step process for forming conformal, planar dielectric layers that are suitable for use as interlevel dielectrics for multi-layer metallization interconnects.

I. Reactor

The early gas chemistry deposition reactors that were applied to semiconductor integrated circuit fabrication used relatively high temperature, thermally-activated chemistry to deposit from a gas onto a heated substrate. Such chemical vapor deposition of a solid onto a surface involves a heterogeneous surface reaction of gaseous species that adsorb onto the surface. The rate of film growth and the film quality depend on the wafer surface temperature and on the gaseous species available.

More recently, low temperature plasma-enhanced deposition and etching techniques have been developed for forming diverse materials, including metals such as aluminum and tungsten, dielectric films such as silicon nitride and silicon dioxide, and semiconductor films such as silicon.

The plasma used in the available plasma-enhanced chemical vapor deposition processes is a low pressure reactant gas discharge which is developed in an RF field. The plasma is, by definition, an electrically neutral ionized gas in which there are equal number densities of electrons and ions. At the relatively low pressures used in PECVD, the discharge is in the "glow" region and the electron energies can be quite high relative to heavy particle energies. The very high electron temperatures increase the density of disassociated species within the plasma which are available for deposition on nearby surfaces (such as substrates). The enhanced supply of reactive free radicals in the PECVD processes makes possible the deposition of dense, good quality films at lower temperatures and at faster deposition rates (300-400 Angstroms per minute) than are typically possible using purely thermally-activated CVD processes (100-200 Angstroms per minute). However, the deposition rates available using conventional plasma-enhanced processes are still relatively low.

Presently, batch-type reactors are used in most commercial PECVD applications. The batch reactors process a relatively large number of wafers at once and, thus, provide relatively high throughput despite the low deposition rates. However, single-wafer reactors have certain advantages, such as the lack of within-batch uniformity problems, which make such reactors attractive, particularly for large, expensive wafers such as 5-8 inch diameter wafers. In addition, and quite obviously, increasing the deposition rate and throughput of such single wafer reactors and further increase their range of useful applications.

II. Thermal CVD of SiO_2; Planarization Process

Recently integrated circuit (IC) technology has advanced from large scale integration (LSI) to very large scale integration (VLSI) and is projected to grow the ultra-large integration (ULSI) over the next several years. This advancement in monolithic circuit integration has been made possible by improvements in the manufacturing equipment as well as in the materials and methods used in processing semiconductor wafers into IC chips. However, the incorporation into IC chips of, first, increasingly complex devices and circuits and, second, greater device densities and smaller minimum feature sizes and smaller separations, imposes increasingly stringent requirements on the basic integrated circuit fabrication steps of masking, film formation, doping and etching.

As an example of the increasing complexity, it is projected that, shortly, typical MOS (metal oxide semiconductor) memory circuits will contain two levels of metal interconnect layers, while MOS logic circuits may well use two to three metal interconnect layers and bipolar digital circuits may require three to four such layers. The increasing complexity, thickness/depth and small size of such multiple interconnect levels make it increasingly difficult to fabricate the required conformal, planar interlevel dielectric layers materials such as silicon dioxide that support and electrically isolate such metal interconnect layers.

The difficulty in forming planarized conformal coatings on small stepped surface topographies is illustrated in FIG. 16. There, a first film such as a

conductor layer 171 has been formed over the existing stepped topography of a partially completed integrated circuit (not shown) and is undergoing the deposition of an interlayer dielectric layer 172 such as silicon dioxide. This is done preparatory to the formation of a second level conductor layer (not shown). Typically, where the mean-free path of the depositing active species is long compared to the step dimensions and where there is no rapid surface migration, the deposition rates at the bottom 173, the sides 174 and the top 175 of the stepped topography are proportional to the associated arrival angles. The bottom and side arrival angles are a function of and are limited by the depth and small width of the trench. Thus, for very narrow and/or deep geometries the thickness of the bottom layer 173 tends to be deposited to a lesser thickness than is the side layer 174 which, in turn, is less than the thickness of top layer 175.

Increasing the pressure used in the deposition process typically will increase the collision rate of the active species and decrease the mean-free path. This would increase the arrival angles and, thus, increase the deposition rate at the sidewalls 714 and bottom 173 of the trench or step. However, and referring to FIG. 17A, this also increases the arrival angle and associated deposition rate at stepped corners 176.

For steps separated by a wide trench, the resulting inwardly sloping film configuration forms cusps 177-177 at the sidewall-bottom interface. It is difficult to form conformal metal and/or dielectric layers over such topographies. As a consequence, it is necessary to separately planarize the topography.

In addition, and referring to FIG. 17B, where the steps are separated by a narrow trench, for example, in dense 256 kilobit VLSI structures, the increased deposition rate at the corner 176 encloses a void 178. Such voids are exposed by subsequent planarization procedures and may allow the second level conductor to penetrate and run along the void and short the conductors and devices along the void.

Summary of the Invention

Objects

In view of the above discussion, it is one object to provide a semiconductor processing reactor which provides uniform deposition over a wide range of pressures, including very high pressures.

It is another related object to provide a versatile single wafer semiconductor processing reactor which can be used for a multiplicity of processes including thermal chemical vapor deposition, plasma-enhanced chemical vapor deposition, plasma-assisted etchback, plasma self-cleaning and sputter topography modification, either alone or in-situ in a multiple process sequence.

It is a related object to provide such a reactor which accomplishes the above objectives and also is adapted for using unstable gases such as TEOS and ozone.

It is another object of the present invention to provide a process for forming highly conformal silicon dioxide layers, even over small dimension stepped topographies in VLSI and ULSI devices, using ozone and TEOS gas chemistry and thermal CVD.

It is also an object of the present invention to provide a planarization process which provides excellent conformal coverage and eliminates cusps and voids.

It is still another object of the present invention to provide a planarization process which can be performed in-situ using a multiple number of steps, in the same plasma reactor chamber, by simply changing the associated reactant gas chemistry and operation conditions.

It is yet another object of the present invention to provide an in-situ multiple step process including plasma deposition and isotropic etching of a wafer for the purpose of optimizing coating conformality and planarization, along with process throughput and wafer characteristics such as low particulates.

Another object is to provide the above-described versatile process characteristics along with the ability to vary the process sequence and the number of steps, including but not limited to the addition of reactor self-cleaning.

Summary

In one specific aspect, our invention relates to a semiconductor processing reactor defining a chamber for mounting a wafer therein and an inlet gas manifold for supplying reactant gases to the wafer. The chamber also incorporates a uniform radial pumping system which includes vacuum exhaust pump means; a gas distributor plate mounted peripherally about the wafer mounting position within the chamber and including a circular array of exhaust holes therein; and a circular channel beneath and communicating with the hole array and having at least a single point connection to the vacuum exhaust pump for flowing gases radially from the inlet manifold across the wafer and through the exhaust port. The channel is of sufficiently large volume and conductance relative to the holes to enable controlled uniform radial gas flow across the wafer to the exhaust holes, thereby promoting uniform flow and processing (etching

and deposition) over a wide range of pressures, including very high pressures up to about one atmosphere.

In another aspect, the present invention is directed to a semiconductor processing reactor which comprises a housing forming a chamber for mounting a wafer horizontally, a vacuum exhaust pumping system communicating with the chamber, and an inlet gas manifold oriented horizontally over the wafer mounting position. The manifold has a central array of process gas apertures configured for dispensing reactant gas uniformly over the wafer and a second peripheral array of purging gas apertures configured for directing purging gas downward to the periphery of the wafer. The hole arrays are also arranged to eliminate radial alignment of holes.

In another aspect, the reactor incorporates a system for circulating fluid of controlled temperature within the manifold for maintaining the internal surfaces within a selected temperature range to prevent condensation and reactions within the manifold and for maintaining the external manifold surfaces above a selected temperature range for eliminating unwanted deposition thereon.

In still another aspect, the reactor of the present invention comprises a thin susceptor for supporting a wafer, susceptor support means for mounting the susceptor in a horizontal position precisely parallel to the gas inlet manifold and means for selectively moving the wafer support means vertically to position the susceptor and support parallel to the gas manifold at selected variable-distance positions closely adjacent the gas manifold. In particular, the variable parallel close spacing can be 0.5 centimeter and smaller.

In still another aspect, the semiconductor processing reactor of the present invention comprises a housing defining a chamber therein adapted for the gas chemistry processing of a wafer positioned within the chamber. A transparent window forms the bottom of the chamber. A thin high emissivity susceptor is used for supporting a wafer within the chamber. A radiant heating module comprising a circular array of lamps mounted in a reflector module is mounted outside the housing for directing a substantially collimated beam of near-infrared radiant energy through the window onto the susceptor with an incident power density substantially higher at the edge of the susceptor than at the center thereof, to heat the wafer uniformly.

Preferably, a second, purge gas manifold is positioned beneath the wafer processing area for providing purging gas flow across the window and upward and across the bottom of the wafer. The combination of the high pressure, the purge flow from the inlet gas manifold and that from the purge gas manifold substantially eliminates deposition on chamber surfaces.

In still another aspect, the reactor of the present invention comprises a deposition gas feedthrough device connected to the gas inlet manifold which comprises tube means adapted for providing co-axial flow of deposition gas on the inside of the tube and purge gas on the outside thereof into the gas inlet manifold. The tube is adapted for connection to ground at the inlet end and to an RF power supply at the outlet or manifold end to provide RF power to the manifold, and has a controlled electrical impedance along its length from the inlet to the outlet end for establishing a constant voltage gradient to prevent breakdown of the gas even at high RF frequencies and voltages.

These and other features discussed below permit reactor operation over a wide pressure regime, that is, over a wide of pressures including high pressures up to approximately one atmosphere. The features also provide uniform susceptor and wafer temperatures, including both absolute temperature uniformity and spatial uniformity across the susceptor/wafer; uniform gas flow distribution across the wafer; and effective purging. The variable parallel close spacing between the electrodes adapts the reactor to various processes. These features and the temperature control of the internal and external gas manifold temperatures enable the advantageous use of very sensitive unstable gases such as ozone and TEOS in processes such as the following.

That is, the present invention also relates to a method for depositing a conformal layer of silicon dioxide onto a substrate by exposing the substrate to a reactive species formed from ozone, oxygen, tetraethylorthosilicate, and a carrier gas within a vacuum chamber, using a total gas pressure within the chamber 10 torr to 200 torr and a substrate temperature within the range of about 200°C to 500°C. Preferably, a substrate temperature of about 375°C ±20°C is used to obtain maximum deposition rates and the chamber pressure is about 40 torr to 120 torr.

In still another aspect, the present invention is embodied in a method for depositing silicon dioxide onto a film or substrate by exposing the substrate to the plasma formed from tetraethylorthosilicate, oxygen and a carrier gas in a chamber using a total gas pressure within the range of about 1 to 50 torr, and a substrate temperature in the range of about 200°C to 500°C. Preferably, the chamber pressure is 8-12 torr and the substrate temperature is about 375°C ±20°C.

In still another aspect, the invention is directed to a method for isotropically etching a silicon dioxide surface comprising the step of exposing a silicon dioxide surface to a plasma formed from fluorinate gas such as NF_3, CF_4 and C_2F_6 in a

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