Sub-quarter Micron Copper Interconnects through Dry Etching Process and its Reliability

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Introduction

Copper is the major candidate material of post-Al alloys in deep sub-micron region, because of low resistivity and long electromigration lifetime (1). Recently, ion milling (1) and chemical mechanical polishing (CMP) (2,3) have been applied to fine Cu interconnects, and these techniques can avoid the difficulty of etching Cu caused by hardly subliming etching-products. However, these are not necessarily the well-established technique for ULSI process.

Our approach is modification of the high temperature dry etching, which includes the self-aligned passivation technique (4). In this work, we have formed TiN/Cu/TiN multilayered interconnects of sub-quarter micron wide using the modified dry etching technique, and evaluated the resistance to electromigration damage (EMD).

Experimental

A multilayered film composed of TiN(0.1μm)/ Cu(0.4μm)/ TiN(0.1μm) was prepared on a thermally oxidized Si wafer by dc magnetron sputtering. A SiO_2 mask for etching Cu layer was prepared by etching through a resist mask obtained by i-line phase-shifting lithography.

Etching was performed on a magnetron reactive ion etching (RIE) system operating at a gas pressure of 30mTorr and a rf power of 500W, and a etching gas of a $SiCl_4$/ Cl_2/ N_2/ NH_3 mixture was used to form a passivation film on a sidewall of interconnect simultaneously. The temperature of a wafer during etching was controlled at 300°C.

After etching, a bilayer composed of SiO_2 (0.2μm) and SiN (0.8μm) was deposited as a passivation layer by plasma-enhanced CVD at 115°C and 350°C, respectively.

The resistance to EMD of the Cu interconnects was investigated using 22mm long and 0.2 - 1μm wide lines.

Results and Discussion

1. Fabrication of 0.2μm Cu interconnect with self-aligned passivation technique

In the ternary gas mixture of $SiCl_4$/ Cl_2/ N_2, a SiON passivation film is formed on the sidewall during etching (4). The sidewall passivation film acts as a barrier to prevent Cu from oxidation in the following SiO_2 deposition process. The side-etching and the thickness of the sidewall passivation film are independently controlled by the [N]/[Cl] ratio and the [Si]/[Cl] ratio, respectively. Here, [N], [Si] and [Cl] represent the amount of each constituent element in the introduced gas mixture. Patterning Cu line without side-etching is achieved when the [N]/[Cl] ratio is more than 2. As shown in Fig.1 (the case of NH_3:0%), thickness of the sidewall film is controlled by the [Si]/[Cl] ratio, and it is saturated when the [Si]/[Cl] ratio is over 0.16. The resulting sidewall film is composed of silicon oxynitride containing small amounts of impurities, such as chlorine of about 2 atomic% (Fig.3(a)). This amount of Cl did not cause corrosion of Cu in our fabrication process. However, the sidewall film without Cl is more suitable for the Cu interconnect which is easy to be corroded by Cl.

Hence, in expectancy of dissociating the Si-Cl bond, NH_3 is introduced to the ternary gas mixture of $SiCl_4$/ Cl_2/ N_2. NH_3 releases Cl atoms on $SiCl_4$ in consequence of stimulating its dissociation. Gas flow of NH_3 and N_2 was controlled so as to be the [N]/[Cl] ratio of 2.4, and NH_3 was added up to 15% of [N] in the etching gas. As shown in Fig.1, thickness of the sidewall film increases with NH_3 flow, and is saturated when addition of NH_3 is over 10%. Fig.2 summarizes the etching rates with the NH_3 flow ratio. Etching rate of SiO_2 decreases monotonously with increasing the NH_3 flow ratio. On the other hand, that of Cu is almost constant in the low ratio region and it abruptly decreases when the flow ratio is over 10 %. The NH_3 flow ratio of 7% gives the highest etching selectivity of 7. The sidewall film of the above case is composed of SiON without detectable impurities such as Cl, as shown in Fig.3(b). These Auger analyses suggest that NH_3 has Cl-releasing activity. The N content is almost equal to that of NH_3 free etching. The resulting as-etched Cu interconnect did not corrode in atmosphere for 2 months. A cross-sectional view of the interconnect after etching is shown in Fig.4. This etching technique enables the micro-fabrication of 0.2μm (Fig.4(a)), and it can be applied to 0.3μm of dense patterns (Fig.4(b)).

2. Resistance to EMD of the TiN/Cu/TiN interconnect

After the etching process, the interconnect was covered with a SiN/ SiO_2 bilayer as a passivation layer and sintered in H_2/ N_2 ambient at 450°C for 2 hours. After sintering, the resistivity estimated from line resistance is about 2 μΩ·cm.

Electromigration test was carried out under the stress current density of $8x10^6 A/cm^2$ in atmosphere. The temperature of the interconnects was controlled at 200°C taking account of Joule heating. Fig.5 shows the resistance change of the 0.6-μm-wide line as typical characteristic of EMD. Slightly and monotonically increasing resistance before catastrophic failure is caused by void growth in Cu. Fig.6 shows the cumulative failure rate under $8x10^6 A/cm^2$ at 200°C. The lifetimes of the dry etched Cu lines are equal to or longer than that of the Cu lines formed by other fabrication methods (1-3). The value of median time to failure (MTF) of the 0.2μm line, 110h, is about an order of magnitude longer than that of the 0.6μm line. This behavior is the same as the Al alloy case which is associated with a bamboo-type grain structure (5). MTF of the 0.2μm line is about three orders of magnitude longer than that of 1.5-μm-wide Al-1%Si/TiW line (3).

Conclusions

We have developed the modified high temperature dry etching technique, which enables anisotropic patterning with a high etching selectivity and self-aligned passivation of a sidewall of interconnect simultaneously. Sub-quarter micron Cu interconnects with long electromigration lifetimes have been prepared successfully using this technique. MTF of the 0.2μm line is 110h and it is equal to or longer than that of the

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Cu lines formed by other fabrication methods.

References

(1) D.S.Gardner,J.Onuki,K.Kudo and Y.Misawa: Proc. VLSI Multilevel Interconnection Conf. (1991) p.99.

(2) N.Misawa,S.Kishii,T.Ohba,Y.Arimoto,Y.Furumura and H.Tsutikawa: VLSI Multilevel Interconnection Conf. (1993) p.353

(3) H.-K.Kang,I.Asano,C.Ryu,S.S.Wong and J.A.T.Norman: Proc. VLSI Multilevel Interconnection Conf. (1993) p.223.

(4) Y.Igarashi,T.Yamanobe,T.Yamaji,S.Nishikawa and T.Ito: SSDM Ext.Abst. (1993) p.549

(5) S.Vaidya,T.T.Sheng and A.K.Sinha: Appl.Phys.Lett. **36** (1980) p.464.

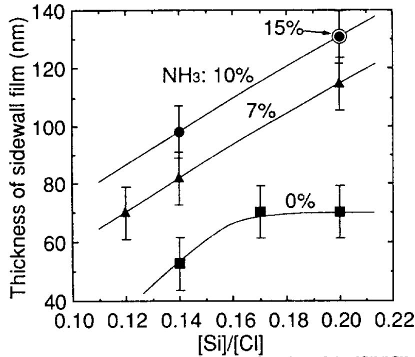

Fig.1. Thickness of the sidewall film as a function of the [Si]/[Cl] ratio on the NH_3 flow ratio of 0, 7, 10 and 15%.

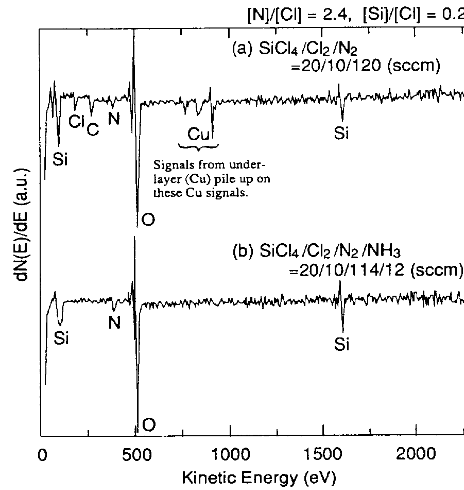

Fig.3. AES spectra of the sidewall films: (a) without and (b) with NH_3 flow.

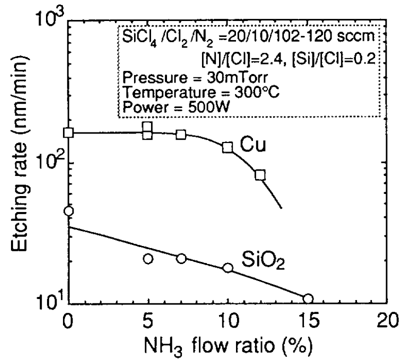

Fig.2. Etching rate of Cu and SiO_2 as a function of the NH_3 flow ratio.

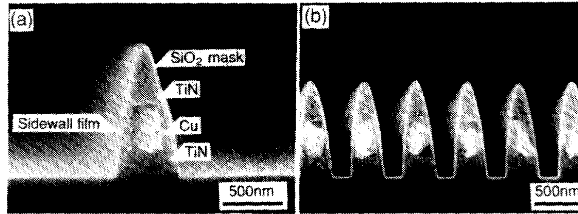

Fig.4. Cross-sectional view of the interconnects after etching(NH_3 = 7%; [Si]/[Cl] = 0.12): (a) 0.2μm wide line; (b) 0.3μm line and space.

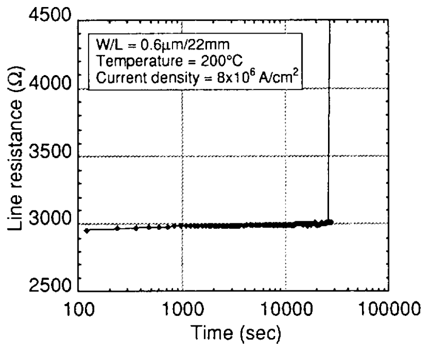

Fig.5. Resistance change of the 0.6μm interconnect under EM test condition.

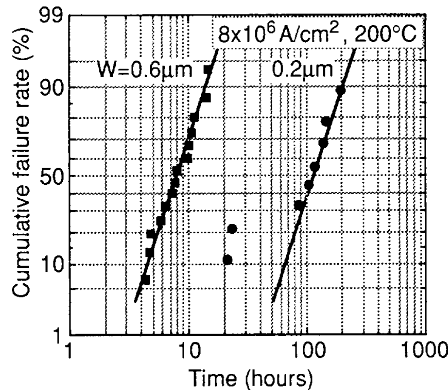

Fig.6. Cumulative failure of interconnects.

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