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[54] **PROCESS FOR CLEANING AN ELECTROSTATIC CHUCK OF A PLASMA ETCHING APPARATUS**

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[52] **U.S. Cl.** **216/37**; 216/71; 134/1.1; 134/1.2; 134/1.3; 134/21

[58] **Field of Search** 216/37, 71; 134/1.1, 134/1.2, 1.3, 21

[56] **References Cited**

U.S. PATENT DOCUMENTS

5,310,453	5/1994	Fukasawa et al.	156/643
5,382,311	1/1995	Ishikawa et al.	156/345
5,507,874	4/1996	Su et al.	134/1
5,585,012	12/1996	Wu et al.	216/71
5,671,119	9/1997	Huang et al.	361/234

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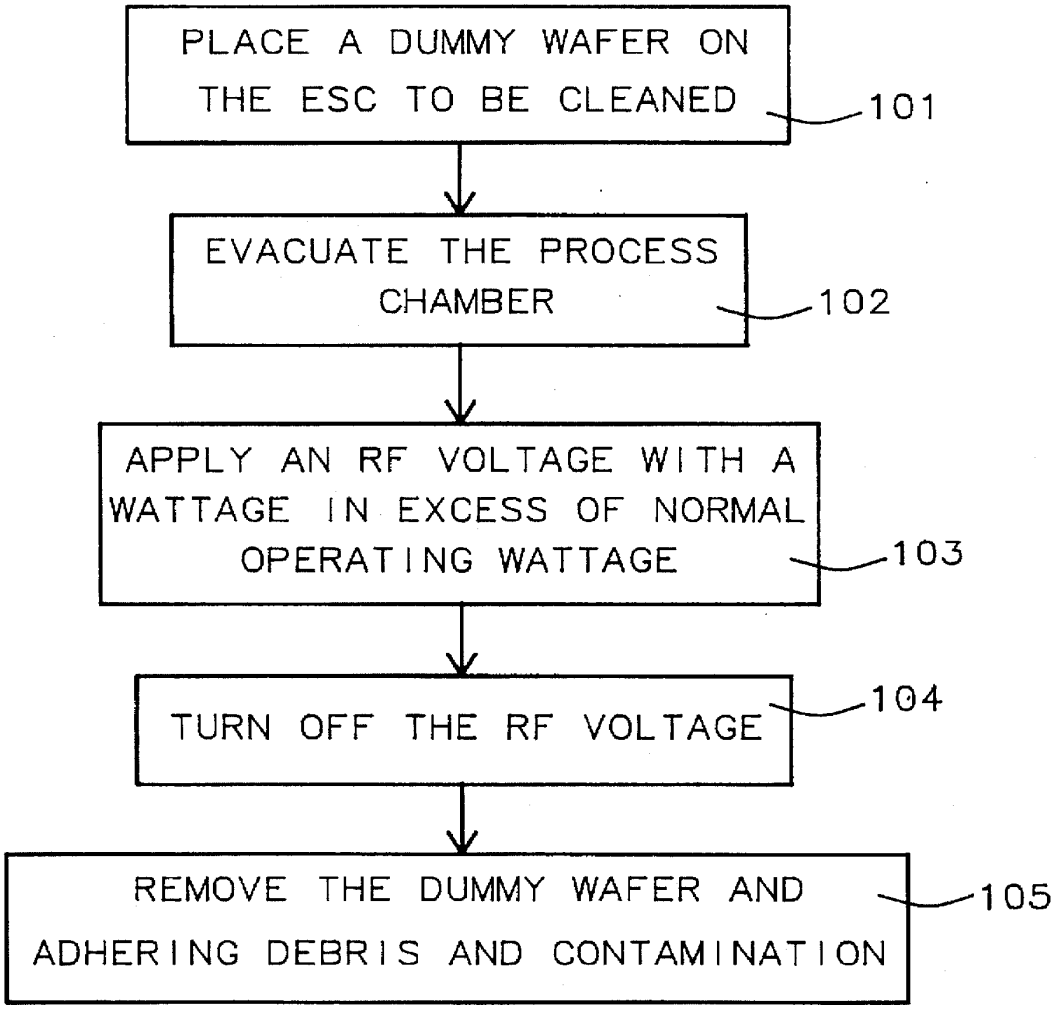
[57] **ABSTRACT**

A method of cleaning an electrostatic chuck of a plasma etching apparatus wherein a dummy wafer is placed on the chuck, the chamber evacuated, and an RF voltage applied that is greater than the normal RF voltage used to etch.

7 Claims, 2 Drawing Sheets



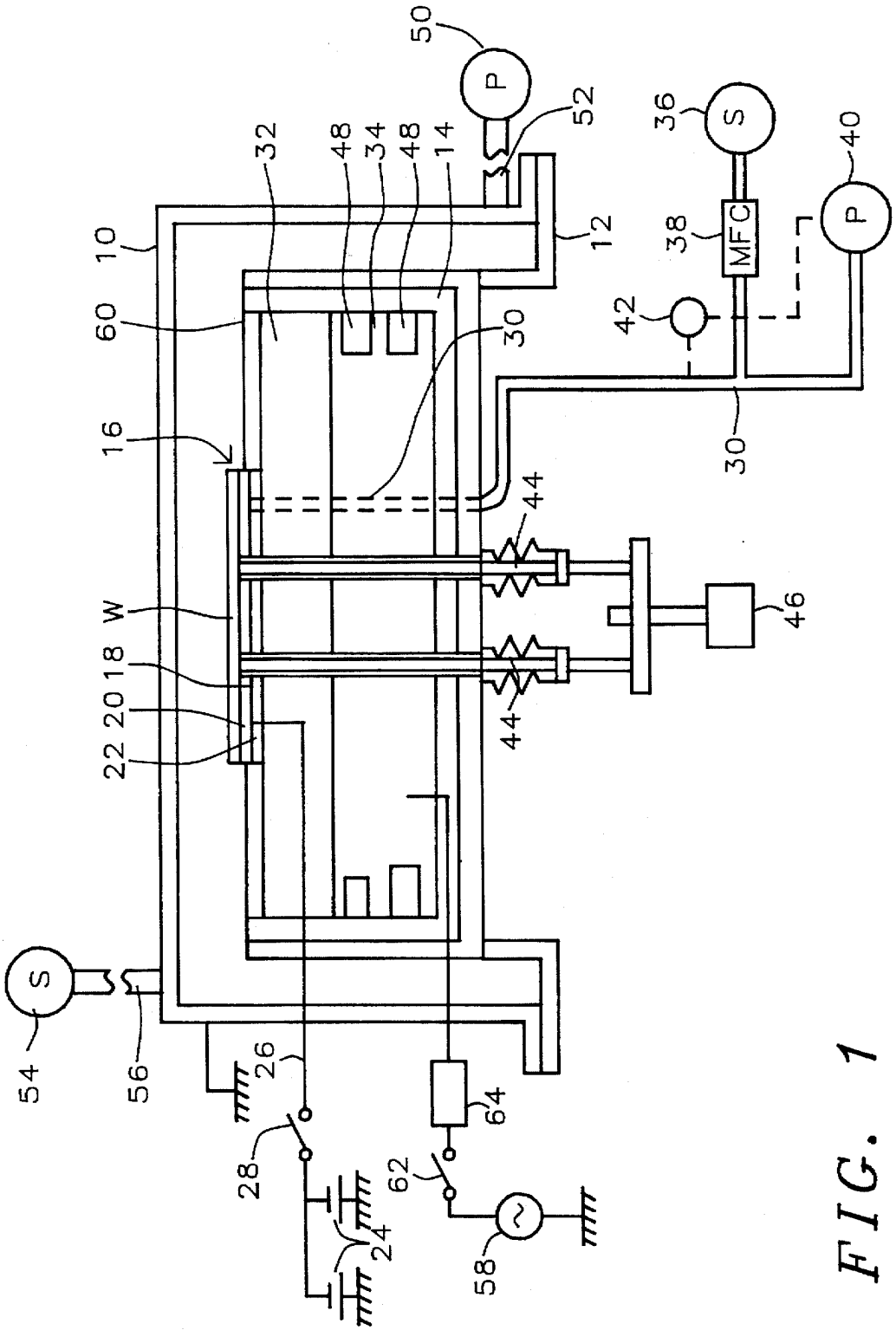


FIG. 1

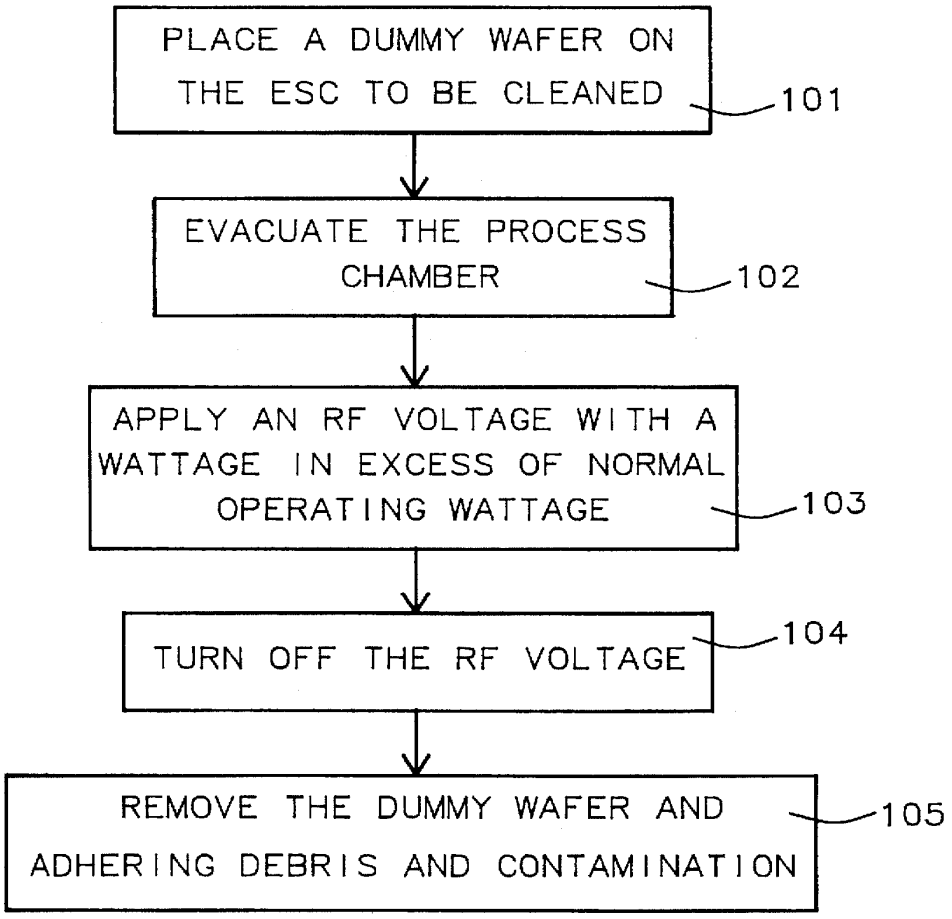


FIG. 2

PROCESS FOR CLEANING AN ELECTROSTATIC CHUCK OF A PLASMA ETCHING APPARATUS

Application Ser. No. 08/620,184, filed Mar. 22, 1996, now U.S. Pat. No. 5,671,119, is a commonly assigned, related, application.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to semiconductor processing, more specifically to cleaning plasma etching apparatus used in semiconductor processing.

2. Description of the Related Art

In semiconductor device manufacturing, various types of plasma processes are used to deposit layers of conductive and dielectric material on semiconductor wafers, and also to blanket etch and selectively etch materials from the wafer. During these processes the wafer is affixed to a wafer chuck in a process chamber and a plasma generated adjacent the wafer surface. Various techniques have evolved to affix the wafer to the wafer chuck. A recent technique for holding the wafer is using an electrostatic chuck, as described in U.S. Pat. No. 5,310,453 and U.S. Pat. No. 5,382,311.

In an electrostatic chuck, a conductive electrode beneath a dielectric wafer support layer is provided. When a high DC voltage is applied to the electrode, positive and negative charges are respectively produced in the wafer and the electrode, so that the wafer is attracted and held on the chuck surface by the Coulomb force acting between the wafer and the electrode. Plasma etching is performed in this state. When the etching is completed, the supply of RF power and the application of the high DC voltage to the electrode are terminated. Subsequently, the processed wafer is unloaded. The electrostatic chuck eliminates the need for mechanical clamp rings, and greatly reduces the probability of forming particles by abrasion etc., which particles cause yield problems and require frequent cleaning of the apparatus.

During the etching process, the temperature of the wafer must be controlled to prevent non-uniform etching which would otherwise produce and adverse effect on the wafers The etch rate increases with temperature increases. This temperature control can be achieved by improving the heat transfer rate between the wafer and wafer chuck. A heat transfer gas, such as He, is supplied to grooves in the top surface of the chuck. The grooves in combination with the wafer form chambers when a wafer is affixed the chuck.

Even though the use of an electrostatic chuck reduces particle contamination, it is inevitable that small particles are formed, and other contamination generated within the process chamber. These particles and contamination when deposited or formed on the wafer chuck surface of an ESC increase the leakage of the heat transfer gas, i.e. He, at the interface of the chuck surface and wafer. This leakage reduces the temperature control of the wafer and the efficiency of wafer cooling techniques. Consequently, the process chamber and the wafer chuck must be cleaned quite frequently. This results in down time for the apparatus, and requires an expensive and time consuming manual apparatus cleaning operation.

SUMMARY OF THE INVENTION

It is an object of the invention to provide a new and more efficient process for cleaning an electrostatic chuck.

Another object of the invention is to provide a new process for removing small particles and other contamination from the top surface of an electrostatic chuck.

Yet another object of the invention is to provide a method of cleaning an electrostatic chuck of a plasma etching apparatus that takes a minimum amount of time, and is less disruptive of the overall semiconductor manufacturing operation.

In accordance with the above objectives, there is provided a process for cleaning an electrostatic chuck of a plasma apparatus in which a dummy wafer is placed on the wafer chuck and the process chamber evacuated. An RF voltage is applied to the chuck with a wattage in excess of the normal operating wattage needed to generate an RF plasma. Subsequently the RF voltage is turned off and the dummy wafer is removed from the chamber along with the adhering debris and contamination.

BRIEF DESCRIPTION OF THE DRAWINGS

The accompanying drawings, which are incorporated in and constitute a part of the specification, illustrate preferred embodiments of the invention and serve to explain the principles of the invention.

FIG. **1** is a schematic view of a typical plasma etching apparatus on which the process of the invention can be performed.

FIG. **2** is a flow diagram that depicts the process steps of the subject invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring now to FIG. **1** of the drawing, there is depicted a plasma etching apparatus, provided with an electrostatic chuck (ESC), which is typical of the apparatus which can be cleaned by applicants process.

The apparatus has a process chamber made up of an upper case **10**, and a lower case **12**, The upper and lower cases are made of a conductive material, such as aluminum. The lower case **12** has a cylindrical shape with a bottom so that an insulating ceramic frame **14** can be fitted therein. An electrostatic chuck **16** has a conductive sheet **18**, serving as a chuck electrode, that is sandwiched between upper and lower dielectric sheets **20** and **22**, preferably made of polyimide. A DC power source **24** is connected to chuck electrode **18** through a feeder path **26** and switch **28**. When a high voltage is applied to electrode **18** from power source **24**, a Coulomb force is generated between wafer W and electrode **18** which attracts and holds the wafer W on the ESC **16**.

In order to improve the heat transfer between the wafer W and the ESC **16**, a heat medium, such as He, is supplied between the wafer and ESC **16**. The heat transfer gas is supplied through a line **30** extending through the ESC **16**, the ceramic frame **14**, and plates **32** and **34**. Line **30** is connected to a gas source **36** through a mass flow controller **38**. In addition, a vacuum pump **40**, having a variable exhaust conductance, is connected to line **30**. Pump **36** is controlled by a pressure controller **42** for detecting the internal pressure of line **30**. Line **30** is connected to grooves (not shown) in the top surface of dielectric sheet **20** of ESC **16**.

A plurality of pusher pins **44** that extend through ESC **16**, plates **32** and **34**, ceramic frame **14**, and lower case **12** are provided for lifting the wafer W off the ESC **16**. The pins are moved to the extended or withdrawn position by motor **46**.

Preferably, susceptor **34** is provided with a cooling jacket **48** to cool the wafer W. A vacuum pump **50** is connected to process chamber, through pipe **52**, to exhaust gas from the

chamber. A source **54** of etching gas is connected to chamber through pipe **56**. The upper case **10** is grounded, and an RF power source **58** is connected to susceptors **32** and **34**, and conductive plate **60**. A switch **62** and an impedance tuner **64** control the power supplied by RF power source **58**.

Referring now to FIG. **2** of the drawings, there is depicted a flow chart which sets forth the process steps of the invention for cleaning debris and contamination from an ESC of the type shown in FIG. **1**, and described above. The debris to be removed consists mainly of small particles of semiconductor material that has been inadvertently broken off wafers being processed. However dust particles and other extraneous material can also become lodged on the vacuum chuck. In addition, other contamination may be deposited on the ESC from photoresist residue, polymer generation during the plasma etch process, hardware erosion, such as AL Cl_3 power, and the like.

The ESC is very sensitive to particle contamination on the surface of the wafer support surface. Particles and debris may change the electrostatic field distribution between the wafer and chuck. Further, the presence of particle contamination will cause higher He leakage, non-uniform wafer temperatures, and varying process performance, i.e. non-uniform etching rates etc. The back side helium flow cooling is based on the assumption of smooth contact surfaces between the chuck surface and wafer surface. The lower the He leak rate, the better the cooling efficiency. The back side He leak rate can be used as an index for the back side cooling efficiency.

Presently the ESC is cleaned by pump purging for at least 60 times. This procedure takes at least 90 minutes and is frequently ineffective. Another cleaning technique is to wet clean the chuck. This procedure takes at least four hours and requires the process chamber to be opened.

In the cleaning process of the invention, the process chamber need not be opened, in automated process applications, and the time required is minimal.

In the process of the invention for cleaning an ESC, a dummy wafer is placed on the wafer chuck, as indicated by block **101** of FIG. **2**. The process chamber is evacuated, as indicated by block **102**, and an RF voltage is applied, as indicated by block **103**. The RF voltage is applied across the electrodes within the process chamber, as is conventional, to provide a plasma. The applied RF voltage that is applied should have a wattage in excess of tie normal operating wattage used in plasma etching operations. Preferably the wattage applied is 100% to 120% of the normal wattage. The RF voltage is applied for a time sufficient to cause the debris and contamination to adhere to the dummy wafer. The time is preferably greater than 15 seconds, more preferably in the range of 20 to 30 seconds.

The RF voltage is then turned off, as indicated by block **104**, and the dummy wafer with the adhering debris and contamination is removed from the ESC, as indicated by block **105**.

A process wafer is then placed on the chuck electrode and processed. After the air has been evacuated, the source of DC power and the inert gas is applied to the chuck electrode. The gas leakage can be monitored to check the cleanliness of the chuck electrode surface. If the leakage is higher than the normal leakage with a clean chuck surface, the cleaning process should be repeated. The leakage is an indicator of the cleanliness of the chuck surface.

Additional advantages and modifications will readily occur to those skilled in the art. Therefore, the invention in its broader aspects is not limited to the specific details, and illustrated examples shown and described herein. Accordingly. various modifications may be made without departing from the spirit or scope of the general inventive concept as defined by the appended claims and their equivalents.

What is claimed is:

1. A process for cleaning debris and contamination from the surface of an electrostatic chuck of a plasma etching apparatus having a process chamber, a source of RF power, an electrostatic wafer chuck within the process chamber, a chuck electrode, and a source of DC power connected to said chuck electrode comprising;

placing a dummy wafer on and in direct contact with the electrostatic wafer chuck,

evacuating the process chamber,

applying an RF voltage with a wattage in excess of the normal wattage applied during normal etching procedure, while refraining to apply the DC power to the chuck electrode,

turning off the RF power,

removing the dummy wafer and the adhering debris and contamination.

2. The method of claim **1** wherein the wattage of the applied RF voltage is in the range of 100 to 120% of the wattage applied during normal etching procedure.

3. The method of claim **2** wherein the RF power is applied for a time in the range of 20 to 30 seconds.

4. The method of claim **1** wherein the cleaning process is performed periodically by inserting dummy wafers into cassettes of wafers to be processed, and sequentially placing the wafers and dummy wafers on the chuck for etching or cleaning the chuck.

5. The method of claim **1** wherein the RF voltage is applied across the process chamber and the wafer chuck.

6. The method of claim **1** which further includes testing the cleanliness of the chuck, comprising;

providing a groove system in the top surface of the chuck,

placing a clean semiconductor wafer on the wafer chuck,

ecacuating the air from the process chamber,

applying a source of DC power to the chuck electrode to secure the wafer to the chuck,

introducing an inert gas into te groove system in the wafer chuck, and

monitoring the gas leakage from the groove system.

7. The method of claim **1** wherein the RF voltage is applied for a time greater than 15 seconds.

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