UNITED STATES PATENT AND TRADEMARK OFFICE

COMMISSIONER FOR PATENTS
UNITED STATES PATENT AND TRADEMARK OFFICE
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APPLICATION NUMBER	FILING DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
09/151,163	09/10/1998	DANIEL L. FLAMM	16655-000810

CONFIRMATION NO. 7361

OC000000006140145

20350
TOWNSEND AND TOWNSEND AND CREW
TWO EMBARCADERO CENTER
EIGHTH FLOOR
SAN FRANCISCO, CA 94111-3834

Date Mailed: 06/01/2001

NOTICE REGARDING POWER OF ATTORNEY

This is in response to the Power of Attorney filed 05/17/2001.

- The withdrawal as attorney in this application has been accepted. Future correspondence will be mailed to the new address of record. 37 CFR 1.33.

Customer Service Center
Initial Patent Examination Division (703) 308-1202

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COMMISSIONER FOR PATENTS
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APPLICATION NUMBER	FILING DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
09/151,163	09/10/1998	DANIEL L. FLAMM	16655-000810

CONFIRMATION NO. 7361

OC000000006140153

DR. DANIEL J. FLAMM
476 GREEN VIEW DRIVE
WALNUT CREEK, CA 94596

Date Mailed: 06/01/2001

NOTICE REGARDING POWER OF ATTORNEY

This is in response to the Power of Attorney filed 05/17/2001.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

Customer Service Center
Initial Patent Examination Division (703) 308-1202

OFFICE COPY

Daniel L. Flamm
476 Green View Drive
Walnut Creek, CA 94596-5459
(925) 947-1909

Transmittal Letter

09/151,163

Date: May 21, 2001

I hereby certify that this is being deposited with the United States Postal Service as first class mail in an envelope addressed to:

Assistant Commissioner for Patents
Washington, D.C. 20231

Date: May 21, 2001

By: Daniel L. Flamm
Daniel L. Flamm

BOX ISSUE FEE
ASSISTANT COMMISSIONER FOR PATENTS
Washington, D.C. 20231

Sir:

Transmitted herewith are the following:

OK to Enter

1) Revocation Under 37 C.F.R. /1.36
2) Fee balance of $15.00.

Daniel L. Flamm
Daniel L. Flamm

016655-0081US
WJBohler

TOWNSEND & TOWNSEND & CREW

UNDER SECRETARY OF COMMERCE FOR INTELLECTUAL PROPERTY AND
DIRECTOR OF THE UNITED STATES PATENT AND TRADEMARK OFFICE
WASHINGTON, D.C. 20231

01 APR -5 AM 8:25

RECEIVED

TOWNSEND & TOWNSEND CREW LLP
TWO EMBARCADERO CENTER 8TH FLOOR
SAN FRANCISCO CA 94111

Mail Date: April 04, 2001
Serial Number: 09/151163
Applicant: FLAMM

NOTICE TO PAY BALANCE OF ISSUE FEE

Your issue fee payment filed on 01/02/01 has been received. However, new patent fees went into effect on October 1, 2000. The final rule entitled "Revision of Patent Fees for Fiscal Year 2001" was published in the *Federal Register*/Vol. 65, No. 156/Friday, August 11, 2000 [49193–49199] and in the U.S. Patent and Trademark Office *Official Gazette*, August 29, 2000 [1237 OG 131–138]. As stated in the final rule, "Any fee amount that is paid on or after the effective date of the fee increase will be subject to the new fees then in effect." The Notice of Allowance and Issue Fee Due (Form PTOL-85) that was mailed to you prior to October 1, 2000, stated an issue fee amount that was in effect prior to October 1, 2000. However, inasmuch as your issue fee was paid on or after October 1, 2000, the new issue fee amount was due.

In accordance with 37 CFR 1.317, you are given a time period of **THREE (3) MONTHS** from the mailing date of this notice during which to pay the **BALANCE DUE** indicated below. This three-month time period may **not** be extended. **If your patent issues before the expiration of the three-month period and if you do not pay the balance due before the expiration of the three-month period, your patent will lapse at the termination of the three-month period.**

TYPE OF ISSUE FEE PAID	Column A ISSUE FEE IN EFFECT AS OF OCT. 1, 2000 large entity / small entity	Column B ISSUE FEE PAID	BALANCE DUE [Col. A minus Col. B]
UTILITY	$1,240.00 / $620.00	$ 605.00	$ 15.00
DESIGN	$440.00 / $220.00	$	$
PLANT	$600.00 / $300.00	$	$

K Laing
Office of Patent Publication
Tel: 703-305-8263

You MUST return a copy of this Notice with your payment.

CERTIFICATE OF MAILING

I hereby certify that this notice and the required additional fee are being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to Box ISSUE FEE, Commissioner for Patents, Washington, D.C. 20231 on the date indicated below.

Printed Name: Daniel L. Flamm Signature: Daniel L. Flamm

Date: May 21, 2001

Adjustment date: 05/25/2001 SLUANG2
01/03/2001 CCHAU2 00000163 09151163
01 FC:631 -605.00 OP

05/25/2001 SLUANG2 00000001 09151163
620.00 OP
01 FC:242

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Assistant Commissioner for Patents
Washington, D.C. 20231

On May 21, 2001

By: Daniel L. Flamm

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	Examiner: L. Scheiner
Daniel L. Flamm	Art Unit: 1641
Application No.: 09/151,163	REVOCATION AND SUBSTITUTION OF POWER OF ATTORNEY UNDER 37 CFR 1.36
Filed: September 10, 1998	
For: PROCESS DEPENDING ON PLASMA DISCHARGES SUSTAINED BY INDUCTIVE COUPLING	

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Pursuant to 37 CFR/1.36, Daniel L. Flamm revokes all previous powers of attorney and hereby designates himself to prosecute this application and transact all business in the Patent and Trademark Office connected therewith.

Please direct all future correspondence regarding the subject application to

Daniel L. Flamm
476 Green View Drive
Walnut Creek, CA 94596

Tel: (925) 947-1909
Fax: (925) 937-2754

Date: May 21, 2001

By: Daniel L. Flamm
Print Name: Daniel L. Flamm

DSD

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to:

Assistant Commissioner for Patents,
Washington, D.C. 20231

on May 14, 2001

TOWNSEND and TOWNSEND and CREW LLP

By Mary Bender

PATENT

Attorney Docket No.: 016655-000810US

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

Daniel L. Flamm et al.

Application No.: 09/151,163
U.S. Patent No.: 6,231,776

Filed: September 10, 1998

For: MULTI-TEMPERATURE PROCESSING

Examiner:

Art Unit:

WITHDRAWAL OF ATTORNEY OR AGENT UNDER 37 CFR § 1.36

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Pursuant to 37 CFR § 1.36, Townsend and Townsend and Crew LLP, attorneys for applicant hereby withdraws from representation relative to the above-identified patent. Please direct all future correspondence regarding the subject patent to applicant at:

Dr. Daniel J. Flamm
476 Green View Drive
Walnut Creek, California 94596

By: William J. Bohler

William J. Bohler
Reg. No. 31,487

TOWNSEND and TOWNSEND and CREW LLP
Two Embarcadero Center, 8th Floor
San Francisco, CA 94111-3834
Tel (415) 576-0200
Fax (415) 576-0300
PA 3135615 v1

UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

APPLICATION NUMBER	FILING DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NO.
09/151,163	09/10/98	FLAMM	D 16655-000810

020350 7542/0119
TOWNSEND AND TOWNSEND AND CREW
TWO EMBARCADERO CENTER
EIGHTH FLOOR
SAN FRANCISCO CA 94111-3834

EXAMINER	
SCHEINER,L	
ART UNIT	PAPER NUMBER
1648	10

DATE MAILED: 01/19/01

Response to Rule 312 Communication

☐ The petition filed on _____ under 37 CFR 1.312(b) is granted. The paper has been forwarded to the examiner for consideration on the merits.

_____

_____
Director,
Patent Examining Group _____

☑ The amendment filed on 1-2-01 under 37 CFR 1.312 has been considered, and has been:

☑ entered.

☐ entered as directed to matters of form not affecting the scope of the invention (Order 3311).

☐ disapproved. See explanation below.

☐ entered in part. See explanation below.

R. W. Thompson Jr
Publishing Division

FORM PTOL-271 (REV. 1-95)

ISSUE FEE TRANSMITTAL

fees, to: Box ISSUE FEE
Assistant Commissioner for Patents
Washington, D.C. 20231

MAILING INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE. Blocks 1 through 4 should be completed where appropriate. All further correspondence including the Issue Fee Receipt, the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Legibly mark-up with any corrections or use Block 1)

020350 HM12/0926
TOWNSEND AND TOWNSEND AND CREW LLP
TWO EMBARCADERO CENTER
EIGHTH FLOOR
SAN FRANCISCO CA 94111

Note: The certificate of mailing below can only be used for domestic mailings of the Issue Fee Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing.

Certificate of Mailing

I hereby certify that this Issue Fee Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Box Issue Fee address above on the date indicated below.

Daniel L. Flamm (Depositor's name)
Daniel L. Flamm (Signature)
December 24, 2000 (Date)

APPLICATION NO.	FILING DATE	TOTAL CLAIMS	EXAMINER AND GROUP ART UNIT	DATE MAILED
09/151,163	09/10/98	012	SCHEINER, L 1648	09/26/00

First Named Applicant: FLAMM, 35 USC 154(b) term ext. = 0 Days.

TITLE OF INVENTION: MULTI-TEMPERATURE PROCESSING

ATTY'S DOCKET NO.	CLASS-SUBCLASS	BATCH NO.	APPLN. TYPE	SMALL ENTITY	FEE DUE	DATE DUE
1 16655-000810	216-068.000	080	UTILITY	YES	$605.00	12/26/00

1. Change of correspondence address or indication of " Fee Address" (37 CFR 1.363). Use of PTO form(s) and Customer Number are recommended, but not required.

☒ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

☒ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47) attached.

2. For printing on the patent front page, list (1) the names of up to 3 registered patent attorneys or agents OR, alternatively, (2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 None
2
3

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)
PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. Inclusion of assignee data is only appropriate when an assignment has been previously submitted to the PTO or is being submitted under separate cover. Completion of this form is NOT a subsitiute for filing an assignment.

(A) NAME OF ASSIGNEE Daniel L. Flamm

(B) RESIDENCE: (CITY & STATE OR COUNTRY) Walnut Creek, California

Please check the appropriate assignee category indicated below (will not be printed on the patent)

☐ individual ☐ corporation or other private group entity ☐ government

4a. The following fees are enclosed (make check payable to Commissioner of Patents and Trademarks):

☒ Issue Fee
☐ Advance Order - # of Copies _____

4b. The following fees or deficiency in these fees should be charged to:

DEPOSIT ACCOUNT NUMBER _____
(ENCLOSE AN EXTRA COPY OF THIS FORM)

☐ Issue Fee
☐ Advance Order - # of Copies _____

The COMMISSIONER OF PATENTS AND TRADEMARKS IS requested to apply the Issue Fee to the application identified above.

(Authorized Signature) Daniel L. Flamm (Date) 12/24/2000

NOTE; The Issue Fee will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the Patent and Trademark Office.

01/03/2001 CCHAU2 00000163 09151163
01 FC:631 605.00 OP

9/00

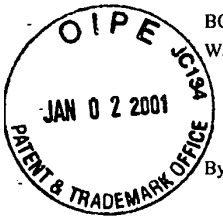
Burden Hour Statement: This form is estimated to take 0.2 hours to complete. Time will vary depending on the needs of the individual case. Any comments on the amount of time required to complete this form should be sent to the Chief Information Officer, Patent and Trademark Office, Washington, D.C. 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND FEES AND THIS FORM TO: Box Issue Fee, Assistant Commissioner for Patents, Washington D.C. 20231

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

TRANSMIT THIS FORM WITH FEE

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: BOX ISSUE FEE, Assistant Commissioner for Patents, Washington, D.C. 20231, on December 24, 2000

By: Daniel L. Flamm



PATENT

#9

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Daniel L. Flamm Application No.: 09/151,163_ Filed: September 10, 1998 For: MULTI—TEMPERATURE PROCESS	Examiner: SCHEINER, L. Art Unit: 1648 Batch No.: S80 **AMENDMENT AFTER ALLOWANCE UNDER 37 CFR/1.312(a)**

BOX ISSUE FEE
Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

In response to the Notice of Allowance mailed September 26, 2000, please amend the above-identified application as follows:

IN THE SPECIFICATION:

NE At page 5, line 19, please delete --9-- after "means".

At page 23, line 11, please insert --be-- after "and".

At page 24, line 15, please insert --615-- after units.

At page 24, line 21, please delete "edge band" and insert --band edge--.

At page 24, line 19, please delete "fluro-optic" and insert --fluoroptic--.

At page 25, line 20, please delete "with the" and insert --with an--.

At page 25, line 24, please delete "fluor optic" and insert --fluoroptic--.

At page 25, line 25, please delete "of chuck" and insert --or chuck--.

At page 26, line 25, please insert --and-- after "limited to two".

At page 26, line 27, please delete "V1" and insert --805--.

At page 26, line 30, please delete "V1 and V2" and insert --805 and 807--.

At page 27, line 2, please delete "V2 and V2" and insert --805 and 807--.

At page 27, line 4, please delete "1 and 2" and insert --801 and 803--.

At page 27, line 5, please delete "TC2 and TC2" and insert --TC1 and TC2--.

At page 27, line 10, please insert --with-- after "controlled".

At page 28, line 8, please insert --)-- after "100°C".

At page 28, line 9, please delete "of" and insert --or--.

At page 28, line 12, please delete "controlled" and insert --control--.

At page 28, line 27, please insert --plasma-- after "oxygen".

At page 29, line 10, please delete "sued" and insert --used--.

At page 29, line 18, please insert --,-- after "step".

At page 29, line 19, please delete "C" and insert --B--.

At page 30, line 6, please delete "DD"" and insert --D--.

At page 30, line 8, please insert --polysilicon-- after "and".

At page 30, line 8, please insert --schematically-- after "are".

At page 30, line 8, please delete "the Fig." and insert --Fig. 10--.

At page 30, line 11, please delete "at endpoint" and insert --beyond the endpoint--.

IN THE DRAWINGS:

Applicant submits new figures 7,8 and 10, consisting of 3 sheets of drawings. Newly submitted figures correct some inadvertent errors in the originally submitted drawings. Amendments to the originally submitted informal figures have been highlighted in red ink.

With respect to Fig. 7, some editorial changes are made to replace several abbreviations with plain English and for consistency with the specification. "Heat xfer when need cool fluid" is deleted and replaced with --Heat exchange when fluid cooling is needed (see, e.g. Specification, p. 25, lines 10--15). The legend accompanying 719, "bypass for use when exit fluid is cool & must be heated before use" is deleted and replaced with --Bypass used when exit fluid must be heated-- (see, e.g. Specification p.25, lines 31 to p. 26, line 4). The two legends accompanying 713, "heat transfer fluid" and "Fluid Reservoir" are deleted and replaced with the coalesced legend --Heat Transfer Fluid Reservoir-- to

improve readability. "2-way solenoid valve accompanying 717" is deleted and replaced with the legend --2-way control valve-- (see, e.g. Specification, p. 25, line 31 through p. 26, line 2). It is noted that the Specification teaches control valves 721 and 717 for diverting fluid flow and does not mention solenoid valves (it is well known in the art that a solenoid valve is an example of a control valve). While the applicant believes that those skilled in the art would understand the invention in full with the original legends, these changes are made for consistency and to avoid any possible confusion on the part of the reader.

With respect to Fig. 8, in the new drawings, the abbreviated phrase "Liquid @ temp" in each of the two legends is deleted and replaced with --Fluid at temperature--. This is done both to improve readability by replacing "@ temp" with correct English and to bring the legend into formal consistency with the language of the specification (see Specification p. 26, line 29 through p. 27 line 6).

With respect to Fig. 10, three typographical errors in labels which appear by the lower curve (e.g. temperature versus time) have been corrected as follows:

"B" along the lower curve is deleted and replaced with --BB--;

the letter "C" by the top of the first temperature step on this curve is deleted and replaced with --B--;

the rightmost "H" letter over this curve is deleted and replaced with --J--.

The legend DD over the top curve in Fig. 10 is deleted since it is not referenced.

Also, axes labeled in conformance with the Specification and the captions in Fig. 10 (see Specification p. 29, lines 21-23, 26) have been placed by the left and bottom of the top curve to improve readability and clarity. A label --Time-- (see Specification, lines 18,26) has been added under the axis of the lower curve for the same reason.

It is respectfully pointed out that the corrections are entirely consistent with the upper curve in Fig. 10 and they conform to the legends in Fig. 10 and to the specification. As concerns correcting "C" on the lower curve to --B--, please note that the legend at the bottom of Fig. 10 designates "B" as that time when the "Cl_2 plasma is ignited" (corresponding to the onset of light emission at point "B" on the upper curve). Similarly, the specification (p.29, lines 19-21) teaches that "tungsten silicide is etched at this temperature until this layer is breached at random locations on the wafer" (the "layer is breached" at point "C" as specified in the caption in Fig. 10: "C. WSi_x begins to clear."). The reference to typographical error "C" in the specification (page 29, line 19) was corrected (e.g. IN THE SPECIFICATION, above). This typographical error is obvious from the language on p.29, lines 22-24 in the Specification which references the change in "the slope of intensity of an

optical light emission" at point C (shown on the upper curve)after the "higher steady state value" (referenced on line 19 of p. 29).

As concerns correcting "B" on the lower curve to --BB--, please observe that in the specification (see p. 29, line 18), reference is made to "BB" as being "at the end of the breakthrough step" when "the control program increases" to "a higher steady state value at time C". The reference label "BB" was absent in the informal drawing Fig. 10 since it was marked as "B" by typographical error.

As concerns the typographical error "H" over the top right hand side of the lower curve it is obvious that the symbol "H" is already used (there is a center label "H")and that the right hand "H" would be out of alphabetical order. Moreover, "J" which is referenced in the caption was absent in the informal drawing. In fact the caption at the bottom of Fig. 10 makes it plain that "H" designates coordinates when "Plasma extinguished and O_2 feed gas flow is started" (also in the Specification, p. 30, lines 14-17) and that step "J" is when "O_2 plasma is extinguished." The caption in Fig. 10 also designates the order of these steps as H, I, J.

While Applicant believes that those skilled in the art would readily understand the invention and would recognize the error in Fig. 10, these corrections and the addition of axes are made to avoid any possible confusion on the part of the reader.

NOTES:

All listed changes to be made in the specification are grammatical, spelling or simple typographical error corrections, excepting the following:

1) At page 5, line 8, reference to item 19 is deleted because there is no item 19 shown in Fig. 1.

2) "615" is inserted in the reference to Fig. 6 "temperature sensing units" to avoid any confusion by a reader. However Applicant believes those skilled in the art would easily understand the reference without this addition.

3) Valves are referenced by numbers in Fig. 8 rather than as "V1" and "V2". Therefore the appropriate reference numbers "805" and "807" are inserted into the specification in place of "V1" and "V2". The reservoirs in Fig. 8 are referenced as 801 and 801 rather than as "1" and "2". The specification is changed accordingly.

4) A word "plasma" was inserted on page 28, line 27 to add clarity. Applicant believes that this is a mere formality and that those skilled in the art would understand that a plasma is implied.

5) A reference to Fig. 10 "C" at page 29, line 19 was corrected to "B" as explained in connection with the above changes "IN THE DRAWINGS."

6) The word "polysilicon" is inserted at page 30, line 8 since it was omitted typographically. Applicant believes that those skilled in the art would understand a

reference to polysilicon nonetheless since polysilicon is indicated elsewhere in the Specification (i.e. p. 30, line 1) as well as in Fig. 8.

7) "DD" is changed to "D" at page 30, line 6 to bring it into conformance with the legend above the top curve of Fig. 10. This also conforms to the lower curve of Fig. 10 where it is shown that temperature is reduced beginning at point D. The legend DD is deleted from above the top curve in Fig. 10 since it is not referenced. Applicant believes those skilled in the art will understand the curves and legend in the informal drawing of Fig. 10 and would recognize the typographical error in the Specification.

8) The word "schematically" is inserted at page 30, line 8 to clarify the nature of the drawing. Applicant believes the explanation of the drawing will be understood by those skilled in the art without this added clarification.

9) At page 30, line 8 "the Fig." is changed to "Fig. 10" to add clarity. Applicant believes this is merely a formality.

10) At page 30, line 11 "at endpoint" is changed to "beyond the endpoint" to bring this statement into conformance with the illustration in Fig. 10. Some etching may continue beyond the endpoint E until the plasma is extinguished at "H." It is well known and understood by those skilled in the art that etching continues beyond an endpoint until a plasma is extinguished.

REMARKS

Entry of this amendment is respectfully urged since it merely cures certain formal defects and does not touch the merits. If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at (925) 947--1909.

Respectfully submitted,

Daniel L. Flamm

Applicant

Daniel L. Flamm
476 Green View Drive
Walnut Creek, California 94596--5459
Tel:(925) 947--1909 / Fax:(925) 937--2754

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to:

Box Issue Fee
Assistant Commissioner of Patents and Trademarks
Washington, D.C. 20231, on December 24, 2000

By Daniel L. Flamm

#9/13
1-19-01
CUT

COPY

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	Examiner: Examiner: L. Scheiner
Daniel L. Flamm	Art Unit: 1648
Serial No.: 09/151,163	Batch No.: S80
Filed: September 10, 1998	LETTER TO OFFICIAL
For: MULTITEMPERATURE PROCESSING	DRAFTSPERSON

Assistant Commissioner of Patents
Washington, D.C. 20231

Sir:

Pursuant to the Notice of Allowability dated September 29, 2000, applicant submits fifteen sheets of formal drawings to be made of record in the above-identified case.

Exercising an abundance of caution, Applicant encloses two alternative sets of formal drawings for Figs. 7, 8, and 10, consisting three sheets each. A First Set, which conforms to the existing Allowance from Examiner Scheiner, contains typographical errors identically present in the original informal drawings. These errors are corrected in the Second Set of formal drawings for Figs. 7, 8 and 10, and these three corrected drawings are provisionally enclosed. Please note that the second set has not yet been reviewed by Examiner Scheiner; hence the first set with typographical errors is formally submitted to be of record at this time. Applicant respectfully hopes that Examiner Scheiner will find that the Second Set is allowable and can be admitted in place of the first set.

Applicant is concurrently submitting an AMENDMENT AFTER ALLOWANCE UNDER 37 CFR § 1.312(a) to Examiner Scheiner in which Applicant respectfully requests that these corrections be allowed. The Applicant wishes to apologize for any inconvenience. Applicant attempted to contact and fax this material to Examiner Scheiner for consideration in advance of the due date, however Examiner Scheiner and colleagues were understandably on holiday vacation and will not return until after the due date of December 26.

Respectfully submitted,

Daniel L. Flamm

476 Green View Drive
Walnut Creek, California 94596-5459
(925) 947-1909

Transmittal Letter

09 151 163 B JC #9

Daniel L. Flamm
476 Green View Drive
Walnut Creek, CA 94596-5459
(925) 947-1909

Date: December 24, 2000

I hereby certify that this is being deposited with the United States Postal Service as first class mail in an envelope addressed to:

BOX ISSUE FEE
Assistant Commissioner for Patents
Washington, D.C. 20231

Date: December 24, 2000

By: Daniel L. Flamm
Daniel L. Flamm

BOX ISSUE FEE
ASSISTANT COMMISSIONER FOR PATENTS
Washington, D.C. 20231

Sir:

Transmitted herewith are the following documents:

1) Amendment After Allowance Under 37 C.F.R. §1.312(a)
2) Letter to Examiner Scheiner and Official Draftsperson
3) Copy of letter to Official Draftsperson;
4) Original and corrected copies of Figs. 7,8,9

MATCH & RETURN

MATCH & RETURN

Daniel L. Flamm

9/00

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

11

In re application of:	Examiner: Examiner: L. Scheiner
Daniel L. Flamm	Art Unit: 1648
Serial No.: 09/151,163	Batch No.: S80
Filed: September 10, 1998	LETTER TO EXAMINER AND OFFICIAL DRAFTSPERSON
For: MULTI-TEMPERATURE PROCESSING	

Assistant Commissioner of Patents
Washington, D.C. 20231

Date: December 23, 2000

Dear Examiner Scheiner and DRAFTSPERSON:

In preparing the formal drawings and reviewing various materials prior to submission for Issue, I found some typographical errors in the Specification and several of the Informal Drawings. I attempted to contact Examiner Scheiner to expedite processing of the enclosed **AMENDMENT AFTER ALLOWANCE UNDER 37 CFR/1.312(a)** , to thereby minimize any inconvenience. However I learned that many staff, including those in Examiner Scheiner's unit are on leave for the holidays.

Using an abundance of caution, I am submitting Formal Drawings which correspond to the Informal Drawings which were in the Application before Examiner Scheiner. However, I am also submitting three Formal Drawings with the corrections submitted in the enclosed **AMENDMENT AFTER ALLOWANCE UNDER 37 CFR/1.312(a)** . It is my hope that Examiner Scheiner may approve the Amendment and that the corrected formalities will be able to be admitted in the published patent.

Respectfully submitted,

Daniel L. Flamm

476 Green View Drive
Walnut Creek, California 94596-5459
Tel: (925) 947-1909
Fax: (925) 937-2754

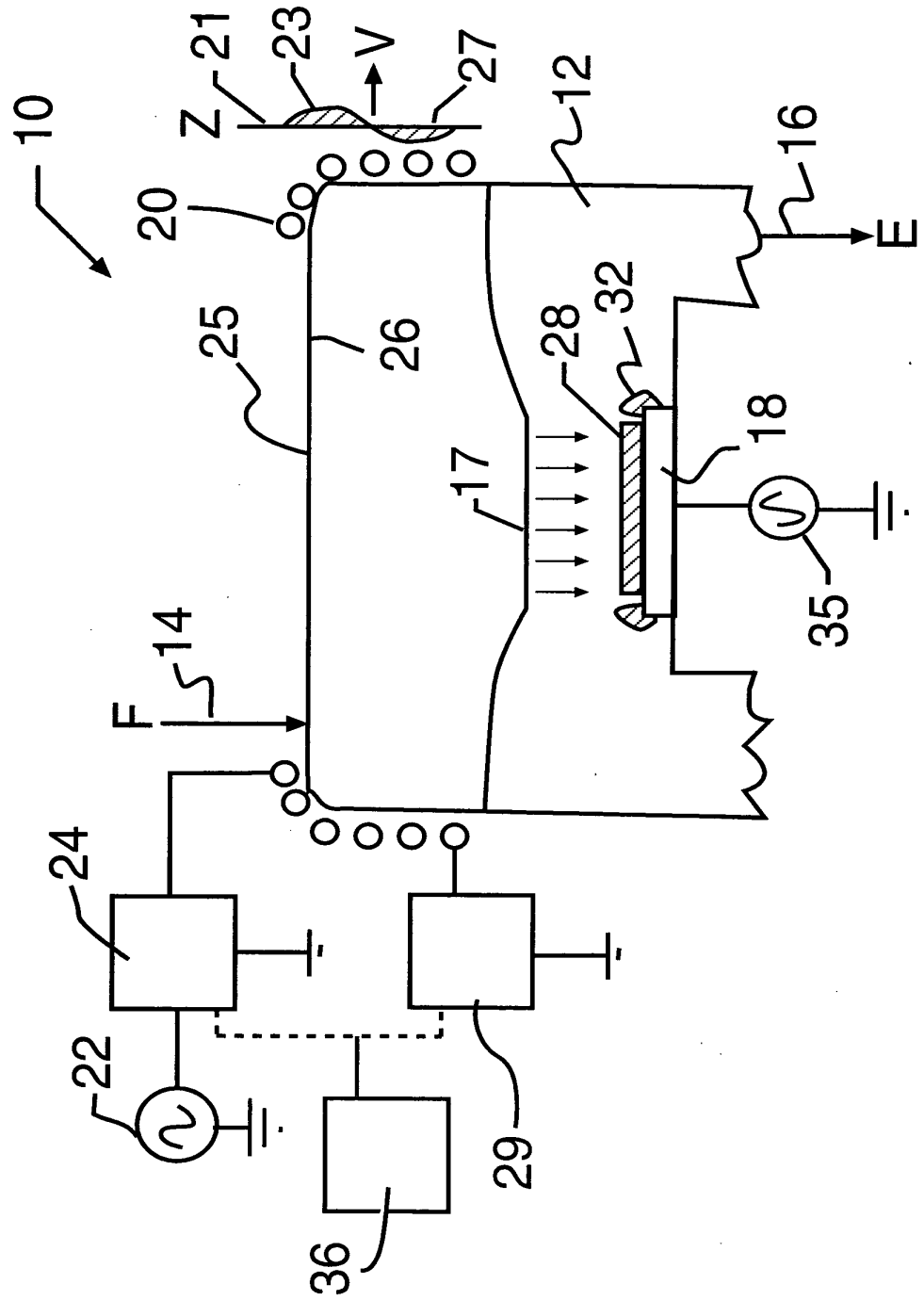


FIG. 1

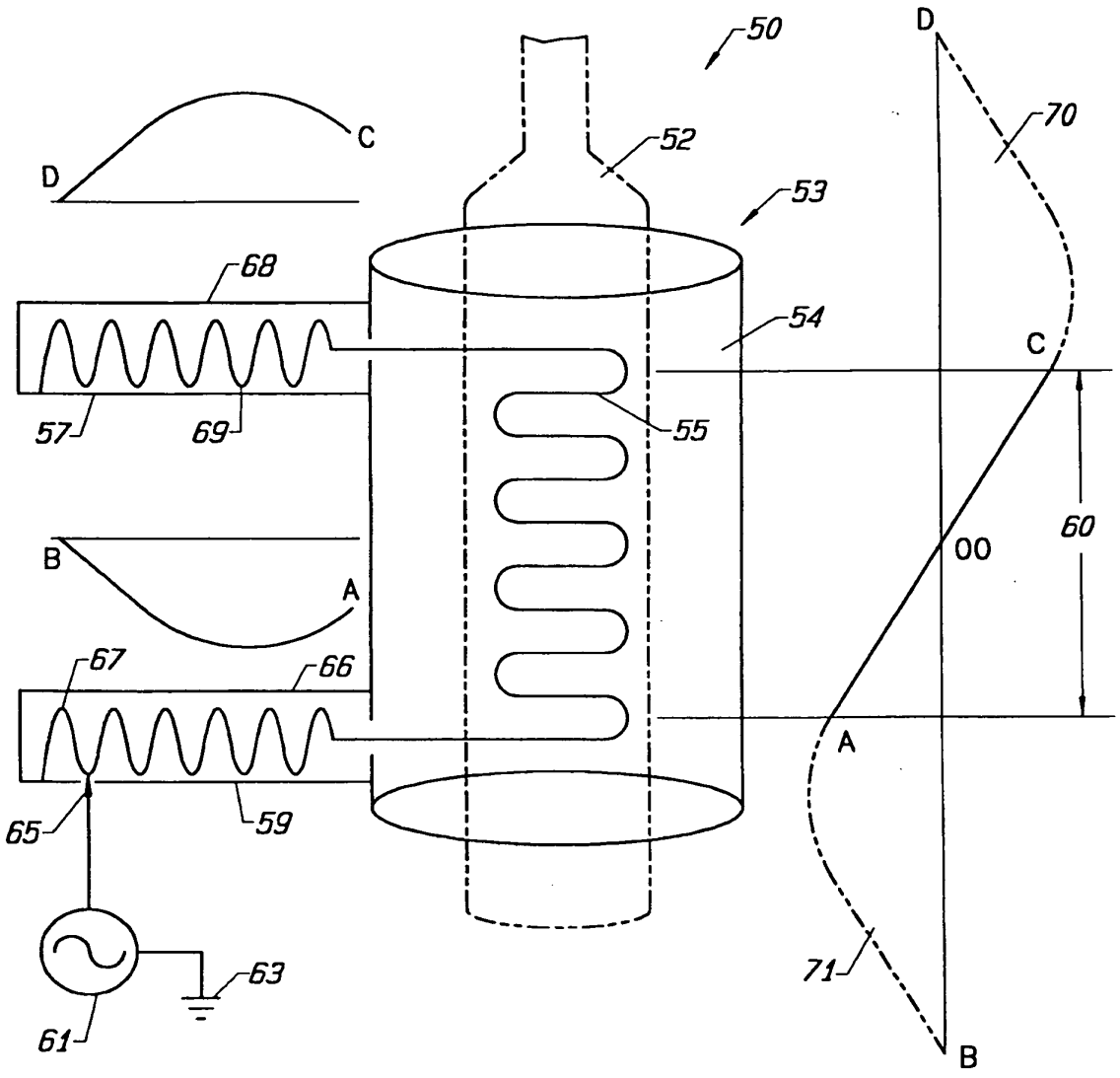


FIG. 2A

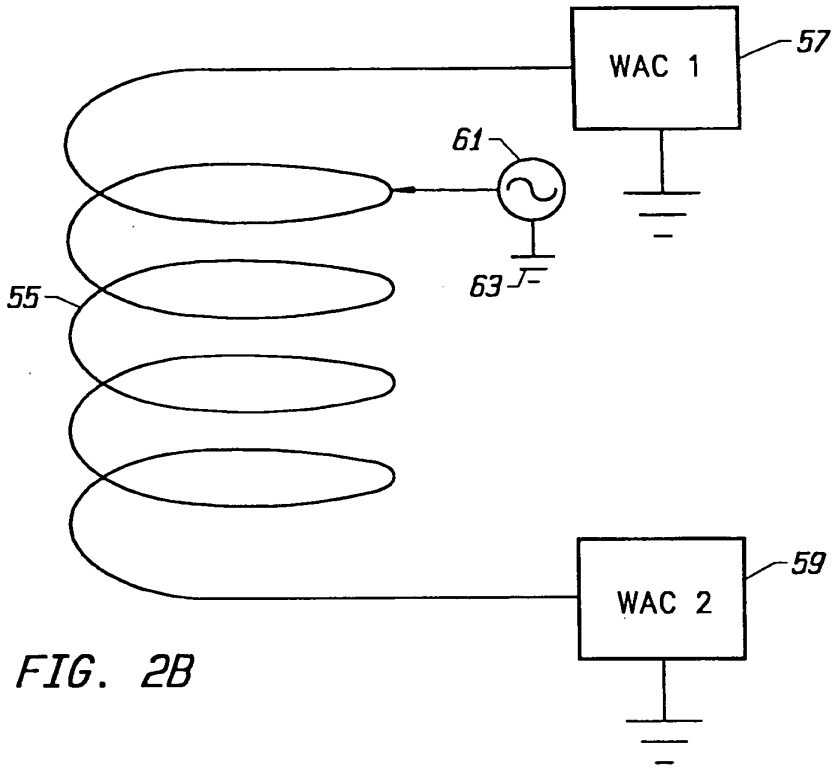


FIG. 2B

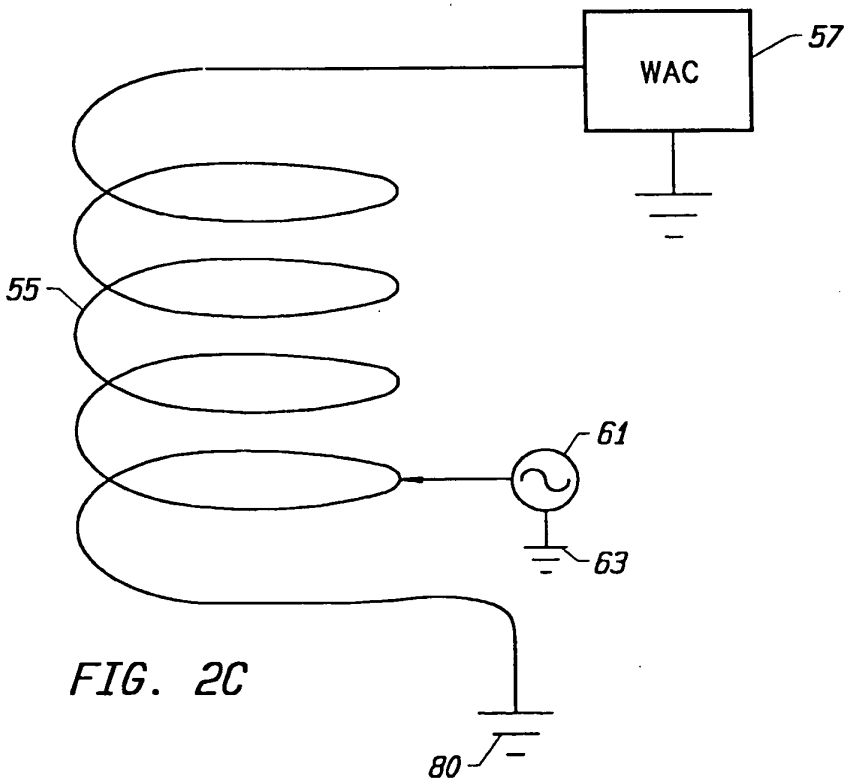


FIG. 2C

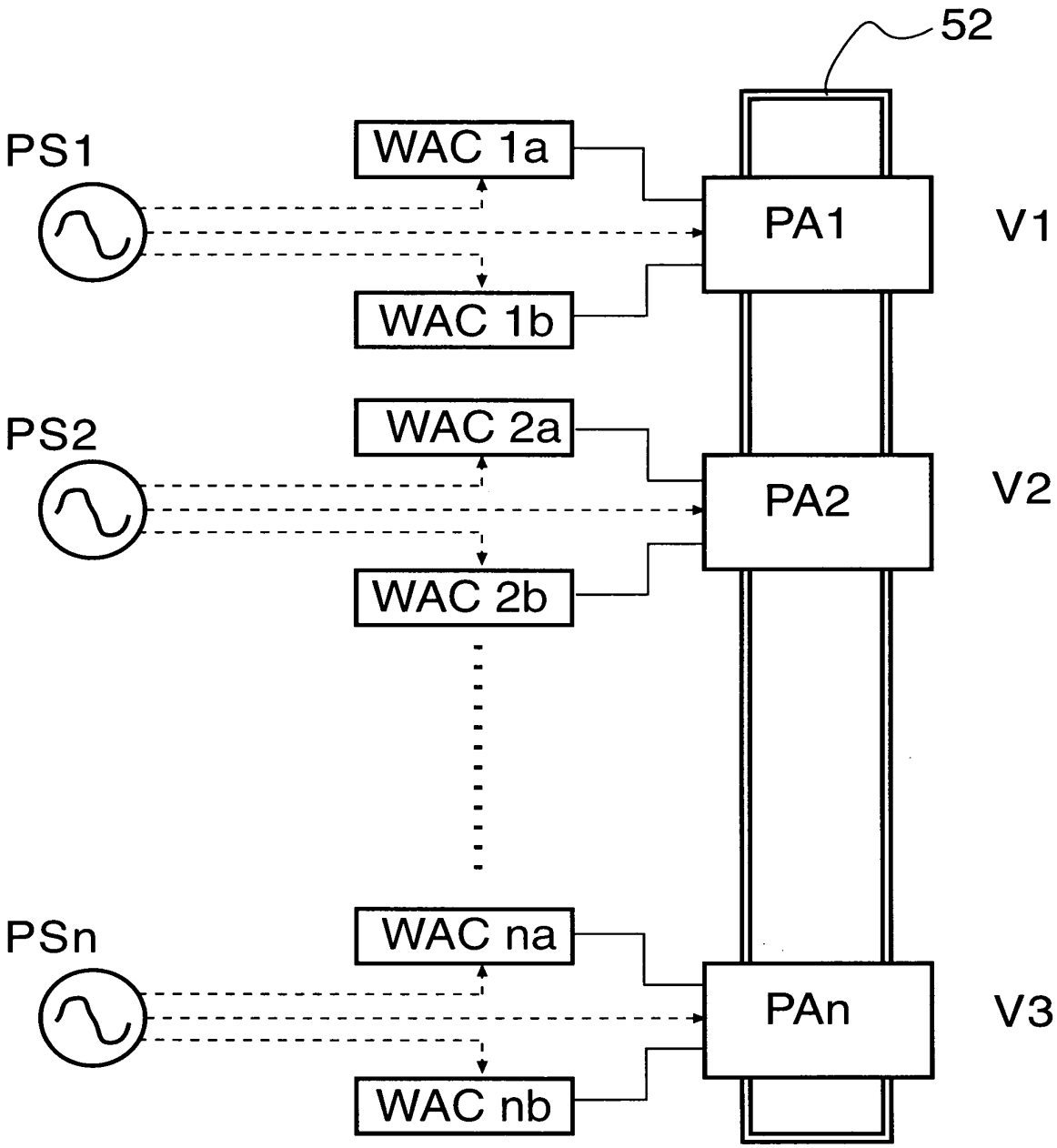


Fig. 2D

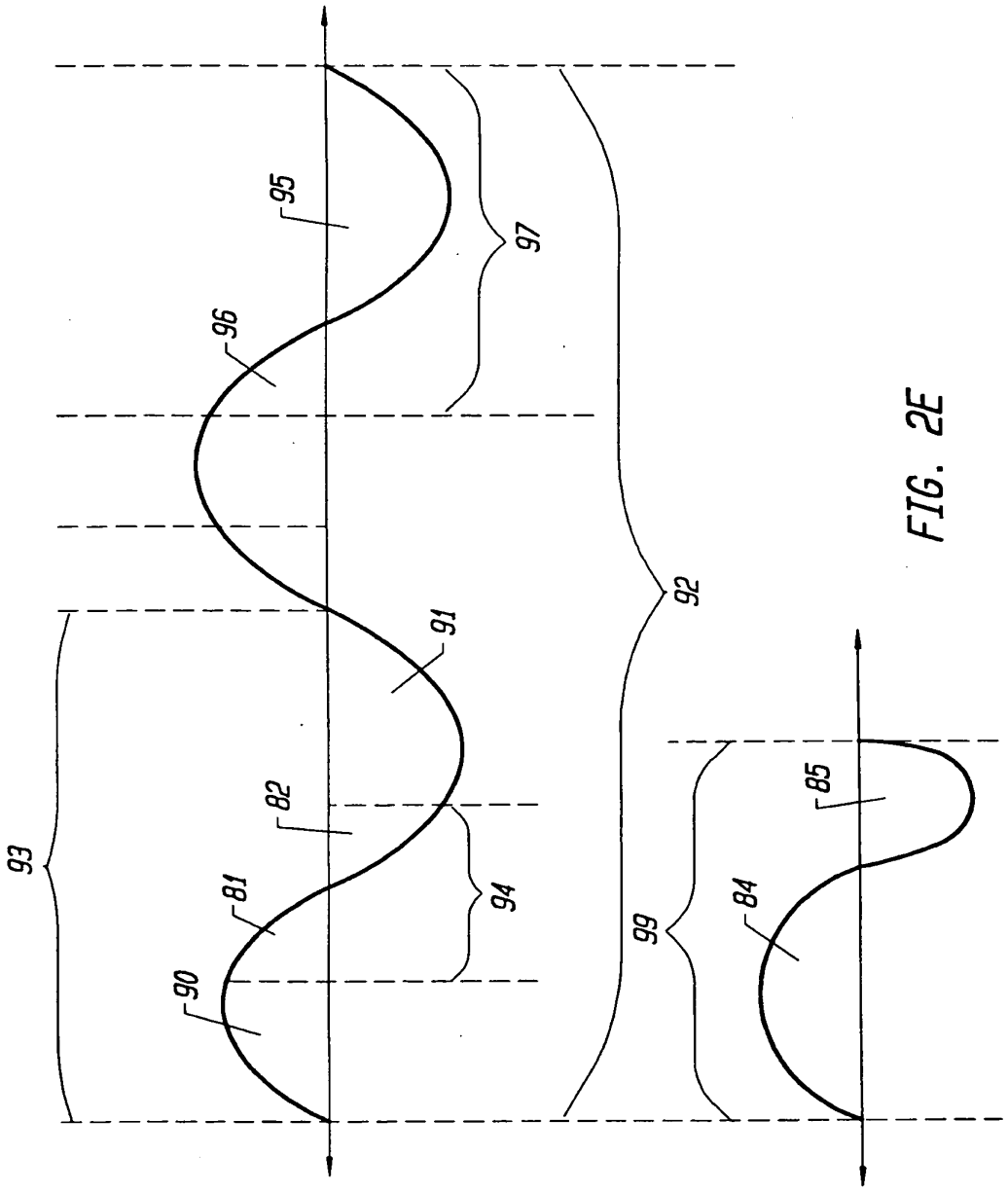


FIG. 2E

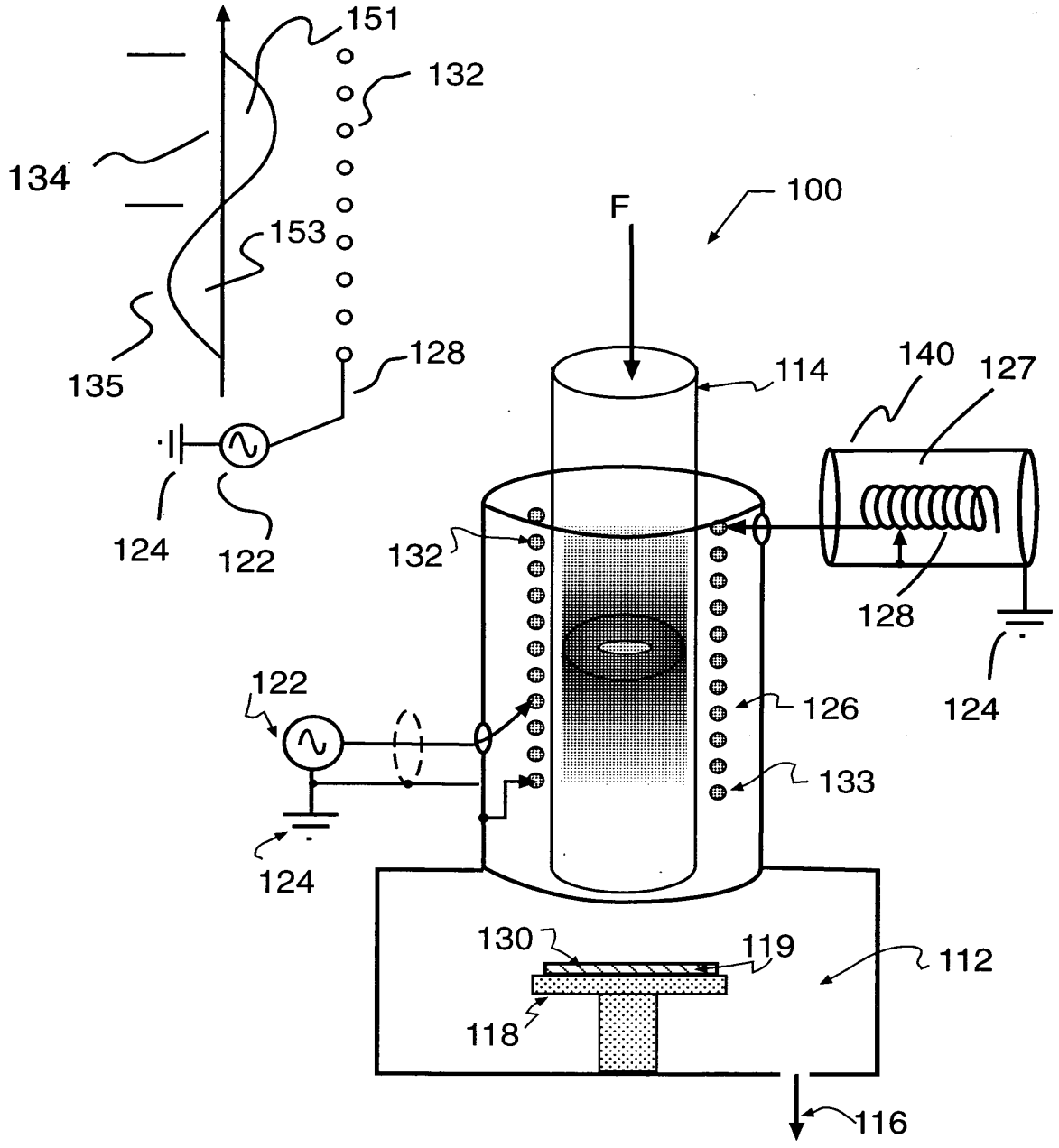


Fig. 3

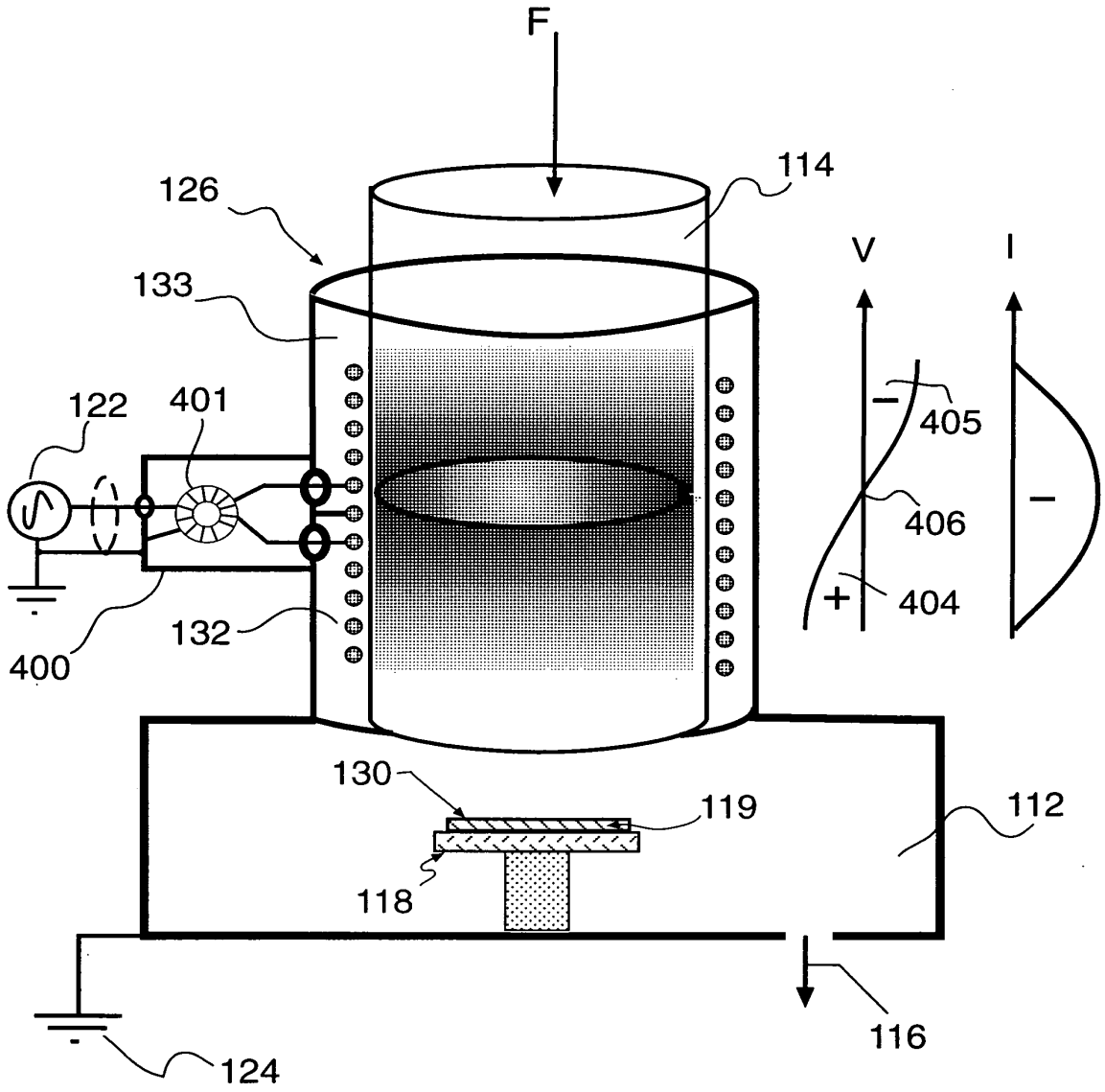


Fig. 4

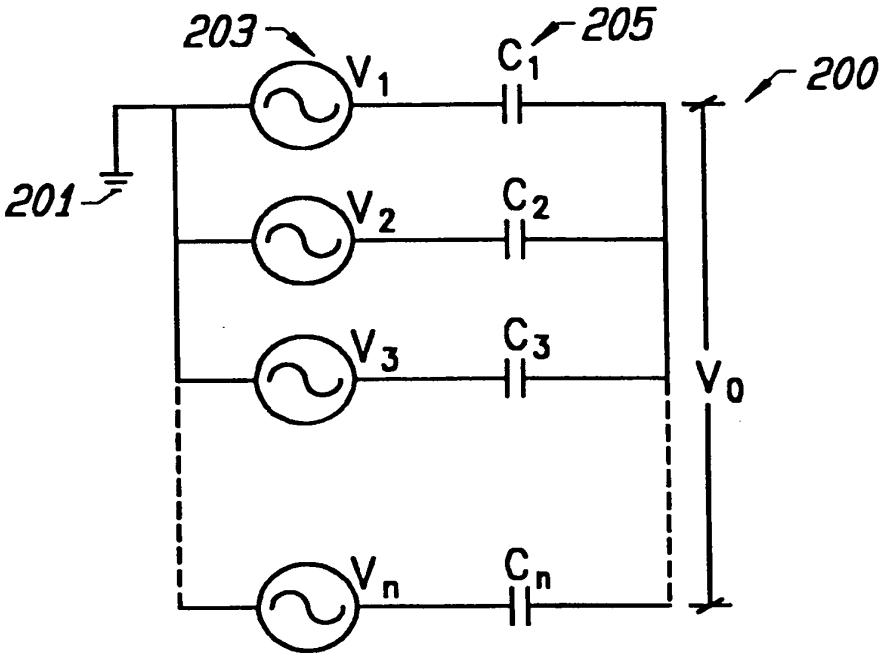


FIG. 5A

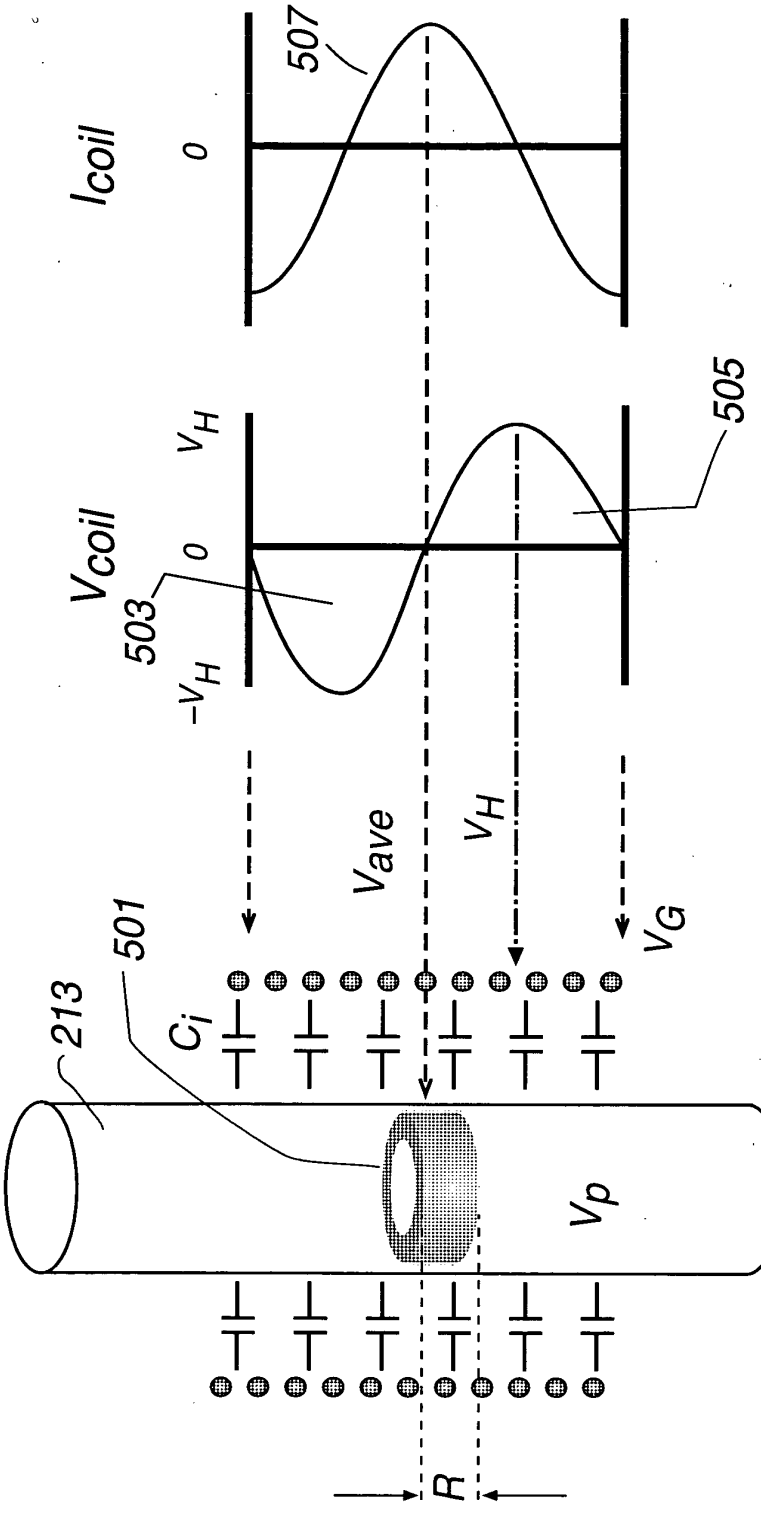


Fig. 5B

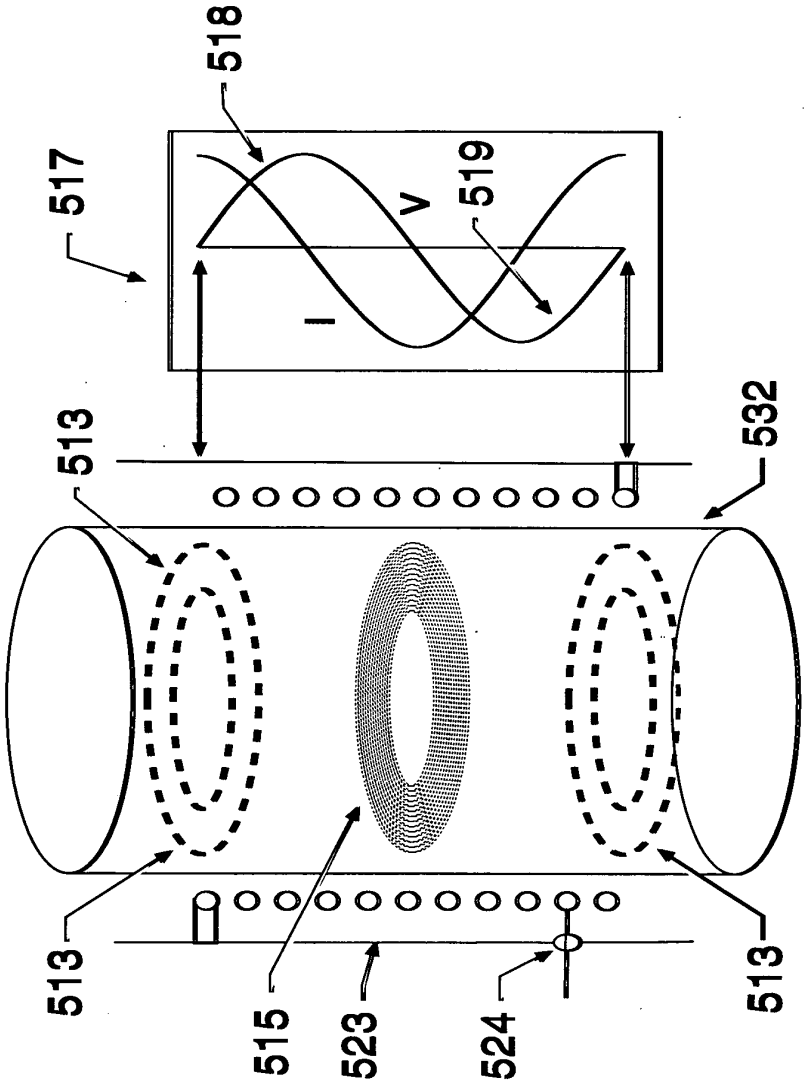


Fig. 5C

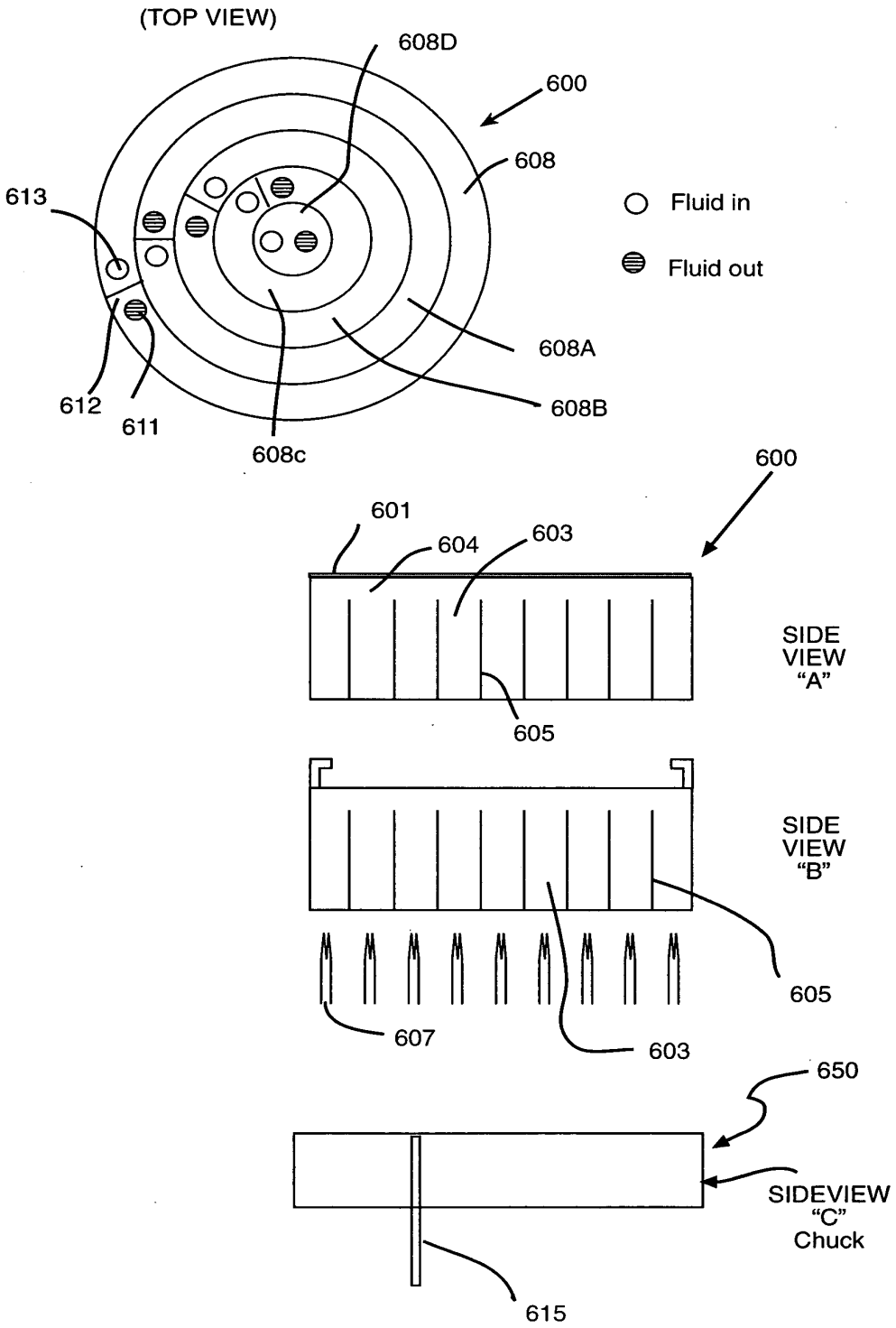


FIG. 6

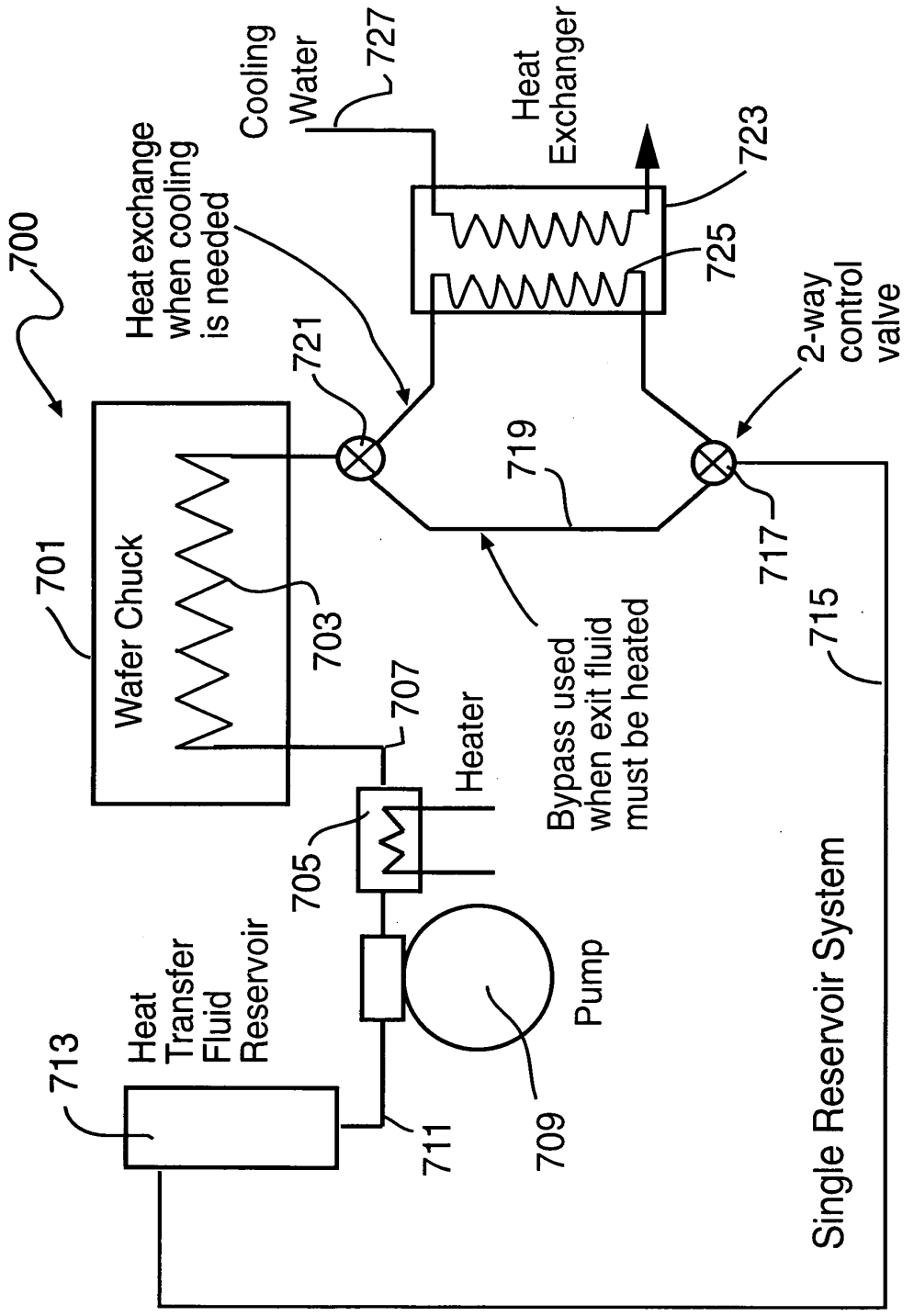


Fig. 7

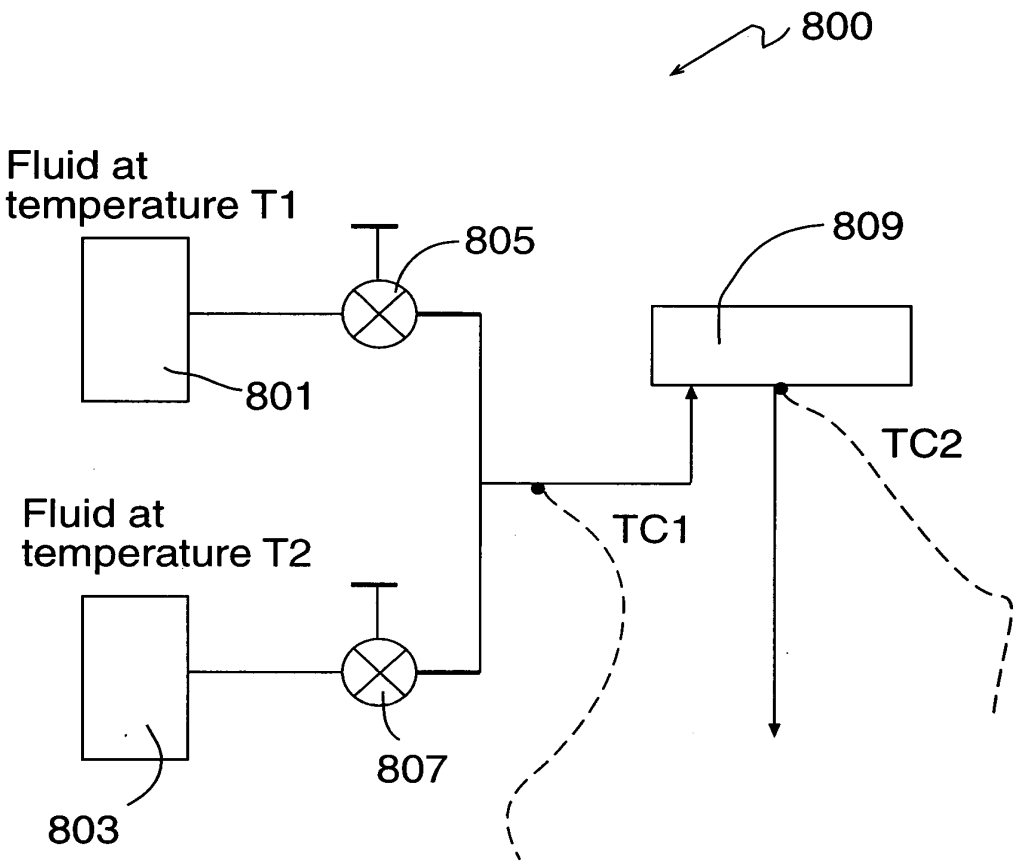


Fig. 8

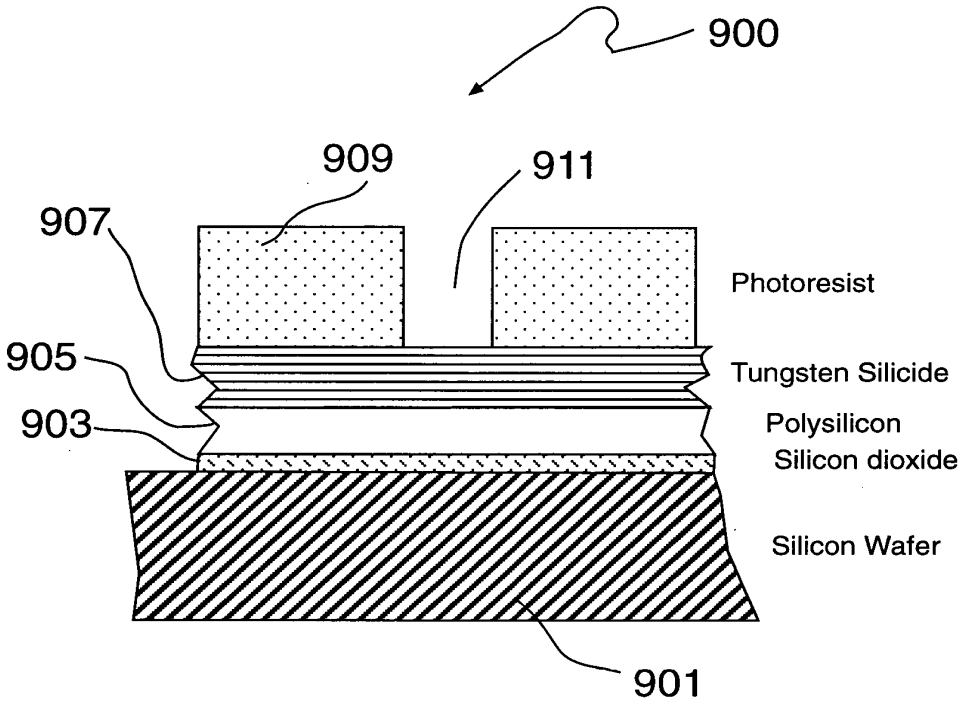
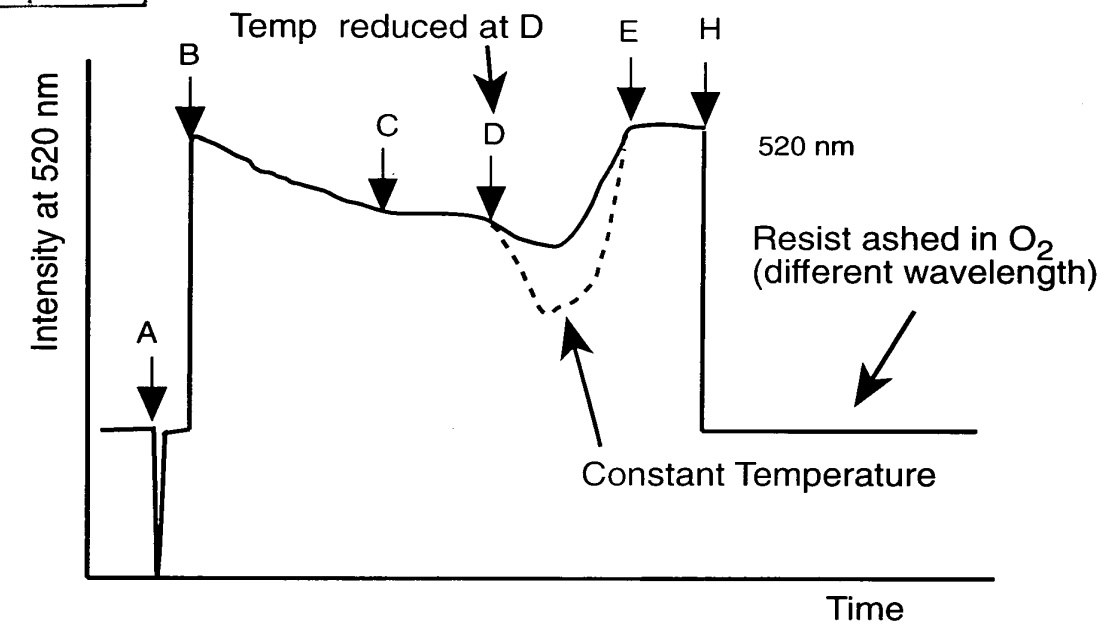
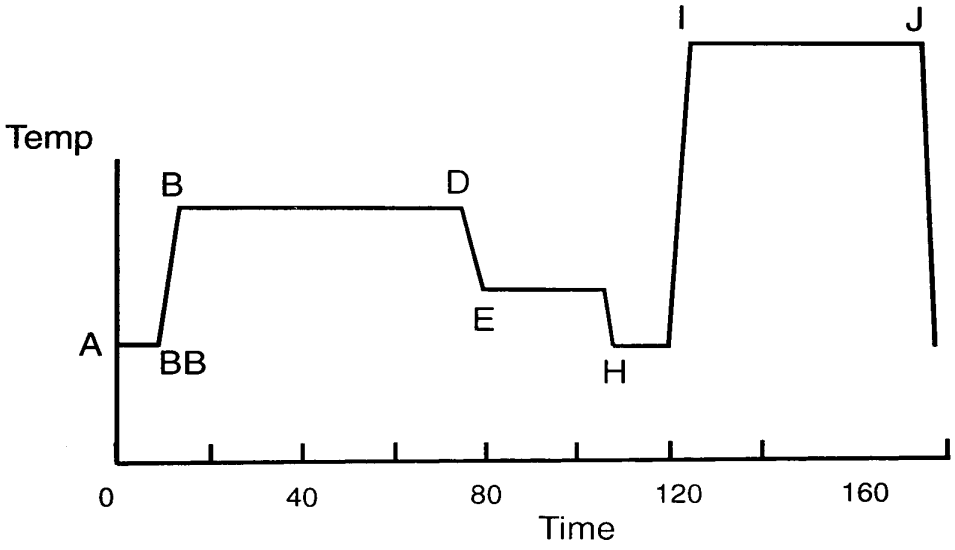


Fig. 9





A. SF_6 native oxide "breakthrough"
B. Cl_2 plasma is ignited
C. WSi_x begins to clear (endpoint)
D. Polysilicon is exposed
E. Polysilicon cleared to oxide
H. Plasma extinguished and O2 feed gas flow is started
I. O_2 plasma is started
J O_2 plasma is extinguished.

Fig. 10

SCORE Placeholder Sheet for IFW Content

Application Number: **09151163** Document Date: **01/02/2001**

The presence of this form in the IFW record indicates that the following document type was received in paper and is scanned and stored in the SCORE database.

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Form Revision Date: December 8, 2006

B D

Transmittal Letter

Serial # 09/151,163

Daniel L. Flamm
476 Green View Drive
Walnut Creek, CA 94596-5459
(925) 947-1909

Date: December 24, 2000

I hereby certify that this is being deposited with the United States Postal Service as first class mail in an envelope addressed to:

BOX ISSUE FEE
Assistant Commissioner for Patents
Washington, D.C. 20231

Date: December 24, 2000

By: Daniel L. Flamm
Daniel L. Flamm

BOX ISSUE FEE
ASSISTANT COMMISSIONER FOR PATENTS
Washington, D.C. 20231

Sir:

Transmitted herewith are the following documents:

1) Issue Fee Transmittal (Part B);
2) Letter to Official Draftsperson
3) Formal Drawings (15 sheets);
4) Amended Formal Drawings (Provisional) (3 sheets);
5) Letter to Examiner and Official Draftsperson

Please find enclosed a check for the issue fee in the amount of $605.00.

[X] **Issue Fee** **$ 605.00**

Daniel L. Flamm
Daniel L. Flamm

UNDER SECRETARY OF COMMERCE FOR INTELLECTUAL PROPERTY AND
DIRECTOR OF THE UNITED STATES PATENT AND TRADEMARK OFFICE
WASHINGTON, D.C. 20231

TOWNSEND & TOWNSEND CREW LLP
TWO EMBARCADERO CENTER 8TH FLOOR
SAN FRANCISCO CA 94111

Mail Date: April 04, 2001
Serial Number: 09/151163
Applicant: FLAMM

NOTICE TO PAY BALANCE OF ISSUE FEE

Your issue fee payment filed on 01/02/01 has been received. However, new patent fees went into effect on October 1, 2000. The final rule entitled "Revision of Patent Fees for Fiscal Year 2001" was published in the *Federal Register*/Vol. 65, No. 156/Friday, August 11, 2000 [49193–49199] and in the U.S. Patent and Trademark Office *Official Gazette*, August 29, 2000 [1237 OG 131–138]. As stated in the final rule, "Any fee amount that is paid on or after the effective date of the fee increase will be subject to the new fees then in effect." The Notice of Allowance and Issue Fee Due (Form PTOL-85) that was mailed to you prior to October 1, 2000, stated an issue fee amount that was in effect prior to October 1, 2000. However, inasmuch as your issue fee was paid on or after October 1, 2000, the new issue fee amount was due.

In accordance with 37 CFR 1.317, you are given a time period of **THREE (3) MONTHS** from the mailing date of this notice during which to pay the **BALANCE DUE** indicated below. This three-month time period may not be extended. **If your patent issues before the expiration of the three-month period and if you do not pay the balance due before the expiration of the three-month period, your patent will lapse at the termination of the three-month period.**

TYPE OF ISSUE FEE PAID	Column A ISSUE FEE IN EFFECT AS OF OCT. 1, 2000 large entity / small entity	Column B ISSUE FEE PAID	BALANCE DUE [Col. A minus Col. B]
UTILITY	$1,240.00 / $620.00	$ 605.00	$ 15.00
DESIGN	$440.00 / $220.00	$	$
PLANT	$600.00 / $300.00	$	$

K Laing
Office of Patent Publication
Tel: 703-305-8263

You MUST return a copy of this Notice with your payment.

CERTIFICATE OF MAILING

I hereby certify that this notice and the required additional fee are being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to Box ISSUE FEE, Commissioner for Patents, Washington, D.C. 20231 on the date indicated below.

Printed Name: _____ Signature: _____

Date: _____

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	Examiner: Examiner: L. Scheiner
Daniel L. Flamm	Art Unit: 1648
Serial No.: 09/151,163	Batch No.: S80
Filed: September 10, 1998	LETTER TO EXAMINER AND OFFICIAL DRAFTSPERSON
For: MULTI-TEMPERATURE PROCESSING	

Assistant Commissioner of Patents
Washington, D.C. 20231

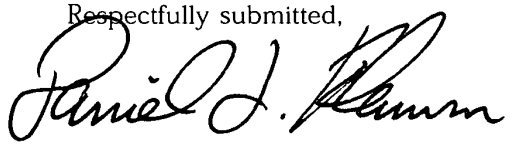
Date: December 23, 2000

Dear Examiner Scheiner and DRAFTSPERSON:

In preparing the formal drawings and reviewing various materials prior to submission for Issue, I found some typographical errors in the Specification and several of the Informal Drawings. I attempted to contact Examiner Scheiner to expedite processing of the enclosed **AMENDMENT AFTER ALLOWANCE UNDER 37 CFR/1.312(a)** , to thereby minimize any inconvenience. However I learned that many staff, including those in Examiner Scheiner's unit are on leave for the holidays.

Using an abundance of caution, I am submitting Formal Drawings which correspond to the Informal Drawings which were in the Application before Examiner Scheiner. However, I am also submitting three Formal Drawings with the corrections submitted in the enclosed **AMENDMENT AFTER ALLOWANCE UNDER 37 CFR/1.312(a)**. It is my hope that Examiner Scheiner may approve the Amendment and that the corrected formalities will be able to be admitted in the published patent.

Respectfully submitted,



Daniel L. Flamm

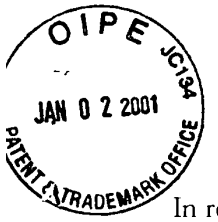
476 Green View Drive
Walnut Creek, California 94596-5459
Tel: (925) 947-1909
Fax: (925) 937-2754

#11.
MR

I hereby certify that this correspondence is deposited with the United States Postal Service as first class mail in an envelope addressed to: Box Issue Fee Assistant Commissioner of Patents and Trademarks Washington, D.C. 20231 on December 24 2000

By Daniel L. Flamm

COPY



PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	
Daniel L. Flamm	Examiner: Examiner: L. Scheiner
Serial No.: 09/151,163	Art Unit: 1648
Filed: September 10, 1998	Batch No.: S80
For: MULTITEMPERATURE PROCESSING	LETTER TO OFFICIAL DRAFTSPERSON

Assistant Commissioner of Patents
Washington, D.C. 20231

Sir:

Pursuant to the Notice of Allowability dated September 29, 2000, applicant submits fifteen sheets of formal drawings to be made of record in the above-identified case.

Exercising an abundance of caution, Applicant encloses two alternative sets of formal drawings for Figs. 7, 8, and 10, consisting three sheets each. A First Set, which conforms to the existing Allowance from Examiner Scheiner, contains typographical errors identically present in the original informal drawings. These errors are corrected in the Second Set of formal drawings for Figs. 7, 8 and 10, and these three corrected drawings are provisionally enclosed. Please note that the second set has not yet been reviewed by Examiner Scheiner; hence the first set with typographical errors is formally submitted to be of record at this time. Applicant respectfully hopes that Examiner Scheiner will find that the Second Set is allowable and can be admitted in place of the first set.

Applicant is concurrently submitting an AMENDMENT AFTER ALLOWANCE UNDER 37 CFR § 1.312(a) to Examiner Scheiner in which Applicant respectfully requests that these corrections be allowed. The Applicant wishes to apologize for any inconvenience. Applicant attempted to contact and fax this material to Examiner Scheiner for consideration in advance of the due date, however Examiner Scheiner and colleagues were understandably on holiday vacation and will not return until after the due date of December 26.

Respectfully submitted,

Daniel L. Flamm

476 Green View Drive
Walnut Creek, California 94596-5459
(925) 947-1909

9/00

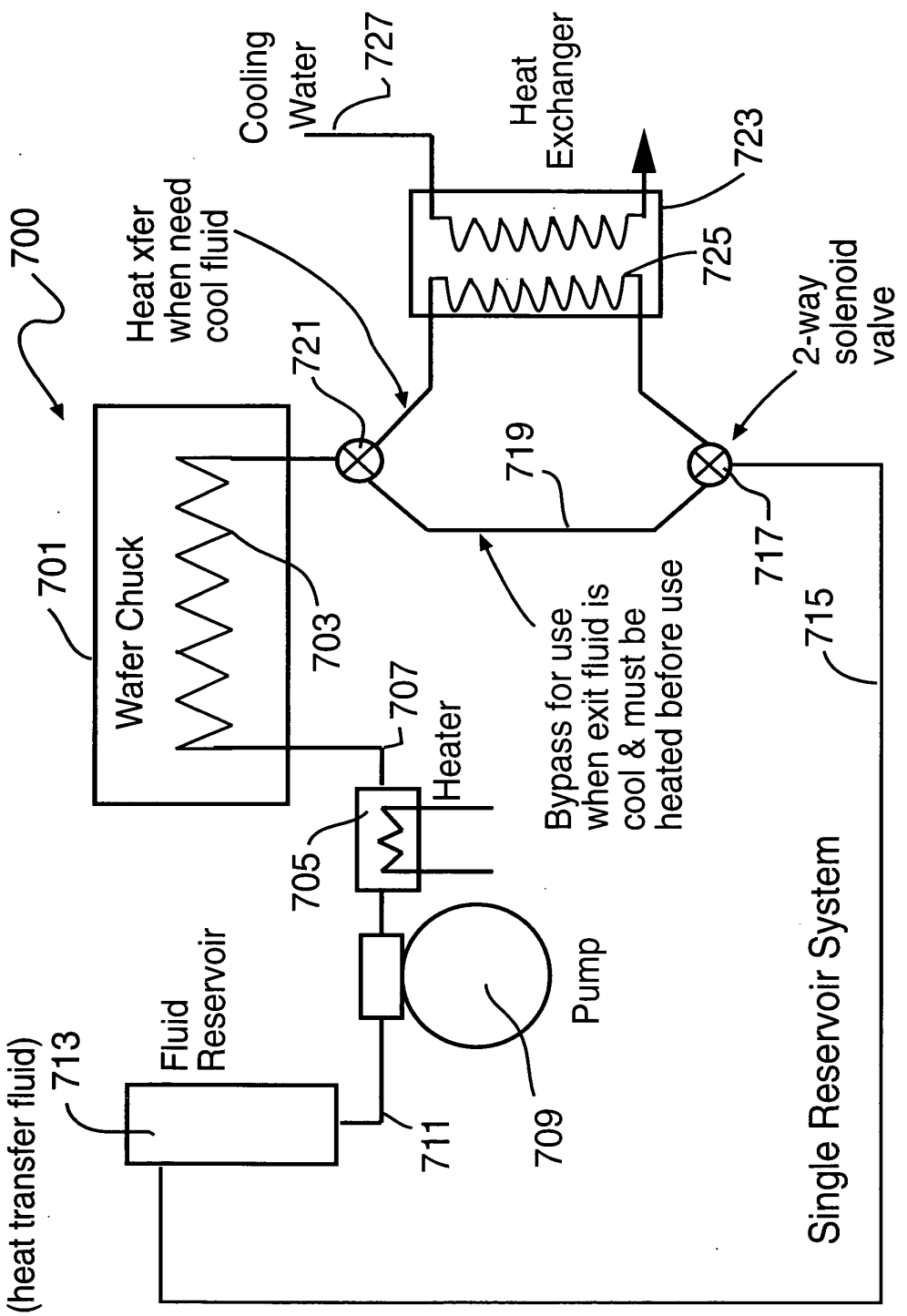

700
Heat xfer when need cool fluid
Cooling Water
727
Heat Exchanger
723
725
721
2-way solenoid valve
719
701
Wafer Chuck
703
707
Heater
705
Bypass for use when exit fluid is cool & must be heated before use
717
715
Single Reservoir System
Fluid Reservoir
(heat transfer fluid)
713
711
709
Pump

Fig. 7

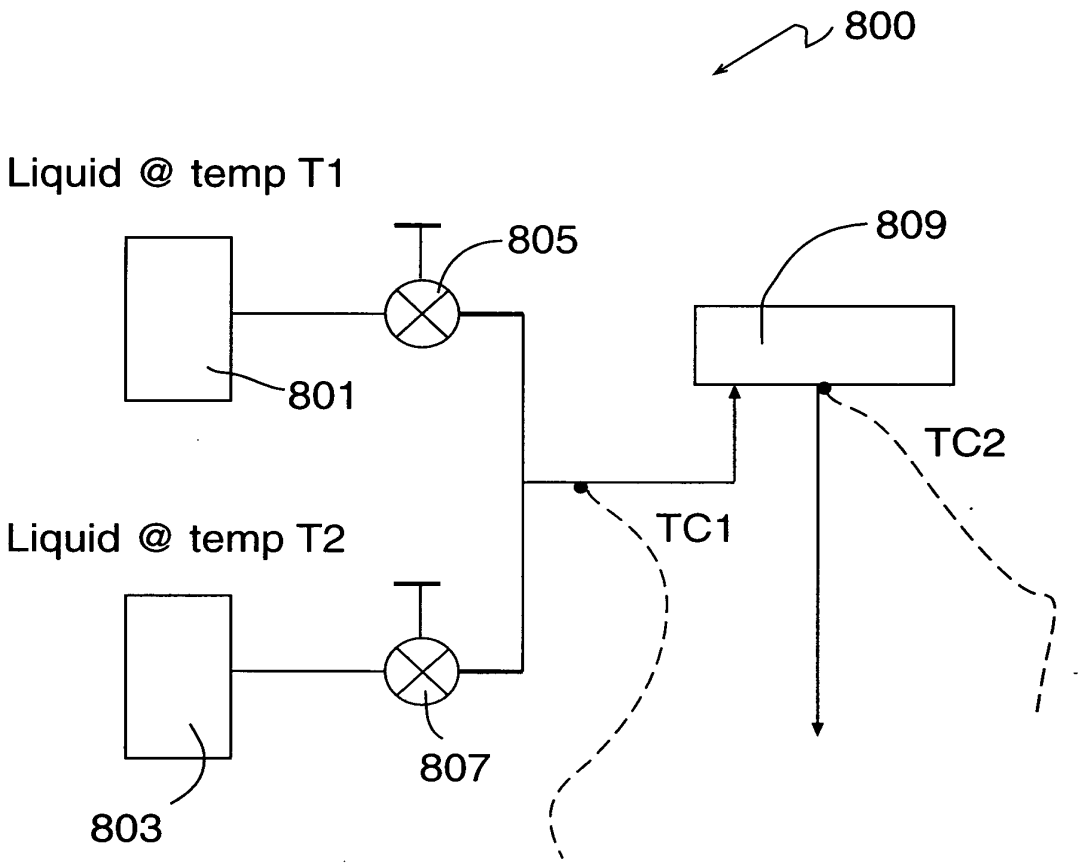
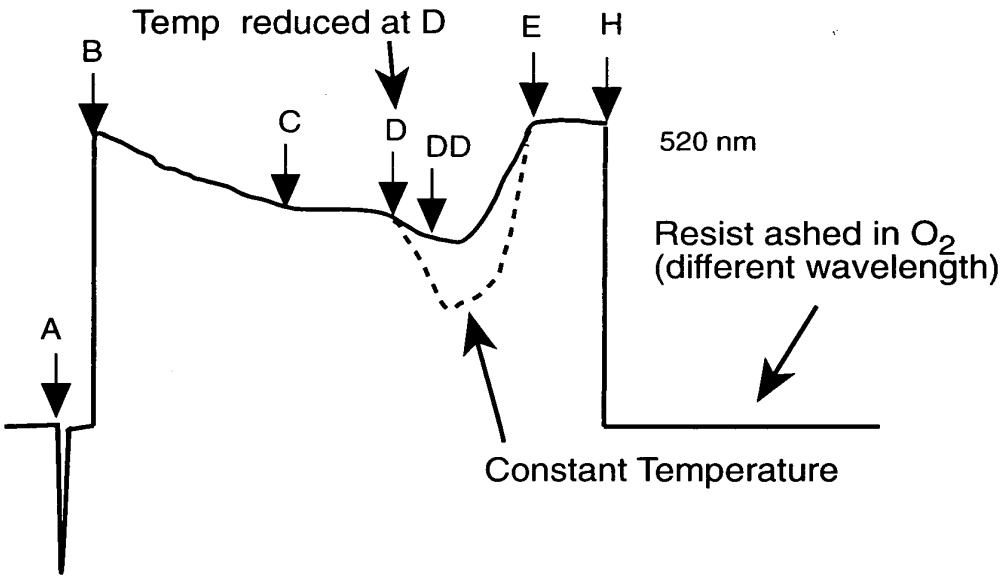
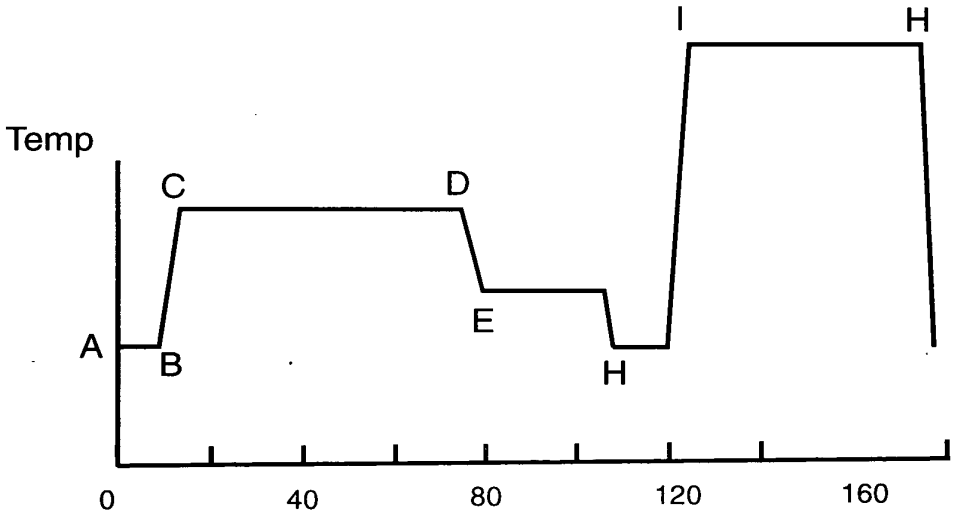


Fig. 8





A. SF_6 native oxide "breakthrough"
B. Cl_2 plasma is ignited
C. WSi_x begins to clear (endpoint)
D. Polysilicon is exposed
E. Polysilicon cleared to oxide
H. Plasma extinguished and O2 feed gas flow is started
I. O_2 plasma is started
J O_2 plasma is extinguished.

Fig. 10

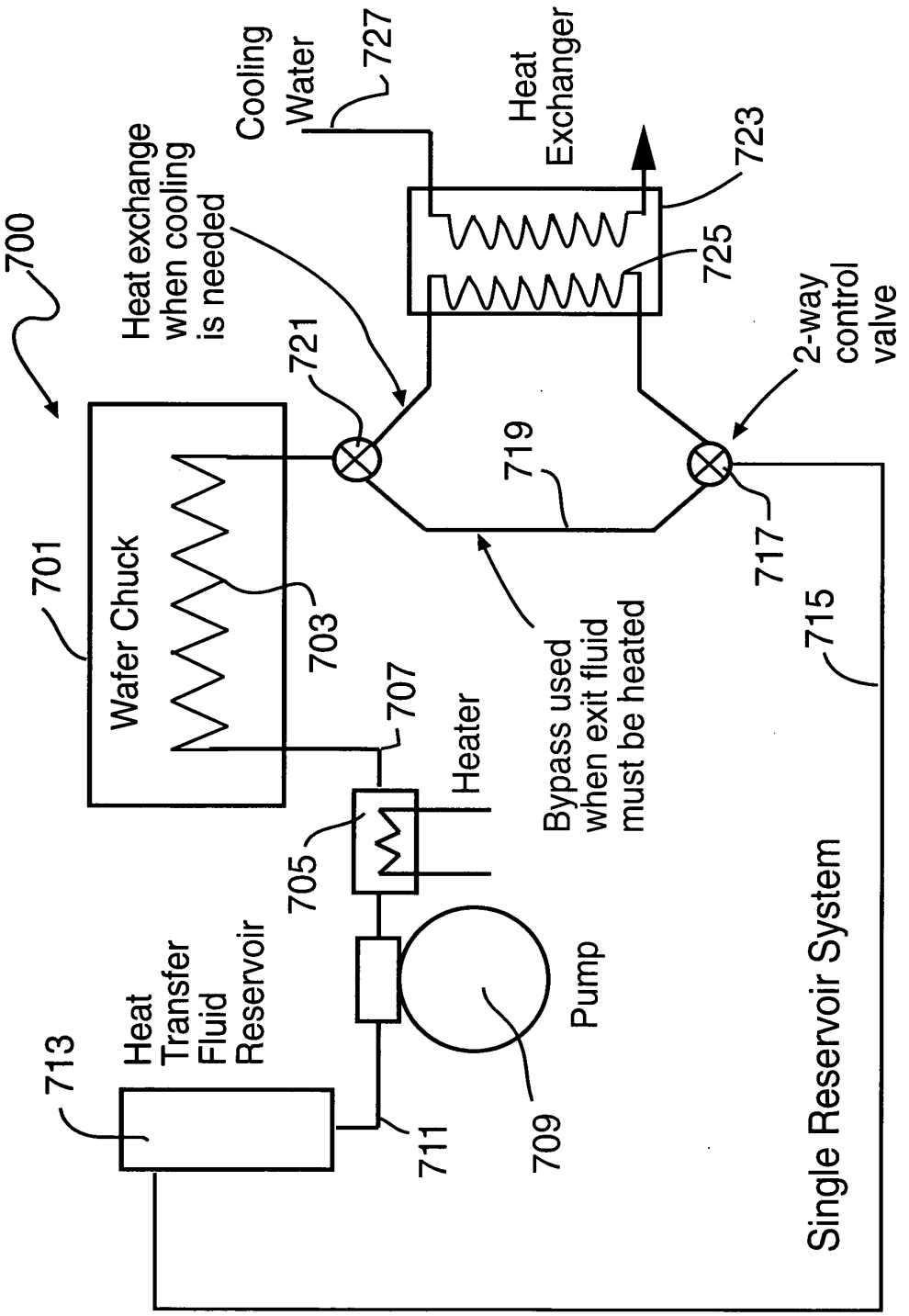

700
Heat exchange when cooling is needed
Cooling Water
727
Heat Exchanger
723
725
2-way control valve
721
719
701
Wafer Chuck
703
707
Heater
705
Bypass used when exit fluid must be heated
717
715
713
Heat Transfer Fluid Reservoir
711
709
Pump
Single Reservoir System

Fig. 7

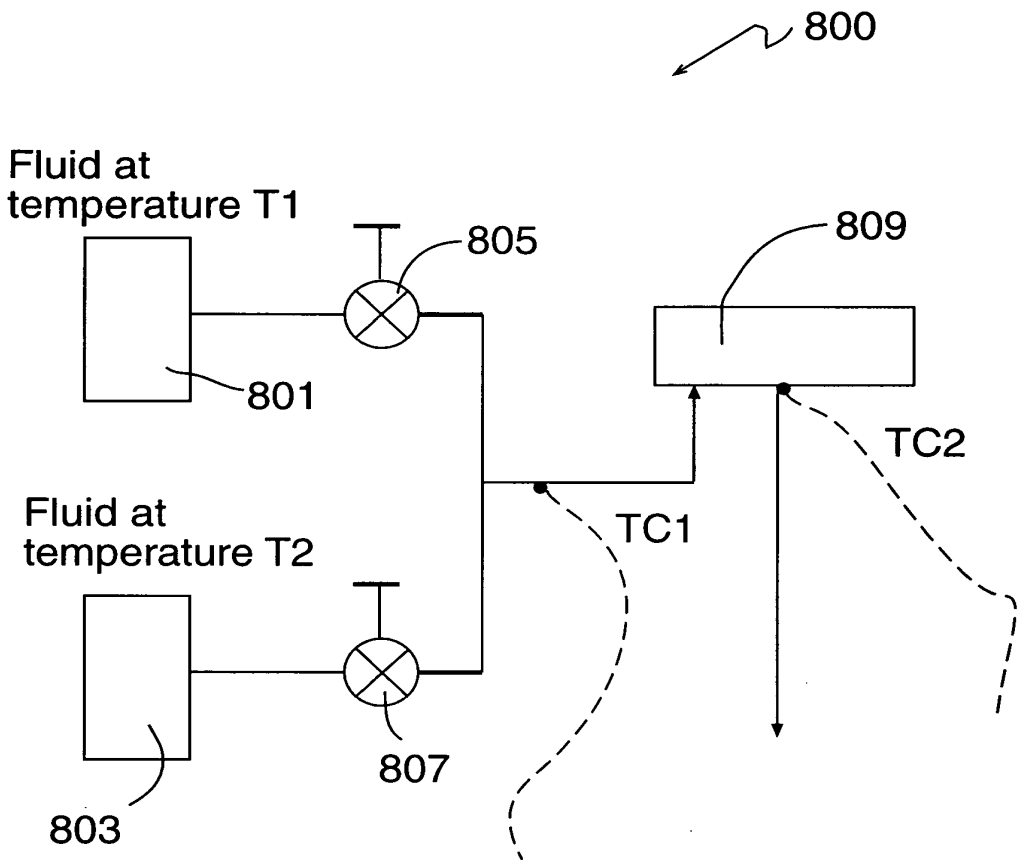
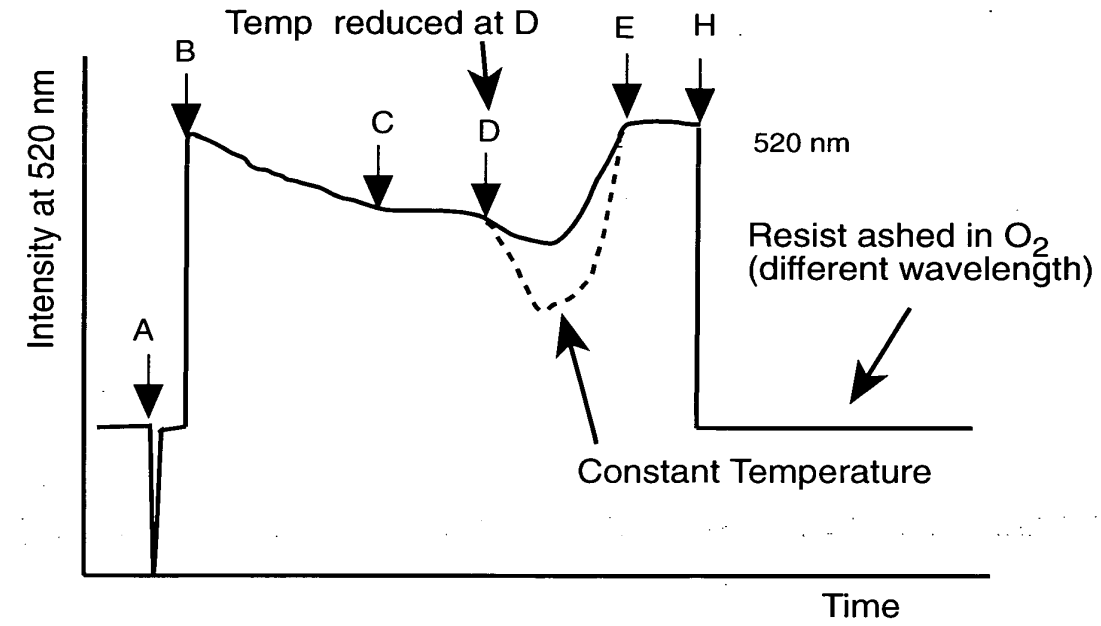
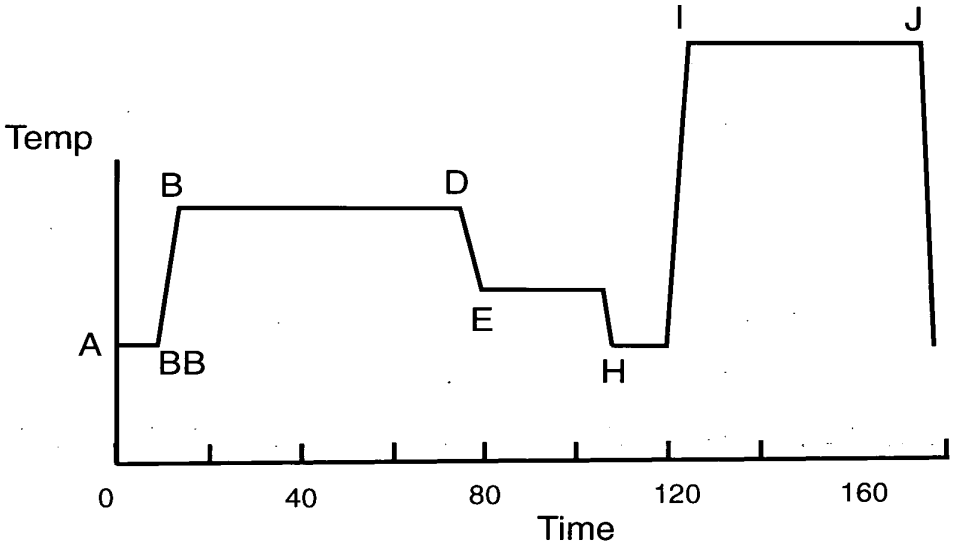

800
Fluid at temperature T1
805
809
801
TC2
Fluid at temperature T2
TC1
807
803

Fig. 8





A. SF_6 native oxide "breakthrough"
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E. Polysilicon cleared to oxide
H. Plasma extinguished and O2 feed gas flow is started
I. O_2 plasma is started
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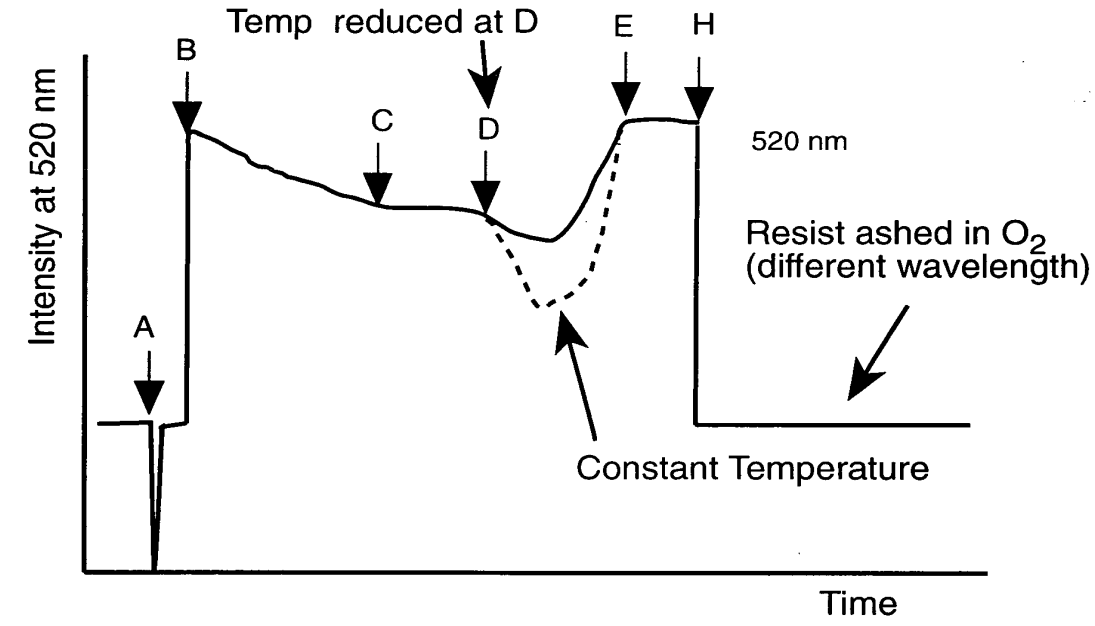
Fig. 10



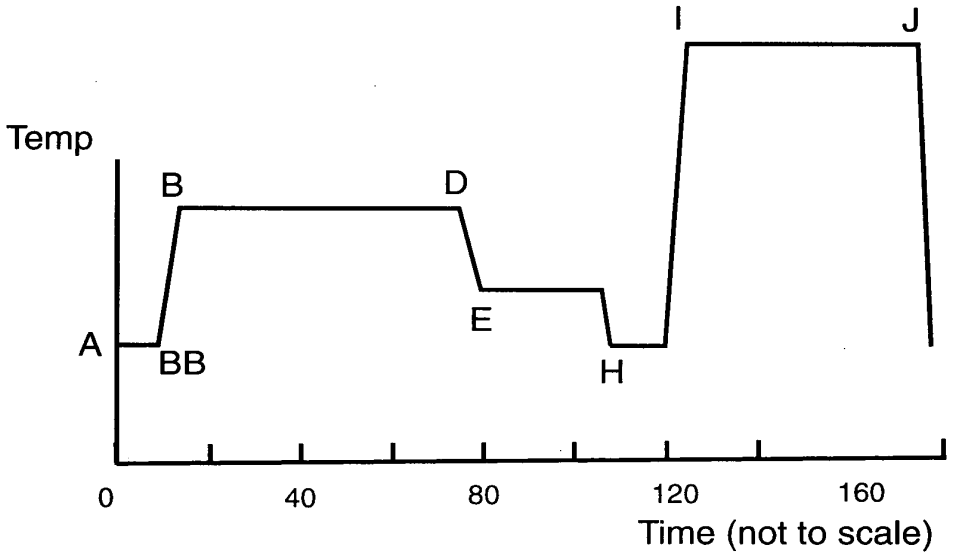


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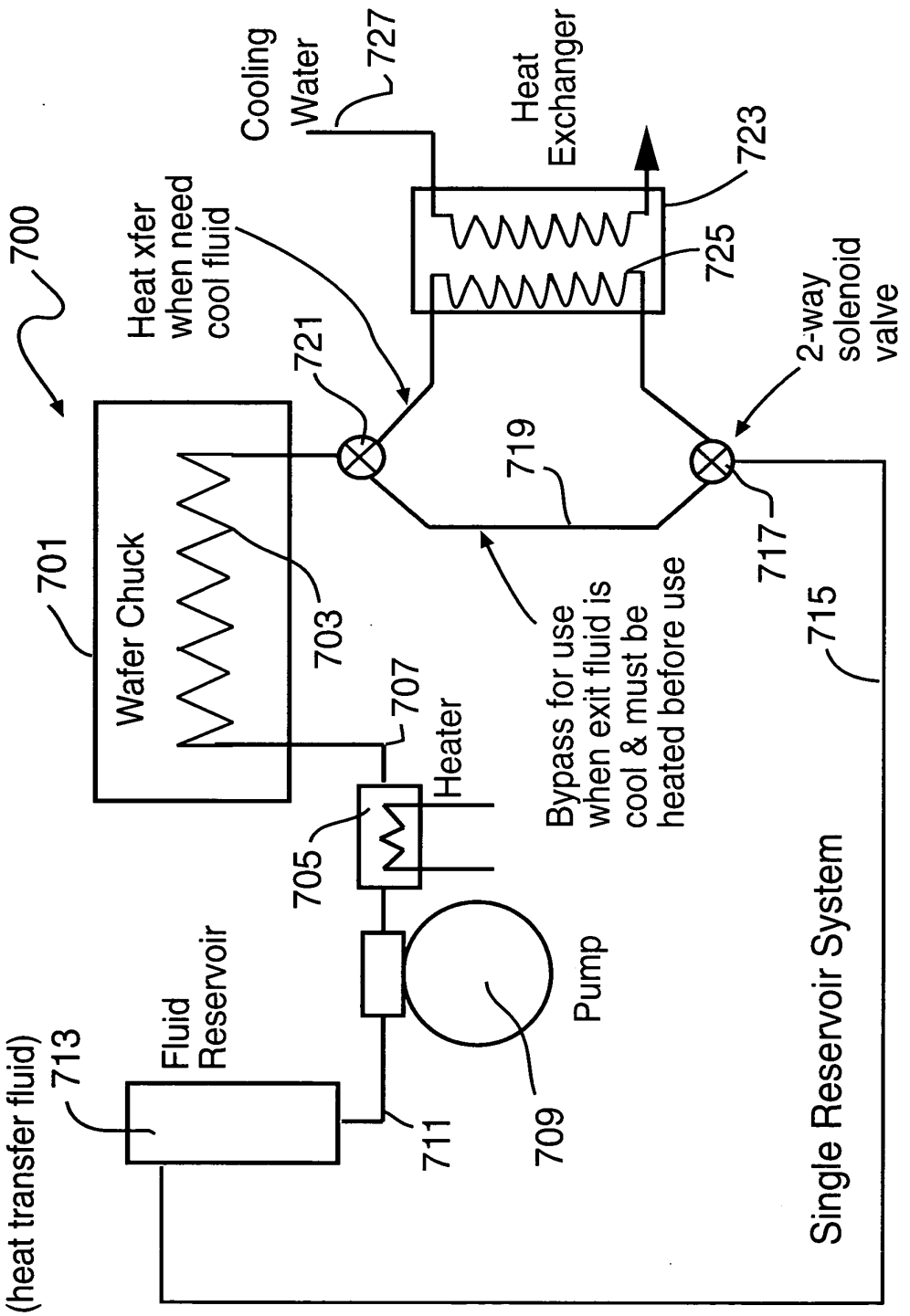
Fig. 10


700
Heat xfer when need cool fluid
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727
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2-way solenoid valve
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Fluid Reservoir
Pump
(heat transfer fluid)
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Single Reservoir System

Fig. 7

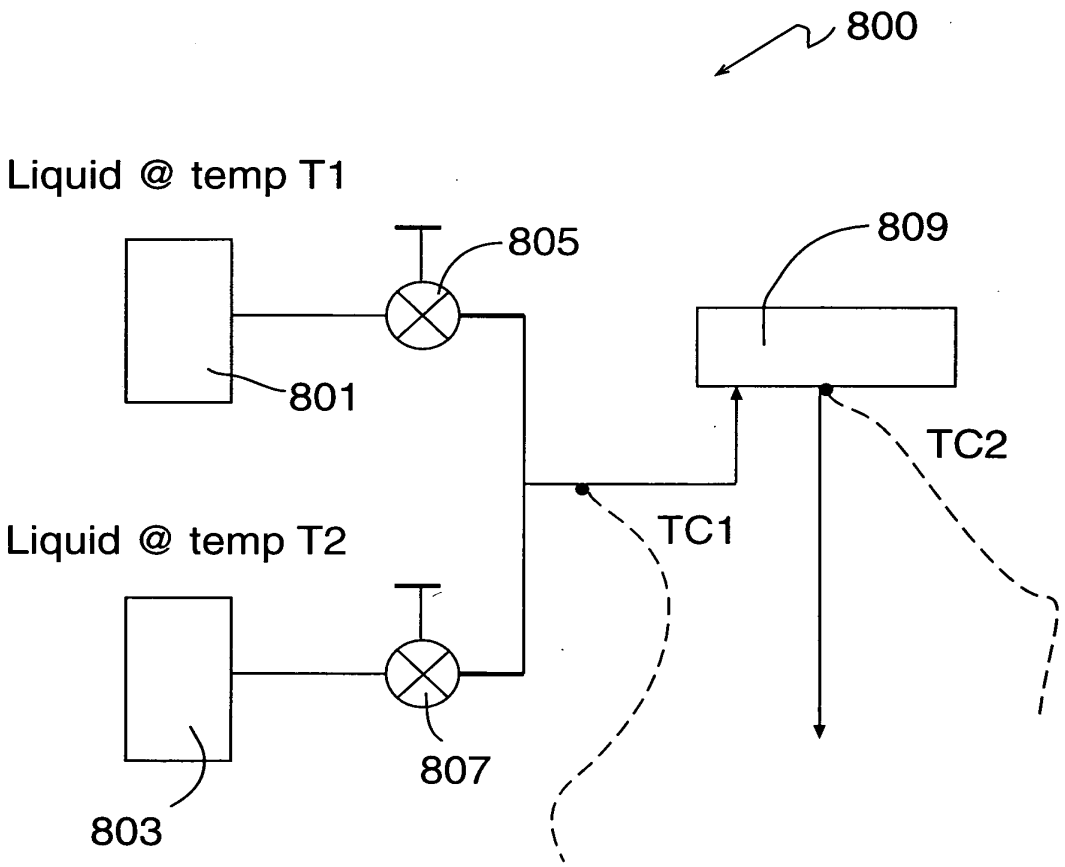
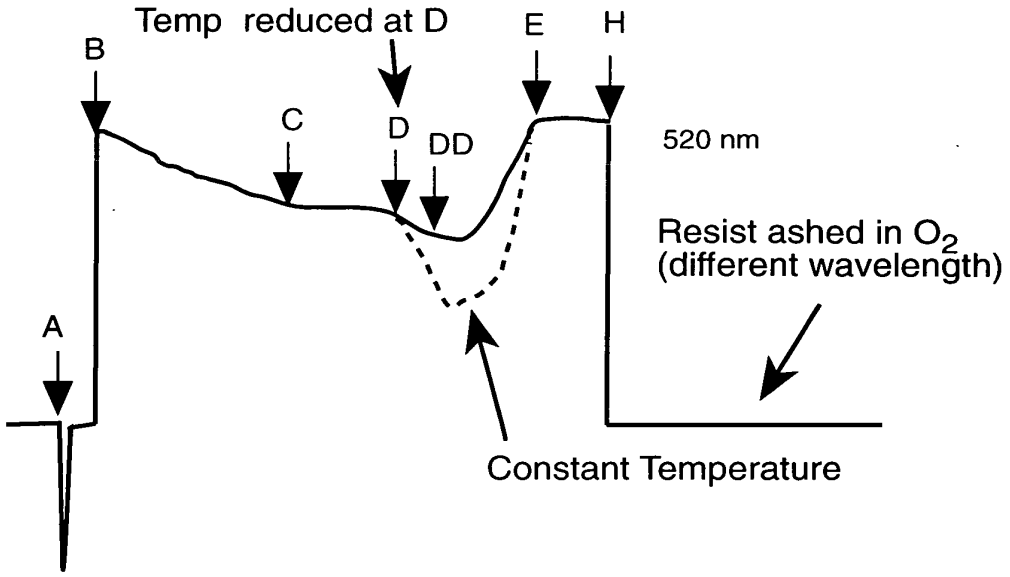
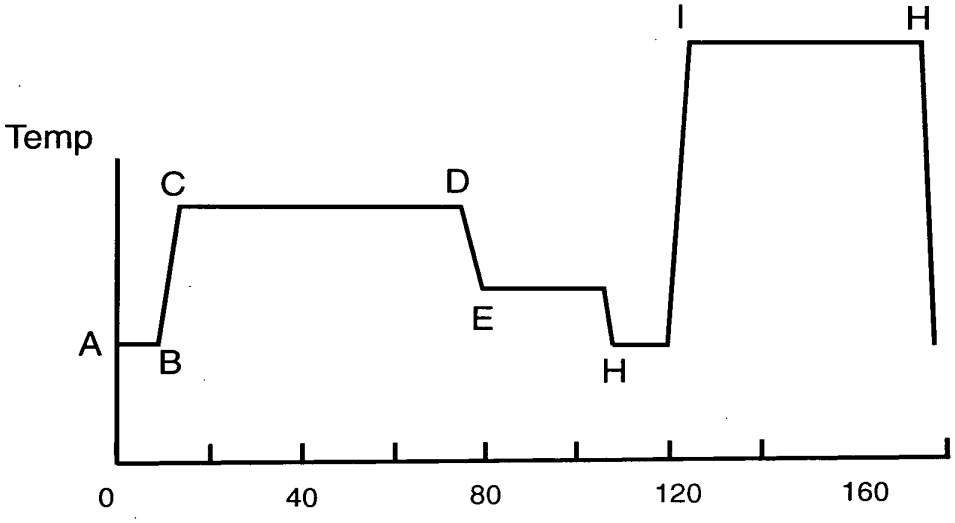


Fig. 8





A. SF_6 native oxide "breakthrough"
B. Cl_2 plasma is ignited
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H. Plasma extinguished and O2 feed gas flow is started
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Fig. 10

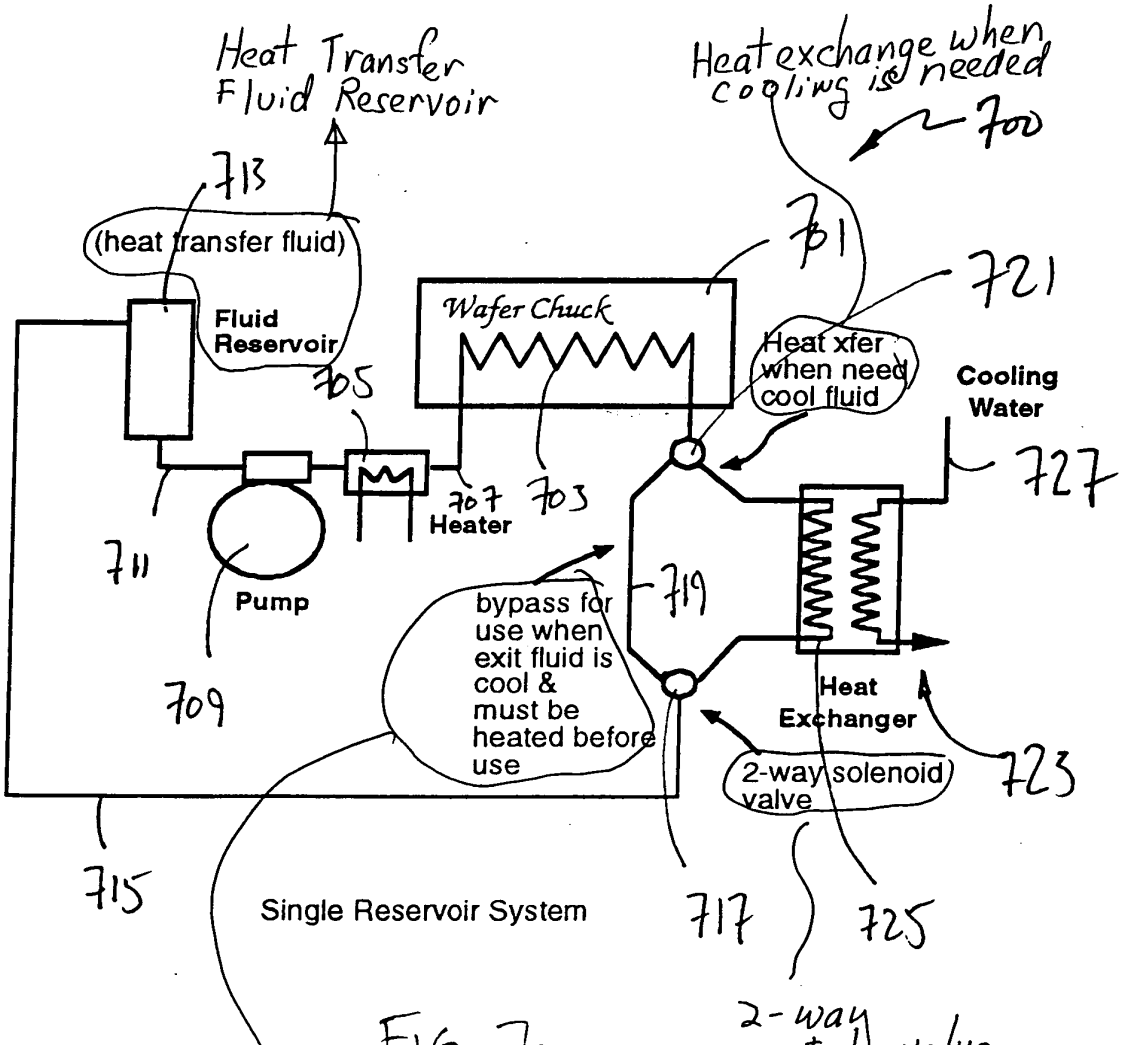

Heat Transfer Fluid Reservoir
Heat exchange when cooling is needed
700
713
(heat transfer fluid)
Fluid Reservoir
705
701
721
Wafer Chuck
Heat xfer when need cool fluid
Cooling Water
727
707
Heater
703
711
Pump
719
bypass for use when exit fluid is cool & must be heated before use
709
Heat Exchanger
723
2-way solenoid valve
715
Single Reservoir System
717
725
2-way control valve
Bypass used when exit fluid must be heated

FIG. 7

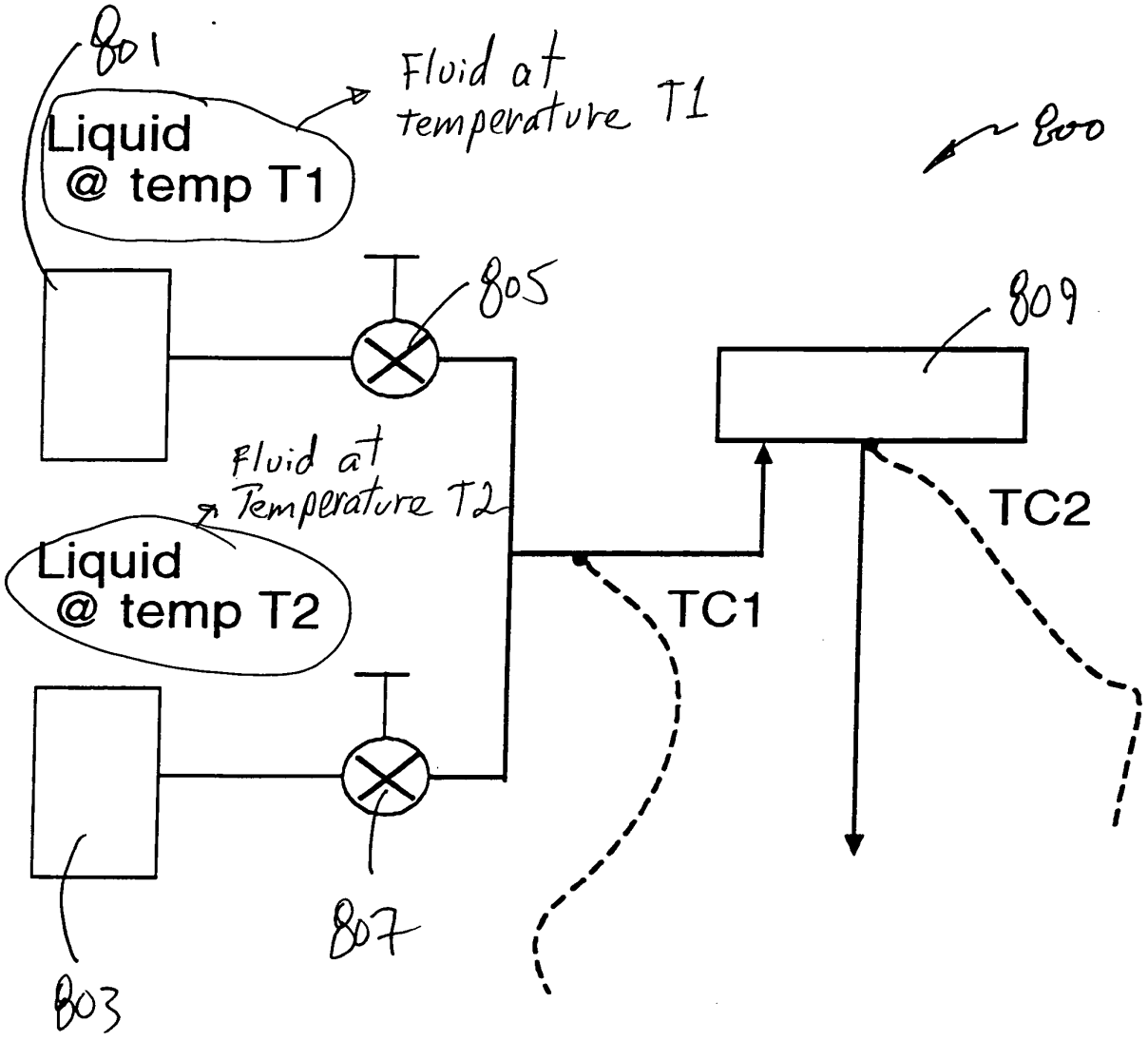

801
Fluid at temperature T1
Liquid @ temp T1
800
805
809
Fluid at Temperature T2
Liquid @ temp T2
TC2
TC1
807
803

Fig. 8

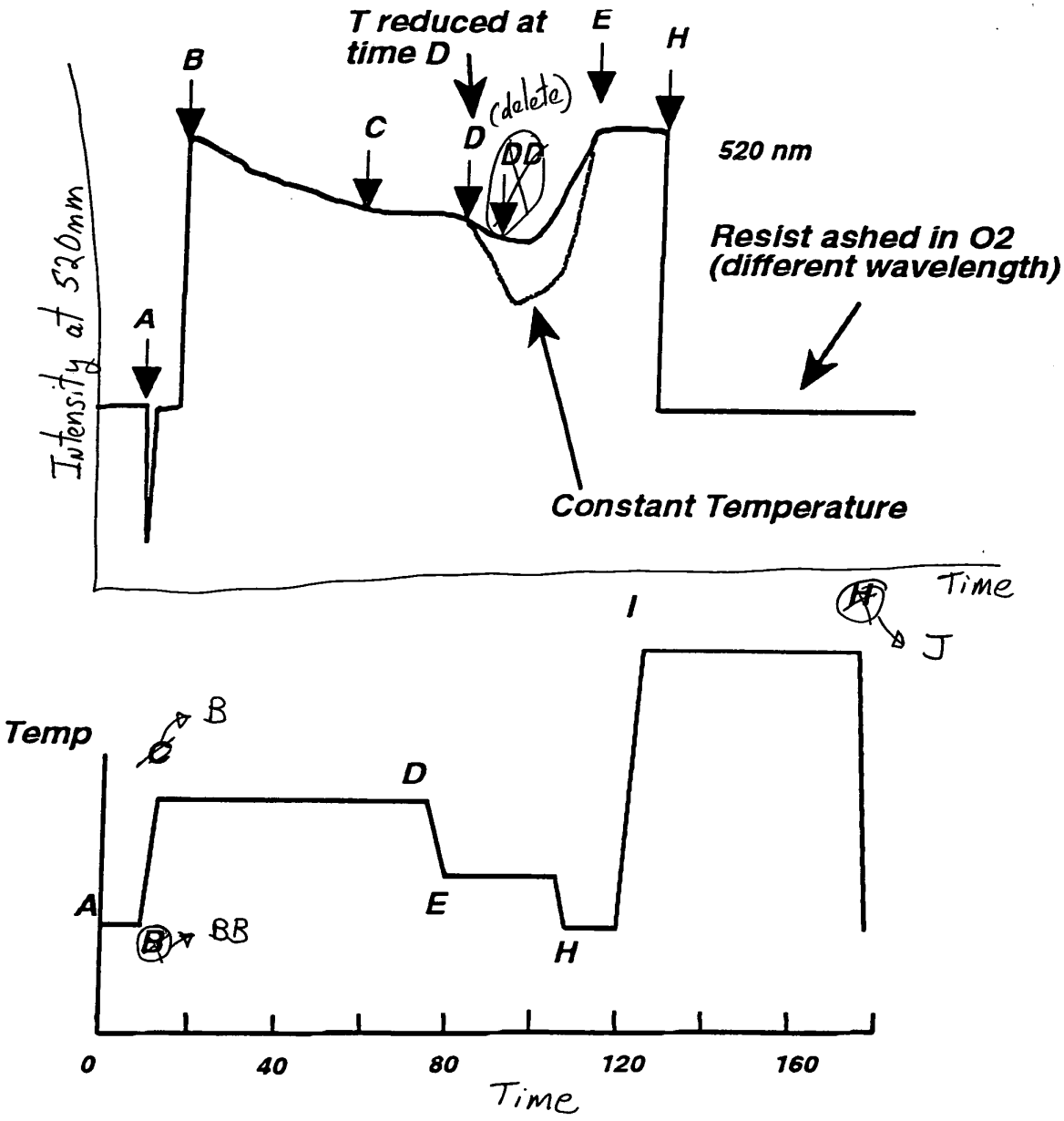


FIG. 10

A. SF_6 native oxide "breakthrough"
B. Cl_2 plasma is ignited
C. WSi_x begins to clear (endpoint)
D. Polysilicon is exposed
E. Polysilicon cleared to oxide
H. Plasma extinguished and O2 feed gas flow is started
I. O2 plasma is started
J O2 plasma is extinguished.

UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office

NOTICE OF ALLOWANCE AND ISSUE FEE DUE

020350 HM12/0926
TOWNSEND AND TOWNSEND AND CREW LLP
TWO EMBARCADERO CENTER
EIGHTH FLOOR
SAN FRANCISCO CA 94111

APPLICATION NO.	FILING DATE	TOTAL CLAIMS	EXAMINER AND GROUP ART UNIT		DATE MAILED
09/151,163	09/10/98	012	SCHEINER, L	1648	09/26/00

First Named Applicant	FLAMM,	35 USC 154(b) term ext. =	0 Days.

TITLE OF INVENTION: MULTI-TEMPERATURE PROCESSING

ATTY'S DOCKET NO.	CLASS-SUBCLASS	BATCH NO.	APPLN. TYPE	SMALL ENTITY	FEE DUE	DATE DUE
1 16655-000810	216-068.000	580	UTILITY	YES	$605.00	12/26/00

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED.

THE ISSUE FEE MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED.

HOW TO RESPOND TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.
If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is changed, pay twice the amount of the FEE DUE shown above and notify the Patent and Trademark Office of the change in status, or
B. If the status is the same, pay the FEE DUE shown above.

If the SMALL ENTITY is shown as NO:

A. Pay FEE DUE shown above, or

B. File verified statement of Small Entity Status before, or with, payment of 1/2 the FEE DUE shown above.

II. Part B-Issue Fee Transmittal should be completed and returned to the Patent and Trademark Office (PTO) with your ISSUE FEE. Even if the ISSUE FEE has already been paid by charge to deposit account, Part B Issue Fee Transmittal should be completed and returned. If you are charging the ISSUE FEE to your deposit account, section "4b" of Part B-Issue Fee Transmittal should be completed and an extra copy of the form should be submitted.

III. All communications regarding this application must give application number and batch number.
Please direct all communications prior to issuance to Box ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PATENT AND TRADEMARK OFFICE COPY

UNITED STAT. DEPARTMENT OF COMMERCE
Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

APPLICATION NUMBER	FILING DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NO.
09/151,163	09/10/98	FLAMM	D 16655-0008:

020350
TOWNSEND AND TOWNSEND AND CREW LLP
TWO EMBARCADERO CENTER
EIGHTH FLOOR
SAN FRANCISCO CA 94111

HM12/0926

EXAMINER	
SCHEINER L	
ART UNIT	**PAPER NUMBER**
1648	8

DATE MAILED: 09/26/00

This is a communication from the examiner in charge of your application.
COMMISSIONER OF PATENTS AND TRADEMARKS

NOTICE OF ALLOWABILITY

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance and Issue Fee Due or other appropriate communication will be mailed in due course.

☒ This communication is responsive to 9/11/00.

☐ The allowed claim(s) is/are 1-12.

☐ The drawings filed on _____ are acceptable.

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number) _____.

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____.

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

A SHORTENED STATUTORY PERIOD FOR RESPONSE to comply with the requirements noted below is set to EXPIRE **THREE MONTHS** FROM THE "DATE MAILED" of this Office action. Failure to timely comply will result in ABANDONMENT of this application. Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

☐ Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL APPLICATION, PTO-152, which discloses that the oath or declaration is deficient. A SUBSTITUTE OATH OR DECLARATION IS REQUIRED.

☒ Applicant MUST submit NEW FORMAL DRAWINGS

☒ because the originally filed drawings were declared by applicant to be informal.

☐ including changes required by the Notice of Draftperson's Patent Drawing Review, PTO-948, attached hereto or to Paper No. _____.

☐ including changes required by the proposed drawing correction filed on _____, which has been approved by the examiner.

☐ including changes required by the attached Examiner's Amendment/Comment.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the reverse side of the drawings. The drawings should be filed as a separate paper with a transmittal letter addressed to the Official Draftperson.

☐ Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Any response to this letter should include, in the upper right hand corner, the APPLICATION NUMBER (SERIES CODE/SERIAL NUMBER). If applicant has received a Notice of Allowance and Issue Fee Due, the ISSUE BATCH NUMBER and DATE of the NOTICE OF ALLOWANCE should also be included.

Attachment(s)

☐ Notice of References Cited, PTO-892

☐ Information Disclosure Statement(s), PTO-1449, Paper No(s). _____

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

☐ Interview Summary, PTO-413

☒ Examiner's Amendment/Comment

☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material

☐ [illegible]'s Statement of Reasons for Allowance

LAURIE SCHEINER
PRIMARY EXAMINER

PTOL-37 (Rev. 10/99)

#8(a)
9/25/00

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Please cancel claims 13-20 without prejudice.

Authorization for this examiner's amendment was given in a telephone interview with Daniel Flamm on September 21, 2000.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Laurie Scheiner, whose telephone number is (703) 308-1122. Any inquiry of a general nature or relating to the status of this application should be directed to the Group 1600 receptionist whose telephone number is (703) 308-0196.

Correspondence related to this application may be submitted to Group 1600 by facsimile transmission. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (November 15, 1989). Official communications should be directed toward one of the following Group 1600 fax numbers: (703) 308-4242 or (703) 305-3014. Informal communications may be submitted directly to the Examiner through the following fax number: (703) 308-4426. Applicants are encouraged to notify the Examiner prior to the submission of such documents to facilitate their expeditious processing and entry.

LAS

Laurie Scheiner/LAS
September 22, 2000

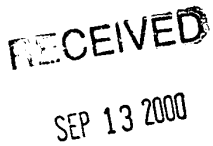
LAURIE SCHEINER
PRIMARY EXAMINER

VALID

Pat. No. 05325146 - 8 Group ID: G Page 1
Issue Date: 11/13/00 User ID: Sjmccoa KS: 402

Warning [Pages Of Foreign References:]
has no references
Warning [Pages Of Other References:]
has no references

Error



GAU 1641

Amendment Transmittal Sheet

Attorney Docket No.: 16655-000810

Date: September 5, 2000

I hereby certify that this is being deposited with the United States Postal Service as first class mail in an envelope addressed to:

Assistant Commissioner for Patents
Washington, D.C. 20231

Date: September 5, 2000

Signed: Daniel J. Hamm

In re application of: Daniel C. Hamm et al.
Application No.: 09/151,163
Filed: September 10, 1998
Group Art Unit: 1641
For: Multi-Temperature Processing

TECH CENTER 1600/2900

THE ASSISTANT COMMISSIONER FOR PATENTS
Washington, D.C. 20231

Sir:

Transmitted herewith is an amendment in the above-identified application.

[X] Small entity status of this application under 37 C.F.R. 1.9 and 1.27 has been established by a verified statement previously submitted.

If any extension of time is needed, then this response should be considered a petition therefor.

The filing fee has been calculated as shown below:

	(Col. 1) CLAIMS REMAINING AFTER AMENDMENT		(Col. 2) HIGHEST NO. PREVIOUSLY PAID FOR	(Col. 3) PRESENT EXTRA
TOTAL	20	MINUS	20	= 0
INDEP.	2	MINUS	2	= 0
[ ] FIRST PRESENTATION OF MULTIPLE DEP. CLAIM				

SMALL ENTITY RATE	SMALL ENTITY ADDIT. FEE	OR	OTHER THAN SMALL ENTITY RATE	OTHER THAN SMALL ENTITY ADDIT. FEE
x $9.00 =	$0		x $18.00 =	$
x $39.00 =	$0		x $78.00 =	$
+ $130.00 =	$0		+ $260.00 =	$
	$0			$
TOTAL ADDIT. FEE	$0	OR	TOTAL	$

* If the entry in Col. 1 is less than the entry in Col. 2, write 0 in Col. 3.

** If the Highest Number Previously Paid For IN THIS SPACE is less than 20, write 20 in this space.

*** If the Highest Number Previously Paid For IN THIS SPACE is less than 3, then write 3 in this space. The Highest Number Previously Paid For (Total or Independent) is the highest number found from the equivalent box in Col. 1 of a prior amendment or the number of claims originally filed.

[X] No fee is due.

Please accept the attached check.

[ ] Claims fee $0

[X] Any additional fees associated with this paper or during the pendency of this application.

PA 172268 v2

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231,
on Sept. 5, 2000

By Daniel L. Flamm

#7 9/18/00

PATENT
Attorney Docket No. 16655-000810

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	
Daniel L. Flamm	Examiner: Scheiner, L.
Application No.: 09/151,163	Art Unit: 1641
Filed: September 10, 1998	AMENDMENT UNDER 37 CFR 1.116
For: Multi-Temperature Processing	

Assistant Commissioner for Patents
Washington, D.C. 20231

Dear Examiner:

In response to the Office Action mailed June 5, 2000, reconsideration and reexamination are respectfully requested in view of these remarks. For the convenience of the Examiner, all pending claims are attached hereto as an Appendix.

REMARKS

Applicant would like to thank Examiner Scheiner for her time in reviewing the present application.

Claims 1-20 are now pending in this application.

Please note that the firm of Townsend and Townsend and Crew, LLP is not representing the Applicant in this response. The Applicant is therefore prosecuting this application pro se. Applicant has no formal training in patent prosecution and is inexperienced in formal maters pertaining to the format thereof. Applicant therefore respectfully requests examiner's assistance and suggestions regarding form of this response and the format of any beneficial modifications to put the form of this invention and claims in conformance with patent office rules and standards.

Applicant does not understand that the scope of the claims should be restricted in a manner to withdraw claims 13-20. If, upon reconsideration, the Examiner, nevertheless, maintains that this restriction is required to meet patent regulations, Applicant requests Examiner's guidance and assistance toward modifying the inventive subject claims 13-20 in a manner that the claimed substance is preserved and set forth in accordance with said regulations.

With respect to Claims 1-12, the Applicant has reviewed U.S. Patent 5,770,099 cited by the Examiner. Applicant observes that the '099 appears to teach temperature of an interior wall which scavenges an etching species. It is noted that the '099 also suggests an interior wall be maintained above a characteristic deposition temperature and that the temperature of said wall (Fig. 1, Fig. 4) may vary in an uncontrolled manner during the processing of substrates (Col. 2, lines 18-32). The '099 makes reference to side walls which change temperature. Applicant recognizes that this terminology can be confusing since the term "side wall" is often used to denote the generally vertical face of a feature which is being etched into a film on a workpiece. However, the Applicant respectfully points out that the '099 uses the term "side wall" to make reference to a (quartz) wall of a plasma processing chamber that has no contact with the workpiece. Furthermore, the '099 makes reference to a polymer film which is comprised of species formed from a gas which is introduced into a plasma etch reactor. On the contrary, the Applicant's invention refers to a film which is introduced into a chamber on a workpiece. The Applicant's invention claims *placing a substrate having a film thereon* on a substrate holder in a chamber and etching a first portion *of said film* at a first temperature and performing a second etching of said film at a second temperature , among other elements.

Applicant respectfully observes that the '099 teaches maintaining temperature of an interior wall (quartz or other materials) of a plasma etching chamber for the purpose of controlling the condensation of a polymer which is comprised or plasma species. The Applicant

respectfully notes that the '099 does not teach a temperature *of the workpiece* nor does it teach performing a first etching of a first portion of said film (e.g. thereon a substrate which is placed in a chamber) at a first temperature in combination with performing a second etching of a second portion of said film at a second temperature, in the manner claimed. Applicant respectfully observes that conventional practice is to maintain the temperature of a substrate workpiece at a desired temperature during processing. This is often achieved at least in part by coupling heating and/or cooling means embedded in a chuck which supports the workpiece (e.g. the cathode assembly referred to in Col. 3, lines 45-47 of the '099) in combination with workpiece and/or chuck temperature sensing and controlling means . A workpiece is conventionally maintained in close thermal contact with a chuck supporting surface by means such as an electrostatic chuck or a pressure of backside helium or other gas. In fact the '099 teaches that various parts of a plasma chamber may comprise a plurality of temperatures during etching, while it fails to teach any temperature of the substrate or of the substrate holder in the manner claimed by the present invention. Respectfully, the Applicant also observes that the '099 does not teach thermal characteristics of a substrate holder in the manner claimed by the present invention nor does it teach thermal characteristics of a substrate holder in combination with performing a first etching of a film at a first temperature and performing a second etching of said film at a second substrate temperature, said temperatures being distinct. Accordingly, claims 1-12 are patentable over the 099 patent.

With respect to claims 13-20, the Applicant respectfully asserts that the '099 does not teach a substrate holder which allows for a change from a first temperature to a second temperature within a characteristic time period to process a film as claimed. Accordingly, claims 13-20 are patentable over the '099 patent as well.

CONCLUSION

Therefore, in view of the remarks above, Applicant respectfully requests that the rejection be removed, that claims 1-12 and 13-20 be allowed, and the case passed to issue. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at (925) 947-1909.

Respectfully submitted,

Date: September 5, 2000

Daniel L. Flamm

476 Green View Drive
Walnut Creek, CA 94596-5459
Tel: (925) 947-1909
Fax: (925) 937-2754

APPENDIX

1. A method of etching a substrate in the manufacture of a device, said method comprising steps of:

placing a substrate having a film thereon on a substrate holder in a chamber, said substrate holder having a selected thermal mass; and

performing a first etching of a first portion of said film at a first temperature and performing a second etching of a second portion of said film at a second temperature, said first temperature being different from said second temperature;

wherein said selected thermal mass allows a change from said first temperature to said second temperature within a characteristic time period to process said film.

2. The method of claim 1 wherein said first temperature is changed to said second temperature by a heat transfer means coupled to said substrate holder.

3. The method of claim 1 wherein said change in temperature is an in-situ process during said first etching step and said second etching step.

4. The method of claim 1 wherein said first etching and said second etching are conducted in a substantially constant plasma environment.

5. The method of claim 1 wherein said first temperature is higher than said second temperature.

6. The method of claim 1 wherein said first temperature is lower than said second temperature.

7. The method of claim 1 wherein said first etching comprises radiation.

8. The method of claim 1 wherein said second etching comprises radiation.

9. The method of claim 1 wherein said first etching is an ion bombardment aided process.

10. The method of claim 1 wherein said second etching is an ion bombardment aided process.

11. The method of claim 1 wherein said first portion of said film is etched before said second portion of said film.

12. The method of claim 1 wherein said second portion of said film is etched before said first portion of said film.

13. Apparatus for etching a substrate in the manufacture of a device, said apparatus comprising:

a chamber;

a substrate holder disposed in said chamber, said substrate holder having a selected thermal mass;

wherein said selected thermal mass of said substrate holder allows for a change from a first temperature to a second temperature within a characteristic time period to process a film.

14. Apparatus of claim 13 further comprising a heat transfer means for changing said first temperature to said second temperature, said heat transfer means being coupled to said substrate holder.

15. Apparatus of claim 13 wherein said change in temperature is an in-situ process within said characteristic time.

16. Apparatus of claim 13 wherein said chamber provides a substantially constant plasma environment.

17. Apparatus of claim 13 wherein said first temperature is higher than said second temperature.

18. Apparatus of claim 13 wherein said first temperature is lower than said second temperature.

19. Apparatus of claim 13 wherein said chamber provides radiation.

20. Apparatus of claim 13 wherein said chamber provides an ion bombardment aided process.

UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office
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Washington, D.C. 20231

APPLICATION NUMBER	FILING DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO.
09/151,163	09/10/98	FLAMM D	16655-000810

020350
TOWNSEND AND TOWNSEND AND CREW LLP
TWO EMBARCADERO CENTER
EIGHTH FLOOR
SAN FRANCISCO CA 94111

HM12/0605

EXAMINER	
SCHEINER, L	
ART UNIT	PAPER NUMBER
1641	6

DATE MAILED: 06/05/00

This is a communication from the examiner in charge of your application.
COMMISSIONER OF PATENTS AND TRADEMARKS

OFFICE ACTION SUMMARY

☒ Responsive to communication(s) filed on 3/27/00

☐ This action is FINAL.

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 1935 D.C. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire 3 month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claims

☒ Claim(s) 1-20 is/are pending in the application.
Of the above, claim(s) 13-20 is/are withdrawn from consideration.
☐ Claim(s) _____ is/are allowed.
☒ Claim(s) 1-12 is/are rejected.
☐ Claim(s) _____ is/are objected to.
☐ Claim(s) _____ are subject to restriction or election requirement.

Application Papers

☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.
☐ The drawing(s) filed on _____ is/are objected to by the Examiner.
☐ The proposed drawing correction, filed on _____ is ☐ approved ☐ disapproved.
☐ The specification is objected to by the Examiner.
☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been

☐ received.
☐ received in Application No. (Series Code/Serial Number) _____.
☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____

☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

☒ Notice of Reference Cited, PTO-892
☐ Information Disclosure Statement(s), PTO-1449, Paper No(s). _____
☐ Interview Summary, PTO-413
☐ Notice of Draftperson's Patent Drawing Review, PTO-948
☐ Notice of Informal Patent Application, PTO-152

–SEE OFFICE ACTION ON THE FOLLOWING PAGES–

Applicant's election of Group I (claims 1-12) in Paper No. 5 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

The requirement is still deemed proper and is therefore made FINAL.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

Claims 1-12 are rejected under 35 U.S.C. 102(a) as being anticipated by Rice et al. (U.S. Patent 5,770,099).

Rice et al. teach a method wherein a substrate is etched at a first portion, and a first temperature; while an etch preventing polymer covers the portion of the film to be etched subsequently, at a second temperature. Temperatures vary such that the first temperature may be higher or lower than the second temperature. First or second portions of substrate may be etched first.

Vinogradov et al. (U.S. Patent 5,965,034) is cited as of interest.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Laurie Scheiner, whose telephone number is (703) 308-1122. Any inquiry of a general nature or relating to the status of this application should be directed to the Group 1600 receptionist whose telephone number is (703) 308-0196.

Correspondence related to this application may be submitted to Group 1600 by facsimile transmission. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (November 15, 1989). Official communications should be directed toward

one of the following Group 1600 fax numbers: (703) 308-4242 or (703) 305-3014. Informal communications may be submitted directly to the Examiner through the following fax number: (703) 308-4426. Applicants are encouraged to notify the Examiner prior to the submission of such documents to facilitate their expeditious processing and entry.

Laurie Scheiner/LAS
June 2, 2000

LAURIE SCHEINER
PRIMARY EXAMINER

Notice of References Cited

Application No.	Applicant(s)
09/151,163	
Examiner	**Group Art Unit** / **Page**
	1641 / Page 1 of 1

U.S. PATENT DOCUMENTS

*		DOCUMENT NO.	DATE	NAME	CLASS	SUBCLASS
	A	5,770,099	6/98	Rice et al.	216	68
	B	5,965,034	10/99	Vinogradov et al.	216	68
	C					
	D					
	E					
	F					
	G					
	H					
	I					
	J					
	K					
	L					
	M					

FOREIGN PATENT DOCUMENTS

*		DOCUMENT NO.	DATE	COUNTRY	NAME	CLASS	SUBCLASS
	N						
	O						
	P						
	Q						
	R						
	S						
	T						

NON-PATENT DOCUMENTS

*		DOCUMENT (Including Author, Title, Source, and Pertinent Pages)	DATE
	U		
	V		
	W		
	X		

GAU 1641
#5
1.127

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to:

Assistant Commissioner for Patents,
Washington, D.C. 20231

on 3/14/00

TOWNSEND and TOWNSEND and CREW LLP

By

PATENT
Attorney Docket No.: 16655-000810US

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

Daniel L. Flamm

Application No.: 09/151,163

Filed: September 10, 1998

For: MULTI-TEMPERATURE PROCESSING

Examiner: L. Scheiner

Art Unit: 1641

RESPONSE TO RESTRICTION REQUIREMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

In response to the restriction requirement mailed February 14, 2000, applicant elects to prosecute claims 1-12 with traverse.

Respectfully submitted,

Steve Y. Cho
Reg. No. 44,612

TOWNSEND and TOWNSEND and CREW LLP
Two Embarcadero Center, 8th Floor
San Francisco, California 94111-3834
Tel (650) 326-2400
Fax (650) 326-2422
SYC:sgk

PA 3057441 v1

UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/151,163	09/10/98	FLAMM	D 16655-000810

020350 HM22/0214
TOWNSEND AND TOWNSEND AND CREW LLP
TWO EMBARCADERO CENTER
EIGHTH FLOOR
SAN FRANCISCO CA 94111

EXAMINER	
SCHEINER,L	
ART UNIT	**PAPER NUMBER**
1641	4

DATE MAILED: 02/14/00

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary

Application No.	Applicant(s)
09/151,163	Flamm
Examiner	**Group Art Unit**
Laurie Scheiner	1645

☐ Responsive to communication(s) filed on _____ .

☐ This action is **FINAL**.

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire ___1___ month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claims

☒ Claim(s) *1-20* is/are pending in the application.

Of the above, claim(s) _____ is/are withdrawn from consideration.

☐ Claim(s) _____ is/are allowed.

☐ Claim(s) _____ is/are rejected.

☐ Claim(s) _____ is/are objected to.

☒ Claims *1-20* are subject to restriction or election requirement.

Application Papers

☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

☐ The proposed drawing correction, filed on _____ is ☐approved ☐disapproved.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number) _____ .

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____ .

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

☐ Notice of References Cited, PTO-892

☐ Information Disclosure Statement(s), PTO-1449, Paper No(s). _____

☐ Interview Summary, PTO-413

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

--- SEE OFFICE ACTION ON THE FOLLOWING PAGES ---

Election/Restriction

1. Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Claims 1-12, drawn to a method of etching, classified in class 216, subclass 2.

II. Claims 13-20, drawn to an apparatus for etching a substrate, classified in class 156, subclass 345.

The inventions are distinct, each from the other because of the following reasons: Inventions II, drawn to an apparatus for etching and Invention I, drawn to a method of etching are related as product and process of use. The inventions can be shown to be distinct if either or both of the following can be shown: (1) the process for using the product as claimed can be practiced with another materially different product or (2) the product as claimed can be used in a materially different process of using that product (MPEP § 806.05(h)). In the instant case the etching may be produced via the apparatus as claimed, or alternatively the substrate may be etched via chemical treatment (e.g. hydrofluoric acid).

Because these inventions are distinct for the reasons given above and have acquired a separate status in the art because of their separate classification and their recognized divergent subject matter, restriction for examination purposes as indicated is proper.

Applicant is advised that the reply to this requirement to be complete must include an election of the invention to be examined even though the requirement be traversed (37 CFR 1.143).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Laurie Scheiner whose telephone number is (703) 308-1122.

LAURIE SCHEINER
PRIMARY EXAMINER

Laurie Scheiner

December 20, 1999

UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

APPLICATION NUMBER	FILING/RECEIPT DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NO./TITLE
09/151,163	09/10/98	FLAMM	D 16655-000810

#3

020350 0242/0929
TOWNSEND AND TOWNSEND AND CREW
TWO EMBARCADERO CENTER EIGHTH FLOOR
SAN FRANCISCO CA 94111

NOT ASSIGNED

1641

DATE MAILED: 09/29/98

OIPE JC34 FEB 01 1999 PATENT & TRADEMARK OFFICE

NOTICE TO FILE MISSING PARTS OF APPLICATION

Filing Date Granted

An Application Number and Filing Date have been assigned to this application. The items indicated below, however, are missing. Applicant is given TWO MONTHS FROM THE DATE OF THIS NOTICE within which to file all required items and pay fees required below to avoid abandonment. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a). **If any of items 1 or 3 through 5 are indicated as missing, the SURCHARGE set forth in 37 CFR 1.16(e) of ☐ $65.00 for a small entity in compliance with 37 CFR 1.27, or ☒ $130.00 for a non-small entity, must also be timely submitted in reply to this NOTICE to avoid abandonment.**

If all required items on this form are filed within the period set above, the total amount owed by applicant as a ☐ small entity (statement filed) ☒ non-small entity is $ 920.00 .

☒ 1. The statutory basic filing fee is:
- ☒ missing.
- ☐ insufficient.

Applicant must submit $ 790.00 to complete the basic filing fee and/or file a small entity statement claiming such status (37 CFR 1.27).

☐ 2. Additional claim fees of $_____, including any multiple dependent claim fees, are required.

$_____ for _____ independent claims over 3.

$_____ for _____ dependent claims over 20.

$_____ for multiple dependent claim surcharge.

Applicant must either submit the additional claim fees or cancel additional claims for which fees are due.

☒ 3. The oath or declaration:
- ☒ is missing or unexecuted.
- ☐ does not cover the newly submitted items.
- ☐ does not identify the application to which it applies.
- ☐ does not include the city and state or foreign country of applicant's residence.

An oath or declaration in compliance with 37 CFR 1. 63, including residence information and identifying the application by the above Application Number and Filing Date is required.

☐ 4. The signature(s) to the oath or declaration is/are by a person other than inventor or person qualified under 37 CFR 1.42, 1.43 or 1.47.

A properly signed oath or declaration in compliance with 37 CFR 1.63, identifying the application by the above Application Number and Filing Date, is required.

☐ 5. The signature of the following joint inventor(s) is missing from the oath or declaration:

_____

An oath or declaration in compliance with 37 CFR 1.63 listing the names of all inventors and signed by the omitted inventor(s), identifying this application by the above Application Number and Filing Date, is required.

☐ 6. A $50.00 processing fee is required since your check was returned without payment (37 CFR 1.21(m)).

☐ 7. Your filing receipt was mailed in error because your check was returned without payment.

☐ 8. The application does not comply with the Sequence Rules.
See attached "Notice to Comply with Sequence Rules 37 CFR 1.821-1.825."

☐ 9. OTHER: _____

Direct the reply and any questions about this notice to "Attention: Box Missing Parts."

A copy of this notice MUST be returned with the reply.

ALEXU 00000054 201430 09151163
65.00 CH
395.00 CH

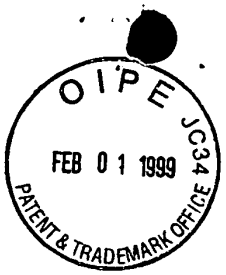
10 B. 00

SECTOR #

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Assistant Commissioner for Patents, Attn: Box Missing Parts, Washington, D.C. 20231, on January 29, 1999

TOWNSEND and TOWNSEND and CREW LLP

By Diane Elzinga



#3

PATENT

Attorney Docket No. 016655-000810

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

Daniel L. Flamm

Serial No.: 09/151,163

Filed: September 10, 1998

For: **MULTI-TEMPERATURE PROCESSING**

Examiner: not assigned

Art Unit: 1641

TRANSMITTAL LETTER - RESPONSE TO NOTICE OF MISSING PARTS

Attn: Box Missing Parts
Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Pursuant to the Notice to File Missing Parts of Application - Filing Date Granted dated September 29, 1998, enclosed are the following to be made of record in the above-identified application:

1) Petition to Extend Time;
2) Executed Declaration and Power of Attorney;
3) Executed Verified Statement Claiming Small Entity Status;
4) Copy of Notice of Missing Parts; and
5) Postcard.

Please charge Deposit Account No. 20-1430 for the following fees:

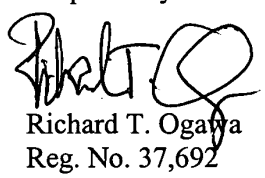
Small entity:	(a) Filing Fee (§ 1.16(a)) (Small Entity)	$380.00
	(b) Excess Claims Fees (§ 1.16(b), (c)):	
	20 - 20 = 0 x $9.00 =	$0.00
	2 - 3 = 0 x $39.00 =	$0.00

(c)	Missing Parts Surcharge	$65.00

TOTAL FEES TO BE CHARGED $445.00

The Commissioner is hereby authorized to charge any additional fees associated with this paper or during the pendency of this application, or credit any overpayment, to Deposit Account No. 20-1430. This Transmittal Letter is submitted in triplicate.

Respectfully submitted,



Richard T. Ogawa
Reg. No. 37,692

TOWNSEND and TOWNSEND and CREW LLP
Two Embarcadero Center, 8th Floor
San Francisco, California 94111-3834
(650) 326-2400
Fax (650) 326-2422
RTO:de
PA 157134 v1

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Assistant Commissioner for Patents Washington, D.C. 20231
on January 29, 1999
By: Diana Elzinga

PATENT
Attorney Docket No.: 16655-000810

#3

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

Daniel L. Flamm

Application No.: 09,151,163

Filed: September 10, 1998

For: **MULTI-TEMPERATURE PROCESSING**

Examiner: unassigned

Art Unit: 1641

PETITION TO EXTEND TIME

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Applicant petitions the Assistant Commissioner of Patents to extend the time for response to the Notice to File Missing Parts, dated September 29, 1998 for 2 months, from November 29, 1998 to January 29, 1999. An appropriate response in the form of a Response to Notice to File Missing Parts is enclosed herewith.

Please charge the fee of $190.00 to the undersigned's Deposit Account No. 20-1430. Please charge any additional fees or credit overpayment to the above deposit account. This petition is submitted in duplicate.

Respectfully submitted,

Richard T. Ogawa
Reg. No. 37,692

02/05/1999 SSALEEKU 00000055 201430 09151163
01 FC:216 190.00 CH

TOWNSEND and TOWNSEND and CREW LLP
Two Embarcadero Center, 8th Floor
San Francisco, California 94111-3834
Tel: (650) 326-2400
Fax: (650) 326-2422
RTO:de

PA 172052 v1

(c)	Missing Parts Surcharge	$65.00
	TOTAL FEES TO BE CHARGED	$445.00

The Commissioner is hereby authorized to charge any additional fees associated with this paper or during the pendency of this application, or credit any overpayment, to Deposit Account No. 20-1430. This Transmittal Letter is submitted in triplicate.

Respectfully submitted,

Richard T. Ogawa
Reg. No. 37,692

TOWNSEND and TOWNSEND and CREW LLP
Two Embarcadero Center, 8th Floor
San Francisco, California 94111-3834
(650) 326-2400
Fax (650) 326-2422
RTO:de
PA 157134 v1

Attorney Docket No.: 016655-000810US

DECLARATION AND POWER OF ATTORNEY

#3

As a below named inventor, I declare that:

My residence, post office address and citizenship are as stated below next to my name; I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural inventors are named below) of the subject matter which is claimed and for which a patent is sought on the invention entitled: **MULTI-TEMPERATURE PROCESSING** the specification of which ____ is attached hereto or _X_ was filed on September 10, 1998 as Application No. 09/151,163 and was amended on _____ (if applicable).

I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above. I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, Section 1.56. I claim foreign priority benefits under Title 35, United States Code, Section 119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s)

Country	Application No.	Date of Filing	Priority Claimed Under 35 USC 119

I hereby claim the benefit under Title 35, United States Code § 119(e) of any United States provisional application(s) listed below:

Application No.	Filing Date

I claim the benefit under Title 35, United States Code, Section 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, Section 1.56 which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

Application No.	Date of Filing	Status

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith.

Richard T. Ogawa , Reg. No.
William J. Bohler , Reg. No. 31.487

Send Correspondence to:	Direct Telephone Calls to: (Name, Reg. No., Telephone No.)
Richard T. Ogawa	

TOWNSEND and TOWNSEND and CREW LLP **Two Embarcadero Center, 8th Floor** **San Francisco, California 94111-3834**	Name: Reg. No.: Telephone:	Richard T. Ogawa 37,692 650-324-6361

Full Name of Inventor 1:	Last Name: FLAMM	First Name: DANIEL	Middle Name or Initial: L.	
Residence & Citizenship:	City: Walnut Creek	State/Foreign Country: CA	Country of Citizenship: US	
Post Office Address:	Post Office Address: 476 Green View Drive	City: Walnut Creek	State/Country: CA	Postal Code: 94596

I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Signature of Inventor 1	Signature of Inventor 2	Signature of Inventor 3
DANIEL L. FLAMM		
Date January 27, 1999	Date	Date

Attorney Docket No.: 016655-000810

VERIFIED STATEMENT (DECLARATION) CLAIMING SMALL ENTITY STATUS
(37 CFR 1.9(f) & 1.27(b)) - INDEPENDENT INVENTOR

Applicant or Patentee: Daniel L. Flamm
Application or Patent No.: 09/151,163
Filed or Issued: September 10, 1998
Title: MULTI-TEMPERATURE PROCESSING

As a below named inventor, I hereby declare that I qualify as an independent inventor as defined in 37 CFR 1.9(c) for purposes of paying reduced fees to the Patent and Trademark Office regarding the invention entitled MULTI-TEMPERATURE PROCESSING described in:

#3

[ ] the specification filed herewith;
[X] Application No. 09/151,163, filed September 10, 1998;
[ ] Patent No. _____, issued _____.

I have not assigned, granted, conveyed or licensed and am under no obligation under contract or law to assign, grant, convey or license, any rights in the invention to any person who would not qualify as an independent inventor under 37 CFR 1.9(c) if that person made the invention, or by any concern that would not qualify as a small business concern under 37 CFR 1.9(d), or a nonprofit organization under 37 CFR 1.9(e).

Each person, concern or organization to which I have assigned, granted, conveyed or licensed or am under an obligation under contract or law to assign, grant, convey or license any rights in the invention is listed below:*

[ ] No such person, concern or organization.
[ ] Persons, concerns or organizations listed below.*

*NOTE: Separate verified statements are required from each named person, concern or organization having rights to the invention averring to their status as small entities. (37 CFR 1.27)

Name: _____
Address: _____

[ ] Individual [ ] Small Business Concern [ ] Nonprofit Organization

Name: _____
Address: _____

[ ] Individual [ ] Small Business Concern [ ] Nonprofit Organization

I acknowledge the duty to file, in this application or patent, notification of any change in status resulting in loss of entitlement to small entity status prior to paying, or at the time of paying, the earliest of the issue fee or any maintenance fee due after the date on which status as a small entity is no longer appropriate. (37 CFR 1.28(b))

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application, any patent issuing thereon, or any patent to which this verified statement is directed.

Name of Inventor Daniel L. Flamm	Name of Inventor	Name of Inventor
Signature of Inventor Daniel L. Flamm	Signature of Inventor	Signature of Inventor
Date January 27, 1999	Date	Date

PA 157183 v1

UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

APPLICATION NUMBER	FILING/RECEIPT DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NO./TITLE
09/151,163	09/10/98	FLAMM	D 16655-000810

020350 0242/0929
TOWNSEND AND TOWNSEND AND CREW
TWO EMBARCADERO CENTER EIGHTH FLOOR
SAN FRANCISCO CA 94111

NOT ASSIGNED

1641

DATE MAILED: 09/29/98

NOTICE TO FILE MISSING PARTS OF APPLICATION
Filing Date Granted

An Application Number and Filing Date have been assigned to this application. The items indicated below, however, are missing. Applicant is given TWO MONTHS FROM THE DATE OF THIS NOTICE within which to file all required items and pay fees required below to avoid abandonment. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a). **If any of items 1 or 3 through 5 are indicated as missing, the SURCHARGE set forth in 37 CFR 1.16(e) of ☐ $65.00 for a small entity in compliance with 37 CFR 1.27, or ☑ $130.00 for a non-small entity, must also be timely submitted in reply to this NOTICE to avoid abandonment.**

If all required items on this form are filed within the period set above, the total amount owed by applicant as a ☐ small entity (statement filed) ☑ non-small entity is $ 920.00 .

☐ 1. The statutory basic filing fee is:
- ☒ missing.
- ☐ insufficient.

Applicant must submit $ 790.00 to complete the basic filing fee and/or file a small entity statement claiming such status (37 CFR 1.27).

☐ 2. Additional claim fees of $_____, including any multiple dependent claim fees, are required.

$_____ for _____ independent claims over 3.

$_____ for _____ dependent claims over 20.

$_____ for multiple dependent claim surcharge.

Applicant must either submit the additional claim fees or cancel additional claims for which fees are due.

☑ 3. The oath or declaration:
- ☑ is missing or unexecuted.
- ☑ does not cover the newly submitted items.
- ☐ does not identify the application to which it applies.
- ☐ does not include the city and state or foreign country of applicant's residence.

An oath or declaration in compliance with 37 CFR 1. 63, including residence information and identifying the application by the above Application Number and Filing Date is required.

☐ 4. The signature(s) to the oath or declaration is/are by a person other than inventor or person qualified under 37 CFR 1.42, 1.43 or 1.47.
A properly signed oath or declaration in compliance with 37 CFR 1.63, identifying the application by the above Application Number and Filing Date, is required.

☐ 5. The signature of the following joint inventor(s) is missing from the oath or declaration:

_____

An oath or declaration in compliance with 37 CFR 1.63 listing the names of all inventors and signed by the omitted inventor(s), identifying this application by the above Application Number and Filing Date, is required.

☐ 6. A $50.00 processing fee is required since your check was returned without payment (37 CFR 1.21(m)).

☐ 7. Your filing receipt was mailed in error because your check was returned without payment.

☐ 8. The application does not comply with the Sequence Rules.
See attached "Notice to Comply with Sequence Rules 37 CFR 1.821-1.825."

☐ 9. OTHER: _____

Direct the reply and any questions about this notice to "Attention: Box Missing Parts."

A copy of this notice MUST be returned with the reply.

10 Box 10

APPLICATION TRANSMITTAL

Customer No. 20350
TOWNSEND and TOWNSEND and CREW LLP
Two Embarcadero Center, 8th Floor
San Francisco, CA 94111-3834
(650) 326-2400

Atty. Docket No. 16655-000810

"Express Mail" Label No. EL140093842US

Date of Deposit September 10, 1998

I hereby certify that this is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10 on the date indicated above and is addressed to:

Assistant Commissioner for Patents
Washington, D.C. 20231

By BRAD FICK

PATENT APPLICATION
ASSISTANT COMMISSIONER FOR PATENTS
Washington, D. C. 20231

Sir:
Transmitted herewith for filing is the [X] patent application, [ ] design patent application, [ ] continuation-in-part patent application of

Inventor(s): Daniel L. Flamm

For: MULTI-TEMPERATURE PLASMA ETCHING PROCESS

[X] This application claims priority from each of the following Application Nos./filing dates:
60/058,650 / 9/11/97 ; 08/567,224 / 12/4/95 ; _____/_____.

[ ] Please amend this application by adding the following before the first sentence: --This application claims the benefit of U.S. Provisional Application No. 60/_____, filed _____, the disclosure of which is incorporated by reference.--

Enclosed are:
[X] Patent Application (incl. 30 pages spec., 3 pages claims, 1 page abstract).
[X] 15 sheet(s) of [ ] formal [X] informal drawing(s).
[ ] An assignment of the invention to _____.
[ ] A [ ] signed [ ] unsigned Declaration & Power of Attorney.
[ ] A verified statement to establish small entity status under 37 CFR 1.9 and 37 CFR 1.27 [ ] is enclosed [ ] was filed in the earliest of the above-identified patent application(s).
[ ] A certified copy of a _____ application.
[ ] Information Disclosure Statement under 37 CFR 1.97.
[ ] A petition to extend time to respond in the parent application of this continuation-in-part application.
[X] Postcard.

Pursuant to 37 CFR 1.53(d), Applicant requests deferral of the filing fee until submission of the Missing Parts of Application.

DO NOT CHARGE THE FILING FEE AT THIS TIME.

2 extra copies of this sheet are enclosed.

Respectfully submitted,
TOWNSEND and TOWNSEND and CREW LLP

Richard T. Ogawa
Reg. No.: 37,692
Attorneys for Applicant

Telephone:
(650) 326-2400

16655\8-1app.trn

Attorney Docket No. 16655-000810

PATENT APPLICATION

MULTI-TEMPERATURE PROCESSING

Inventor:

Daniel L. Flamm, a citizen of the United States, residing at 476 Green View Drive, Walnut Creek, California 94596

Entity Status:

Small

TOWNSEND and TOWNSEND and CREW LLP
Two Embarcadero Center, 8th Floor
San Francisco, CA 9411-3834
(650) 326-2400

MULTI-TEMPERATURE PROCESSING

CROSS-REFERENCE TO RELATED APPLICATIONS

This present application is a continuation-in-part of U.S. Application Serial No. 60/058,650 (Attorney Docket No.16655-000600) filed September 11, 1997, and a continuation-in-part of U.S. Application Serial No. 08/567,224 filed December 4, 1995 (Attorney Docket No. 16655-5), which are hereby incorporated by reference for all purposes.

BACKGROUND OF THE INVENTION

This invention relates generally to plasma processing. More particularly, one aspect of the invention is for greatly improved plasma processing of devices using an in-situ temperature application technique. Another aspect of the invention is illustrated in an example with regard to plasma etching or resist stripping used in the manufacture of semiconductor devices. The invention is also of benefit in plasma assisted chemical vapor deposition (CVD) for the manufacture of semiconductor devices. But it will be recognized that the invention has a wider range of applicability. Merely by way of example, the invention also can be applied in other plasma etching applications, and deposition of materials such as silicon, silicon dioxide, silicon nitride, polysilicon, among others.

Plasma processing techniques can occur in a variety of semiconductor manufacturing processes. Examples of plasma processing techniques occur in chemical dry etching (CDE), ion-assisted etching (IAE), and plasma enhanced chemical vapor deposition (PECVD), including remote plasma deposition (RPCVD) and ion-assisted plasma enhanced chemical vapor deposition (IAPECVD). These plasma processing techniques often rely upon radio frequency power (rf) supplied to an inductive coil for providing power to produce with the aid of a plasma.

Plasmas can be used to form neutral species (i.e., uncharged) for purposes of removing or forming films in the manufacture of integrated circuit

devices. For instance, chemical dry etching is a technique which generally depends on gas-surface reactions involving these neutral species without substantial ion bombardment.

In a number of manufacturing processes, ion bombardment to substrate surfaces is often undesirable. This ion bombardment, however, is known to have harmful effects on properties of material layers in devices and excessive ion bombardment flux and energy can lead to intermixing of materials in adjacent device layers, breaking down oxide and "wear out," injecting of contaminative material formed in the processing environment into substrate material layers, harmful changes in substrate morphology (e.g. amophotization), etc.

Ion assisted etching processes, however, rely upon ion bombardment to the substrate surface in defining selected films. But these ion assisted etching processes commonly have a lower selectivity relative to conventional CDE processes. Hence, CDE is often chosen when high selectivity is desired and ion bombardment to substrates is to be avoided.

In generally most, if not all, of the above processes maintain temperature in a "batch" mode. That is, the temperature of surfaces in a chamber and of the substrate being processed in such chamber are controlled to be at a substantially a single value of temperature during processing.

From the above it is seen that an improved technique, including a method and apparatus, for plasma processing is often desired.

SUMMARY OF THE INVENTION

The present invention provides a technique, including a method and apparatus, for fabricating a product using a plasma discharge. One aspect of the present technique relies upon multi-step etching processes for selectively removing a film on a workpiece using differing temperatures. It overcomes serious disadvantages of prior art methods in which throughput and etching rate were lowered in order to avoid excessive device damage to a workpiece. In particular, this technique is extremely beneficial for removing resist masks which have been used to effect selective ion implantation of a substrate in some embodiments. In general,

implantation of ions into a resist masking surface causes the upper surface of said resist to become extremely cross-linked and contaminated by materials from the ion bombardment. If the cross-linked layer is exposed to excessive temperature, it is prone to rupture and forms contaminative particulate matter. Hence, the entire resist layer is often processed at a low temperature to avoid this particle problem. Processing at a lower temperature often requires excessive time which lowers throughput. Accordingly, the present invention overcomes these disadvantages of conventional processes by rapidly removing a majority of resist at a higher temperature after an ion implanted layer is removed without substantial particle generation at a lower temperature.

In another aspect, the present invention provides a process which utilizes temperature changes to achieve high etch rates while simultaneously maintaining high etch selectivity between a layer which is being pattered or removed other material layers. An embodiment of this process advantageously employs a sequence of temperature changes as an unexpected means to avoid various types of processing damage to the a device and material layers. A novel inventive means for effecting a suitable controlled change in temperature as part of a process involves the use of a workpiece support which has low thermal mass in comparison to the heat transfer means. In an aspect of this invention, a fluid is utilized to change the temperature of a workpiece. In another aspect, the thermal capacity of a circulating fluid is sufficiently greater than the thermal capacity of the workpiece support that it permits maintaining the workpiece at a substantially uniform temperature.

Still another aspect of the invention provides an apparatus for etching a substrate in the manufacture of a device using different temperatures during etching. The apparatus includes a chamber and a substrate holder disposed in the chamber. The substrate holder has a selected thermal mass to facilitate changing the temperature of the substrate to be etched. That is, the selected thermal mass of the substrate holder allows for a change from a first temperature to a second temperature within a characteristic time period to process a film. The present apparatus can, for example, provide different processing temperatures during an etching process or the like.

The present invention achieves these benefits in the context of known process technology. However, a further understanding of the nature and advantages of the present invention may be realized by reference to the latter portions of the specification and attached drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a simplified diagram of a plasma etching apparatus according to the present invention;

Figs. 2A-2E are simplified configurations using wave adjustment circuits according to the present invention;

Fig. 3 is a simplified diagram of a chemical vapor deposition apparatus according to the present invention;

Fig. 4 is a simplified diagram of a stripper according to the present invention;

Figs. 5A-5C are more detailed simplified diagrams of a helical resonator according to the present invention;

Fig. 6 is a simplified block diagram of a substrate holder according to the present invention;

Fig. 7 is a simplified diagram of a temperature control system according to an embodiment of the present invention;

Fig. 8 is a simplified diagram of a fluid reservoir system according to an embodiment of the present invention;

Fig. 9 is a simplified diagram of a simplified diagram of a semiconductor substrate according to an embodiment of the present invention; and

Fig. 10 is a simplified flow diagram of a heating process according to the present invention.

DETAILED DESCRIPTION OF THE INVENTION

Fig. 1 is a simplified diagram of a plasma etch apparatus 10 according to the present invention. This etch apparatus is provided with an inductive applicator, e.g., inductive coil. This etch apparatus depicted, however, is merely an

illustration, and should not limit the scope of the claims as defined herein. One of ordinary skilled in the art may implement the present invention with other treatment chambers and the like.

The etch apparatus includes a chamber 12, a feed source 14, an exhaust 16, a product support check or pedestal 18, an inductive applicator 20, a radio frequency ("rf") power source 22 to the inductive applicator 20, wave adjustment circuits 24, 29 (WACs), a radio frequency power source 35 to the pedestal 18, a controller 36, an agile temperature control means 19, and other elements. Optionally, the etch apparatus includes a gas distributor 17.

The chamber 12 can be any suitable chamber capable of housing a product 28, such as a wafer to be etched, and for providing a plasma discharge therein. The chamber can be a domed chamber for providing a uniform plasma distribution over the product 28 to be etched, but the chamber also can be configured in other shapes or geometries, e.g., flat ceiling, truncated pyramid, cylindrical, rectangular, etc. Depending upon the application, the chamber is selected to produce a uniform entity density over the pedestal 18, providing a high density of entities (i.e., etchant species) for etching uniformity.

The product support chuck can rapidly change its temperature in ways defined herein as well as others. The wafer is often thermally coupled to the support check which permits maintaining the wafer temperature in a known relationship with respect to the chuck. Coupling will often comprise an electrostatic chuck or mechanical clamps, which apply a pressure to bring the product into close proximity with the support check, which enables a relatively good thermal contact between the wafer and support chuck. The support chuck and wafer are often maintained at a substantially equal temperature. A pressure of gas is often applied through small openings in the support chuck behind the wafer in order to improve thermal contact and heat transfer between the wafer and support chuck.

The present chamber includes a dome 25 having an interior surface 26 made of quartz or other suitable materials. The exterior surface of the chamber is typically a dielectric material such as a ceramic or the like. Chamber 12 also includes a process kit with a focus ring 32, a cover (not shown), and other elements.

Preferably, the plasma discharge is derived from the inductively coupled plasma source that is a de-coupled plasma source ("DPS") or a helical resonator, although other sources can be employed.

The de-coupled source originates from rf power derived from the inductive applicator 20. Inductively coupled power is derived from the power source 22. The rf signal frequencies ranging from 800 kHz to 80 MHz can be provided to the inductive applicator 20. Preferably, the rf signal frequencies range from 5 MHz to 60 MHz. The inductive applicator (e.g., coil, antenna, transmission line, etc.) overlying the chamber ceiling can be made using a variety of shapes and ranges of shapes. For example, the inductive applicator can be a single integral conductive film, a transmission line, or multiple coil windings. The shape of the inductive applicator and its location relative to the chamber are selected to provide a plasma overlying the pedestal to improve etch uniformity.

The plasma discharge (or plasma source) is derived from the inductive applicator 20 operating with selected phase 23 and anti-phase 27 potentials (i.e., voltages) that substantially cancel each other. The controller 36 is operably coupled to the wave adjustment circuits 24, 29. In one embodiment, wave adjustment circuits 24, 29 provide an inductive applicator operating at full-wave multiples 21. This embodiment of full-wave multiple operation provides for balanced capacitance of phase 23 and anti-phase voltages 27 along the inductive applicator (or coil adjacent to the plasma). This full-wave multiple operation reduces or substantially eliminates the amount of capacitively coupled power from the plasma source to chamber bodies (e.g., pedestal, walls, wafer, etc.) at or close to ground potential. Alternatively, the wave adjustment circuits 24, 29 provide an inductive applicator that is effectively made shorter or longer than a full-wave length multiple by a selected amount, thereby operating at selected phase and anti-phase voltages that are not full-wave multiples. Alternatively, more than two, one or even no wave adjustment circuits can be provided in other embodiments. But in all of these above embodiments, the phase and anti-phase potentials substantially cancel each other, thereby providing substantially no capacitively coupled power from the plasma source to the chamber bodies.

In alternative embodiments, the wave adjustment circuit can be configured to provide selected phase and anti-phase coupled voltages coupled from the inductive applicator to the plasma that do not cancel. This provides a controlled potential between the plasma and the chamber bodies, e.g., the substrate, grounded surfaces, walls, etc. In one embodiment, the wave adjustment circuits can be used to selectively reduce current (i.e., capacitively coupled current) to the plasma. This can occur when certain high potential difference regions of the inductive applicator to the plasma are positioned (or kept) away from the plasma region (or inductor-containing-the-plasma region) by making them go into the wafer adjustment circuit assemblies, which are typically configured outside of the plasma region. In this embodiment, capacitive current is reduced and a selected degree of symmetry between the phase and anti-phase of the coupled voltages is maintained, thereby providing a selected potential or even substantially ground potential. In other embodiments, the wave adjustment circuits can be used to selectively increase current (i.e., capacitively coupled current) to the plasma.

As shown, the wave adjustment circuits are attached (e.g., connected, coupled, etc.) to ends of the inductive applicator. Alternatively, each of these wave adjustment circuits can be attached at an intermediate position away from the inductive application ends. Accordingly, upper and lower tap positions for respective wave adjustment circuits can be adjustable. But both the inductive applicator portions below and above each tap position are active. That is, they both can interact with the plasma discharge.

A sensing apparatus can be used to sense plasma voltage which is used to provide automatic tuning of the wave adjustment circuits and any rf matching circuit between the rf generator and the plasma treatment chamber. This sensing apparatus can maintain the average AC potential at zero or a selected value relative to ground or any other reference value. This wave adjustment circuit provides for a selected potential difference between the plasma source and chamber bodies. These chamber bodies may be at a ground potential or a potential supplied by another bias supply, e.g., See Fig. 1 reference numeral 35. Examples of wave adjustment circuits are described by way of the Figs. below.

For instance, Figs. 2A to 2E are simplified configurations using the wave adjustment circuits according to the present invention. These simplified configurations should not limit the scope of the claims herein. In an embodiment, these wave adjustment circuits employ substantially equal circuit elements (e.g., inductors, capacitors, transmission line sections, and others) such that the electrical length of the wave adjustment circuits in series with the inductive applicator coupling power to the plasma is substantially an integral multiple of one wavelength. In other embodiments, the circuit elements provide for inductive applicators at other wavelength multiples, e.g., one-sixteenth-wave, one-eighth-wave, quarter-wave, half-wave, three-quarter wave, etc. In these embodiments (e.g., full-wave multiple, half-wave, quarter-wave, etc.), the phase and anti-phase relationship between the plasma potentials substantially cancel each other. In further embodiments, the wave adjustment circuits employ circuit elements that provide plasma applicators with phase and anti-phase potential relationships that do not cancel each other out using a variety of wave length portions.

Fig. 2A is a simplified illustration of a plasma source 50 using wave adjustment circuits and an agile temperature chuck 75 according to an embodiment of the present invention. This plasma source 50 includes a discharge tube 52, an inductive applicator 55, an exterior shield 54, an upper wave adjustment circuit 57, a lower wave adjustment circuit 59, an rf power supply 61, and other elements. The upper wave adjustment circuit 57 is a helical coil transmission line portion 69, outside of the plasma source region 60. Lower wave adjustment circuit 59 also is a helical coil transmission line portion 67 outside of the plasma source region 60. The power supply 61 is attached 65 to this lower helical coil portion 67, and is grounded 63. Each of the wave adjustment circuits also are shielded 66, 68.

In this embodiment, the wave adjustment circuits are adjusted to provide substantially zero AC voltage at one point on the inductive coil (refer to point 00 in Fig. 2A). This embodiment also provides substantially equal phase 70 and anti-phase 71 voltage distributions in directions about this point (refer to 00-A and 00-C in Fig. 2A) and provides substantially equal capacitance coupling to the plasma from physical inductor elements (00-C) and (00-A), carrying the phase and anti-phase

potentials. Voltage distributions 00-A and 00-C are combined with C-D and A-B (shown by the phantom lines) to substantially comprise a full-wave voltage distribution in this embodiment where the desired configuration is a selected phase/antiphase portion of a full-wave inductor (or helical resonator) surrounding the plasma source discharge tube.

In this embodiment, it is desirable to reduce or minimize capacitive coupling current from the inductive element to the plasma discharge in the plasma source. Since the capacitive current increases monotonically with the magnitude of the difference of peak phase and anti-phase voltages, which occur at points A and C in Fig. 2A, this coupling can be lessened by reducing this voltage difference. In Fig. 2A, for example, it is achieved by way of two wave adjustment circuits 57, 59. Coil 55 (or discharge source) is a helical resonator and the wave adjustment circuits 57, 59 are helical resonators.

The discharge source helical resonator 53 can be constructed using conventional design formulae. Generally, this helical resonator includes an electrical length which is a selected phase portion "x" (A to 00 to C) of a full-wave helical resonator. The helical resonator wave adjustment circuits are each selected to jointly comprise a portion (2π-x) of full-wave helical resonators. Physical parameters for the wave adjustment helical resonators can be selected to realize practical physical dimensions and appropriate Q, Z_o, etc values. In particular, some or even all of the transmission line parameters (Q, Z_o, etc.) of the wave adjustment circuit sections may be selected to be substantially the same as the transmission line parameters of the inductive applicator. The portion of the inductive plasma applicator helical resonator, on the other hand, is designed and sized to provide selected uniformity values over substrate dimensions within an economical equipment size and reduced Q.

The wave adjustment circuit provides for external rf power coupling, which can be used to control and match power to the plasma source, as compared to conventional techniques used in helical resonators and the like. In particular, conventional techniques often match to, couple power to, or match to the impedance of the power supply to the helical resonator by varying a tap position along the coil

above the grounded position, or selecting a fixed tap position relative to a grounded coil end and matching to the impedance at this position using a conventional matching network, e.g., LC network, π network, etc. Varying this tap position along the coil within a plasma source is often cumbersome and generally imposes difficult mechanical design problems. Using the fixed tap and external matching network also is cumbersome and can cause unanticipated changes in the discharge Q, and therefore influences its operating mode and stability. In the present embodiments, the wave adjustment circuits can be positioned outside of the plasma source (or constrained in space containing the inductive coil, e.g., See Fig. 2A. Accordingly, the mechanical design (e.g., means for varying tap position, change in the effective rf power coupling point by electrical means, etc.) of the tap position are simplified relative to those conventional techniques.

In the present embodiment, rf power is fed into the lower wave adjustment circuit 59. Alternatively, rf power can be fed into the upper wave adjustment circuit (not shown). The rf power also can be coupled directly into the inductive plasma coupling applicator (e.g., coil, etc.) in the wave adjustment circuit design, as illustrated by Fig. 2B. Alternatively, other applications will use a single wave adjustment circuit, as illustrated by Fig. 2C. Power can be coupled into this wave adjustment circuit or by conventional techniques such as a tap in the coil phase. In some embodiments, this tap in the coil phase is positioned above the grounded end. An external impedance matching network may then be operably coupled to the power for satisfactory power transfer efficiency from, for example, a conventional coaxial cable to impedances (current to voltage rations) existing between the wave adjustment circuit terminated end of the applicator and the grounded end.

A further embodiment using multiple inductive plasma applicators also is provided, as shown in Fig. 2D. This embodiment includes multiple plasma applicators (PA1, PA2...PAn). These plasma applicators respectively provide selected combinations of inductively coupled power and capacitively coupled power from respective voltage potentials (V1, V2...Vn). Each of these plasma applicators derives power from its power source (PS1, PS2...PSn) either directly through an appropriate matching or coupling network or by coupling to a wave adjustment

circuit as described. Alternatively, a single power supply using power splitters and impedance matching networks can be coupled to each (or more than two) of the plasma applicators. Alternatively, more than one power supply can be used where at least one power supply is shared among more than one plasma applicator. Each power source is coupled to its respective wave adjustment circuits (WAC1, WAC2...WACn).

Generally, each plasma applicator has an upper wave adjustment circuit (e.g., WAC 1a, WAC 2a...WACna) and a lower wave adjustment circuit (e.g., WAC1b, WAC 2b...WACnb). The combination of upper and lower wave adjustment circuits are used to adjust the plasma source potential for each plasma source zone. Alternatively, a single wave adjustment circuit can be used for each plasma applicator. Each wave adjustment circuit can provide substantially the same impedance characteristics, or substantially distinct impedance characteristics. Of course, the particular configuration used will depend upon the application.

For instance, multiple plasma applicators can be used to employ distinct excitation frequencies for selected zones in a variety of applications. These applications include film deposition using plasma enhanced chemical deposition, etching by way of ion enhanced etching or chemical dry etching and others. Plasma cleaning also can be performed by way of the multiple plasma applicators. Specifically, at least one of the plasma applicators will define a cleaning plasma used for cleaning purposes. In one embodiment, this cleaning plasma can have an oxygen containing species. This cleaning plasma is defined by using an oxygen discharge, which is sustained by microwave power to a cavity or resonant microwave chamber abutting or surrounding a conventional dielectric vessel. Of course, a variety of other processes also can be performed by way of this multiple plasma applicator embodiment.

This present application using multiple plasma applicators can provide a multi-zone (or multi-chamber) plasma source without the use of conventional mechanical separation means (e.g., baffles, separate process chambers, etc.). Alternatively, the degree of interaction between adjacent zones or chambers can be relaxed owing to the use of voltage potential control via wave adjustment circuits.

This plasma source provides for multiple plasma source chambers, each with its own control via its own plasma applicator. Accordingly, each plasma applicator provides a physical zone region (i.e., plasma source) with selected plasma characteristics (e.g., capacitively coupled current, inductively coupled current, etc.). These zones can be used alone or can be combined with other zones. Of course, the particular configuration will depend upon the application.

In the present embodiments, the wave adjustment circuit can be made from any suitable combination of element(s) such as various types of transmission lines, circuits, etc. These transmission lines include conventional solid or air dielectric coaxial cable, or ordinary, repeating inductor/capacitor discrete approximations to transmission lines, and others. These types of transmission lines are co-axial transmission lines, balanced parallel transmission lines, so called slow wave transmission lines with a spiral inner conductor (e.g., selected portions of a helical resonator, etc.), and others. Individual lumped, fixed, or adjustable combinations of resistors, capacitors, and inductors (e.g., matching networks, etc.) also can be used in place of transmission line sections for the wave adjustment circuit. These general types of wave adjustment circuits are frequency dependent, and can be termed frequency dependent wave adjustment circuits (or FDWACs).

Frequency independent elements also can be used as the wave adjustment circuits. These wave adjustment circuits can be termed frequency independent WACs (or FIWACs). Frequency independent wave adjustment circuits include degenerate cases such as short-circuit connections to ground or an infinite impedance (i.e., open circuit), and others. Frequency independent wave adjustment circuits can be used alone, or in combination with the frequency dependent wave adjustment circuits. Alternatively, the frequency dependent wave adjustment circuits can be used alone or in combination with other wave adjustment circuits. Other variations, alternative constructions, and modifications also may be possible depending upon the application.

With regard to operation of the wave adjustment circuits, various embodiments can be used, as illustrated by Fig. 2E. The wave adjustment circuits are used to select a wave length portion to be applied in the plasma applicator. In

some embodiments, the average rf plasma potential is maintained close to ground potential by providing substantially equal phase 90, 81 and anti-phase 91, 82 capacitively coupled portions of the inductive applicator. This can occur in multi-wave embodiments 92, full-wave embodiments 93, half-wave multiple embodiments, quarter-wave multiple embodiments, or any other embodiments 94.

In alternative embodiments, it is desirable to maintain an elevated source plasma voltage relative to ground potential to induce a controlled ion plasma flux (or ion bombardment) to the product substrate (or any other chamber bodies). These embodiments are provided by selecting distinct electrical lengths for each of the wave adjustment circuit sections such that the capacitive coupled current from a phase section of the inductive plasma applicator is in excess of capacitive coupled current from its anti-phase portion. In these embodiments, the wave adjustment circuit provides a deliberate imbalance between the phase and anti-phase of the coupled voltages. In some embodiments 97, this occurs by shifting the zero voltage nodes along the process chamber axially, thereby achieving a bias relative to the plasma discharge. As shown, the phase 95 is imbalanced relative to its anti-phase 96. In other embodiments 99, one phase portion 84 is imbalanced by way of a different period relative to its complementary phase portion 85. Other embodiments are provided where the source plasma voltage is lower relative to ground potential. In the embodiments where imbalance is desirable, the potential difference between the phase and anti-phase potential portions is reduced (or minimized) when the amount of sputtering (e.g., wall sputtering, etc.) is reduced. The amount of sputtering, however, can be increased (or maximized) by increasing the potential difference between the phase and anti-phase potential portions. Sputtering is desirable in, for example, sputtering a quartz target, cleaning applications, and others. Of course, the type of operation used will depend upon the application.

Current maxima on an inductive applicator with distributed capacitance (e.g., helical resonator transmission line, etc.) occur at voltage minima. In particular, conventional quarter-wave helical resonator current is substantially at a relative maximum at its grounded end of the coil, and to a lesser extend in the nearby coil elements. Therefore, partial inductive coupling of power, if it occurs, will tend

to be at this grounded end. In conventional half-wave helical resonators, inductive coupling tends to occur at each of the two grounded ends.

In the present invention, substantially anti-symmetric phase and anti-phase inductive half-wave and other fractional wave applicator sections support substantially more inductive coupling at a selected rf voltage node, e.g., Fig. 2A reference numeral 00. This effect is caused by high current flow in the inductor applicator zones (or sections) both directly above and below the node (corresponding to inductor elements in the phase and anti-phase sections at and immediately adjacent to the rf voltage zero point). It should be noted that conventional quarter and half-wave inductively coupled inductive applicators have inductive coupling which abruptly declines below the grounded coil locations because the coil terminates and voltage extrema are present at these locations. This generally produces conventional quarter and half-wave helical resonators that tend to operate in a capacitive mode, or with a substantial fraction of power which is capacitively coupled to the plasma, unless the plasma is shielded from coil voltages, as noted above.

In a specific embodiment, the power system includes selected circuit elements for effective operation. The power system includes an rf power source. This rf power source can be any suitable rf generator capable of providing a selected or continuously variable frequency in a range from about 800 kHz to about 80 MHz. Many generators are useful. Preferably, generators capable of operating into short and open-circuit loads without damage are used for industrial applications. One example of a suitable generator is a fixed frequency rf generator 28.12 MHz - 3 kW CX-3000 power supply made by Comdel, Inc. of Beverly, Massachusetts. A suitable variable frequency power supply arrangement capable of the 3 kW output over an 800 kHz to 50 MHz range can be made by driving an IFI Model TCCX3500 High Power Wide Band Amplifier with a Hewlett Packard HP116A, 0-50 MHz Pulse/Function Generator. Other generators including those capable of higher or lower power also can be used depending upon the application.

Power from the generator can be transmitted to the plasma source by conventional coaxial cable transmission line. An example of this transmission line is RG8/U and other higher temperature rated cable (e.g., RG1151U, etc.) with a

coaxial TEFLON™ dielectric. In some embodiments, power is fed to conventional end-grounded half-wave helical resonators by positioning a movable tap on the helical coil and connecting a power source between the tap and the ground. In other embodiments, matching networks can be introduced between the coaxial cable power feed and the helical coil tap for flexibility. The matching network will depend on the selected wave configuration and wave adjustment circuits. In a balanced half-wave helical resonator embodiment, for example, the ends of the resonator coil can be terminated with wave adjustment circuits which substantially have zero susceptance. In particular, the wave adjustment circuit is designed as an open circuit by making no electrical connections to the ends of the coil, or establishing an electrical equivalence thereof. Alternatively, the ends of the coil are isolated by high series impedance chokes, thereby maintaining DC coupling to a fixed reference potential. These types of wave adjustment circuits are frequency independent and are "degenerate" cases. In these embodiments, the rf power is provided such that the phase and anti-phase current flows above and below the electrical midpoint (i.e., zero voltage node, etc.) of the coil. This provides for substantially balanced phase and anti-phase current flow from the power source stabilizing desired operation in coil voltages above the midpoint of the coil, and also provides substantially equal phase and anti-phase voltages.

The embodiments described above also can be applied to other plasma processing applications, e.g., PECVD, plasma immersion ion implantation (PIII), stripping, sputtering. For instance, Fig. 3 is a simplified CVD apparatus 100 according to the present invention. The present CVD apparatus includes a chamber 112, a feed source 114, an exhaust 116, a pedestal 118, a power source 122, a ground 124, a helical resonator 126, and other elements. The helical resonator 126 has a coil 132, an outer shield 133, and other elements. The chamber can be any suitable chamber capable of housing a product 119 such as a wafer for deposition, and for providing a plasma discharge therein. Preferably, the chamber is a right circular cylinder chamber for providing an uniform plasma species distribution over the product. But the chamber can also be configured in the form of rectangular right cylinder, a truncated cone, and the like. The chamber and fixtures are constructed

from aluminum and quartz, and other suitable materials. The plasma discharge is derived from a plasma source which is preferably a helical resonator discharge or other inductive discharge using a wave adjustment circuit or other techniques to selectively adjust phase-anti-phase potentials. The present CVD apparatus provides for deposition of a dielectric material, e.g., silicon dioxide or the like.

The product 119 having an upper surface 130 is placed into the present CVD apparatus for deposition, e.g., plasma enhanced chemical vapor deposition (PECVD), and others. Examples of deposition materials include a dielectric material such as a silicon dioxide (SiO_2), a phosphosilicate glass (PSG), a borophosphosilicate glass (BPSG), a silicon nitride (Si_3N_4), among others.

In one embodiment, the deposition occurs by introducing a mixture comprising organic silane, oxygen, and an inert gas such as helium or argon according to the present invention. The organic silane can be any suitable organic silicate material such TEOS, HMDS, OMCTS, and the like. Deposition is also conformal in selected instances. As for the oxygen, it includes a flow rate of about 1 liter/per minute and less. A relative flow rate between the organic silane such as TEOS and oxygen ranges from about 1:40 to about 2:1, and is preferably less than about 1:2 in certain applications. A deposition temperature of the organic silane-oxygen layer ranges from about 300 to about 500°C, and can also be at other temperatures. Pressures in the range of 1 to 7 Torr are generally used. Of course, other concentrations, temperatures, materials, and flow rates can be used depending upon the particular application.

This chamber also includes a wave adjustment circuit 127. The wave adjustment circuit 127 is used to provide a helical coil operating with capacitive coupling to selected phase and anti-phase voltages. This portion 127 of the wave adjustment circuit coil also is shielded 140 to prevent rf from interfering with the plasma discharge or external elements, e.g., equipment, power, etc. The coil shield 140 is made of a conductive material such as copper, aluminum, or the like. In one embodiment, an operating frequency is selected and the wave adjustment circuit is adjusted to short circuit the upper end of the helical applicator coil to ground 124. This provides a helical coil operating at approximately a full-wave multiple and has

substantially equal phase and anti-phase sections. This full-wave multiple operation provides for balanced capacitance of phase 151 and anti-phase 153 voltages along the coil 132 adjacent to the plasma source. Full-wave multiple operation reduces or even substantially eliminates the amount of capacitively coupled power from the plasma source to chamber bodies (e.g., pedestal, walls, wafer, etc.) at or close to ground potential.

In the present embodiment, the wave adjustment circuit 127 is a variable coil portion 128 of a spiral transmission line, which is selectively placed outside the outer shield 133. Accordingly, when the wave adjustment circuit is adjusted to become a short circuit, the plasma source "sees" only a selected full-wave multiple comprising substantially equal phase 151 and anti-phase 153 of the entire instantaneous AC voltages 134, 135. In this embodiment, stress of the deposited oxide film is often tensile, which can be undesirable.

Alternatively, the wave adjustment circuit 127 provides a helical resonator operating at selected phase and anti-phase voltages that are not full-wave multiples. This wave adjustment circuit provides for a selected amount of capacitive coupling from the plasma source to the chamber bodies. Stress of the deposited oxide film in this embodiment can be made to be zero or slightly compressive. In some embodiments, the oxide films can be deposited with an rf plasma potential of several hundred volts between the plasma source and the substrate to decrease the tendency of the oxide film to absorb moisture. This can occur by adjusting the wave adjustment circuit to add in a small section of transmission line outside of the source and correspondingly shortening the applicator coil (by moving the lower point at which the applicator coil is short-circuited and thereby decreasing the inductance of the applicator coil and electrical length of the helical resonator 126 (e.g., spiral transmission line, etc.)). Of course, the selected amount of capacitive coupling will depend upon the application.

Fig. 4 is a simplified diagram of a resist stripper according to the present invention. The present stripping apparatus includes similar elements as the previous described CVD apparatus. The present stripping apparatus includes a chamber 112, a feed source 114, an exhaust 116, a pedestal 118, which can be an

agile temperature controlled chuck, an rf power source 122, a ground 124, a helical resonator 126, and other elements. The helical resonator 126 includes a coil 132, an outer shield 133, a wave adjustment circuit 400, and other elements. The chamber can be any suitable chamber capable of housing a product 119 such as a photoresist coated wafer for stripping, and for providing a plasma discharge therein. The plasma discharge is derived from a plasma source, which is preferably a helical resonator discharge or other inductive discharge using a wave adjustment circuit or other techniques to selectively adjust phase/anti-phase potentials. Of course, in some applications other configurations such as parallel plate capacitive discharges and microwave powered discharges such as electron cyclotron resonance machines, resonant cavities and slow waver applicator structures may also be suitable. The present stripping apparatus provides for stripping or ashing photoresist, e.g., implant hardened, etc. Further examples of such a stripping apparatus are described in the experiments section below.

In this embodiment, the wave adjustment circuits rely upon open circuits (i.e., zero susceptance). Power transfer can be effected with a balanced feed such as an inductively-coupled push-pull arrangement with means such as coupled inductors. Techniques for constructing these coupled inductors are described in, for example, "The ARRL Antenna Book," R.D. Straw, Editor, The American Radio Relay League, Newington, CT (1994) and "The Radio Handbook," W.I. Orr, Editor, Engineering Ltd, Indiana (1962), which are both hereby incorporated by reference for all purposes. In one embodiment, a ferrite or powdered iron core "balun" (balanced-unbalanced) toroidal transformer (i.e., broadband transmission transformer, broadband transformer, etc.) 401 can be used to provide balanced matching from a conventional unbalanced coaxial transmission line. Techniques for constructing toroidal baluns are described in, for example, "Transmission Line Transformers," J. Sevick, 2nd Edition, American Radio Relay League, Newington, CT (1990). The toroidal transformer is coupled between the rf power source 122 and the coil 132. The midpoint 406 between the phase 405 and anti-phase voltage on the coil is effectively rf grounded, hence it may be convenient to directly ground this midpoint of the inductive application in some embodiments for stability. This

permits alternate operation in which power may be coupled into the inductive applicator (e.g., coil, etc.) with a conventional unbalanced feed line tapped on one side of the center. Push-pull balanced coupling ignites the plasma more easily than conventional unbalanced coil tap matching and generally is easier to adjust in selected applications.

Referring to the helical resonator embodiments operating at substantially equal phase and anti-phase potentials, Fig. 5A is a simplified diagram 200 of an equivalent circuit diagram of some of them. The diagram is merely an illustration and should not limit the scope of the claims herein. The equivalent circuit diagram includes a plurality of rf power supplies (V_1, V_2, $V_3 \ldots V_n$) 203, representing for example, a single rf power source. These power supplies are connected in parallel to each other. One end of the power supply is operably coupled to a ground connection 201. The other end of the power supplies can be represented as being connected to a respective capacitor (C_1, C_2, $C_3 \ldots C_n$). Each of these capacitors are connected in parallel to each other. During this mode of operation, no significant voltage difference exists between any of the common side of the capacitors, as they are all connected to each other in parallel.

Fig. 5B is a simplified diagram of instantaneous AC voltage and current along a helical resonator coil of Fig. 5A where each end of the inductive applicator is short circuited. The diagram is merely an illustration and should not limit the scope of the claims herein. This diagram includes the discharge tube 213 and an inductive plasma discharge (or plasma source) 501 therein. As shown, the plasma discharge includes an intensified "donut-shaped" glow region 501 that occupies a limited range (R) of the discharge tube 213. The plasma discharge has an average voltage potential (V_{ave}) of magnitude that is substantially within a few zero volts (i.e., the ground potential). As can be seen, the plasma discharge 501 has capacitively coupling elements to V_H and V_G. But the average voltage potential of this plasma discharge is substantially zero. This operation provides for balanced capacitance of phase 503 and anti-phase 505 voltages along the coil adjacent to the plasma, thereby substantially preventing capacitively coupling from the plasma source to chamber bodies. As also shown, a current maxima 507 exists at V_{ave}, which

corresponds to an inflection point between the phase 503 and the anti-phase 505.

In an alternative operating mode, rings of plasma caused by inductively coupled plasma current are visible near top and bottom extremes of the inductive applicator, as illustrated by Fig. 5C. This operating mode is generally for a full-wave 517 inductive coupling coil operated at a very high power, e.g., maximum power input to the inductive applicator is often limited by thermal considerations and breakdown. The rings 513, 515 of current in the plasma discharge are simulated by maximum coil current areas corresponding to voltage minima at the top and bottom shorted ends of the coil. Under these high power conditions, subordinate current rings are detectable and some excitation is often visible in the intermediate regions. This excitation is partially caused by capacitively driven currents within the discharge coupled to the voltage maximum and voltage minimum positions along the inductive applicator.

Alternatively, subordinate inductive plasma current rings at the top and bottom ends 513 of the resonator do not appear with limited input power. The coil current and inductive flux fall beyond the ends of the inductive applicator so that a single inductive ring 515 in the center portion is more stable, provided that the conductivity of the plasma is large enough to support a single current ring at a specified input power.

In alternative applications using high power operation, no secondary plasma current rings may be desirable. These applications often have substantially minimum internal capacitive coupling. In these applications, the inductive applicator (e.g., coil) abutting the vacuum vessel may be shortened from a full wave to an appropriate length such that only the central current maxima exists on the coil abutting the plasma source and the potential difference between maximum and minimum voltage on the applicator is substantially reduced. The present application is achieved by stabilizing the desired waveform along the applicator by appropriate impedance wave adjustment circuits.

An effective conventional method employed to avoid plasma potential shift in conventional commercially available inductive sources is to shield the plasma from the electrical fields on the inductive coupling element (commonly a multi-turn

coil) by inserting a grounded conductive member between the inductive driving element and the plasma discharge tube. Shielding is, however, cumbersome and inconvenient and has serious disadvantages in practice. Shields couple to inductive applicator elements and can cause wide excursions in the natural resonance frequency, which are not predicted by conventional analytical design formulae. This often results in laborious trail and error and iterative mechanical designs to achieve a desired resonance.

Another disadvantage of shielding is that shields often make it difficult to achieve initial ignition of the plasma since shields generally exclude capacitive electric fields in the plasma discharge tube. Those with skill in the art will recognize that in practice, substantial ionization (e.g. charge carriers) must be present in the tube volume before in inductive plasma current can be sustained. Thus, it is often said that a capacitive plasma must be ignited first in order to sustain an inductive plasma. This is not completely true since other external means of generating ionization (e.g. an intense photoionizing source, electron beams, etc.) can be used to generate the ionization which is prerequisite to sustaining an inductive plasma. However, a capacitive discharge is often a convenient and cost-effective means to ignite some plasma which is a prerequisite to starting and sustaining an inductive discharge.

In general, wave adjustment circuits are employed to substantially diminish capacitive coupling between a plasma source and an inductive applicator. If most capacitive coupling is removed, it may be difficult to ignite a plasma. However, wave adjustment circuits also provide a means to overcome the difficulty with igniting a plasma in the absence of capacitive coupling under steady state operating conditions. This means is provided by electrically, mechanically, or electromechanically tuning the wave adjustment circuits prior to the time of desired plasma ignition in a manner which generates an additional imbalance and capacitive coupling to the discharge volume. Of course, the characteristics of the plasma as a load to the applicator will dynamically change during ignition. The wave adjustment circuit can also be continuously tuned under feedback control during ignition in order to provide a desired voltage coupling and diminish undesired transients during plasma

breakdown.

Insertion of the shield close to high voltage RF point in a network (such as the voltage maximum points in a helical resonator or the high potential driven side of a TCP coil) also causes large displacement currents to flow through the capacitance between the shield and coil. This high potential difference is also a potential cause of damaging rf breakdown across the air gap, hence the gap may require protection by inconvenient solid or liquid dielectric insulation. The displacement current flow causes power loss and requires that higher power RF generating equipment be used to compensate for the power loss. Coupling loss in the plasma source structure is also undesirable from the standpoint of thermal control. These limitations are overcome by the present invention using the wave adjustment circuits, an inductive applicator of selected phase length, and other elements.

Fig. 6 is a simplified block diagram of a substrate holder 600 according to the present invention. This diagram is merely an illustration and should not limit the scope of the claims herein. One of ordinary skill in the art would recognize other variations, modifications, and alternatives. The substrate holder 600 or suceptor includes, among others, a lower or backside surface 608, which includes a plurality of concentric zones 608A, 608B, 608C, and 608D. In a specific embodiment, each of the zones can be in fluidic communication with each other and can be partly separated from each other. Each of the zones can have an inlet 613 and an outlet 611. Fluid enters the inlet, traverses in an annular manner in the zone, and leaves the outlet. A baffle can separate the inlet from the outlet. Each of the zones can have an inlet and outlet, which are independent from the other inlets and outlets. Alternatively, the inlet and outlets can be in fluid communication with each other.

The side-view diagram shown as "SIDE-VIEW A" illustrates a plurality of zones 603, which correspond to each of the concentric zones 608A, 608B, 608C, and 608D. Each zone is separated, in part, from each other by a baffle 605. Each baffle extends from a lower region of the substrate holder toward an upper portion of the substrate holder, but does not touch the upper surface 601 of the substrate holder. In preferred embodiments, the baffles do not touch the upper surface. Accordingly, the temperature of the baffles, which may be different from

the fluid, does not create an uneven temperature distribution along the upper surface 601. Additionally, the upper region 604, which is an open region within the substrate holder, provides fluid communication between each of the zones. Fluid communication in connection with the upper surface also provides an even distribution of temperature along the upper surface.

The fluid can be used to heat or cool the upper surface of the substrate holder. In a specific embodiment, the fluid generally should have a relatively high thermal conductivity and large heat capacity. The fluid should also be substantially non-corrosive, easy to transport, and can withstand a relatively large temperature range and still maintain its fluid characteristics. Additionally, the fluid should be able to be pumped and substantially non-reactive with the substrate holder material itself. The fluid can be any commercial heat transfer fluid selected for the desirable temperature range. As noted, the substrate holder and upper surface cools down or is heated up by way of the fluid. The fluid can traverse through the zones and can absorb thermal energy or release thermal energy by an external heat transfer device such as the one described below, but can be others.

In a specific embodiment, the substrate holder also includes a plurality of heating elements 607. The heating elements can selectively heat one or more zones in a desirable manner. As shown in the "SIDE-VIEW B" diagram, each of the heating elements can be directed to a single zone 603, which has an adjacent baffle 605. Alternatively, the heating elements can be directed to multiple zones or other specific regions of the substrate and in particular the backside of the substrate according to some embodiments. The heating elements can be any suitable device for supplying heat energy to the fluid. The heat can be supplied by single or in combination using radiation, conduction, and convention. As merely an example, the heating element can be a resistive heating unit, an infrared heating unit, and others. Of course, the type of heating unit used depends highly upon the application. Alternatively, the heating unit can also be replaced by cooling units.

The present invention provides a substantially uniform temperature distribution along the upper surface 601 of the substrate holder. In a specific embodiment, the uniformity of the temperature is within one Degree Celsius along

the entire surface which comes in contact with the object such as the wafer. Preferably, the wafer temperature also tracks the temperature uniformity of the upper surface. In other embodiments, the uniformity of the of the temperature is within one-tenth of a Degree Celsius along the entire surface which comes in contact with the object such as the wafer. Preferably, the wafer also has a uniform temperature distribution along the wafer.

The substrate has an upper surface, which holds an object in a secure manner during processing. The upper surface is generally made of a suitable material that has desirable heat transfer characteristics. In a specific embodiment, the upper surface is made using a low thermal mass, high conductivity material. As merely an example, the upper surface can be a diamond-like or diamond film overlying a copper or copper-like substrate. Of course, the type of surface used depends upon the application.

In a specific embodiment, the substrate holder also has temperature sensing units such as the one shown in "SIDE-VIEW C." The temperature sensing unit can be any suitable unit that is capable of being adapted to the upper surface of the substrate holder. Alternatively, the temperature sensing unit can measure the temperature of the fluid or lower surface of the substrate holder. As merely an example, the temperature sensing unit is a "fluro-optic" sensor unit made by a company called Luxtron in Santa Clara, California. Alternatively, the sensing unit can be an edge band IR sensor or the like. The sensing unit is capable of measuring a variety of spatial locations along the upper or lower surface of the substrate holder. The substrate holder can be implemented using a variety of systems for heating and/or cooling applications such as the one described below, but can be others.

Fig. 7 is a simplified diagram of a temperature control system 700 according to an embodiment of the present invention. This diagram is merely an illustration and should not limit the scope of the claims herein. One of ordinary skill in the art would recognize other variations, modifications, and alternatives. Among other elements, the system 700 can be used to heat and/or cool the wafer chuck or substrate holder 701. As shown, system 700 includes substrate holder 701, which is coupled to a heating unit 705 by way of line 707. Heating unit 705 is coupled to

fluid reservoir 713 and pump 709 by way of line 711.

Fluid from the fluid reservoir is pumped from the reservoir through the heating unit, which selectively sets the temperature of the fluid. The fluid leaves the heating unit at the selected temperature and traverses through the substrate holder, which can be similar to the one shown above, but can also be others. The fluid temperature selectively transfers energy in the form of heat to the wafer holder to a desirable temperature. Fluid leaves the substrate holder and traverses through node 721 and branch 719. Fluid traverse through branch 719 and node 717. Fluid leaves node 717 and returns back to the fluid reservoir via line 715.

In an alternative embodiment, the fluid can also be cooled using a heat exchanger 723. The fluid leaves the substrate holder and enters node 721. Fluid then enters the heat exchanger and traverses through loop 725. Thermal energy in the form of heat transfers to fluid in loop 723, which is cooler in temperature and draws heat away from the heat in the fluid in loop 725. In a specific embodiment, cooling fluid 727 enters and leaves the heat exchanger.

In a specific embodiment, system 700 operates in a manner to program a process temperature of the substrate holder. In this process, the reservoir with a suitable heat transfer fluid is maintained at a temperature below the desired process temperature. The fluid is circulated through the substrate holder or wafer chuck by the pump. The fluid line downstream of the pump is equipped with the electrical heater which is capable of heating the fluid to a desired temperature. The desired fluid temperature is determined by comparing the desired wafer or wafer chuck set point temperature to a measured wafer or wafer chuck temperature (this measurement can performed with a thermocouple, thermistor, pyrometer, fluor optic sensor or other sensing means). If the measured temperature of the wafer of chuck is below the desired temperature, a suitable control algorithm such as a proportional controller or a proportional-integral-derivative (i.e., PID) controller algorithm increases the temperature by supplying more power to the heater.

The temperature of fluid emerging from the chuck is also measured (normally there will be a small temperature difference since there is heat exchange between the fluid and chuck). If this temperature is above the desired fluid temperature

the fluid stream is diverted to a heat exchanger via control valves 1 and 2, which are respectively at nodes 721 and 717. If this temperature is less than or equal to the desired fluid temperature the fluid stream can be made to bypass the heat exchanger, or optionally can be heated in a heat exchange system. Since the temperature of commonly used heat exchangers cannot be changed rapidly, the heat exchanger is usually maintained at a single temperature sufficiently below the lowest desired fluid temperature to achieve the lowest desired temperature to be attained. The heat exchanger, fluid flow rate, coolant-side fluid temperature, heater power, chuck, etc. should be designed using conventional means to permit the heater to bring the fluid to a setpoint temperature and bring the temperature of the chuck and wafer to predetermined temperatures within specified time intervals and within specified uniformity limits.

In a preferred embodiment, the present invention uses a microprocessor based system to oversee the operations of the system described above. The microprocessor based system can have input and output ports, which are coupled to each of the elements, e.g., pump, heater, fluid reservoir, substrate holder. The microprocessor based unit selectively turns ON and/or OFF one or more of the elements to control the temperature of the substrate holder to provide a uniform distribution of temperature across the surface of the substrate holder.

In an alternative embodiment, Fig. 8 is a simplified diagram of a multiple fluid reservoir system 800 according to an embodiment of the present invention. This diagram is merely an illustration and should not limit the scope of the claims herein. One of ordinary skill in the art would recognize other variations, modifications, and alternatives. As shown, system 800 depicts an automatic system for agile temperature control of the substrate holder or wafer chuck 809 using two reservoirs 801, 803, but is not limited to two can be more than two, if desirable. The wafer chuck can be rapidly brought to temperature T1 by directing flow through proportional control valve V1 to the wafer chuck. Similarly, the chuck can be brought substantially to a temperature T2 by directing only a flow from the reservoir T2 to the wafer chuck. Temperature sensor TC1 measures the temperature of the heat transfer fluid entering the wafer chuck and sensor TC2 monitors temperature of fluid exiting the wafer chuck. Valves V1 and V2 are controlled by a control system which adjusts the

total volumetric flow rate of fluid flowing into the wafer chuck as well as the ratio of fluid flowing through V1 and V2. The ratio is set so that the temperature monitored by TC1 is at a predetermined value selected to achieve a desired wafer chuck temperature. The flow rate of a fluid flowing from both reservoir 1 and 2 is metered by conventional means and set to fix the temperature difference measured between TC2 and TC2 at a pre-specified difference. This difference is selected to meet a temperature uniformity specification. The temperature difference allowed is chosen so that etching nonuniformities caused by temperature gradients are below a predetermined permissible level which includes an allowance for normal variability in measurements, sensor, the control system etc. The flows can be digitally controlled proportional metering values as illustrated or alternately they can be controlled by computer-controlled variable speed pumps, as will be well known to those skilled in the art. In addition to the sensors TC1 and TC2, it is convenient to monitor the top surface chuck temperature and the wafer temperature so that TC1 can be selected to maintain the wafer temperature within a specific amount of a wafer etching or CVD temperature (when the chuck and etching temperature are greater than the temperature of the chamber walls, the wafer temperature will generally be slightly less than the chuck temperature owing to heat transfer resistance between the chuck and wafer and thermal coupling between the wafer and surrounding chamber walls).

Fig. 9 is a simplified diagram of a simplified diagram of a semiconductor substrate 900 according to an embodiment of the present invention. This diagram is merely an illustration and should not limit the scope of the claims herein. One of ordinary skill in the art would recognize other variations, modifications, and alternatives. As shown, the substrate is a stack of layers that is to be patterned. The stack includes a dielectric layer such as a thin 100Å gate oxide layer 903 on a substrate (e.g., silicon wafer) 901 on which 2000Å of tungsten silicide 907 or other material is deposited on the conductive layer, which can be polysilicon 905. A masking layer such as 2 microns of photoresist 909 is spin coated over the tungsten silicide and patterned by conventional photolithography techniques. The patterned layer includes an opening 911, which exposes the underlying tungsten silicide layer. It is desired to anisotropically etch the stack down to the silicon dioxide layer in order to

define a patterned structure which can be an EEPROM device or other integrated circuit element. Although this can be accomplished by etching in a conventional parallel plate reactor using a chlorine bearing plasma, it can be difficult to avoid removing excessive polysilicon during the overetching period, which is required to assure that the polysilicon is completely removed from within the unmasked regions. Furthermore, the resist mask must generally be removed after etching this stack. Since the temperature for the stack etch (i.e., often 50°C to 100°C is too low to achieve an adequate resist stripping rate (generally a rate of a few microns per minute is desirable), stripping is often done in a separate chamber of in separate resist stripping equipment.

The temperature is programmed by use of this invention to achieve better control of the etching process as well as to permit stripping the resist in the same chamber and controlled by the same process program which is used for stack etching.

A process according to the present invention can be briefly outlined as follows:

(1) Provide patterned stack in chamber;

(2) Perform native oxide breakthrough using sulfur hexafluoride bearing plasma;

(3) Ignite chlorine bearing plasma;

(4) Etch tungsten silicide layer at a first substrate temperature;

(5) Detect polysilicon layer;

(6) Perform over etch to clear tungsten;

(7) Expose polysilicon;

(8) Etch polysilicon;

(9) Clear polysilicon to oxide;

(10) Stop chlorine bearing plasma;

(11) Feed oxygen;

(12) Ignite oxygen;

(13) Strip photoresist at a second substrate temperature; and

(14) Extinguish oxygen plasma

The above sequence of steps are merely examples to show an etching process that uses more than one temperature. Here, the etching process for tungsten silicide and

polysilicon occurs at a first temperature and an ashing process occurs at a second temperature, where the first temperature is lower than the second temperature. By way of the present invention, multiple temperatures can be used in a single chamber to perform multiple processes. Details of the present invention are shown by way of Fig. 10, for example.

Fig. 10 is a simplified flow diagram of a heating process according to the present invention. This diagram is merely an illustration and should not limit the scope of the claims herein. One of ordinary skill in the art would recognize other variations, modifications, and alternatives. As shown, an isotropic breakthrough step during which an SF_6 plasma is sued to remove very thin native oxide can be conducted at a low temperature such as room temperature. Ordinarily the breakthrough step is conducted at a high temperature. High temperatures have a serious disadvantage in that the etching rate of both oxide and tungsten silicide by SF_6 may be isotropic. Therefore the duration of the breakthrough step, especially if the native oxide layer is thin, must often be limited to a few seconds to avoid undesired undercut. At low temperature the etching rate is slower and therefore the extent to which materials under the native oxide are etched is easier to control.

At the end of the breakthrough step at time BB, the control program increases within several seconds to a higher steady state value at time C. The tungsten silicide is etched at this temperature until this layer is breached at random locations on the wafer. This endpoint is conveniently observed by a change in the slope of intensity of an optical light emission from the plasma such as optical emission at 530nm (point C in Fig. 10). The complete removal of the unmasked tungsten silicide areas is similarly signaled by a change in light emission such as that shown at point D (at time D all "patches" of the tungsten silicide are "cleared" from unmasked polysilicon areas; the signal begins to rapidly decease at time D because at constant temperature, polysilicon consumes chlorine more rapidly than tungsten silicide (e.g. a faster etch rate) and optical emission at this wavelength originates from a chlorine species.

Since it is not practical to change chuck temperature, at this point the etch rate would increase rapidly. As a consequence it can often be difficult to detect and terminate the polysilicon etching step when the thin oxide layer is reached. Another

problem associated with the use of a single temperature for both silicide and polysilicon layers is that chlorine etching processes often undercut (etch along the mask direction, sideways- e.g. the etch is partly isotropic) silicon at the elevated temperatures suitable for a low residue tungsten silicide etch. Therefore it is highly desirable and advantageous to reduce the etching temperature during the polysilicon etch. The wafer temperature is gradually reduced at point DD in order to achieve a slower and more anisotropic polysilicon etching step. The temperature necessary to etch tungsten silicide and during this temperature programmed sequence are compared in the Fig. The emission signal intensity increases when the temperature is lowered because the rate of consumption of chlorine species by the etching process is slowed (the rate decreases with decreasing temperature). Stopping the etch process at endpoint where all of the silicon has "cleared," denoted by E is also easier and less critical because attack on the oxide has also slowed.

At point H the stack etch is complete and the plasma is extinguished. The flow of feed gas comprising Cl_2 for etching is stopped and a flow of O_2 is started. A plasma discharge in oxygen at elevated temperatures will strip resist rapidly. At time I the wafer temperature is increased rapidly to a selected value in the range 180-220° C and a plasma is ignited to remove the resist. After a selected interval the plasma is extinguished again and the chuck temperature rapidly lowered. These sequences of steps merely provide an example of the present invention. Other examples can also occur and the description above should not be limiting in any manner.

While the invention has been described with reference to specific embodiments, various alternatives, modifications, and equivalents may be used. In fact, the invention also can be applied to almost any type of plasma discharge apparatus. This discharge apparatus can include an apparatus for plasma immersion ion implantation or growing diamonds, TCPs, and others. This discharge apparatus can be used for the manufacture of flat panel displays, disks, integrated circuits, diamonds, semiconductor materials, bearings, raw materials, and the like. Therefore, the above description should not be taken as limiting the scope of the invention which is defined by the appended claims.

WHAT IS CLAIMED IS:

1. A method of etching a substrate in the manufacture of a device, said method comprising steps of:

placing a substrate having a film thereon on a substrate holder in a chamber, said substrate holder having a selected thermal mass; and

performing a first etching of a first portion of said film at a first temperature and performing a second etching of a second portion of said film at a second temperature, said first temperature being different from said second temperature;

wherein said selected thermal mass allows a change from said first temperature to said second temperature within a characteristic time period to process said film.

2. The method of claim 1 wherein said first temperature is changed to said second temperature by a heat transfer means coupled to said substrate holder.

3. The method of claim 1 wherein said change in temperature is an in-situ process during said first etching step and said second etching step.

4. The method of claim 1 wherein said first etching and said second etching are conducted in a substantially constant plasma environment.

5. The method of claim 1 wherein said first temperature is higher than said second temperature.

6. The method of claim 1 wherein said first temperature is lower than said second temperature.

7. The method of claim 1 wherein said first etching comprises radiation.

8. The method of claim 1 wherein said second etching comprises radiation.

9. The method of claim 1 wherein said first etching is an ion bombardment aided process.

10. The method of claim 1 wherein said second etching is an ion bombardment aided process.

11. The method of claim 1 wherein said first portion of said film is etched before said second portion of said film.

12. The method of claim 1 wherein said second portion of said film is etched before said first portion of said film.

13. Apparatus for etching a substrate in the manufacture of a device, said apparatus comprising:

a chamber;

a substrate holder disposed in said chamber, said substrate holder having a selected thermal mass;

wherein said selected thermal mass of said substrate holder allows for a change from a first temperature to a second temperature within a characteristic time period to process a film.

14. Apparatus of claim 13 further comprising a heat transfer means for changing said first temperature to said second temperature, said heat transfer means being coupled to said substrate holder.

15. Apparatus of claim 13 wherein said change in temperature is an in-situ process within said characteristic time.

16. Apparatus of claim 13 wherein said chamber provides a substantially constant plasma environment.

17. Apparatus of claim 13 wherein said first temperature is higher than said second temperature.

18. Apparatus of claim 13 wherein said first temperature is lower than said second temperature.

19. Apparatus of claim 13 wherein said chamber provides radiation.

20. Apparatus of claim 13 wherein said chamber provides an ion bombardment aided process.

MULTI-TEMPERATURE PROCESSING

ABSTRACT OF THE DISCLOSURE

The present invention provides a technique, including a method and apparatus, for etching a substrate in the manufacture of a device. The apparatus includes a chamber and a substrate holder disposed in the chamber. The substrate holder has a selected thermal mass to facilitate changing the temperature of the substrate to be etched during etching processes. That is, the selected thermal mass of the substrate holder allows for a change from a first temperature to a second temperature within a characteristic time period to process a film. The present technique can, for example, provide different processing temperatures during an etching process or the like.

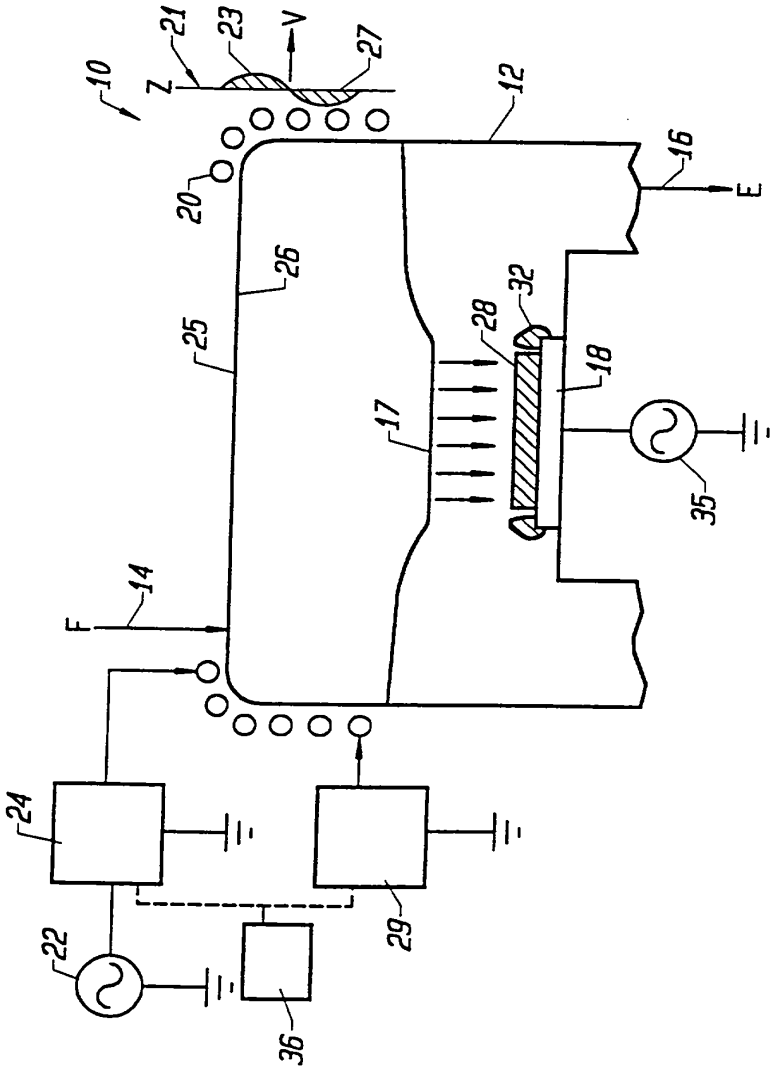


FIG. 1

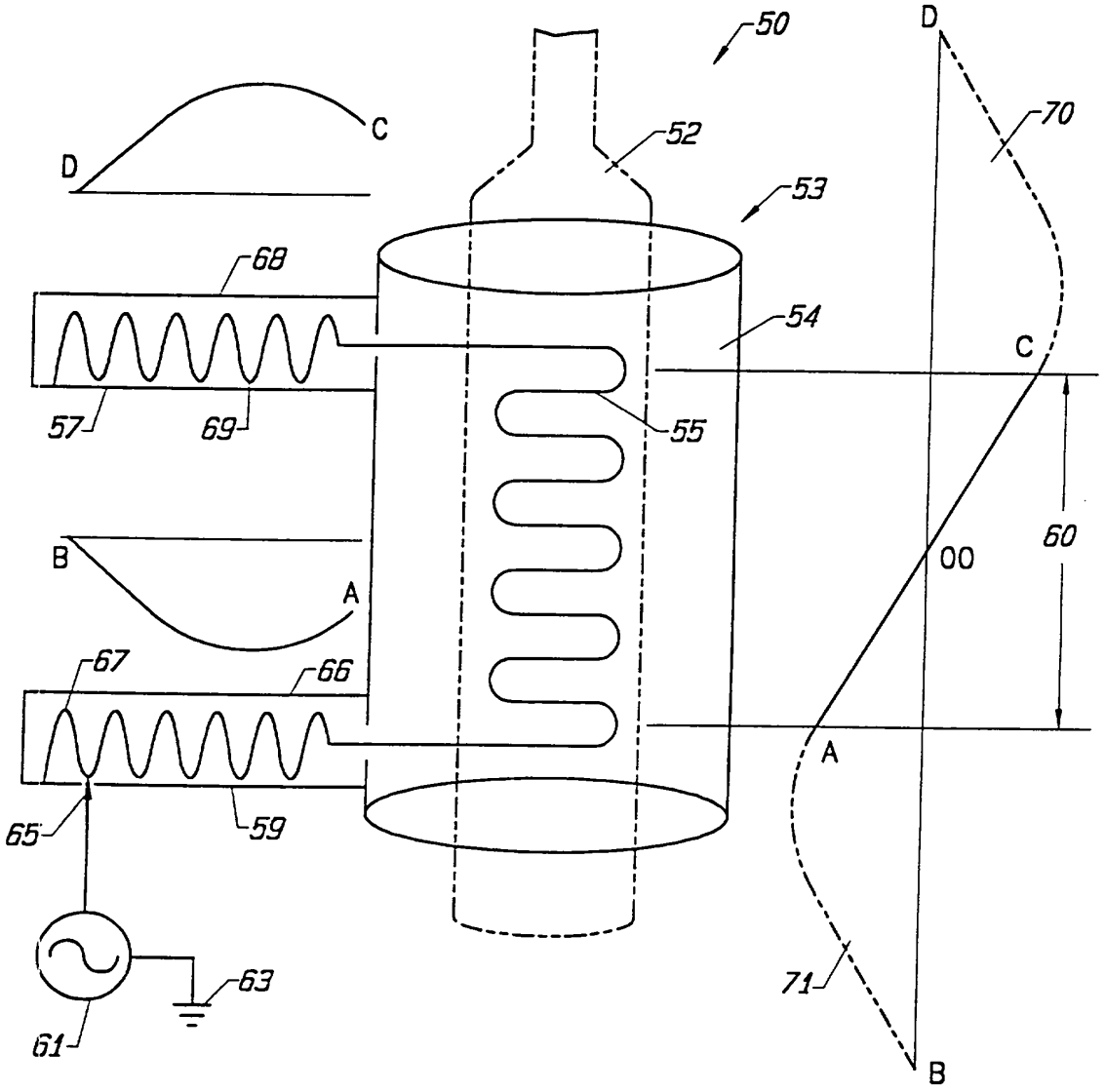


FIG. 2A

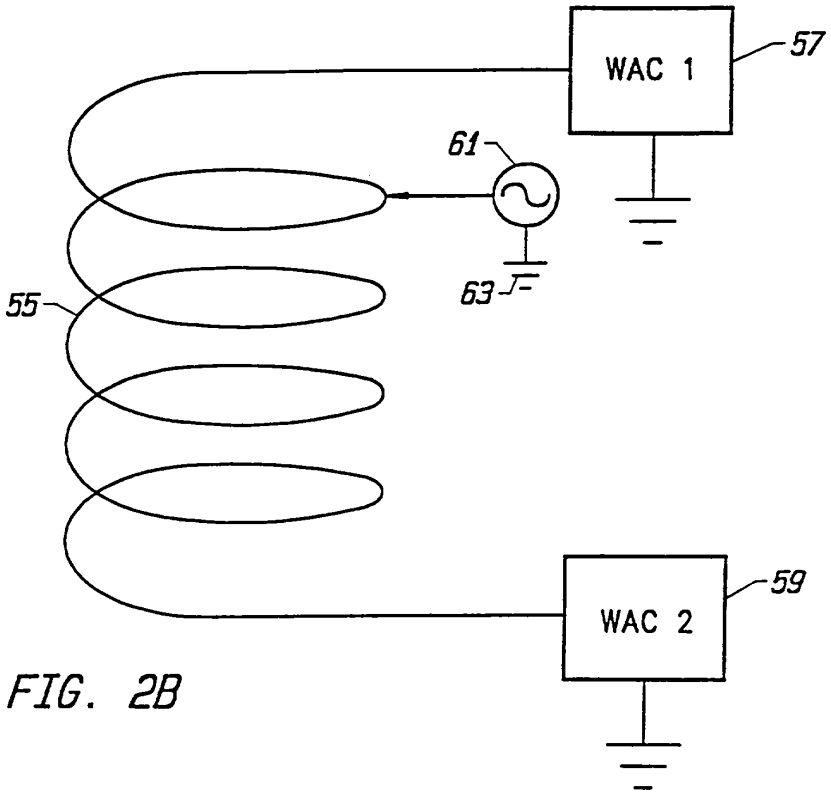


FIG. 2B

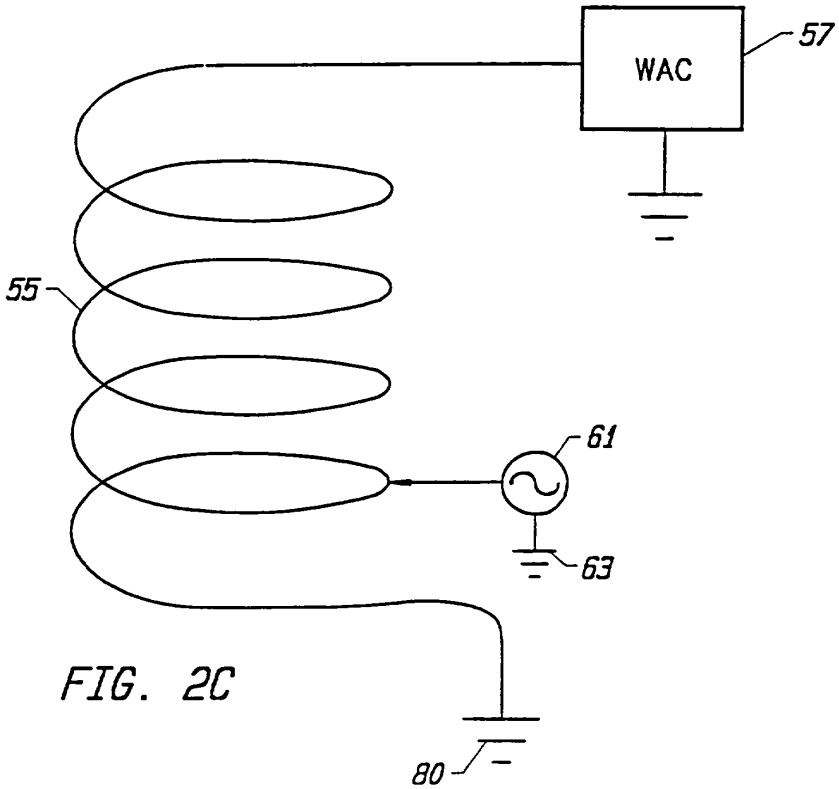


FIG. 2C

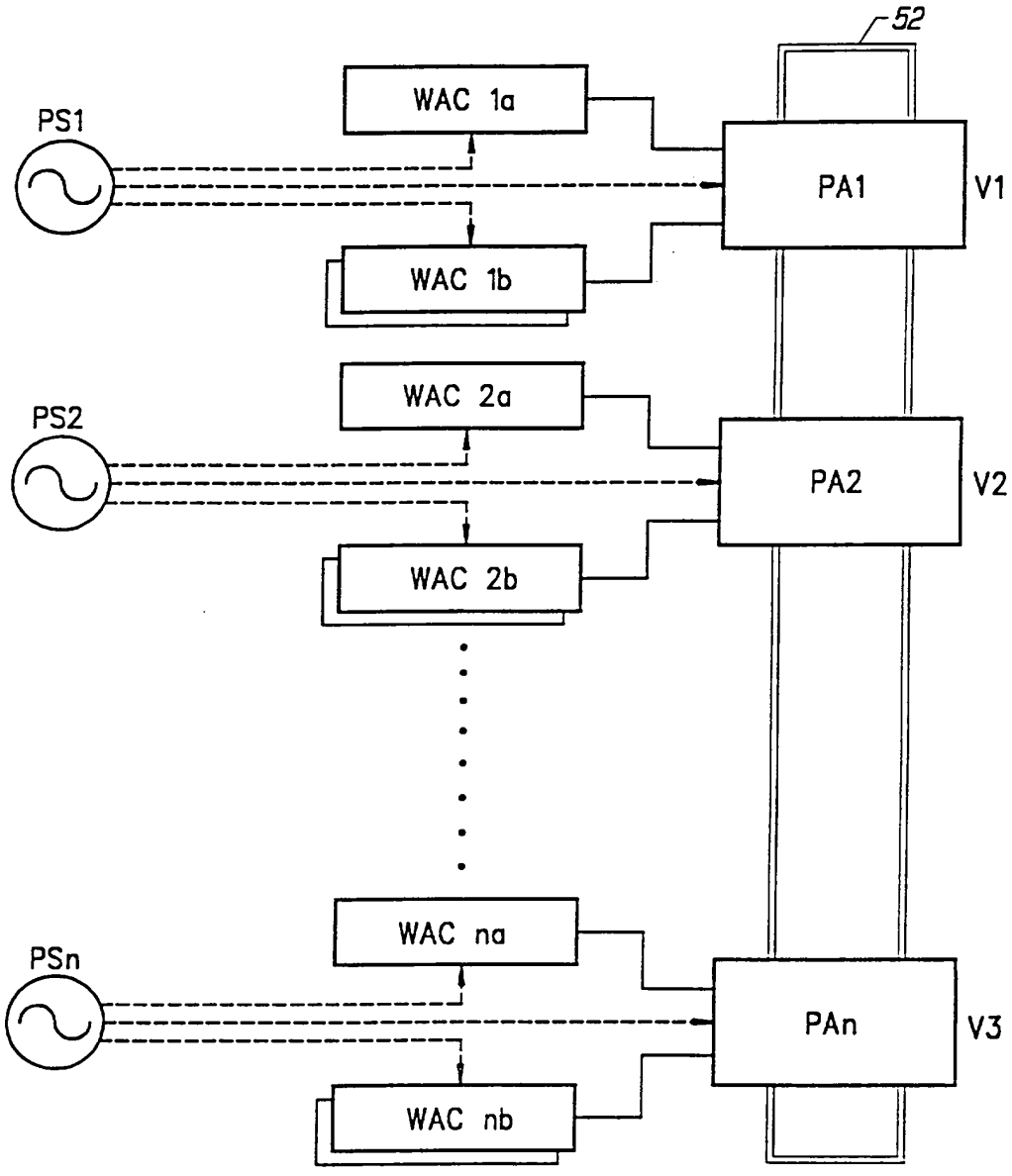


FIG. 2D

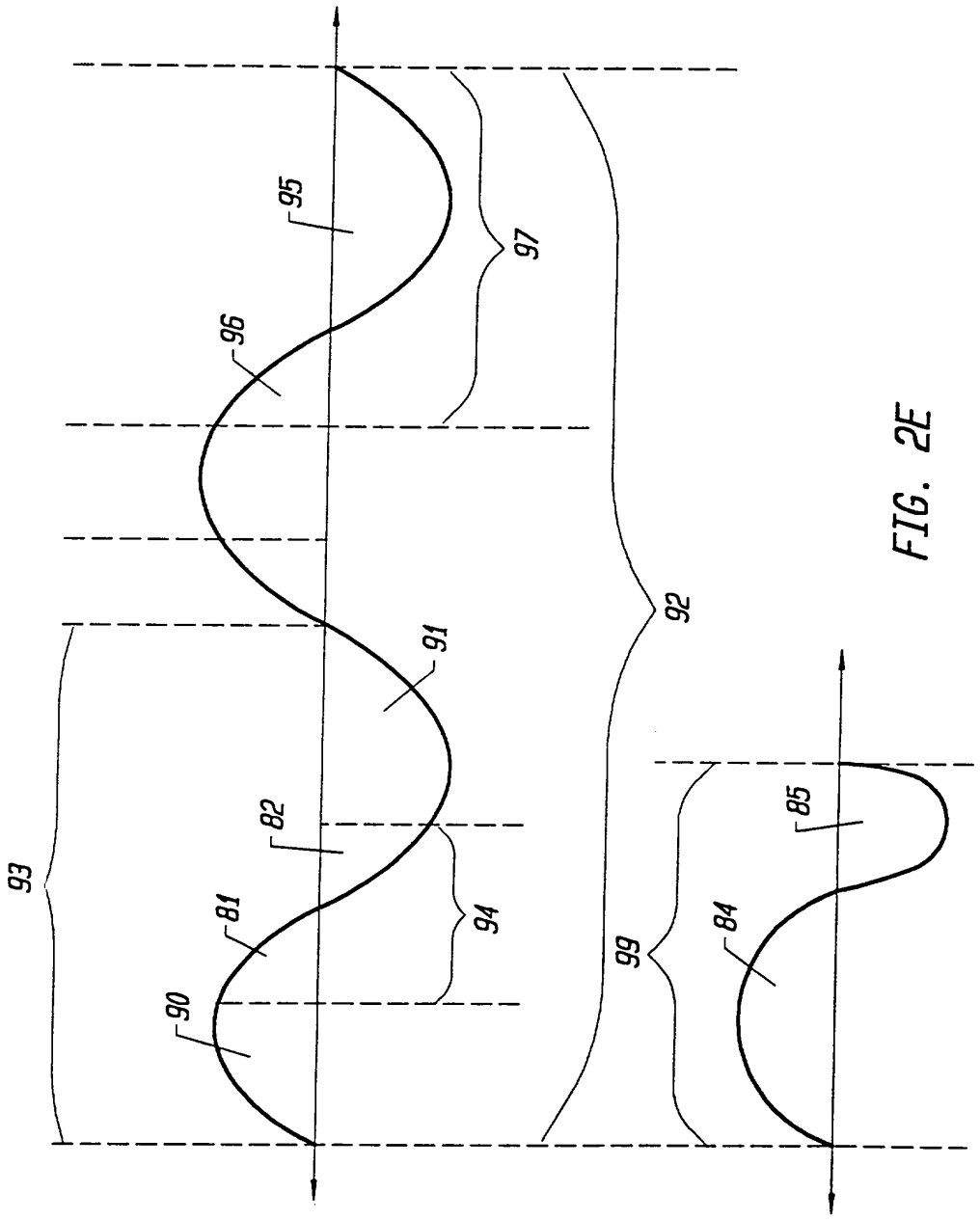


FIG. 2E

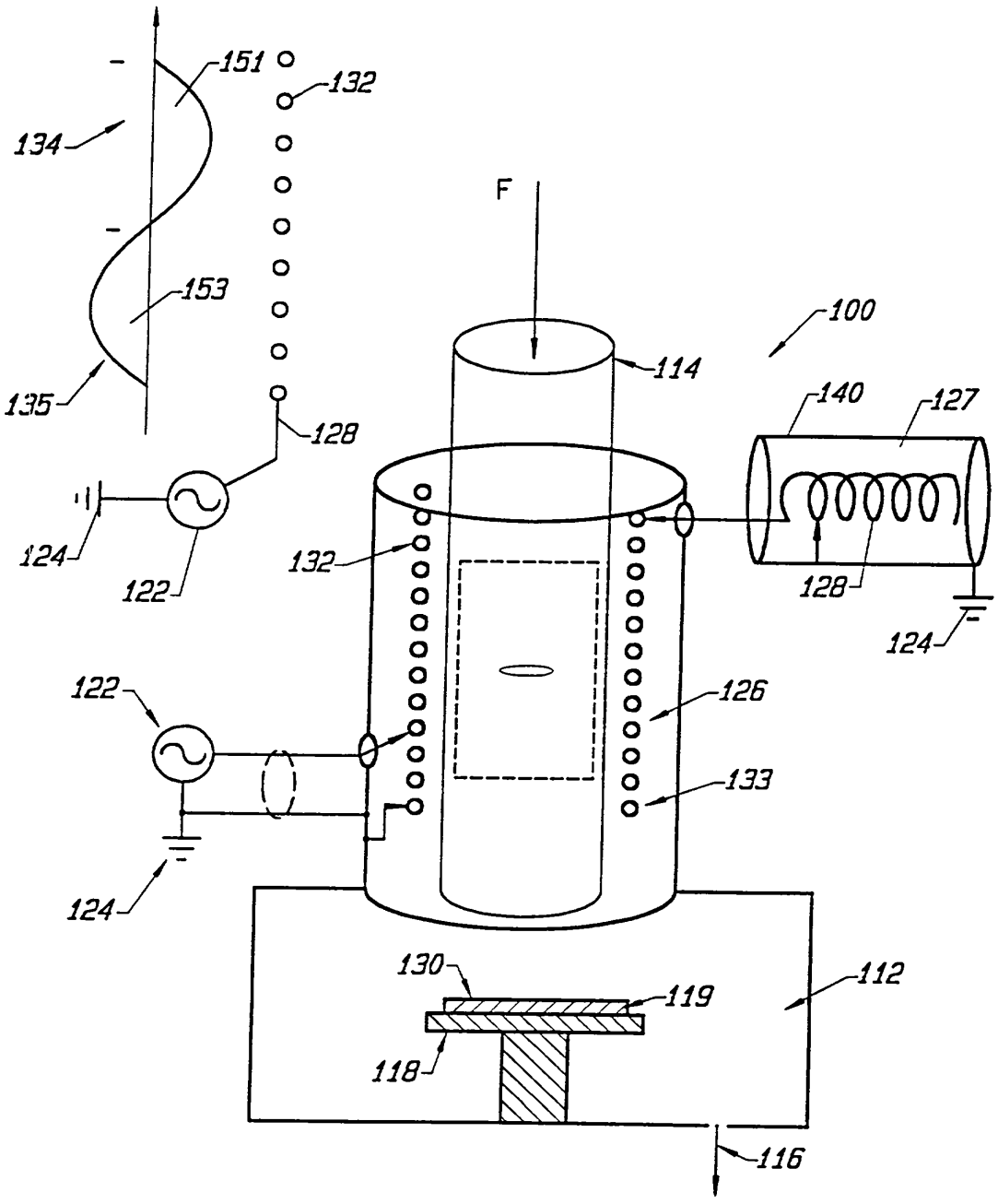

151
132
134
F
153
100
114
135
140
127
128
124
122
132
128
124
122
126
133
124
130
119
112
118
116

FIG. 3

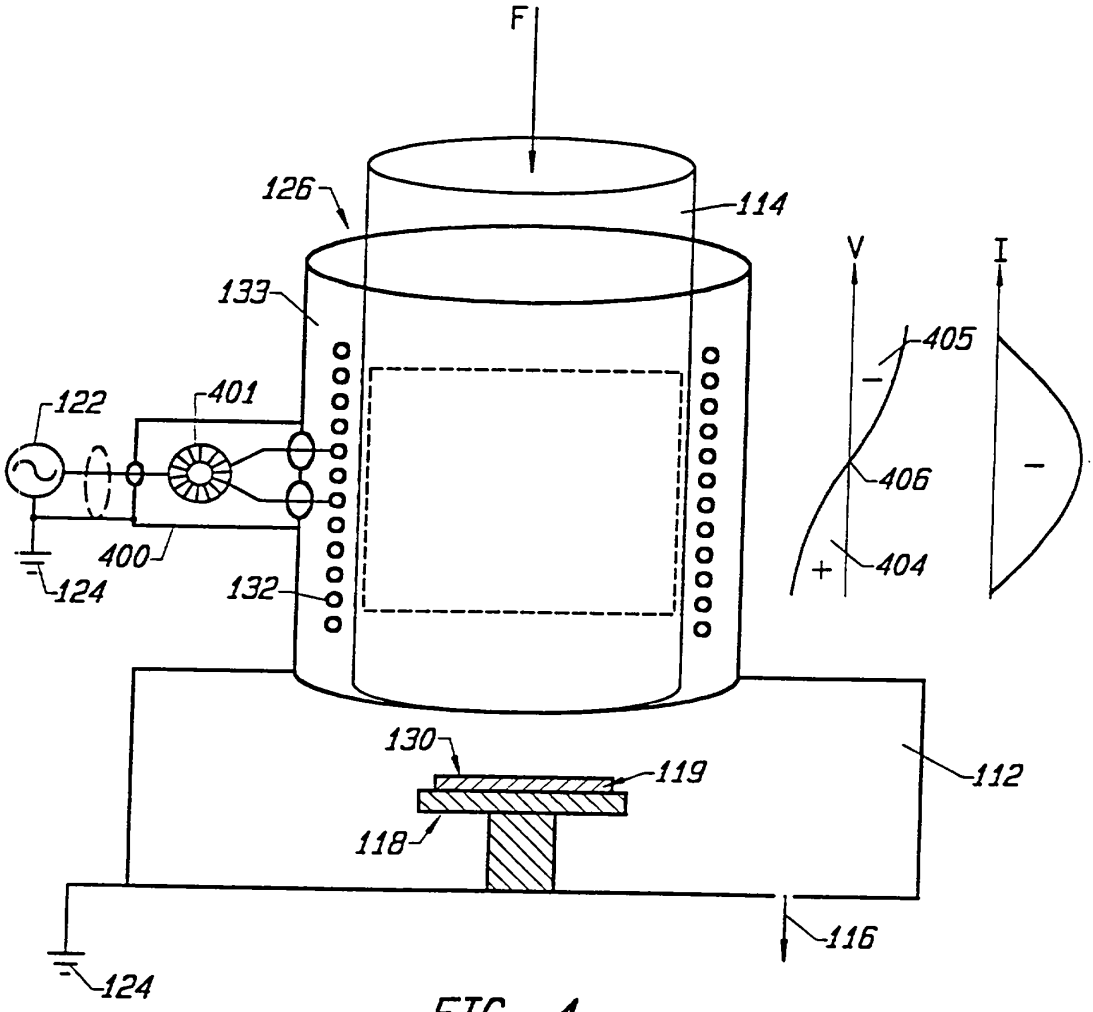

F
126
114
133
122
401
V
I
405
406
404
400
124
132
130
119
112
118
116
124

FIG. 4

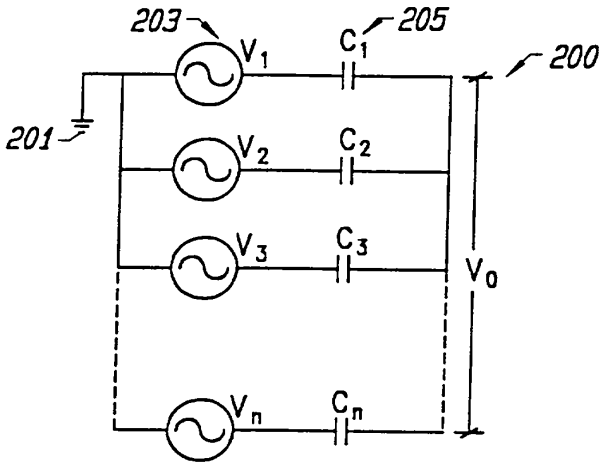


FIG. 5A

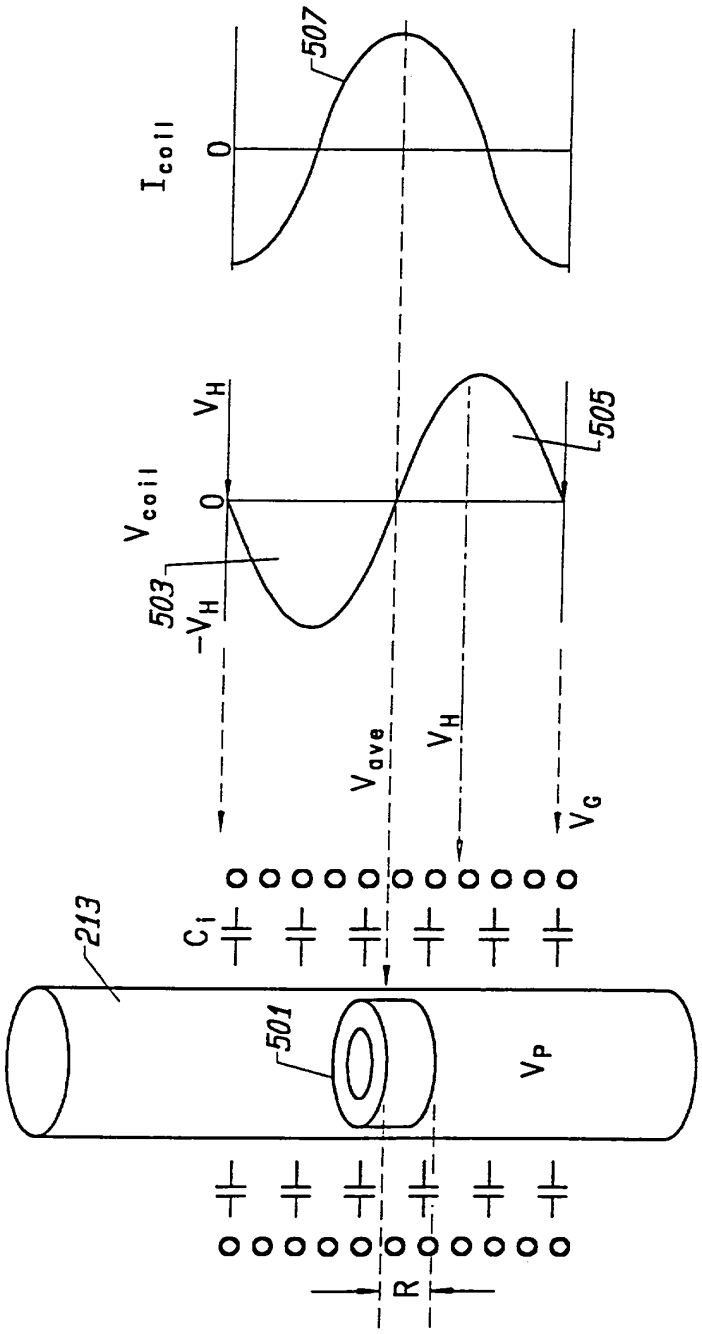


FIG. 5B

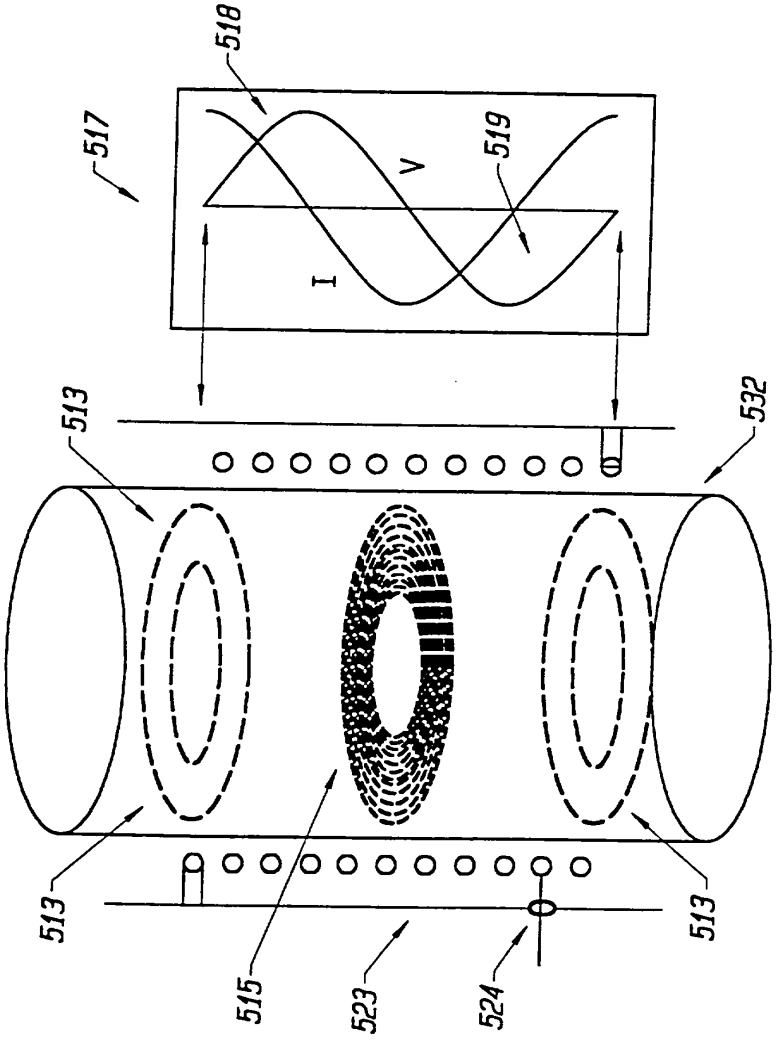


FIG. 5C

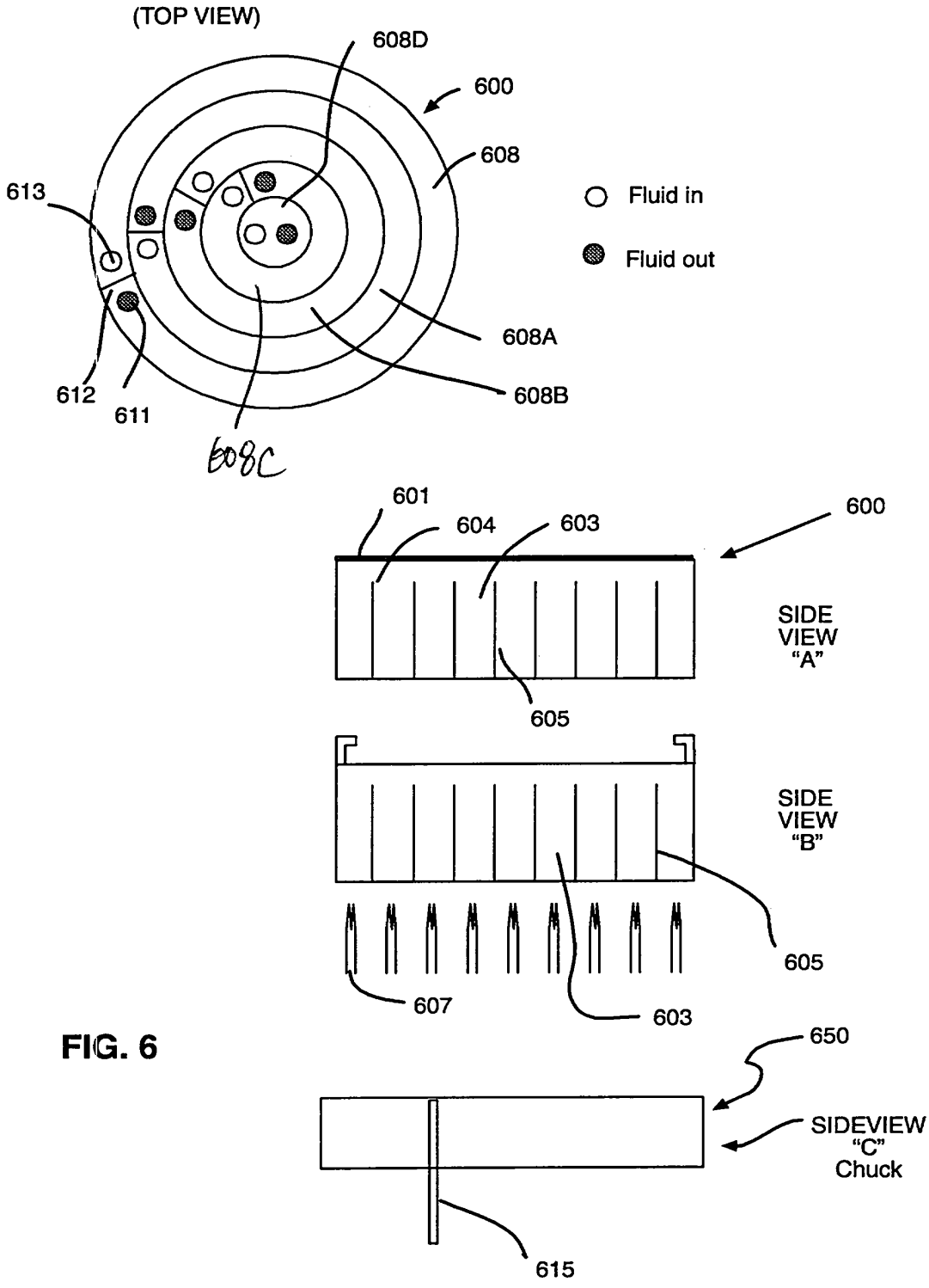

(TOP VIEW)
608D
600
608
613
Fluid in
Fluid out
608A
608B
612
611
608C
601
604
603
600
SIDE VIEW "A"
605
SIDE VIEW "B"
605
607
603
650
SIDEVIEW "C" Chuck
615

FIG. 6

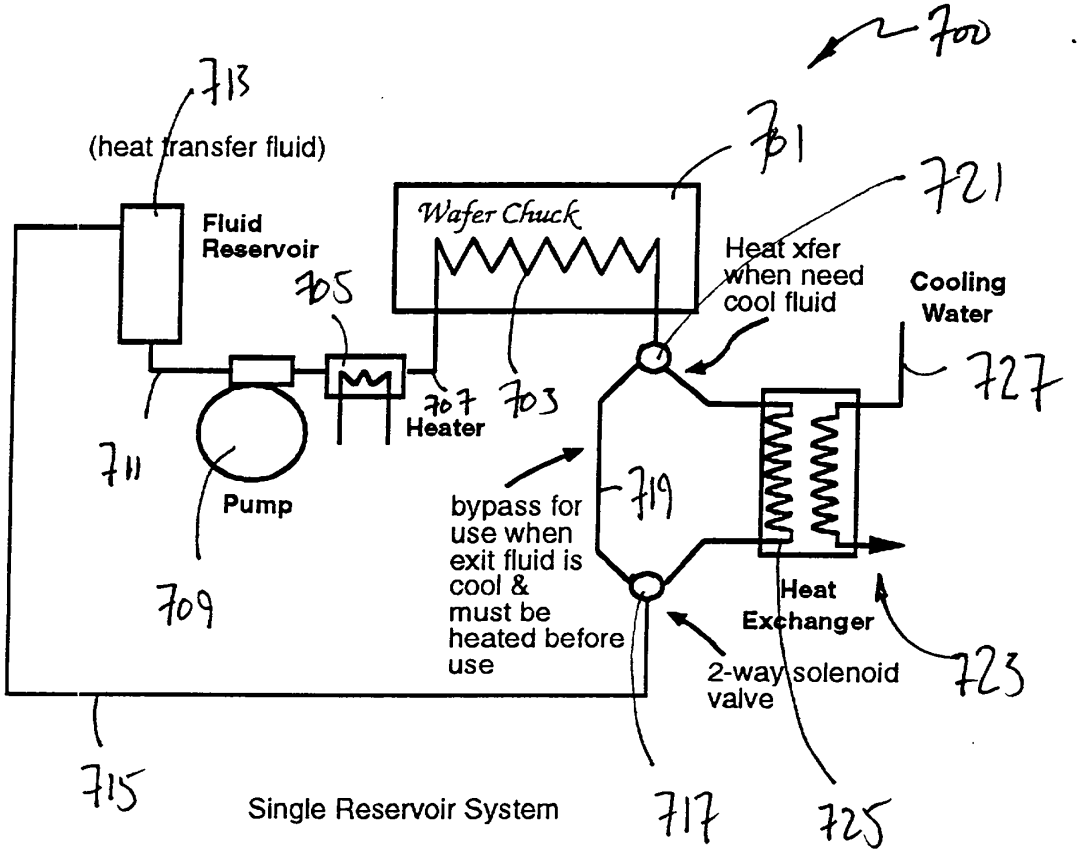

700
713
(heat transfer fluid)
701
721
Fluid Reservoir
Wafer Chuck
Heat xfer when need cool fluid
Cooling Water
705
727
707
Heater
703
711
Pump
bypass for use when exit fluid is cool & must be heated before use
719
Heat Exchanger
723
2-way solenoid valve
709
715
Single Reservoir System
717
725

FIG. 7

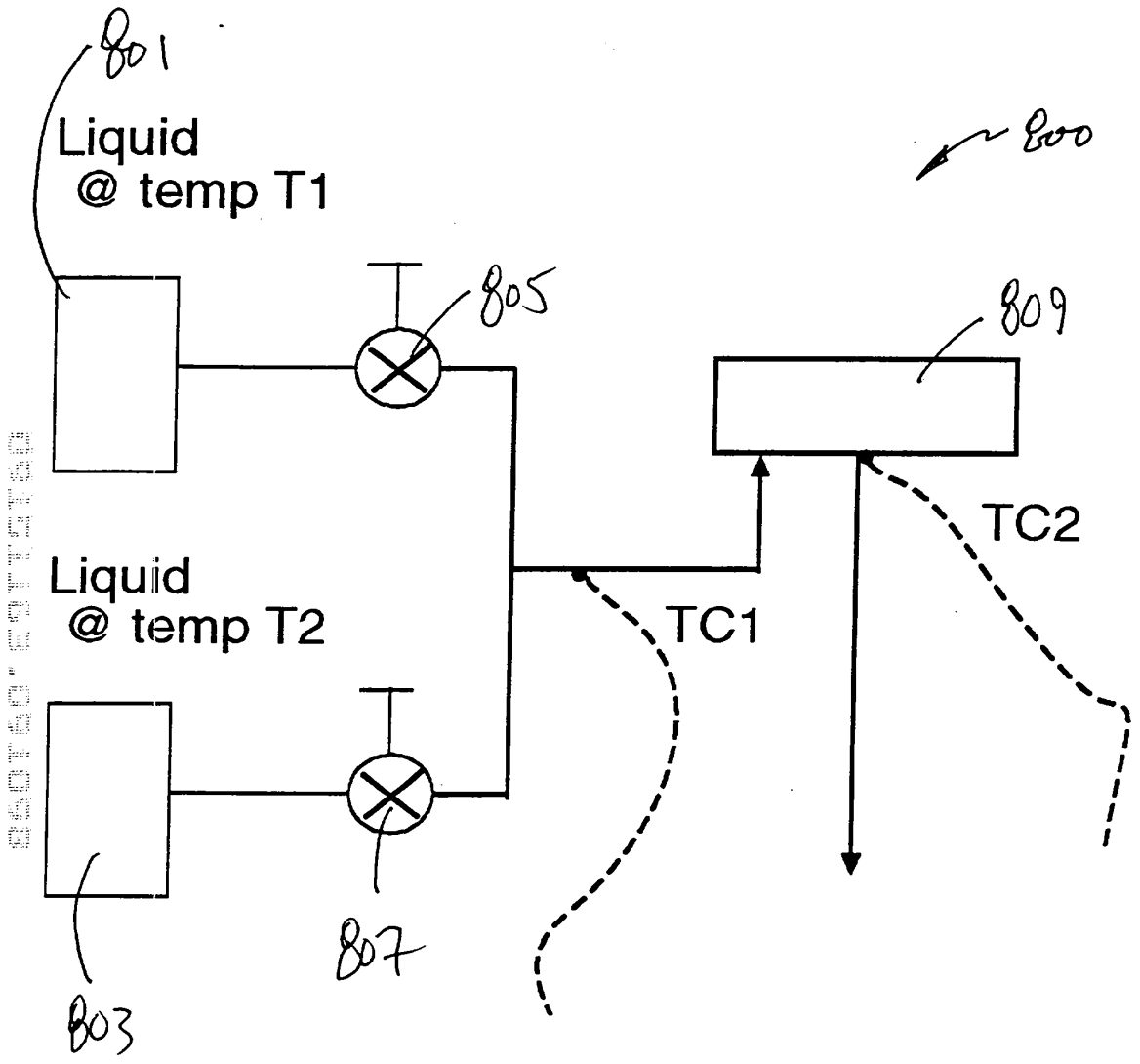


Fig. 8

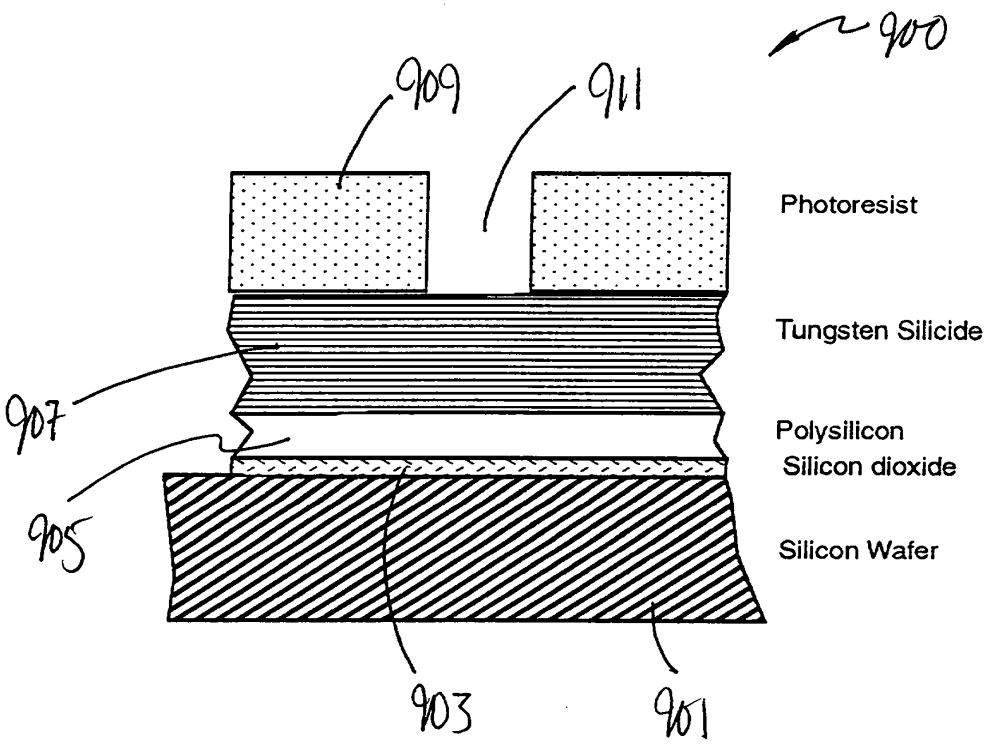
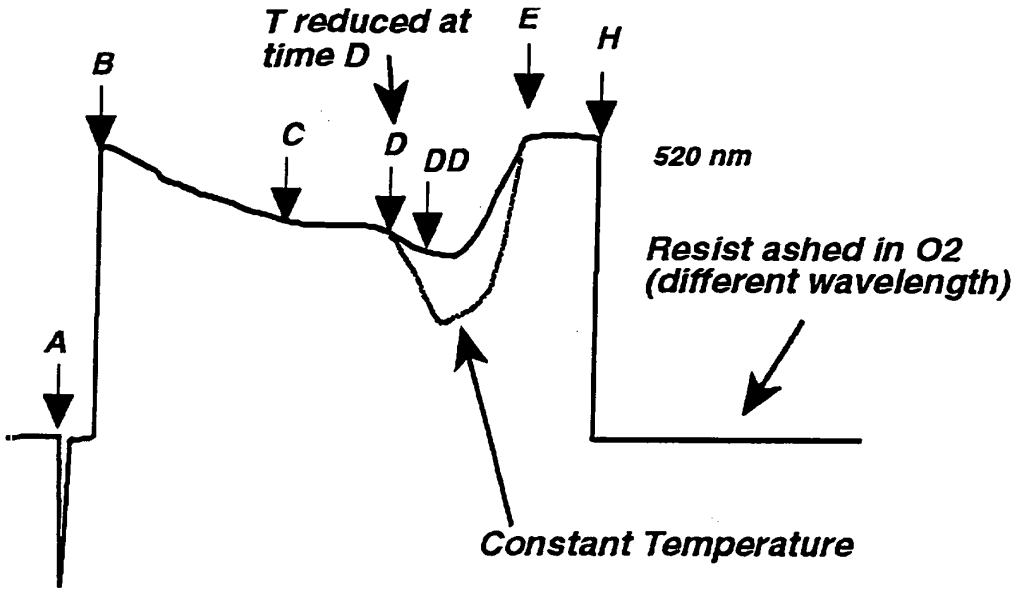
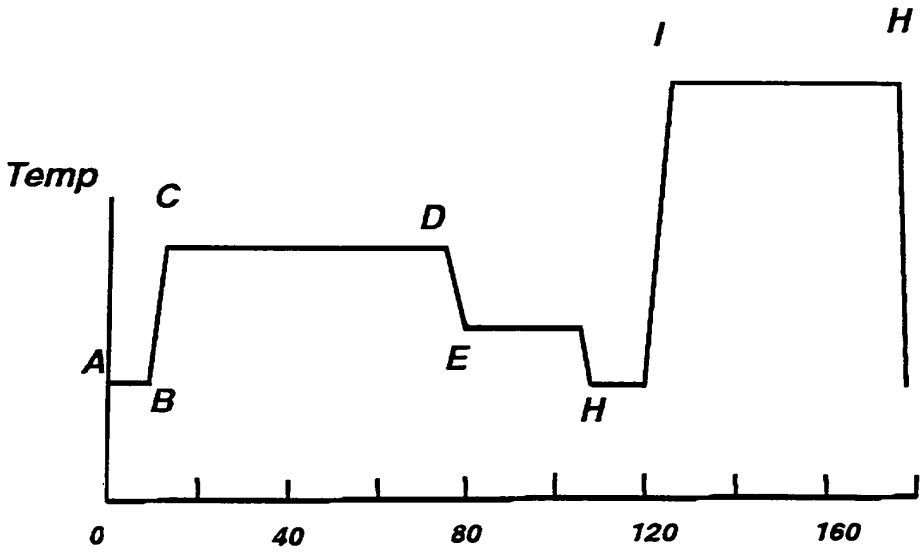

900
909
911
Photoresist
Tungsten Silicide
907
Polysilicon
Silicon dioxide
905
Silicon Wafer
903
901

FIG. 9





A. SF_6 native oxide "breakthrough"
B. Cl_2 plasma is ignited
C. WSi_x begins to clear (endpoint)
D. Polysilicon is exposed
E. Polysilicon cleared to oxide
H. Plasma extinguished and O2 feed gas flow is started
I. O2 plasma is started
J O2 plasma is extinguished.

FIG. 10

PRINT OF DRAWINGS
AS ORIGINALLY FILED

United States Patent & Trademark Office

Office of Initial Patent Examination -- Scanning Division

Application deficiencies found during scanning:

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   - ☐ Papers are not typewritten or mechanically printed in permanent ink on one side.
   - ☐ Papers contain improper margins. Each sheet must have a left margin of at least 2.5 cm (1") and top, bottom and right margins of at least 2.0 cm (3/4").
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   - ☐ The drawings or copy of drawings are not suitable for electronic reproduction.
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APPLICATION TRANSMITTAL

Customer No. 20350
TOWNSEND and TOWNSEND and CREW LLP
Two Embarcadero Center, 8th Floor
San Francisco, CA 94111-3834
(650) 326-2400

Atty. Docket No. 16655-000810

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Date of Deposit September 10, 1998

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Assistant Commissioner for Patents
Washington, D.C. 20231

By BRAD HICK

PATENT APPLICATION
ASSISTANT COMMISSIONER FOR PATENTS
Washington, D. C. 20231

Sir:
Transmitted herewith for filing is the [X] patent application, [ ] design patent application, [ ] continuation-in-part patent application of

Inventor(s): Daniel L. Flamm

For: MULTI-TEMPERATURE PLASMA ETCHING PROCESS

[X] This application claims priority from each of the following Application Nos./filing dates:
60/058,650 / 9/11/97 ; 08/567,224 / 12/4/95 ; _____ / _____.

[ ] Please amend this application by adding the following before the first sentence: --This application claims the benefit of U.S. Provisional Application No. 60/_____, filed _____, the disclosure of which is incorporated by reference.--

Enclosed are:
[X] Patent Application (incl. 30 pages spec., 3 pages claims, 1 page abstract).
[X] 15 sheet(s) of [ ] formal [X] informal drawing(s).
[ ] An assignment of the invention to _____.
[ ] A [ ] signed [ ] unsigned Declaration & Power of Attorney.
[ ] A verified statement to establish small entity status under 37 CFR 1.9 and 37 CFR 1.27 [ ] is enclosed [ ] was filed in the earliest of the above-identified patent application(s).
[ ] A certified copy of a _____ application.
[ ] Information Disclosure Statement under 37 CFR 1.97.
[ ] A petition to extend time to respond in the parent application of this continuation-in-part application.
[X] Postcard.

Pursuant to 37 CFR 1.53(d), Applicant requests deferral of the filing fee until submission of the Missing Parts of Application.

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2 extra copies of this sheet are enclosed.

Respectfully submitted,
TOWNSEND and TOWNSEND and CREW LLP

Richard T. Ogawa
Reg. No.: 37,692
Attorneys for Applicant

Telephone:
(650) 326-2400
16655\8-1app.trn

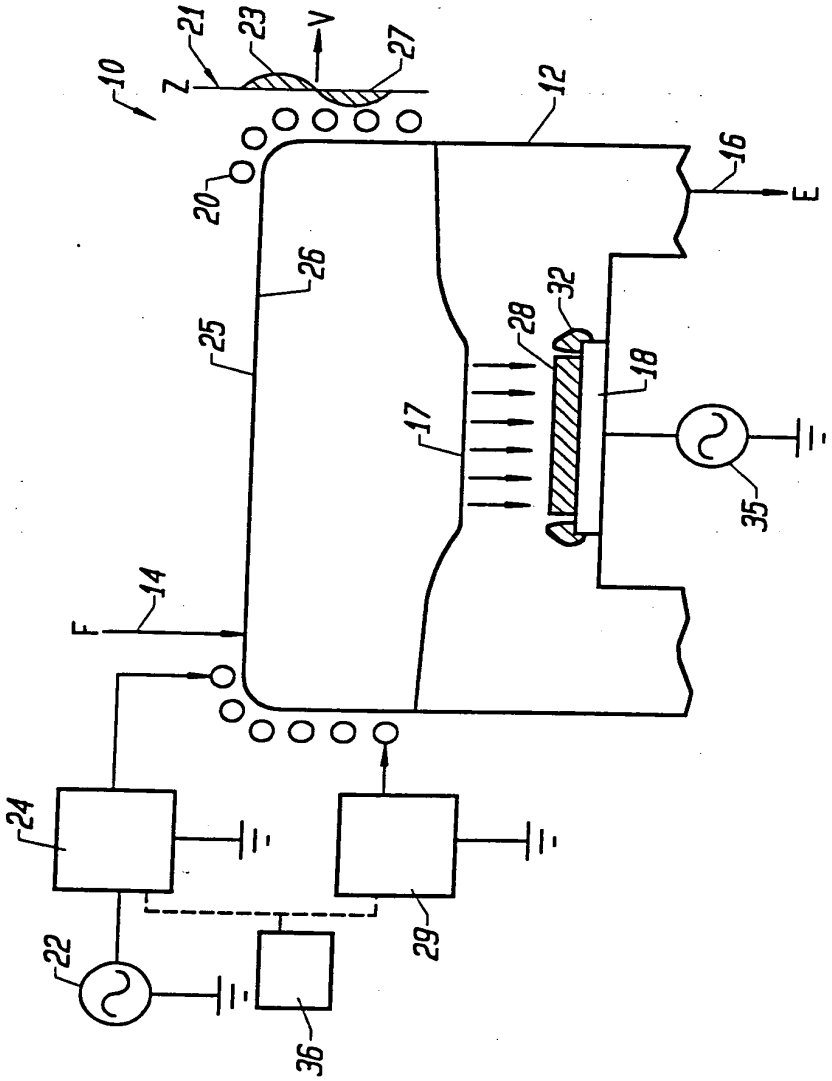


FIG. 1

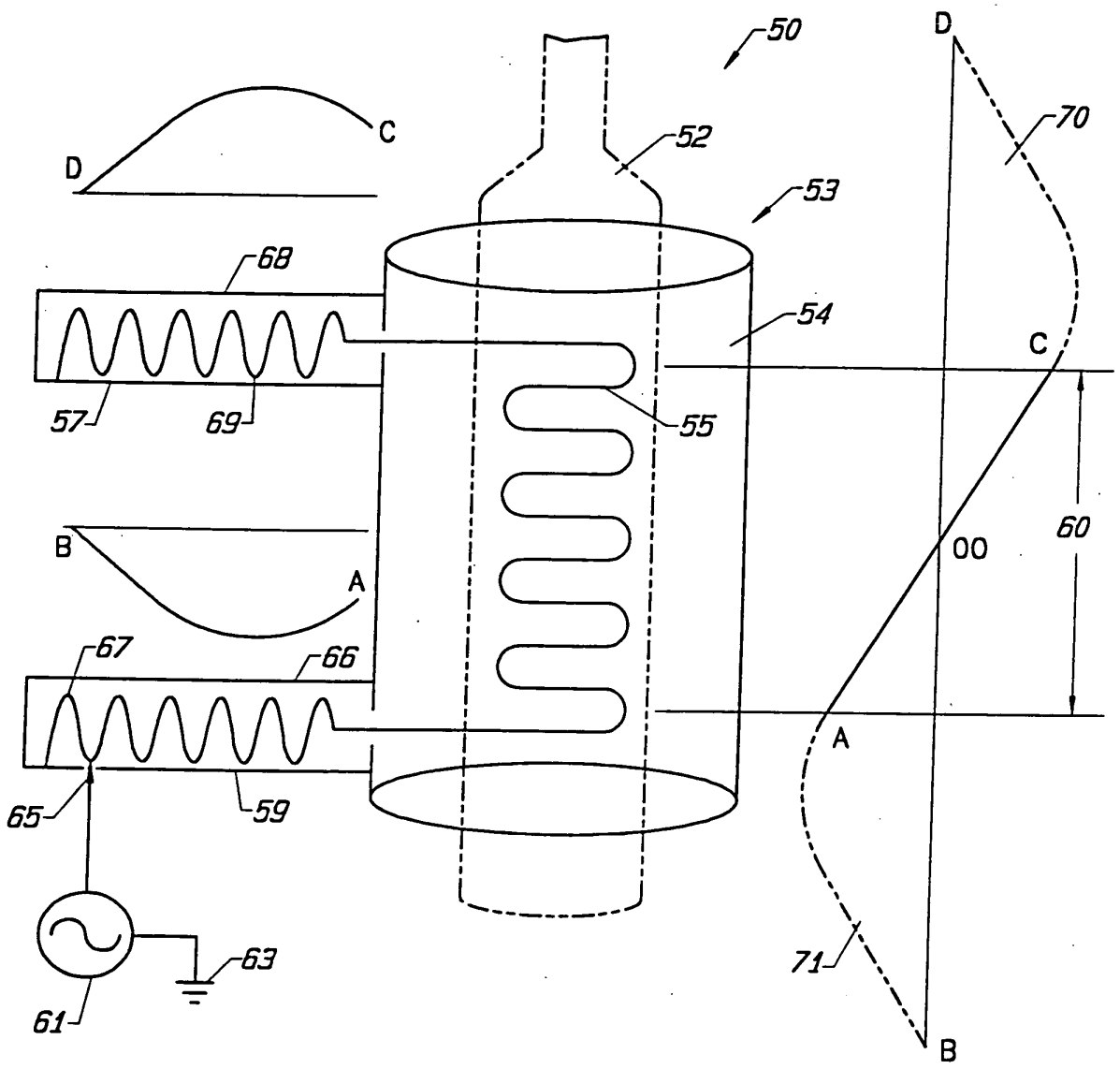


FIG. 2A

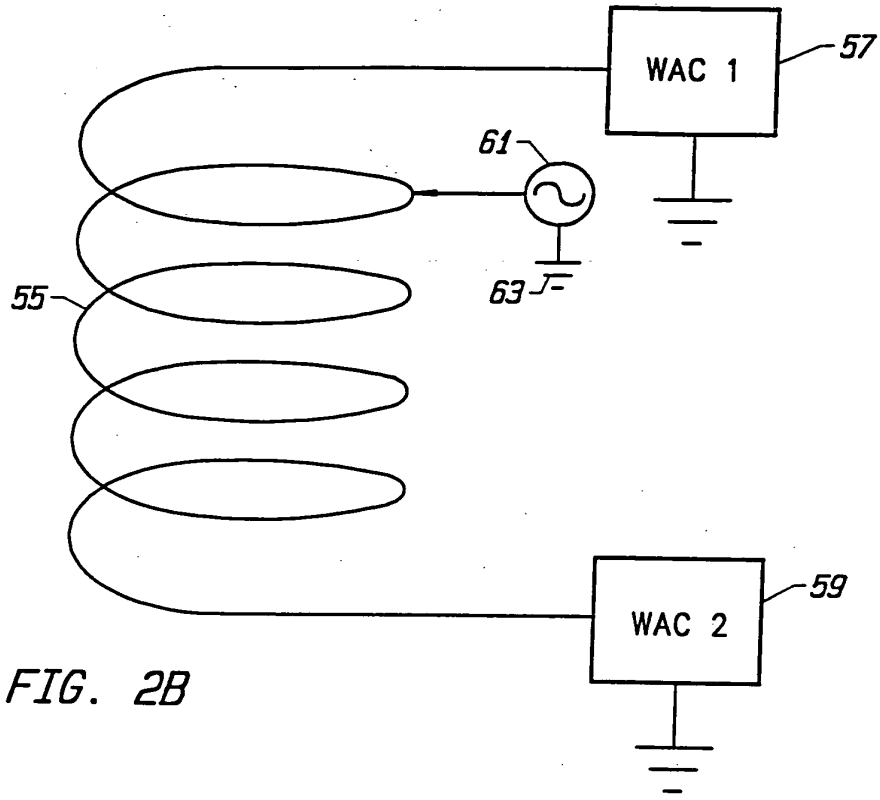


FIG. 2B

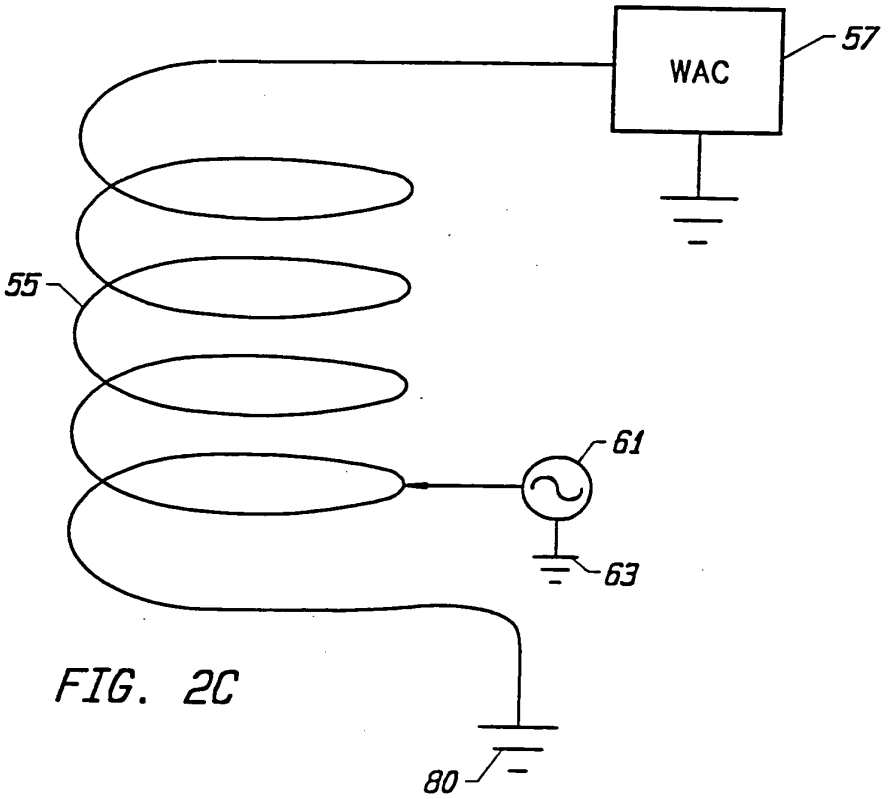


FIG. 2C

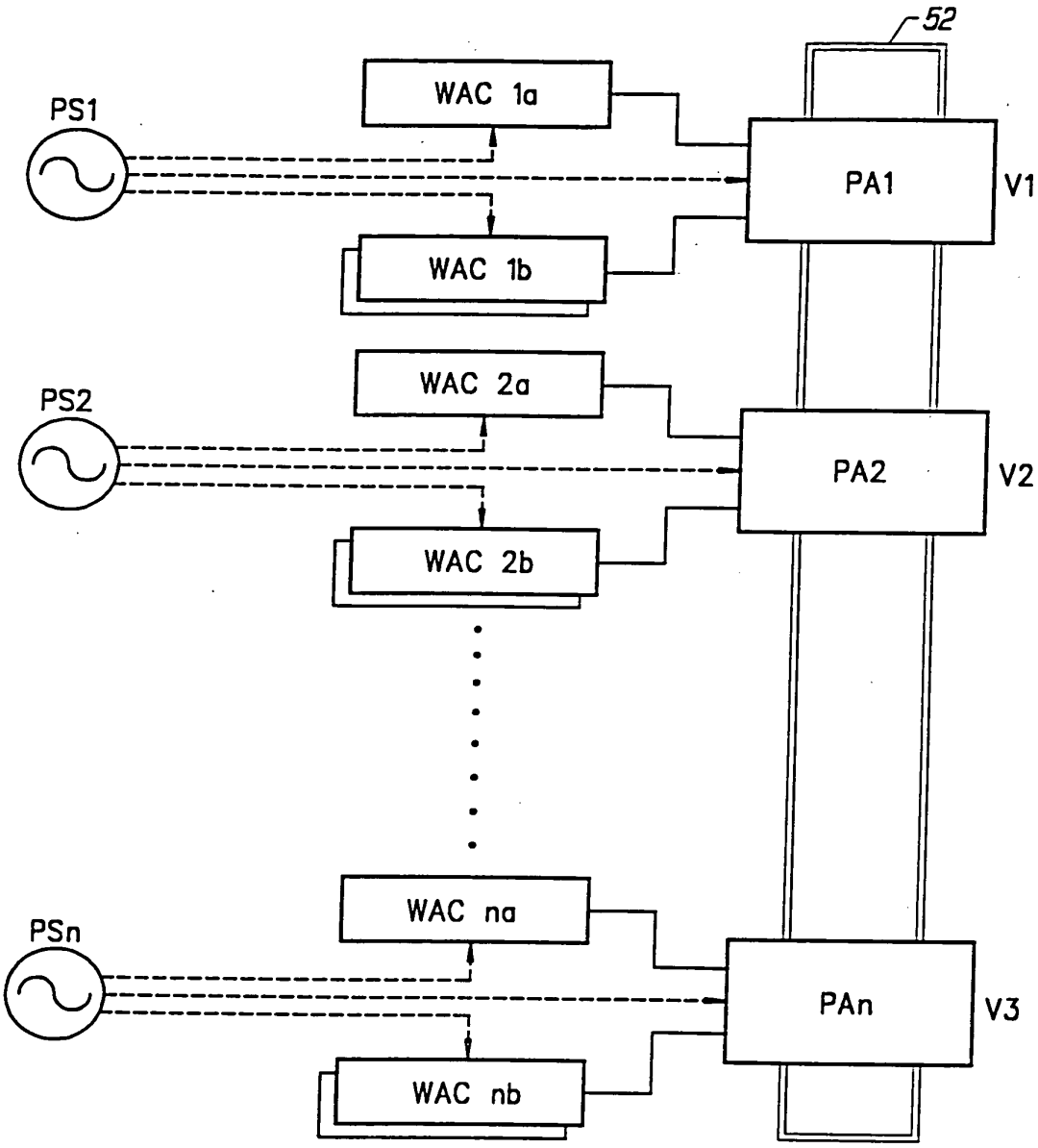

52
WAC 1a
PS1
PA1
V1
WAC 1b
WAC 2a
PS2
PA2
V2
WAC 2b
WAC na
PSn
PAn
V3
WAC nb

FIG. 2D

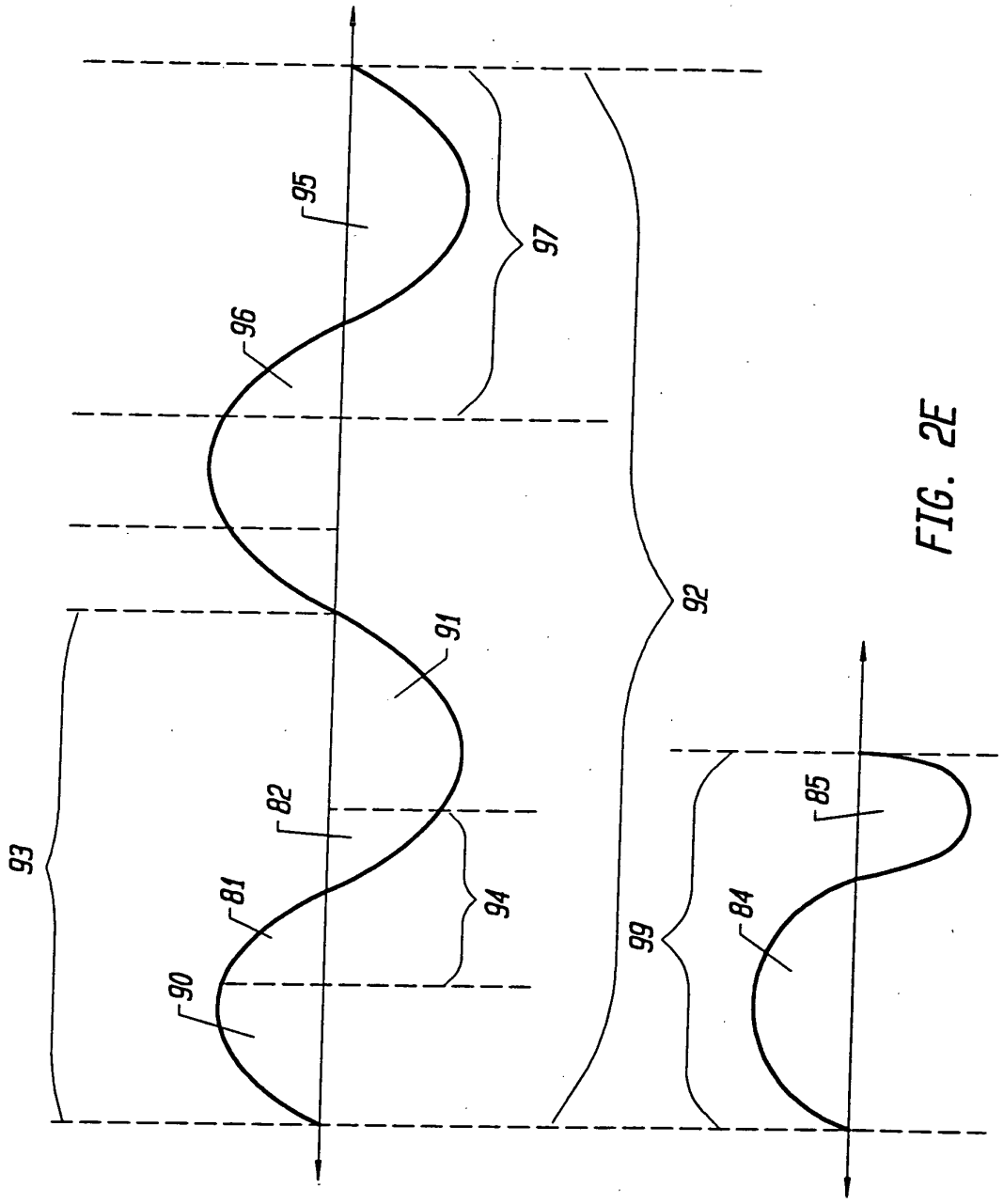


FIG. 2E

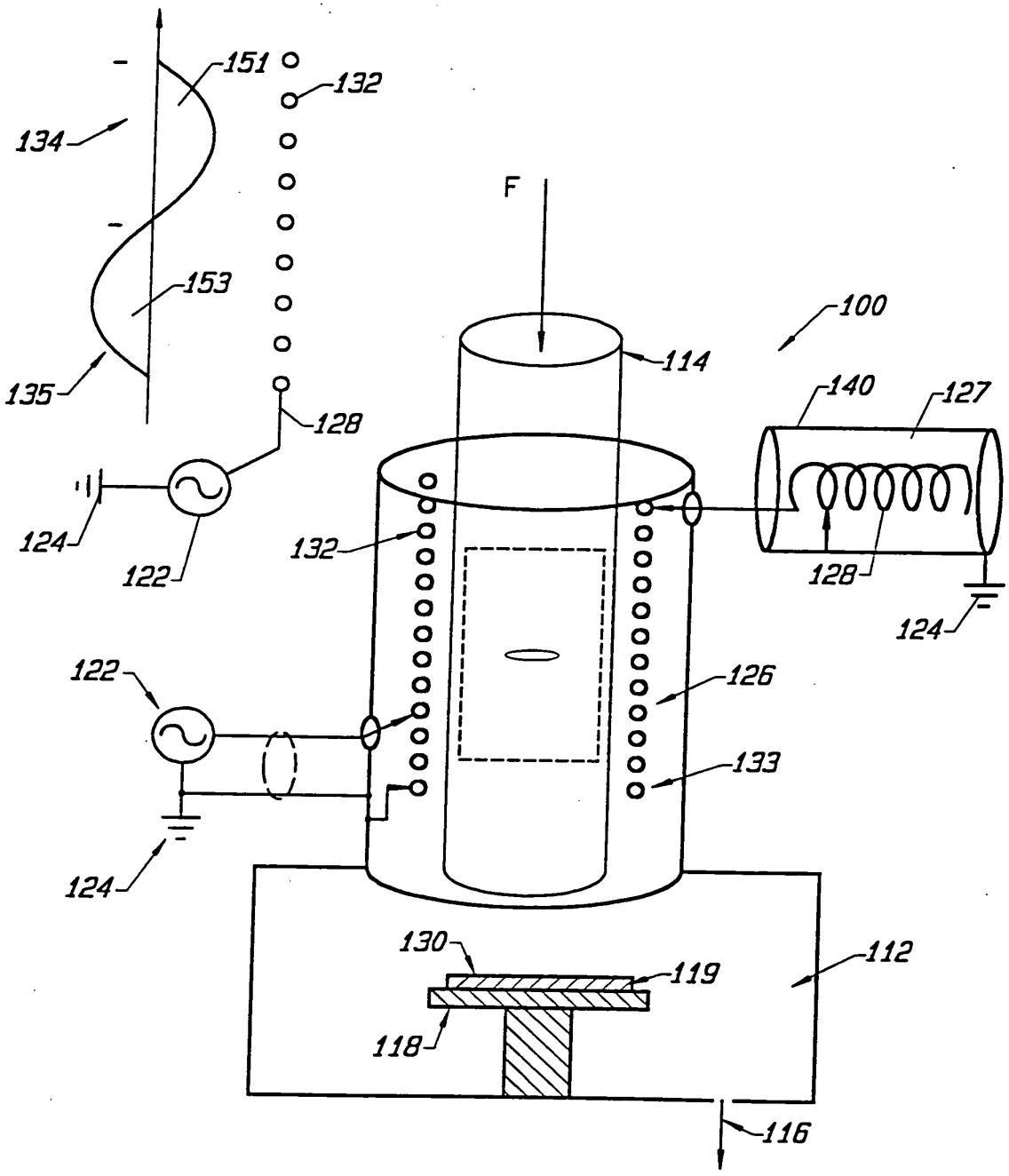


FIG. 3

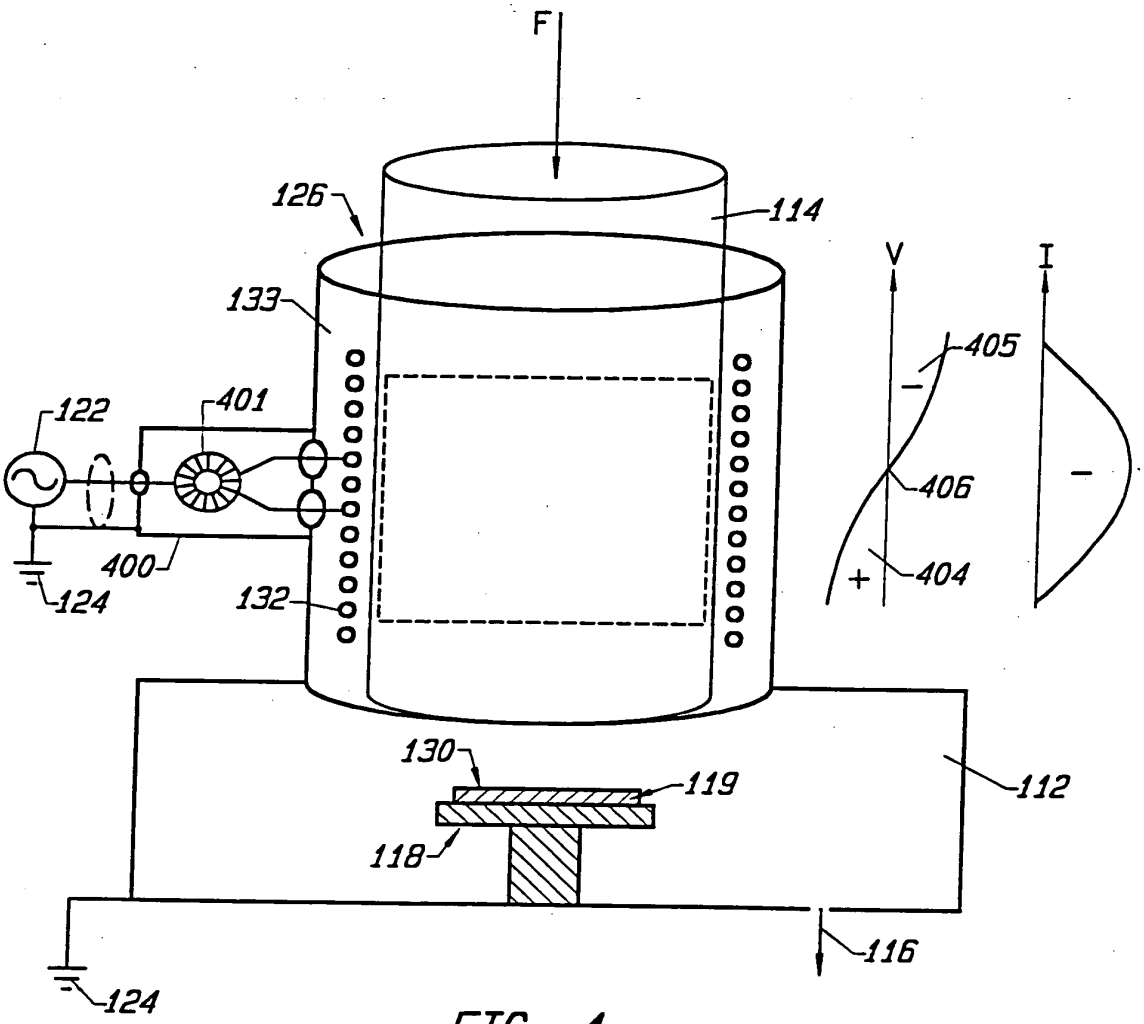

F
126
114
133
122
401
405
V
I
406
404
400
124
132
130
119
112
118
116
124

FIG. 4

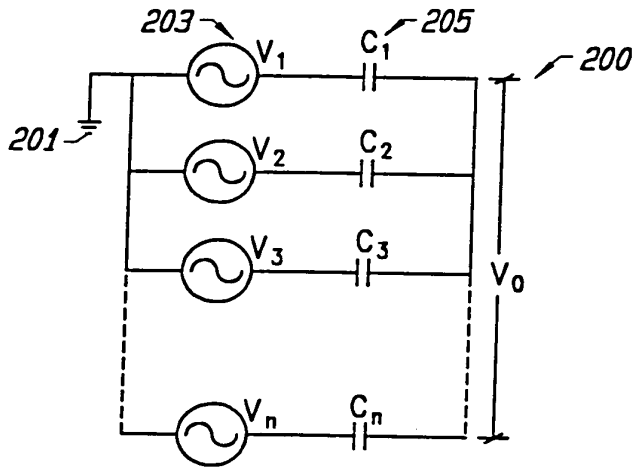


FIG. 5A

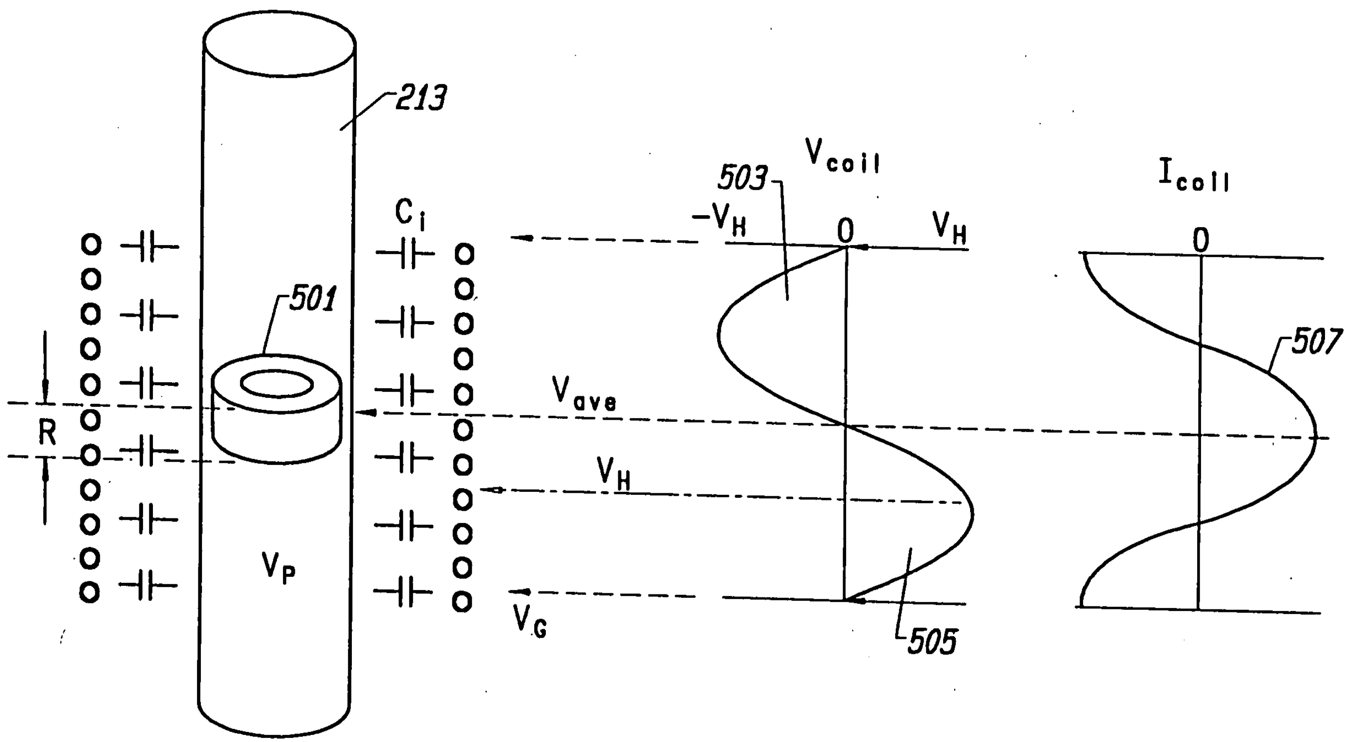


FIG. 5B

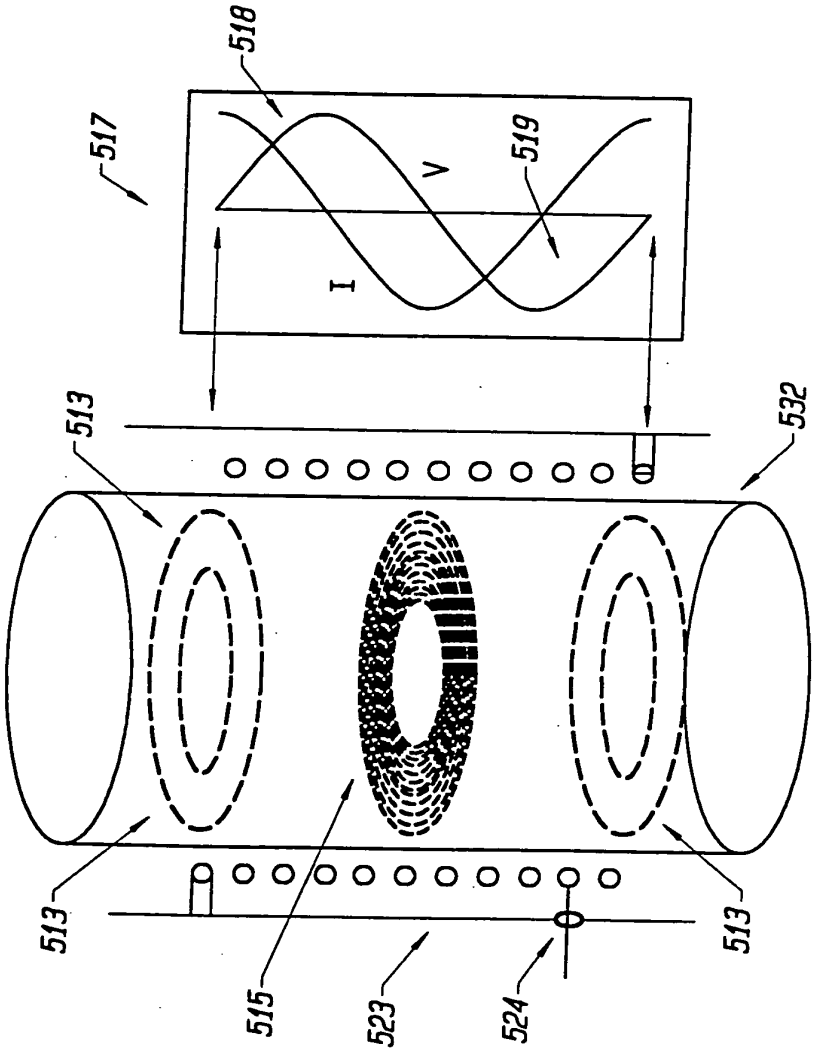


FIG. 5C

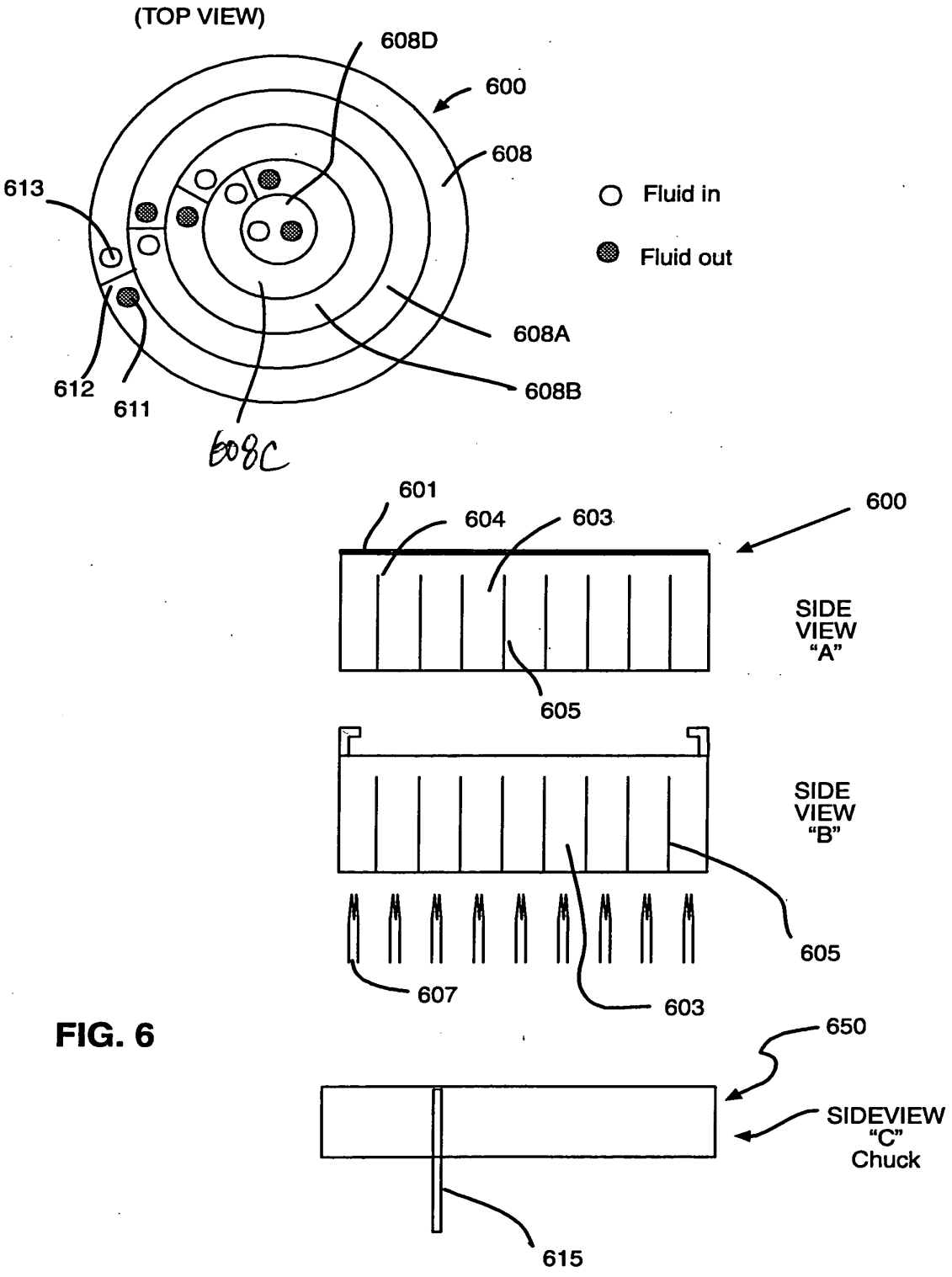

(TOP VIEW)
608D
600
608
613
Fluid in
Fluid out
608A
608B
612
611
608C
601
604
603
600
SIDE VIEW "A"
605
SIDE VIEW "B"
605
607
603
650
SIDEVIEW "C" Chuck
615

FIG. 6

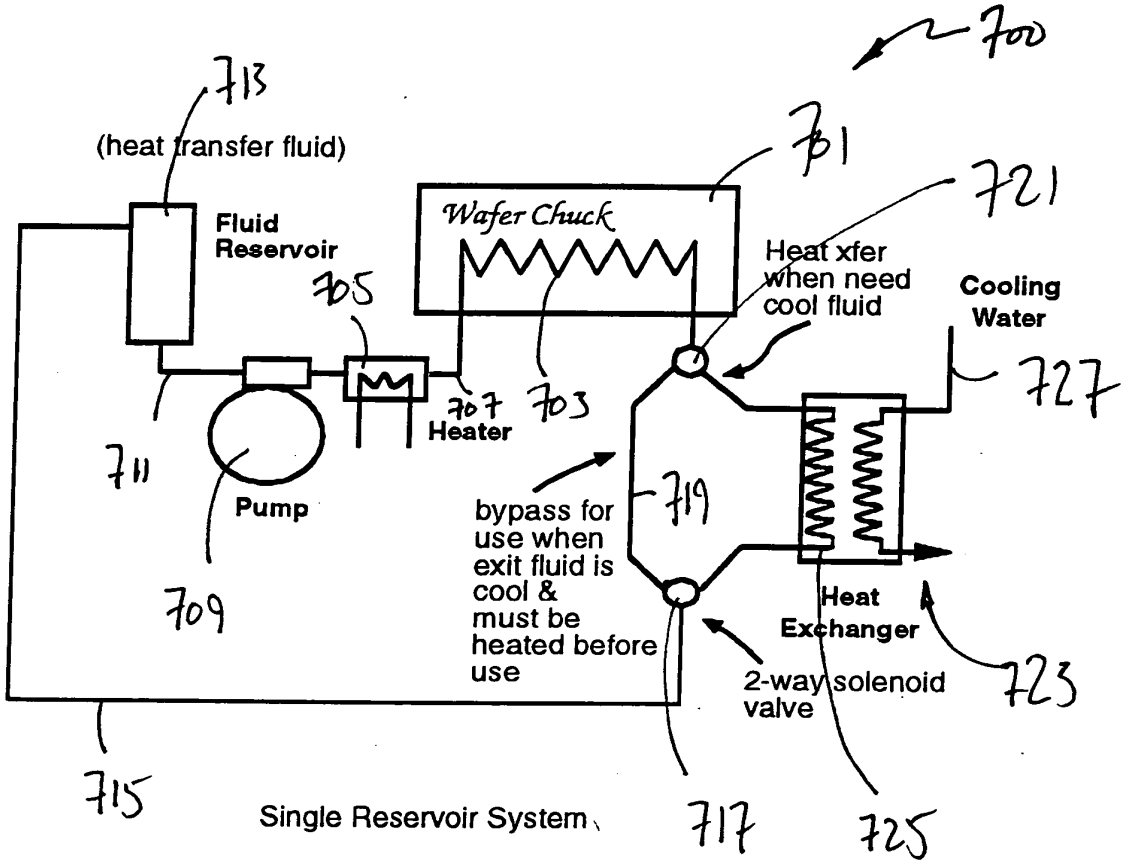

700
713
(heat transfer fluid)
Fluid Reservoir
701
Wafer Chuck
721
Heat xfer when need cool fluid
Cooling Water
727
705
707
Heater
703
711
Pump
709
bypass for use when exit fluid is cool & must be heated before use
719
Heat Exchanger
723
2-way solenoid valve
715
Single Reservoir System
717
725

FIG. 7

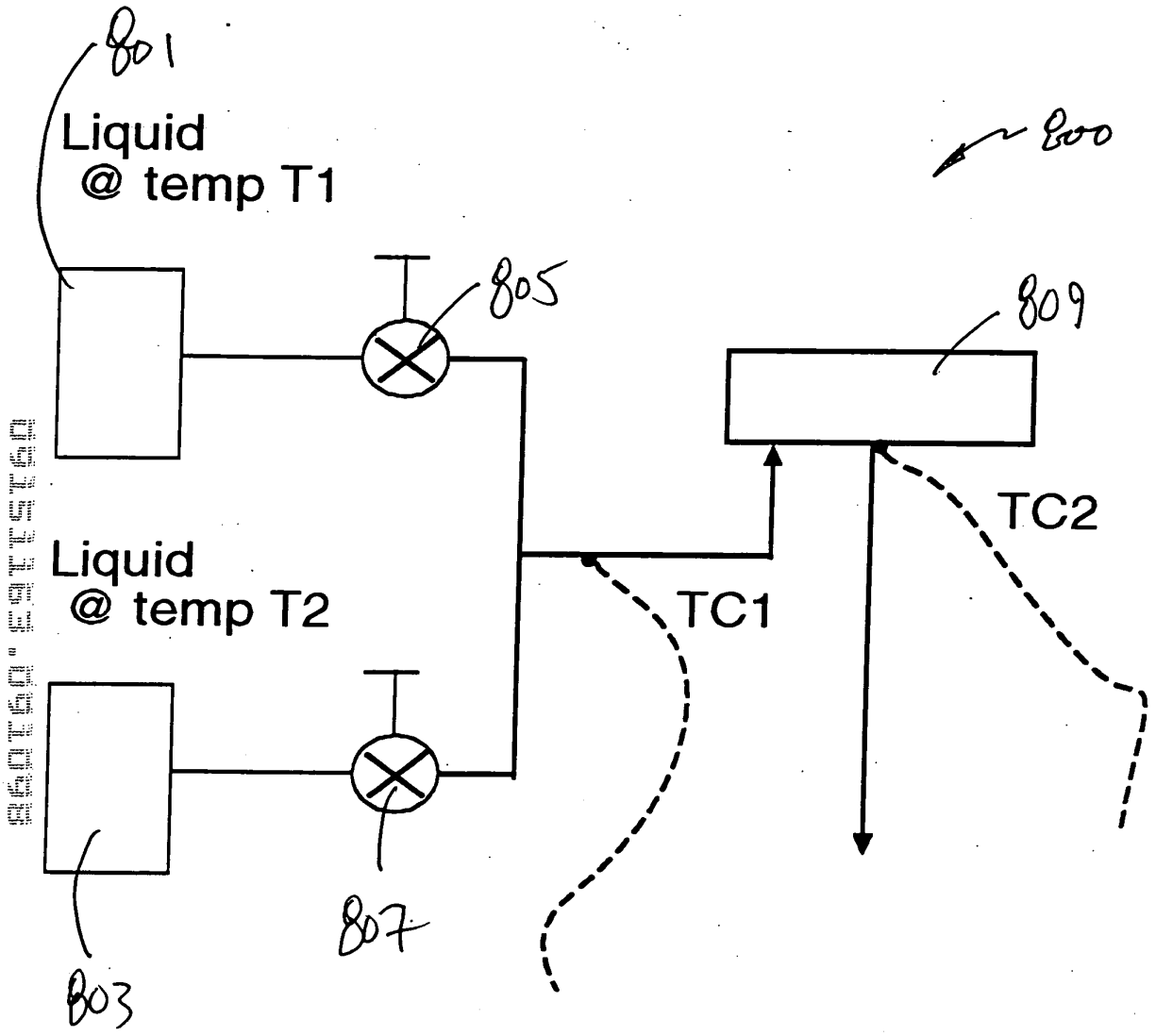


Fig. 8

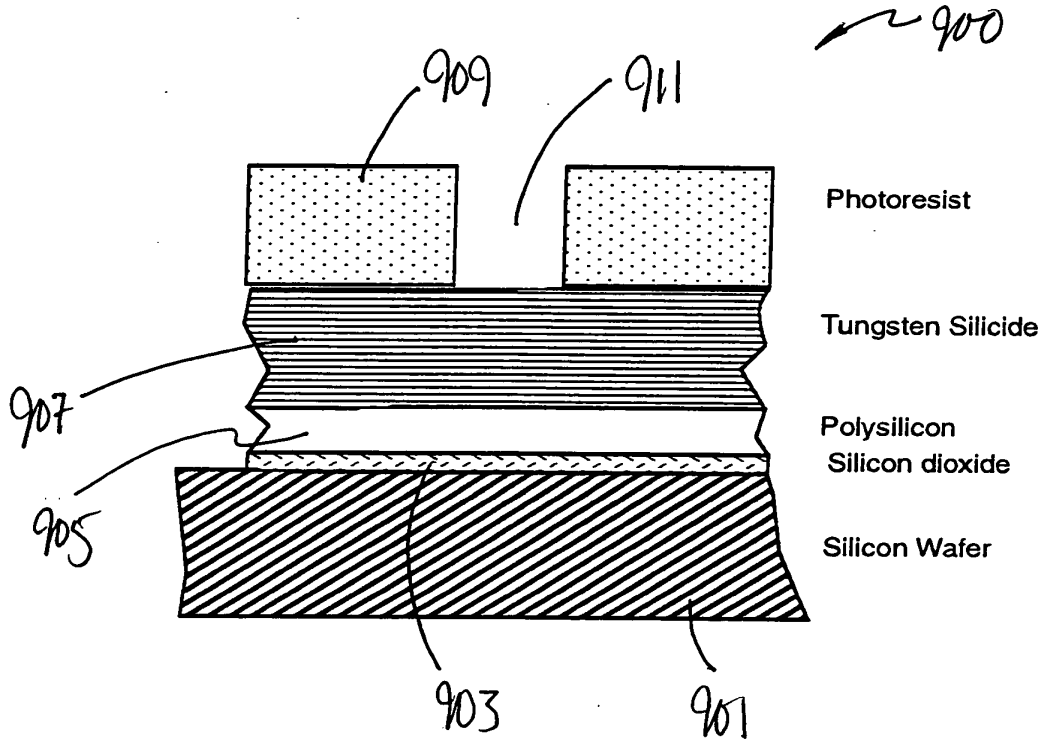
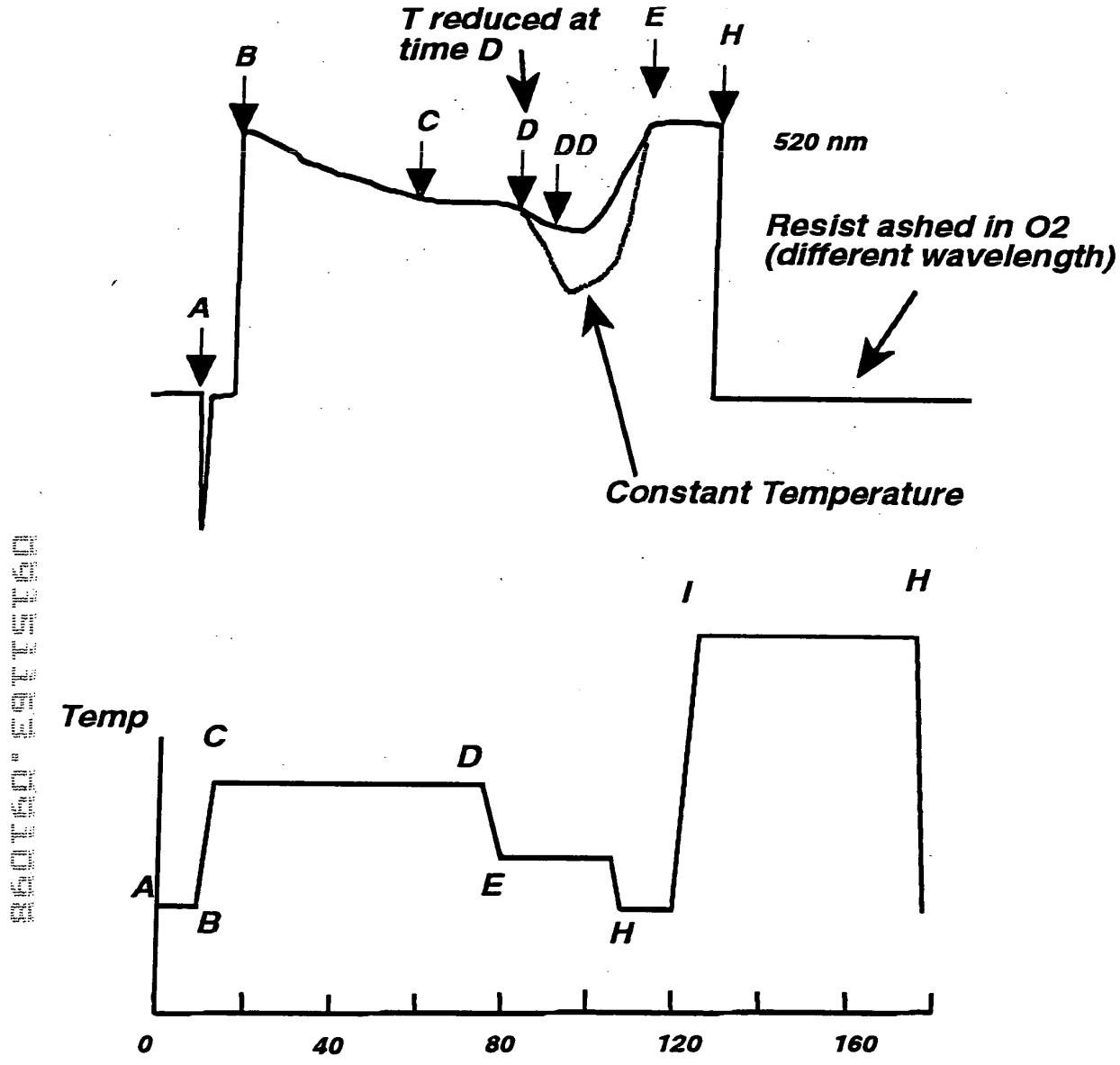

900
909
911
Photoresist
Tungsten Silicide
907
Polysilicon
Silicon dioxide
905
Silicon Wafer
903
901

FIG. 9



A. SF_6 native oxide "breakthrough"
B. Cl_2 plasma is ignited
C. WSi_x begins to clear (endpoint)
D. Polysilicon is exposed
E. Polysilicon cleared to oxide
H. Plasma extinguished and O2 feed gas flow is started
I. O2 plasma is started
J O2 plasma is extinguished.

FIG. 10

Attorney Docket No. 16655-000810

PATENT APPLICATION

MULTI-TEMPERATURE PROCESSING

Inventor:

Daniel L. Flamm, a citizen of the United States, residing at 476 Green View Drive, Walnut Creek, California 94596

Entity Status:

Small

TOWNSEND and TOWNSEND and CREW LLP
Two Embarcadero Center, 8th Floor
San Francisco, CA 9411-3834
(650) 326-2400

Attorney Docket No. 16655-000810

MULTI-TEMPERATURE PROCESSING

CROSS-REFERENCE TO RELATED APPLICATIONS

This present application is a continuation-in-part of U.S. Application Serial No. 60/058,650 (Attorney Docket No.16655-000600) filed September 11, 1997, and a continuation-in-part of U.S. Application Serial No. 08/567,224 filed December 4, 1995 (Attorney Docket No. 16655-5) now abandoned, which are hereby incorporated by reference for all purposes.

BACKGROUND OF THE INVENTION

This invention relates generally to plasma processing. More particularly, one aspect of the invention is for greatly improved plasma processing of devices using an in-situ temperature application technique. Another aspect of the invention is illustrated in an example with regard to plasma etching or resist stripping used in the manufacture of semiconductor devices. The invention is also of benefit in plasma assisted chemical vapor deposition (CVD) for the manufacture of semiconductor devices. But it will be recognized that the invention has a wider range of applicability. Merely by way of example, the invention also can be applied in other plasma etching applications, and deposition of materials such as silicon, silicon dioxide, silicon nitride, polysilicon, among others.

Plasma processing techniques can occur in a variety of semiconductor manufacturing processes. Examples of plasma processing techniques occur in chemical dry etching (CDE), ion-assisted etching (IAE), and plasma enhanced chemical vapor deposition (PECVD), including remote plasma deposition (RPCVD) and ion-assisted plasma enhanced chemical vapor deposition (IAPECVD). These plasma processing techniques often rely upon radio frequency power (rf) supplied to an inductive coil for providing power to produce with the aid of a plasma.

Plasmas can be used to form neutral species (i.e., uncharged) for purposes of removing or forming films in the manufacture of integrated circuit

devices. For instance, chemical dry etching is a technique which generally depends on gas-surface reactions involving these neutral species without substantial ion bombardment.

In a number of manufacturing processes, ion bombardment to substrate surfaces is often undesirable. This ion bombardment, however, is known to have harmful effects on properties of material layers in devices and excessive ion bombardment flux and energy can lead to intermixing of materials in adjacent device layers, breaking down oxide and "wear out," injecting of contaminative material formed in the processing environment into substrate material layers, harmful changes in substrate morphology (e.g. amophotization), etc.

Ion assisted etching processes, however, rely upon ion bombardment to the substrate surface in defining selected films. But these ion assisted etching processes commonly have a lower selectivity relative to conventional CDE processes. Hence, CDE is often chosen when high selectivity is desired and ion bombardment to substrates is to be avoided.

In generally most, if not all, of the above processes maintain temperature in a "batch" mode. That is, the temperature of surfaces in a chamber and of the substrate being processed in such chamber are controlled to be at a substantially a single value of temperature during processing.

From the above it is seen that an improved technique, including a method and apparatus, for plasma processing is often desired.

SUMMARY OF THE INVENTION

The present invention provides a technique, including a method and apparatus, for fabricating a product using a plasma discharge. One aspect of the present technique relies upon multi-step etching processes for selectively removing a film on a workpiece using differing temperatures. It overcomes serious disadvantages of prior art methods in which throughput and etching rate were lowered in order to avoid excessive device damage to a workpiece. In particular, this technique is extremely beneficial for removing resist masks which have been used to effect selective ion implantation of a substrate in some embodiments. In general,

implantation of ions into a resist masking surface causes the upper surface of said resist to become extremely cross-linked and contaminated by materials from the ion bombardment. If the cross-linked layer is exposed to excessive temperature, it is prone to rupture and forms contaminative particulate matter. Hence, the entire resist layer is often processed at a low temperature to avoid this particle problem. Processing at a lower temperature often requires excessive time which lowers throughput. Accordingly, the present invention overcomes these disadvantages of conventional processes by rapidly removing a majority of resist at a higher temperature after an ion implanted layer is removed without substantial particle generation at a lower temperature.

In another aspect, the present invention provides a process which utilizes temperature changes to achieve high etch rates while simultaneously maintaining high etch selectivity between a layer which is being pattered or removed other material layers. An embodiment of this process advantageously employs a sequence of temperature changes as an unexpected means to avoid various types of processing damage to the a device and material layers. A novel inventive means for effecting a suitable controlled change in temperature as part of a process involves the use of a workpiece support which has low thermal mass in comparison to the heat transfer means. In an aspect of this invention, a fluid is utilized to change the temperature of a workpiece. In another aspect, the thermal capacity of a circulating fluid is sufficiently greater than the thermal capacity of the workpiece support that it permits maintaining the workpiece at a substantially uniform temperature.

Still another aspect of the invention provides an apparatus for etching a substrate in the manufacture of a device using different temperatures during etching. The apparatus includes a chamber and a substrate holder disposed in the chamber. The substrate holder has a selected thermal mass to facilitate changing the temperature of the substrate to be etched. That is, the selected thermal mass of the substrate holder allows for a change from a first temperature to a second temperature within a characteristic time period to process a film. The present apparatus can, for example, provide different processing temperatures during an etching process or the like.

The present invention achieves these benefits in the context of known process technology. However, a further understanding of the nature and advantages of the present invention may be realized by reference to the latter portions of the specification and attached drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a simplified diagram of a plasma etching apparatus according to the present invention;

Figs. 2A-2E are simplified configurations using wave adjustment circuits according to the present invention;

Fig. 3 is a simplified diagram of a chemical vapor deposition apparatus according to the present invention;

Fig. 4 is a simplified diagram of a stripper according to the present invention;

Figs. 5A-5C are more detailed simplified diagrams of a helical resonator according to the present invention;

Fig. 6 is a simplified block diagram of a substrate holder according to the present invention;

Fig. 7 is a simplified diagram of a temperature control system according to an embodiment of the present invention;

Fig. 8 is a simplified diagram of a fluid reservoir system according to an embodiment of the present invention;

Fig. 9 is a simplified diagram of a simplified diagram of a semiconductor substrate according to an embodiment of the present invention; and

Fig. 10 is a simplified flow diagram of a heating process according to the present invention.

DETAILED DESCRIPTION OF THE INVENTION

Fig. 1 is a simplified diagram of a plasma etch apparatus 10 according to the present invention. This etch apparatus is provided with an inductive applicator, e.g., inductive coil. This etch apparatus depicted, however, is merely an

illustration, and should not limit the scope of the claims as defined herein. One of ordinary skilled in the art may implement the present invention with other treatment chambers and the like.

The etch apparatus includes a chamber 12, a feed source 14, an exhaust 16, a product support check or pedestal 18, an inductive applicator 20, a radio frequency ("rf") power source 22 to the inductive applicator 20, wave adjustment circuits 24, 29 (WACs), a radio frequency power source 35 to the pedestal 18, a controller 36, an agile temperature control means 19, and other elements. Optionally, the etch apparatus includes a gas distributor 17.

The chamber 12 can be any suitable chamber capable of housing a product 28, such as a wafer to be etched, and for providing a plasma discharge therein. The chamber can be a domed chamber for providing a uniform plasma distribution over the product 28 to be etched, but the chamber also can be configured in other shapes or geometries, e.g., flat ceiling, truncated pyramid, cylindrical, rectangular, etc. Depending upon the application, the chamber is selected to produce a uniform entity density over the pedestal 18, providing a high density of entities (i.e., etchant species) for etching uniformity.

The product support chuck can rapidly change its temperature in ways defined herein as well as others. The wafer is often thermally coupled to the support check which permits maintaining the wafer temperature in a known relationship with respect to the chuck. Coupling will often comprise an electrostatic chuck or mechanical clamps, which apply a pressure to bring the product into close proximity with the support check, which enables a relatively good thermal contact between the wafer and support chuck. The support chuck and wafer are often maintained at a substantially equal temperature. A pressure of gas is often applied through small openings in the support chuck behind the wafer in order to improve thermal contact and heat transfer between the wafer and support chuck.

The present chamber includes a dome 25 having an interior surface 26 made of quartz or other suitable materials. The exterior surface of the chamber is typically a dielectric material such as a ceramic or the like. Chamber 12 also includes a process kit with a focus ring 32, a cover (not shown), and other elements.

Preferably, the plasma discharge is derived from the inductively coupled plasma source that is a de-coupled plasma source ("DPS") or a helical resonator, although other sources can be employed.

The de-coupled source originates from rf power derived from the inductive applicator 20. Inductively coupled power is derived from the power source 22. The rf signal frequencies ranging from 800 kHz to 80 MHz can be provided to the inductive applicator 20. Preferably, the rf signal frequencies range from 5 MHz to 60 MHz. The inductive applicator (e.g., coil, antenna, transmission line, etc.) overlying the chamber ceiling can be made using a variety of shapes and ranges of shapes. For example, the inductive applicator can be a single integral conductive film, a transmission line, or multiple coil windings. The shape of the inductive applicator and its location relative to the chamber are selected to provide a plasma overlying the pedestal to improve etch uniformity.

The plasma discharge (or plasma source) is derived from the inductive applicator 20 operating with selected phase 23 and anti-phase 27 potentials (i.e., voltages) that substantially cancel each other. The controller 36 is operably coupled to the wave adjustment circuits 24, 29. In one embodiment, wave adjustment circuits 24, 29 provide an inductive applicator operating at full-wave multiples 21. This embodiment of full-wave multiple operation provides for balanced capacitance of phase 23 and anti-phase voltages 27 along the inductive applicator (or coil adjacent to the plasma). This full-wave multiple operation reduces or substantially eliminates the amount of capacitively coupled power from the plasma source to chamber bodies (e.g., pedestal, walls, wafer, etc.) at or close to ground potential. Alternatively, the wave adjustment circuits 24, 29 provide an inductive applicator that is effectively made shorter or longer than a full-wave length multiple by a selected amount, thereby operating at selected phase and anti-phase voltages that are not full-wave multiples. Alternatively, more than two, one or even no wave adjustment circuits can be provided in other embodiments. But in all of these above embodiments, the phase and anti-phase potentials substantially cancel each other, thereby providing substantially no capacitively coupled power from the plasma source to the chamber bodies.

In alternative embodiments, the wave adjustment circuit can be configured to provide selected phase and anti-phase coupled voltages coupled from the inductive applicator to the plasma that do not cancel. This provides a controlled potential between the plasma and the chamber bodies, e.g., the substrate, grounded surfaces, walls, etc. In one embodiment, the wave adjustment circuits can be used to selectively reduce current (i.e., capacitively coupled current) to the plasma. This can occur when certain high potential difference regions of the inductive applicator to the plasma are positioned (or kept) away from the plasma region (or inductor-containing-the-plasma region) by making them go into the wafer adjustment circuit assemblies, which are typically configured outside of the plasma region. In this embodiment, capacitive current is reduced and a selected degree of symmetry between the phase and anti-phase of the coupled voltages is maintained, thereby providing a selected potential or even substantially ground potential. In other embodiments, the wave adjustment circuits can be used to selectively increase current (i.e., capacitively coupled current) to the plasma.

As shown, the wave adjustment circuits are attached (e.g., connected, coupled, etc.) to ends of the inductive applicator. Alternatively, each of these wave adjustment circuits can be attached at an intermediate position away from the inductive application ends. Accordingly, upper and lower tap positions for respective wave adjustment circuits can be adjustable. But both the inductive applicator portions below and above each tap position are active. That is, they both can interact with the plasma discharge.

A sensing apparatus can be used to sense plasma voltage which is used to provide automatic tuning of the wave adjustment circuits and any rf matching circuit between the rf generator and the plasma treatment chamber. This sensing apparatus can maintain the average AC potential at zero or a selected value relative to ground or any other reference value. This wave adjustment circuit provides for a selected potential difference between the plasma source and chamber bodies. These chamber bodies may be at a ground potential or a potential supplied by another bias supply, e.g., See Fig. 1 reference numeral 35. Examples of wave adjustment circuits are described by way of the Figs. below.

For instance, Figs. 2A to 2E are simplified configurations using the wave adjustment circuits according to the present invention. These simplified configurations should not limit the scope of the claims herein. In an embodiment, these wave adjustment circuits employ substantially equal circuit elements (e.g., inductors, capacitors, transmission line sections, and others) such that the electrical length of the wave adjustment circuits in series with the inductive applicator coupling power to the plasma is substantially an integral multiple of one wavelength. In other embodiments, the circuit elements provide for inductive applicators at other wavelength multiples, e.g., one-sixteenth-wave, one-eighth-wave, quarter-wave, half-wave, three-quarter wave, etc. In these embodiments (e.g., full-wave multiple, half-wave, quarter-wave, etc.), the phase and anti-phase relationship between the plasma potentials substantially cancel each other. In further embodiments, the wave adjustment circuits employ circuit elements that provide plasma applicators with phase and anti-phase potential relationships that do not cancel each other out using a variety of wave length portions.

Fig. 2A is a simplified illustration of a plasma source 50 using wave adjustment circuits and an agile temperature chuck 75 according to an embodiment of the present invention. This plasma source 50 includes a discharge tube 52, an inductive applicator 55, an exterior shield 54, an upper wave adjustment circuit 57, a lower wave adjustment circuit 59, an rf power supply 61, and other elements. The upper wave adjustment circuit 57 is a helical coil transmission line portion 69, outside of the plasma source region 60. Lower wave adjustment circuit 59 also is a helical coil transmission line portion 67 outside of the plasma source region 60. The power supply 61 is attached 65 to this lower helical coil portion 67, and is grounded 63. Each of the wave adjustment circuits also are shielded 66, 68.

In this embodiment, the wave adjustment circuits are adjusted to provide substantially zero AC voltage at one point on the inductive coil (refer to point 00 in Fig. 2A). This embodiment also provides substantially equal phase 70 and anti-phase 71 voltage distributions in directions about this point (refer to 00-A and 00-C in Fig. 2A) and provides substantially equal capacitance coupling to the plasma from physical inductor elements (00-C) and (00-A), carrying the phase and anti-phase

potentials. Voltage distributions 00-A and 00-C are combined with C-D and A-B (shown by the phantom lines) to substantially comprise a full-wave voltage distribution in this embodiment where the desired configuration is a selected phase/antiphase portion of a full-wave inductor (or helical resonator) surrounding the plasma source discharge tube.

In this embodiment, it is desirable to reduce or minimize capacitive coupling current from the inductive element to the plasma discharge in the plasma source. Since the capacitive current increases monotonically with the magnitude of the difference of peak phase and anti-phase voltages, which occur at points A and C in Fig. 2A, this coupling can be lessened by reducing this voltage difference. In Fig. 2A, for example, it is achieved by way of two wave adjustment circuits 57, 59. Coil 55 (or discharge source) is a helical resonator and the wave adjustment circuits 57, 59 are helical resonators.

The discharge source helical resonator 53 can be constructed using conventional design formulae. Generally, this helical resonator includes an electrical length which is a selected phase portion "x" (A to 00 to C) of a full-wave helical resonator. The helical resonator wave adjustment circuits are each selected to jointly comprise a portion (2π-x) of full-wave helical resonators. Physical parameters for the wave adjustment helical resonators can be selected to realize practical physical dimensions and appropriate Q, Z_o, etc values. In particular, some or even all of the transmission line parameters (Q, Z_o, etc.) of the wave adjustment circuit sections may be selected to be substantially the same as the transmission line parameters of the inductive applicator. The portion of the inductive plasma applicator helical resonator, on the other hand, is designed and sized to provide selected uniformity values over substrate dimensions within an economical equipment size and reduced Q.

The wave adjustment circuit provides for external rf power coupling, which can be used to control and match power to the plasma source, as compared to conventional techniques used in helical resonators and the like. In particular, conventional techniques often match to, couple power to, or match to the impedance of the power supply to the helical resonator by varying a tap position along the coil

above the grounded position, or selecting a fixed tap position relative to a grounded coil end and matching to the impedance at this position using a conventional matching network, e.g., LC network, π network, etc. Varying this tap position along the coil within a plasma source is often cumbersome and generally imposes difficult mechanical design problems. Using the fixed tap and external matching network also is cumbersome and can cause unanticipated changes in the discharge Q, and therefore influences its operating mode and stability. In the present embodiments, the wave adjustment circuits can be positioned outside of the plasma source (or constrained in space containing the inductive coil, e.g., See Fig. 2A. Accordingly, the mechanical design (e.g., means for varying tap position, change in the effective rf power coupling point by electrical means, etc.) of the tap position are simplified relative to those conventional techniques.

In the present embodiment, rf power is fed into the lower wave adjustment circuit 59. Alternatively, rf power can be fed into the upper wave adjustment circuit (not shown). The rf power also can be coupled directly into the inductive plasma coupling applicator (e.g., coil, etc.) in the wave adjustment circuit design, as illustrated by Fig. 2B. Alternatively, other applications will use a single wave adjustment circuit, as illustrated by Fig. 2C. Power can be coupled into this wave adjustment circuit or by conventional techniques such as a tap in the coil phase. In some embodiments, this tap in the coil phase is positioned above the grounded end. An external impedance matching network may then be operably coupled to the power for satisfactory power transfer efficiency from, for example, a conventional coaxial cable to impedances (current to voltage rations) existing between the wave adjustment circuit terminated end of the applicator and the grounded end.

A further embodiment using multiple inductive plasma applicators also is provided, as shown in Fig. 2D. This embodiment includes multiple plasma applicators (PA1, PA2...PAn). These plasma applicators respectively provide selected combinations of inductively coupled power and capacitively coupled power from respective voltage potentials (V1, V2...Vn). Each of these plasma applicators derives power from its power source (PS1, PS2...PSn) either directly through an appropriate matching or coupling network or by coupling to a wave adjustment

circuit as described. Alternatively, a single power supply using power splitters and impedance matching networks can be coupled to each (or more than two) of the plasma applicators. Alternatively, more than one power supply can be used where at least one power supply is shared among more than one plasma applicator. Each power source is coupled to its respective wave adjustment circuits (WAC1, WAC2...WACn).

Generally, each plasma applicator has an upper wave adjustment circuit (e.g., WAC 1a, WAC 2a...WACna) and a lower wave adjustment circuit (e.g., WAC1b, WAC 2b...WACnb). The combination of upper and lower wave adjustment circuits are used to adjust the plasma source potential for each plasma source zone. Alternatively, a single wave adjustment circuit can be used for each plasma applicator. Each wave adjustment circuit can provide substantially the same impedance characteristics, or substantially distinct impedance characteristics. Of course, the particular configuration used will depend upon the application.

For instance, multiple plasma applicators can be used to employ distinct excitation frequencies for selected zones in a variety of applications. These applications include film deposition using plasma enhanced chemical deposition, etching by way of ion enhanced etching or chemical dry etching and others. Plasma cleaning also can be performed by way of the multiple plasma applicators. Specifically, at least one of the plasma applicators will define a cleaning plasma used for cleaning purposes. In one embodiment, this cleaning plasma can have an oxygen containing species. This cleaning plasma is defined by using an oxygen discharge, which is sustained by microwave power to a cavity or resonant microwave chamber abutting or surrounding a conventional dielectric vessel. Of course, a variety of other processes also can be performed by way of this multiple plasma applicator embodiment.

This present application using multiple plasma applicators can provide a multi-zone (or multi-chamber) plasma source without the use of conventional mechanical separation means (e.g., baffles, separate process chambers, etc.). Alternatively, the degree of interaction between adjacent zones or chambers can be relaxed owing to the use of voltage potential control via wave adjustment circuits.

This plasma source provides for multiple plasma source chambers, each with its own control via its own plasma applicator. Accordingly, each plasma applicator provides a physical zone region (i.e., plasma source) with selected plasma characteristics (e.g., capacitively coupled current, inductively coupled current, etc.). These zones can be used alone or can be combined with other zones. Of course, the particular configuration will depend upon the application.

In the present embodiments, the wave adjustment circuit can be made from any suitable combination of element(s) such as various types of transmission lines, circuits, etc. These transmission lines include conventional solid or air dielectric coaxial cable, or ordinary, repeating inductor/capacitor discrete approximations to transmission lines, and others. These types of transmission lines are co-axial transmission lines, balanced parallel transmission lines, so called slow wave transmission lines with a spiral inner conductor (e.g., selected portions of a helical resonator, etc.), and others. Individual lumped, fixed, or adjustable combinations of resistors, capacitors, and inductors (e.g., matching networks, etc.) also can be used in place of transmission line sections for the wave adjustment circuit. These general types of wave adjustment circuits are frequency dependent, and can be termed frequency dependent wave adjustment circuits (or FDWACs).

Frequency independent elements also can be used as the wave adjustment circuits. These wave adjustment circuits can be termed frequency independent WACs (or FIWACs). Frequency independent wave adjustment circuits include degenerate cases such as short-circuit connections to ground or an infinite impedance (i.e., open circuit), and others. Frequency independent wave adjustment circuits can be used alone, or in combination with the frequency dependent wave adjustment circuits. Alternatively, the frequency dependent wave adjustment circuits can be used alone or in combination with other wave adjustment circuits. Other variations, alternative constructions, and modifications also may be possible depending upon the application.

With regard to operation of the wave adjustment circuits, various embodiments can be used, as illustrated by Fig. 2E. The wave adjustment circuits are used to select a wave length portion to be applied in the plasma applicator. In

some embodiments, the average rf plasma potential is maintained close to ground potential by providing substantially equal phase 90, 81 and anti-phase 91, 82 capacitively coupled portions of the inductive applicator. This can occur in multi-wave embodiments 92, full-wave embodiments 93, half-wave multiple embodiments, quarter-wave multiple embodiments, or any other embodiments 94.

In alternative embodiments, it is desirable to maintain an elevated source plasma voltage relative to ground potential to induce a controlled ion plasma flux (or ion bombardment) to the product substrate (or any other chamber bodies). These embodiments are provided by selecting distinct electrical lengths for each of the wave adjustment circuit sections such that the capacitive coupled current from a phase section of the inductive plasma applicator is in excess of capacitive coupled current from its anti-phase portion. In these embodiments, the wave adjustment circuit provides a deliberate imbalance between the phase and anti-phase of the coupled voltages. In some embodiments 97, this occurs by shifting the zero voltage nodes along the process chamber axially, thereby achieving a bias relative to the plasma discharge. As shown, the phase 95 is imbalanced relative to its anti-phase 96. In other embodiments 99, one phase portion 84 is imbalanced by way of a different period relative to its complementary phase portion 85. Other embodiments are provided where the source plasma voltage is lower relative to ground potential. In the embodiments where imbalance is desirable, the potential difference between the phase and anti-phase potential portions is reduced (or minimized) when the amount of sputtering (e.g., wall sputtering, etc.) is reduced. The amount of sputtering, however, can be increased (or maximized) by increasing the potential difference between the phase and anti-phase potential portions. Sputtering is desirable in, for example, sputtering a quartz target, cleaning applications, and others. Of course, the type of operation used will depend upon the application.

Current maxima on an inductive applicator with distributed capacitance (e.g., helical resonator transmission line, etc.) occur at voltage minima. In particular, conventional quarter-wave helical resonator current is substantially at a relative maximum at its grounded end of the coil, and to a lesser extend in the nearby coil elements. Therefore, partial inductive coupling of power, if it occurs, will tend

to be at this grounded end. In conventional half-wave helical resonators, inductive coupling tends to occur at each of the two grounded ends.

In the present invention, substantially anti-symmetric phase and anti-phase inductive half-wave and other fractional wave applicator sections support substantially more inductive coupling at a selected rf voltage node, e.g., Fig. 2A reference numeral 00. This effect is caused by high current flow in the inductor applicator zones (or sections) both directly above and below the node (corresponding to inductor elements in the phase and anti-phase sections at and immediately adjacent to the rf voltage zero point). It should be noted that conventional quarter and half-wave inductively coupled inductive applicators have inductive coupling which abruptly declines below the grounded coil locations because the coil terminates and voltage extrema are present at these locations. This generally produces conventional quarter and half-wave helical resonators that tend to operate in a capacitive mode, or with a substantial fraction of power which is capacitively coupled to the plasma, unless the plasma is shielded from coil voltages, as noted above.

In a specific embodiment, the power system includes selected circuit elements for effective operation. The power system includes an rf power source. This rf power source can be any suitable rf generator capable of providing a selected or continuously variable frequency in a range from about 800 kHz to about 80 MHz. Many generators are useful. Preferably, generators capable of operating into short and open-circuit loads without damage are used for industrial applications. One example of a suitable generator is a fixed frequency rf generator 28.12 MHz - 3 kW CX-3000 power supply made by Comdel, Inc. of Beverly, Massachusetts. A suitable variable frequency power supply arrangement capable of the 3 kW output over an 800 kHz to 50 MHz range can be made by driving an IFI Model TCCX3500 High Power Wide Band Amplifier with a Hewlett Packard HP116A, 0-50 MHz Pulse/Function Generator. Other generators including those capable of higher or lower power also can be used depending upon the application.

Power from the generator can be transmitted to the plasma source by conventional coaxial cable transmission line. An example of this transmission line is RG8/U and other higher temperature rated cable (e.g., RG1151U, etc.) with a

coaxial TEFLON™ dielectric. In some embodiments, power is fed to conventional end-grounded half-wave helical resonators by positioning a movable tap on the helical coil and connecting a power source between the tap and the ground. In other embodiments, matching networks can be introduced between the coaxial cable power feed and the helical coil tap for flexibility. The matching network will depend on the selected wave configuration and wave adjustment circuits. In a balanced half-wave helical resonator embodiment, for example, the ends of the resonator coil can be terminated with wave adjustment circuits which substantially have zero susceptance. In particular, the wave adjustment circuit is designed as an open circuit by making no electrical connections to the ends of the coil, or establishing an electrical equivalence thereof. Alternatively, the ends of the coil are isolated by high series impedance chokes, thereby maintaining DC coupling to a fixed reference potential. These types of wave adjustment circuits are frequency independent and are "degenerate" cases. In these embodiments, the rf power is provided such that the phase and anti-phase current flows above and below the electrical midpoint (i.e., zero voltage node, etc.) of the coil. This provides for substantially balanced phase and anti-phase current flow from the power source stabilizing desired operation in coil voltages above the midpoint of the coil, and also provides substantially equal phase and anti-phase voltages.

The embodiments described above also can be applied to other plasma processing applications, e.g., PECVD, plasma immersion ion implantation (PIII), stripping, sputtering. For instance, Fig. 3 is a simplified CVD apparatus 100 according to the present invention. The present CVD apparatus includes a chamber 112, a feed source 114, an exhaust 116, a pedestal 118, a power source 122, a ground 124, a helical resonator 126, and other elements. The helical resonator 126 has a coil 132, an outer shield 133, and other elements. The chamber can be any suitable chamber capable of housing a product 119 such as a wafer for deposition, and for providing a plasma discharge therein. Preferably, the chamber is a right circular cylinder chamber for providing an uniform plasma species distribution over the product. But the chamber can also be configured in the form of rectangular right cylinder, a truncated cone, and the like. The chamber and fixtures are constructed

from aluminum and quartz, and other suitable materials. The plasma discharge is derived from a plasma source which is preferably a helical resonator discharge or other inductive discharge using a wave adjustment circuit or other techniques to selectively adjust phase-anti-phase potentials. The present CVD apparatus provides for deposition of a dielectric material, e.g., silicon dioxide or the like.

The product 119 having an upper surface 130 is placed into the present CVD apparatus for deposition, e.g., plasma enhanced chemical vapor deposition (PECVD), and others. Examples of deposition materials include a dielectric material such as a silicon dioxide (SiO_2), a phosphosilicate glass (PSG), a borophosphosilicate glass (BPSG), a silicon nitride (Si_3N_4), among others.

In one embodiment, the deposition occurs by introducing a mixture comprising organic silane, oxygen, and an inert gas such as helium or argon according to the present invention. The organic silane can be any suitable organic silicate material such TEOS, HMDS, OMCTS, and the like. Deposition is also conformal in selected instances. As for the oxygen, it includes a flow rate of about 1 liter/per minute and less. A relative flow rate between the organic silane such as TEOS and oxygen ranges from about 1:40 to about 2:1, and is preferably less than about 1:2 in certain applications. A deposition temperature of the organic silane-oxygen layer ranges from about 300 to about 500°C, and can also be at other temperatures. Pressures in the range of 1 to 7 Torr are generally used. Of course, other concentrations, temperatures, materials, and flow rates can be used depending upon the particular application.

This chamber also includes a wave adjustment circuit 127. The wave adjustment circuit 127 is used to provide a helical coil operating with capacitive coupling to selected phase and anti-phase voltages. This portion 127 of the wave adjustment circuit coil also is shielded 140 to prevent rf from interfering with the plasma discharge or external elements, e.g., equipment, power, etc. The coil shield 140 is made of a conductive material such as copper, aluminum, or the like. In one embodiment, an operating frequency is selected and the wave adjustment circuit is adjusted to short circuit the upper end of the helical applicator coil to ground 124. This provides a helical coil operating at approximately a full-wave multiple and has

substantially equal phase and anti-phase sections. This full-wave multiple operation provides for balanced capacitance of phase 151 and anti-phase 153 voltages along the coil 132 adjacent to the plasma source. Full-wave multiple operation reduces or even substantially eliminates the amount of capacitively coupled power from the plasma source to chamber bodies (e.g., pedestal, walls, wafer, etc.) at or close to ground potential.

In the present embodiment, the wave adjustment circuit 127 is a variable coil portion 128 of a spiral transmission line, which is selectively placed outside the outer shield 133. Accordingly, when the wave adjustment circuit is adjusted to become a short circuit, the plasma source "sees" only a selected full-wave multiple comprising substantially equal phase 151 and anti-phase 153 of the entire instantaneous AC voltages 134, 135. In this embodiment, stress of the deposited oxide film is often tensile, which can be undesirable.

Alternatively, the wave adjustment circuit 127 provides a helical resonator operating at selected phase and anti-phase voltages that are not full-wave multiples. This wave adjustment circuit provides for a selected amount of capacitive coupling from the plasma source to the chamber bodies. Stress of the deposited oxide film in this embodiment can be made to be zero or slightly compressive. In some embodiments, the oxide films can be deposited with an rf plasma potential of several hundred volts between the plasma source and the substrate to decrease the tendency of the oxide film to absorb moisture. This can occur by adjusting the wave adjustment circuit to add in a small section of transmission line outside of the source and correspondingly shortening the applicator coil (by moving the lower point at which the applicator coil is short-circuited and thereby decreasing the inductance of the applicator coil and electrical length of the helical resonator 126 (e.g., spiral transmission line, etc.)). Of course, the selected amount of capacitive coupling will depend upon the application.

Fig. 4 is a simplified diagram of a resist stripper according to the present invention. The present stripping apparatus includes similar elements as the previous described CVD apparatus. The present stripping apparatus includes a chamber 112, a feed source 114, an exhaust 116, a pedestal 118, which can be an

agile temperature controlled chuck, an rf power source 122, a ground 124, a helical resonator 126, and other elements. The helical resonator 126 includes a coil 132, an outer shield 133, a wave adjustment circuit 400, and other elements. The chamber can be any suitable chamber capable of housing a product 119 such as a photoresist coated wafer for stripping, and for providing a plasma discharge therein. The plasma discharge is derived from a plasma source, which is preferably a helical resonator discharge or other inductive discharge using a wave adjustment circuit or other techniques to selectively adjust phase/anti-phase potentials. Of course, in some applications other configurations such as parallel plate capacitive discharges and microwave powered discharges such as electron cyclotron resonance machines, resonant cavities and slow waver applicator structures may also be suitable. The present stripping apparatus provides for stripping or ashing photoresist, e.g., implant hardened, etc. Further examples of such a stripping apparatus are described in the experiments section below.

In this embodiment, the wave adjustment circuits rely upon open circuits (i.e., zero susceptance). Power transfer can be effected with a balanced feed such as an inductively-coupled push-pull arrangement with means such as coupled inductors. Techniques for constructing these coupled inductors are described in, for example, "The ARRL Antenna Book," R.D. Straw, Editor, The American Radio Relay League, Newington, CT (1994) and "The Radio Handbook," W.I. Orr, Editor, Engineering Ltd, Indiana (1962), which are both hereby incorporated by reference for all purposes. In one embodiment, a ferrite or powdered iron core "balun" (balanced-unbalanced) toroidal transformer (i.e., broadband transmission transformer, broadband transformer, etc.) 401 can be used to provide balanced matching from a conventional unbalanced coaxial transmission line. Techniques for constructing toroidal baluns are described in, for example, "Transmission Line Transformers," J. Sevick, 2nd Edition, American Radio Relay League, Newington, CT (1990). The toroidal transformer is coupled between the rf power source 122 and the coil 132. The midpoint 406 between the phase 405 and anti-phase voltage on the coil is effectively rf grounded, hence it may be convenient to directly ground this midpoint of the inductive application in some embodiments for stability. This

permits alternate operation in which power may be coupled into the inductive applicator (e.g., coil, etc.) with a conventional unbalanced feed line tapped on one side of the center. Push-pull balanced coupling ignites the plasma more easily than conventional unbalanced coil tap matching and generally is easier to adjust in selected applications.

Referring to the helical resonator embodiments operating at substantially equal phase and anti-phase potentials, Fig. 5A is a simplified diagram 200 of an equivalent circuit diagram of some of them. The diagram is merely an illustration and should not limit the scope of the claims herein. The equivalent circuit diagram includes a plurality of rf power supplies (V_1, V_2, V_3...V_n) 203, representing for example, a single rf power source. These power supplies are connected in parallel to each other. One end of the power supply is operably coupled to a ground connection 201. The other end of the power supplies can be represented as being connected to a respective capacitor (C_1, C_2, C_3...C_n). Each of these capacitors are connected in parallel to each other. During this mode of operation, no significant voltage difference exists between any of the common side of the capacitors, as they are all connected to each other in parallel.

Fig. 5B is a simplified diagram of instantaneous AC voltage and current along a helical resonator coil of Fig. 5A where each end of the inductive applicator is short circuited. The diagram is merely an illustration and should not limit the scope of the claims herein. This diagram includes the discharge tube 213 and an inductive plasma discharge (or plasma source) 501 therein. As shown, the plasma discharge includes an intensified "donut-shaped" glow region 501 that occupies a limited range (R) of the discharge tube 213. The plasma discharge has an average voltage potential (V_{ave}) of magnitude that is substantially within a few zero volts (i.e., the ground potential). As can be seen, the plasma discharge 501 has capacitively coupling elements to V_H and V_G. But the average voltage potential of this plasma discharge is substantially zero. This operation provides for balanced capacitance of phase 503 and anti-phase 505 voltages along the coil adjacent to the plasma, thereby substantially preventing capacitively coupling from the plasma source to chamber bodies. As also shown, a current maxima 507 exists at V_{ave}, which

corresponds to an inflection point between the phase 503 and the anti-phase 505.

In an alternative operating mode, rings of plasma caused by inductively coupled plasma current are visible near top and bottom extremes of the inductive applicator, as illustrated by Fig. 5C. This operating mode is generally for a full-wave 517 inductive coupling coil operated at a very high power, e.g., maximum power input to the inductive applicator is often limited by thermal considerations and breakdown. The rings 513, 515 of current in the plasma discharge are simulated by maximum coil current areas corresponding to voltage minima at the top and bottom shorted ends of the coil. Under these high power conditions, subordinate current rings are detectable and some excitation is often visible in the intermediate regions. This excitation is partially caused by capacitively driven currents within the discharge coupled to the voltage maximum and voltage minimum positions along the inductive applicator.

Alternatively, subordinate inductive plasma current rings at the top and bottom ends 513 of the resonator do not appear with limited input power. The coil current and inductive flux fall beyond the ends of the inductive applicator so that a single inductive ring 515 in the center portion is more stable, provided that the conductivity of the plasma is large enough to support a single current ring at a specified input power.

In alternative applications using high power operation, no secondary plasma current rings may be desirable. These applications often have substantially minimum internal capacitive coupling. In these applications, the inductive applicator (e.g., coil) abutting the vacuum vessel may be shortened from a full wave to an appropriate length such that only the central current maxima exists on the coil abutting the plasma source and the potential difference between maximum and minimum voltage on the applicator is substantially reduced. The present application is achieved by stabilizing the desired waveform along the applicator by appropriate impedance wave adjustment circuits.

An effective conventional method employed to avoid plasma potential shift in conventional commercially available inductive sources is to shield the plasma from the electrical fields on the inductive coupling element (commonly a multi-turn

coil) by inserting a grounded conductive member between the inductive driving element and the plasma discharge tube. Shielding is, however, cumbersome and inconvenient and has serious disadvantages in practice. Shields couple to inductive applicator elements and can cause wide excursions in the natural resonance frequency, which are not predicted by conventional analytical design formulae. This often results in laborious trail and error and iterative mechanical designs to achieve a desired resonance.

Another disadvantage of shielding is that shields often make it difficult to achieve initial ignition of the plasma since shields generally exclude capacitive electric fields in the plasma discharge tube. Those with skill in the art will recognize that in practice, substantial ionization (e.g. charge carriers) must be present in the tube volume before in inductive plasma current can be sustained. Thus, it is often said that a capacitive plasma must be ignited first in order to sustain an inductive plasma. This is not completely true since other external means of generating ionization (e.g. an intense photoionizing source, electron beams, etc.) can be used to generate the ionization which is prerequisite to sustaining an inductive plasma. However, a capacitive discharge is often a convenient and cost-effective means to ignite some plasma which is a prerequisite to starting and sustaining an inductive discharge.

In general, wave adjustment circuits are employed to substantially diminish capacitive coupling between a plasma source and an inductive applicator. If most capacitive coupling is removed, it may be difficult to ignite a plasma. However, wave adjustment circuits also provide a means to overcome the difficulty with igniting a plasma in the absence of capacitive coupling under steady state operating conditions. This means is provided by electrically, mechanically, or electromechanically tuning the wave adjustment circuits prior to the time of desired plasma ignition in a manner which generates an additional imbalance and capacitive coupling to the discharge volume. Of course, the characteristics of the plasma as a load to the applicator will dynamically change during ignition. The wave adjustment circuit can also be continuously tuned under feedback control during ignition in order to provide a desired voltage coupling and diminish undesired transients during plasma

breakdown.

Insertion of the shield close to high voltage RF point in a network (such as the voltage maximum points in a helical resonator or the high potential driven side of a TCP coil) also causes large displacement currents to flow through the capacitance between the shield and coil. This high potential difference is also a potential cause of damaging rf breakdown across the air gap, hence the gap may require protection by inconvenient solid or liquid dielectric insulation. The displacement current flow causes power loss and requires that higher power RF generating equipment be used to compensate for the power loss. Coupling loss in the plasma source structure is also undesirable from the standpoint of thermal control. These limitations are overcome by the present invention using the wave adjustment circuits, an inductive applicator of selected phase length, and other elements.

Fig. 6 is a simplified block diagram of a substrate holder 600 according to the present invention. This diagram is merely an illustration and should not limit the scope of the claims herein. One of ordinary skill in the art would recognize other variations, modifications, and alternatives. The substrate holder 600 or suceptor includes, among others, a lower or backside surface 608, which includes a plurality of concentric zones 608A, 608B, 608C, and 608D. In a specific embodiment, each of the zones can be in fluidic communication with each other and can be partly separated from each other. Each of the zones can have an inlet 613 and an outlet 611. Fluid enters the inlet, traverses in an annular manner in the zone, and leaves the outlet. A baffle can separate the inlet from the outlet. Each of the zones can have an inlet and outlet, which are independent from the other inlets and outlets. Alternatively, the inlet and outlets can be in fluid communication with each other.

The side-view diagram shown as "SIDE-VIEW A" illustrates a plurality of zones 603, which correspond to each of the concentric zones 608A, 608B, 608C, and 608D. Each zone is separated, in part, from each other by a baffle 605. Each baffle extends from a lower region of the substrate holder toward an upper portion of the substrate holder, but does not touch the upper surface 601 of the substrate holder. In preferred embodiments, the baffles do not touch the upper surface. Accordingly, the temperature of the baffles, which may be different from

the fluid, does not create an uneven temperature distribution along the upper surface 601. Additionally, the upper region 604, which is an open region within the substrate holder, provides fluid communication between each of the zones. Fluid communication in connection with the upper surface also provides an even distribution of temperature along the upper surface.

The fluid can be used to heat or cool the upper surface of the substrate holder. In a specific embodiment, the fluid generally should have a relatively high thermal conductivity and large heat capacity. The fluid should also be substantially non-corrosive, easy to transport, and can withstand a relatively large temperature range and still maintain its fluid characteristics. Additionally, the fluid should be able to be pumped and substantially non-reactive with the substrate holder material itself. The fluid can be any commercial heat transfer fluid selected for the desirable temperature range. As noted, the substrate holder and upper surface cools down or is heated up by way of the fluid. The fluid can traverse through the zones and can absorb thermal energy or release thermal energy by an external heat transfer device such as the one described below, but can be others.

In a specific embodiment, the substrate holder also includes a plurality of heating elements 607. The heating elements can selectively heat one or more zones in a desirable manner. As shown in the "SIDE-VIEW B" diagram, each of the heating elements can be directed to a single zone 603, which has an adjacent baffle 605. Alternatively, the heating elements can be directed to multiple zones or other specific regions of the substrate and in particular the backside of the substrate according to some embodiments. The heating elements can be any suitable device for supplying heat energy to the fluid. The heat can be supplied by single or in combination using radiation, conduction, and convention. As merely an example, the heating element can be a resistive heating unit, an infrared heating unit, and others. Of course, the type of heating unit used depends highly upon the application. Alternatively, the heating unit can also be replaced by cooling units.

The present invention provides a substantially uniform temperature distribution along the upper surface 601 of the substrate holder. In a specific embodiment, the uniformity of the temperature is within one Degree Celsius along

the entire surface which comes in contact with the object such as the wafer. Preferably, the wafer temperature also tracks the temperature uniformity of the upper surface. In other embodiments, the uniformity of the of the temperature is within one-tenth of a Degree Celsius along the entire surface which comes in contact with the object such as the wafer. Preferably, the wafer also has a uniform temperature distribution along the wafer.

The substrate has an upper surface, which holds an object in a secure manner during processing. The upper surface is generally made of a suitable material that has desirable heat transfer characteristics. In a specific embodiment, the upper surface is made using a low thermal mass, high conductivity material. As merely an example, the upper surface can be a diamond-like or diamond film overlying a copper or copper-like substrate. Of course, the type of surface used depends upon the application.

In a specific embodiment, the substrate holder also has temperature sensing units such as the one shown in "SIDE-VIEW C." The temperature sensing unit can be any suitable unit that is capable of being adapted to the upper surface of the substrate holder. Alternatively, the temperature sensing unit can measure the temperature of the fluid or lower surface of the substrate holder. As merely an example, the temperature sensing unit is a "fluro-optic" sensor unit made by a company called Luxtron in Santa Clara, California. Alternatively, the sensing unit can be an edge band IR sensor or the like. The sensing unit is capable of measuring a variety of spatial locations along the upper or lower surface of the substrate holder. The substrate holder can be implemented using a variety of systems for heating and/or cooling applications such as the one described below, but can be others.

Fig. 7 is a simplified diagram of a temperature control system 700 according to an embodiment of the present invention. This diagram is merely an illustration and should not limit the scope of the claims herein. One of ordinary skill in the art would recognize other variations, modifications, and alternatives. Among other elements, the system 700 can be used to heat and/or cool the wafer chuck or substrate holder 701. As shown, system 700 includes substrate holder 701, which is coupled to a heating unit 705 by way of line 707. Heating unit 705 is coupled to

fluid reservoir 713 and pump 709 by way of line 711.

Fluid from the fluid reservoir is pumped from the reservoir through the heating unit, which selectively sets the temperature of the fluid. The fluid leaves the heating unit at the selected temperature and traverses through the substrate holder, which can be similar to the one shown above, but can also be others. The fluid temperature selectively transfers energy in the form of heat to the wafer holder to a desirable temperature. Fluid leaves the substrate holder and traverses through node 721 and branch 719. Fluid traverse through branch 719 and node 717. Fluid leaves node 717 and returns back to the fluid reservoir via line 715.

In an alternative embodiment, the fluid can also be cooled using a heat exchanger 723. The fluid leaves the substrate holder and enters node 721. Fluid then enters the heat exchanger and traverses through loop 725. Thermal energy in the form of heat transfers to fluid in loop 723, which is cooler in temperature and draws heat away from the heat in the fluid in loop 725. In a specific embodiment, cooling fluid 727 enters and leaves the heat exchanger.

In a specific embodiment, system 700 operates in a manner to program a process temperature of the substrate holder. In this process, the reservoir with a suitable heat transfer fluid is maintained at a temperature below the desired process temperature. The fluid is circulated through the substrate holder or wafer chuck by the pump. The fluid line downstream of the pump is equipped with ~~the~~ electrical heater which is capable of heating the fluid to a desired temperature. The desired fluid temperature is determined by comparing the desired wafer or wafer chuck set point temperature to a measured wafer or wafer chuck temperature (this measurement can performed with a thermocouple, thermistor, pyrometer, fluor optic sensor or other sensing means). If the measured temperature of the wafer ~~or~~ chuck is below the desired temperature, a suitable control algorithm such as a proportional controller or a proportional-integral-derivative (i.e., PID) controller algorithm increases the temperature by supplying more power to the heater.

The temperature of fluid emerging from the chuck is also measured (normally there will be a small temperature difference since there is heat exchange between the fluid and chuck). If this temperature is above the desired fluid temperature

the fluid stream is diverted to a heat exchanger via control valves 1 and 2, which are respectively at nodes 721 and 717. If this temperature is less than or equal to the desired fluid temperature the fluid stream can be made to bypass the heat exchanger, or optionally can be heated in a heat exchange system. Since the temperature of commonly used heat exchangers cannot be changed rapidly, the heat exchanger is usually maintained at a single temperature sufficiently below the lowest desired fluid temperature to achieve the lowest desired temperature to be attained. The heat exchanger, fluid flow rate, coolant-side fluid temperature, heater power, chuck, etc. should be designed using conventional means to permit the heater to bring the fluid to a setpoint temperature and bring the temperature of the chuck and wafer to predetermined temperatures within specified time intervals and within specified uniformity limits.

In a preferred embodiment, the present invention uses a microprocessor based system to oversee the operations of the system described above. The microprocessor based system can have input and output ports, which are coupled to each of the elements, e.g., pump, heater, fluid reservoir, substrate holder. The microprocessor based unit selectively turns ON and/or OFF one or more of the elements to control the temperature of the substrate holder to provide a uniform distribution of temperature across the surface of the substrate holder.

In an alternative embodiment, Fig. 8 is a simplified diagram of a multiple fluid reservoir system 800 according to an embodiment of the present invention. This diagram is merely an illustration and should not limit the scope of the claims herein. One of ordinary skill in the art would recognize other variations, modifications, and alternatives. As shown, system 800 depicts an automatic system for agile temperature control of the substrate holder or wafer chuck 809 using two reservoirs 801, 803, but is not limited to two and can be more than two, if desirable. The wafer chuck can be rapidly brought to temperature T1 by directing flow through proportional control valve 805 to the wafer chuck. Similarly, the chuck can be brought substantially to a temperature T2 by directing only a flow from the reservoir T2 to the wafer chuck. Temperature sensor TC1 measures the temperature of the heat transfer fluid entering the wafer chuck and sensor TC2 monitors temperature of fluid exiting the wafer chuck. Valves 805 and 807 are controlled by a control system which adjusts the

total volumetric flow rate of fluid flowing into the wafer chuck as well as the ratio of fluid flowing through V1 and V2. The ratio is set so that the temperature monitored by TC1 is at a predetermined value selected to achieve a desired wafer chuck temperature. The flow rate of a fluid flowing from both reservoir 1 and 2 is metered by conventional means and set to fix the temperature difference measured between TC2 and TC2 at a pre-specified difference. This difference is selected to meet a temperature uniformity specification. The temperature difference allowed is chosen so that etching nonuniformities caused by temperature gradients are below a predetermined permissible level which includes an allowance for normal variability in measurements, sensor, the control system etc. The flows can be digitally controlled proportional metering values as illustrated or alternately they can be controlled by computer-controlled variable speed pumps, as will be well known to those skilled in the art. In addition to the sensors TC1 and TC2, it is convenient to monitor the top surface chuck temperature and the wafer temperature so that TC1 can be selected to maintain the wafer temperature within a specific amount of a wafer etching or CVD temperature (when the chuck and etching temperature are greater than the temperature of the chamber walls, the wafer temperature will generally be slightly less than the chuck temperature owing to heat transfer resistance between the chuck and wafer and thermal coupling between the wafer and surrounding chamber walls).

Fig. 9 is a simplified diagram of a simplified diagram of a semiconductor substrate 900 according to an embodiment of the present invention. This diagram is merely an illustration and should not limit the scope of the claims herein. One of ordinary skill in the art would recognize other variations, modifications, and alternatives. As shown, the substrate is a stack of layers that is to be patterned. The stack includes a dielectric layer such as a thin 100Å gate oxide layer 903 on a substrate (e.g., silicon wafer) 901 on which 2000Å of tungsten silicide 907 or other material is deposited on the conductive layer, which can be polysilicon 905. A masking layer such as 2 microns of photoresist 909 is spin coated over the tungsten silicide and patterned by conventional photolithography techniques. The patterned layer includes an opening 911, which exposes the underlying tungsten silicide layer. It is desired to anisotropically etch the stack down to the silicon dioxide layer in order to

define a patterned structure which can be an EEPROM device or other integrated circuit element. Although this can be accomplished by etching in a conventional parallel plate reactor using a chlorine bearing plasma, it can be difficult to avoid removing excessive polysilicon during the overetching period, which is required to assure that the polysilicon is completely removed from within the unmasked regions. Furthermore, the resist mask must generally be removed after etching this stack. Since the temperature for the stack etch (i.e., often 50°C to 100°C) is too low to achieve an adequate resist stripping rate (generally a rate of a few microns per minute is desirable), stripping is often done in a separate chamber or in separate resist stripping equipment.

The temperature is programmed by use of this invention to achieve better control of the etching process as well as to permit stripping the resist in the same chamber and controlled by the same process program which is used for stack etching.

A process according to the present invention can be briefly outlined as follows:

(1) Provide patterned stack in chamber;

(2) Perform native oxide breakthrough using sulfur hexafluoride bearing plasma;

(3) Ignite chlorine bearing plasma;

(4) Etch tungsten silicide layer at a first substrate temperature;

(5) Detect polysilicon layer;

(6) Perform over etch to clear tungsten;

(7) Expose polysilicon;

(8) Etch polysilicon;

(9) Clear polysilicon to oxide;

(10) Stop chlorine bearing plasma;

(11) Feed oxygen;

(12) Ignite oxygen plasma;

(13) Strip photoresist at a second substrate temperature; and

(14) Extinguish oxygen plasma

The above sequence of steps are merely examples to show an etching process that uses more than one temperature. Here, the etching process for tungsten silicide and

polysilicon occurs at a first temperature and an ashing process occurs at a second temperature, where the first temperature is lower than the second temperature. By way of the present invention, multiple temperatures can be used in a single chamber to perform multiple processes. Details of the present invention are shown by way of Fig. 10, for example.

Fig. 10 is a simplified flow diagram of a heating process according to the present invention. This diagram is merely an illustration and should not limit the scope of the claims herein. One of ordinary skill in the art would recognize other variations, modifications, and alternatives. As shown, an isotropic breakthrough step during which an SF_6 plasma is used to remove very thin native oxide can be conducted at a low temperature such as room temperature. Ordinarily the breakthrough step is conducted at a high temperature. High temperatures have a serious disadvantage in that the etching rate of both oxide and tungsten silicide by SF_6 may be isotropic. Therefore the duration of the breakthrough step, especially if the native oxide layer is thin, must often be limited to a few seconds to avoid undesired undercut. At low temperature the etching rate is slower and therefore the extent to which materials under the native oxide are etched is easier to control.

At the end of the breakthrough step at time BB, the control program increases within several seconds to a higher steady state value at time C. The tungsten silicide is etched at this temperature until this layer is breached at random locations on the wafer. This endpoint is conveniently observed by a change in the slope of intensity of an optical light emission from the plasma such as optical emission at 530nm (point C in Fig. 10). The complete removal of the unmasked tungsten silicide areas is similarly signaled by a change in light emission such as that shown at point D (at time D all "patches" of the tungsten silicide are "cleared" from unmasked polysilicon areas; the signal begins to rapidly decease at time D because at constant temperature, polysilicon consumes chlorine more rapidly than tungsten silicide (e.g. a faster etch rate) and optical emission at this wavelength originates from a chlorine species.

Since it is not practical to change chuck temperature, at this point the etch rate would increase rapidly. As a consequence it can often be difficult to detect and terminate the polysilicon etching step when the thin oxide layer is reached. Another

problem associated with the use of a single temperature for both silicide and polysilicon layers is that chlorine etching processes often undercut (etch along the mask direction, sideways- e.g. the etch is partly isotropic) silicon at the elevated temperatures suitable for a low residue tungsten silicide etch. Therefore it is highly desirable and advantageous to reduce the etching temperature during the polysilicon etch. The wafer temperature is gradually reduced at point DD in order to achieve a slower and more anisotropic polysilicon etching step. The temperature necessary to etch tungsten silicide and during this temperature programmed sequence are compared in ~~the Fig~~. The emission signal intensity increases when the temperature is lowered because the rate of consumption of chlorine species by the etching process is slowed (the rate decreases with decreasing temperature). Stopping the etch process at endpoint where all of the silicon has "cleared," denoted by E is also easier and less critical because attack on the oxide has also slowed.

At point H the stack etch is complete and the plasma is extinguished. The flow of feed gas comprising Cl_2 for etching is stopped and a flow of O_2 is started. A plasma discharge in oxygen at elevated temperatures will strip resist rapidly. At time I the wafer temperature is increased rapidly to a selected value in the range 180-220° C and a plasma is ignited to remove the resist. After a selected interval the plasma is extinguished again and the chuck temperature rapidly lowered. These sequences of steps merely provide an example of the present invention. Other examples can also occur and the description above should not be limiting in any manner.

While the invention has been described with reference to specific embodiments, various alternatives, modifications, and equivalents may be used. In fact, the invention also can be applied to almost any type of plasma discharge apparatus. This discharge apparatus can include an apparatus for plasma immersion ion implantation or growing diamonds, TCPs, and others. This discharge apparatus can be used for the manufacture of flat panel displays, disks, integrated circuits, diamonds, semiconductor materials, bearings, raw materials, and the like. Therefore, the above description should not be taken as limiting the scope of the invention which is defined by the appended claims.

WHAT IS CLAIMED IS:

1. A method of etching a substrate in the manufacture of a device, said method comprising steps of:

placing a substrate having a film thereon on a substrate holder in a chamber, said substrate holder having a selected thermal mass; and

performing a first etching of a first portion of said film at a first temperature and performing a second etching of a second portion of said film at a second temperature, said first temperature being different from said second temperature;

wherein said selected thermal mass allows a change from said first temperature to said second temperature within a characteristic time period to process said film.

2. The method of claim 1 wherein said first temperature is changed to said second temperature by a heat transfer means coupled to said substrate holder.

3. The method of claim 1 wherein said change in temperature is an in-situ process during said first etching step and said second etching step.

4. The method of claim 1 wherein said first etching and said second etching are conducted in a substantially constant plasma environment.

5. The method of claim 1 wherein said first temperature is higher than said second temperature.

6. The method of claim 1 wherein said first temperature is lower than said second temperature.

7. The method of claim 1 wherein said first etching comprises radiation.

8. The method of claim 1 wherein said second etching comprises radiation.

9. The method of claim 1 wherein said first etching is an ion bombardment aided process.

10. The method of claim 1 wherein said second etching is an ion bombardment aided process.

11. The method of claim 1 wherein said first portion of said film is etched before said second portion of said film.

12. The method of claim 1 wherein said second portion of said film is etched before said first portion of said film.

13. Apparatus for etching a substrate in the manufacture of a device, said apparatus comprising:

a chamber;

a substrate holder disposed in said chamber, said substrate holder having a selected thermal mass;

wherein said selected thermal mass of said substrate holder allows for a change from a first temperature to a second temperature within a characteristic time period to process a film.

14. Apparatus of claim 13 further comprising a heat transfer means for changing said first temperature to said second temperature, said heat transfer means being coupled to said substrate holder.

15. Apparatus of claim 13 wherein said change in temperature is an in-situ process within said characteristic time.

16. Apparatus of claim 13 wherein said chamber provides a substantially constant plasma environment.

17. Apparatus of claim 13 wherein said first temperature is higher than said second temperature.

18. Apparatus of claim 13 wherein said first temperature is lower than said second temperature.

19. Apparatus of claim 13 wherein said chamber provides radiation.

20. Apparatus of claim 13 wherein said chamber provides an ion bombardment aided process.

MULTI-TEMPERATURE PROCESSING

ABSTRACT OF THE DISCLOSURE

The present invention provides a technique, including a method and apparatus, for etching a substrate in the manufacture of a device. The apparatus includes a chamber and a substrate holder disposed in the chamber. The substrate holder has a selected thermal mass to facilitate changing the temperature of the substrate to be etched during etching processes. That is, the selected thermal mass of the substrate holder allows for a change from a first temperature to a second temperature within a characteristic time period to process a film. The present technique can, for example, provide different processing temperatures during an etching process or the like.

SERIAL NUMBER	FILING DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
09/151,163	09/10/98	216	1641	16655-000810

APPLICANT

DANIEL L. FLAMM, WALNUT CREEK, CA.

CONTINUING DOMESTIC DATA********
VERIFIED PROVISIONAL APPLICATION NO. 60/058,650 09/11/97
AND A CIP OF 08/567,224 12/04/95 ABN

371 (NAT'L STAGE) DATA********
VERIFIED

LCM

FOREIGN APPLICATIONS********
VERIFIED

LCM

FOREIGN FILING LICENSE GRANTED 09/24/98 ***** SMALL ENTITY *****

Foreign Priority claimed 35 USC 119 (a-d) conditions met	STATE OR COUNTRY	SHEETS DRAWING	TOTAL CLAIMS	INDEPENDENT CLAIMS
☐yes ☐no ☐yes ☒no ☐Met after Allowance	CA	15	20	3
Verified and Acknowledged LCM Examiner's Initials ____ Initials				

ADDRESS

SEE CUSTOMER NUMBER: 020350

TITLE

MULTI-TEMPERATURE PROCESSING

FILING FEE RECEIVED	FEES: Authority has been given in Paper	☐ All Fees ☐ 1.16 Fees (Filing)

PATENT APPLICATION FEE DETERMINATION RECORD

Effective October 1, 1997

Application or Docket Number

CLAIMS AS FILED - PART I

	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY TYPE ☐ RATE	SMALL ENTITY FEE	OR	OTHER THAN SMALL ENTITY RATE	OTHER THAN SMALL ENTITY FEE
BASIC FEE				395.00	OR		790.00
TOTAL CLAIMS	20 minus 20 =	*	x$11=		OR	x$22=	
INDEPENDENT CLAIMS	3 minus 3 =	*	x41=		OR	x82=	
MULTIPLE DEPENDENT CLAIM PRESENT			+135=		OR	+270=	
			TOTAL		OR	TOTAL	790

* If the difference in column 1 is less than zero, enter "0" in column 2

11

CLAIMS AS AMENDED - PART II

AMENDMENT A

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				

SMALL ENTITY RATE	SMALL ENTITY ADDITIONAL FEE	OR	OTHER THAN SMALL ENTITY RATE	OTHER THAN SMALL ENTITY ADDITIONAL FEE
x$11=		OR	x$22=	
x41=		OR	x82=	
+135=		OR	+270=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

AMENDMENT B

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				

SMALL ENTITY RATE	SMALL ENTITY ADDITIONAL FEE	OR	OTHER THAN SMALL ENTITY RATE	OTHER THAN SMALL ENTITY ADDITIONAL FEE
x$11=		OR	x$22=	
x41=		OR	x82=	
+135=		OR	+270=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

AMENDMENT C

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				

SMALL ENTITY RATE	SMALL ENTITY ADDITIONAL FEE	OR	OTHER THAN SMALL ENTITY RATE	OTHER THAN SMALL ENTITY ADDITIONAL FEE
x$11=		OR	x$22=	
x41=		OR	x82=	
+135=		OR	+270=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20."
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3."
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

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NOTICE OF FILING/CLAIM FEE(S) DUE

TO ENSURE PROPER CREDIT OF FEES, PLEASE RETURN A COPY OF THIS FEE CALCULATION SHEET WITH YOUR RESPONSE.

APPLICATION NUMBER: 15/163

Total Fee Calculation

	Fee Code Sm./Lg.	Total # Claims		Number Extra	X	Fee Sm. Entity	Fee Lg. Entity	= Total
Basic Filing Fee	201/101						790	
Total Claims >20	203/103	20	-20 =		X			
Independent Claims >3	202/102	3	-3 =		X			
Mult. Dep Claim Present	204/104							
Surcharge	205/105							
English Translation	139						130	
TOTAL FEE CALCULATION								

Fees due upon filing the application:

Total Filing Fees Due = $ 790

Less Filing Fees Submitted - $ ✓

BALANCE DUE = $ 920