Paper No._____

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

CISCO SYSTEMS, INC.,
Petitioner

v.

TQ DELTA LLC,
Patent Owner

Case IPR2016-01466
Patent No. 8,611,404

PETITIONER'S REPLY

TABLE OF CONTENTS

PETITIONER'S UPDATED EXHIBIT LIST

August 23, 2017

Ex. 1001	U.S. Patent No. 8,611,404 to Greszczuk et al.
Ex. 1002	Prosecution File History of U.S. Patent No. 8,611,404
Ex. 1003	Declaration of Sayfe Kiaei under 37 C.F.R. § 1.68
Ex. 1004	Curriculum Vitae of Dr. Sayfe Kiaei
Ex. 1005	U.S. Patent No. 5,956,323 to Bowie
Ex. 1006	U.S. Patent No. 6,075,814 to Yamano et al.
Ex. 1007	ANSI T1.413-1995
Ex. 1008	Declaration of David Bader
Ex. 1009	U.S. Patent No. 6,084,881 to Fosmark et al.
Ex. 1010	Declaration of Dr. Chrissan in IPR2016-01160
Ex. 1011	Deposition Transcript of Dr. Chrissan
Ex. 1012	Second Declaration of Dr. Sayfe Kiaei
Ex. 1013	Standard Dictionary of Computer and Information Processing (1977)
Ex. 1014	Reserved
Ex. 1015	Reserved
Ex. 1016	Reserved
Ex. 1017	Reserved
Ex. 1018	Reserved
Ex. 1019	District Court Claim Construction Order
Ex. 1020	Tina Rathbone, MORE MODEMS FOR DUMMIES (1996) (selected pages)
Ex. 1021	Copyright registration for Ex.1020

I. Introduction

Patent Owner argues that the combination set forth in the Petition does not teach: (1) storing fine gain and bit allocation parameters in low power mode; (2) exiting low power mode without the need for retraining; (3) transmitting/receiving a synchronization signal in full power mode; and (4) transmitting/receiving a synchronization signal in the low power mode. Patent Owner also argues that there is no motivation to combine Bowie, Yamano, and the ANSI specification. These arguments rely on narrow claim constructions and a mischaracterization of the references. As shown below, Patent Owner's arguments do not refute the obviousness of the challenged claims.

II. Claim Construction

A. Petitioner's construction of "synchronization signal" is the broadest reasonable interpretation.

Petitioner, Patent Owner, and the Board each propose distinct constructions for this term. The Board's construction is "*a signal allowing frame synchronization between the transmitter of the signal and the receiver of the signal*." Institution Decision, 6. Patent Owner argues that this construction is incorrect because it "seems to implicate the wrong kind of synchronization." Response, 18. Petitioner agrees that by referring to only frame synchronization, the Board's construction incorrectly limits "*synchronization signal*" to just frame synchronization.

There is no dispute that the '404 patent describes both frame synchronization

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